TOSHIBA e-MMC Module

1GB / 2GB / 4GB / 8GB / 16GB / 32GB THGBM1GxDxEBAIx Series

INTRODUCTION

THGBM1GxDxEBAIx series are 1-GB , 2-GB , 4-GB , 8-GB , 16-GB and 32-GB densities of e-MMC Module products housed in 153/169 ball BGA package. This unit is utilized advanced TOSHIBA NAND flash device(s) and controller chip assembled as Multi Chip Module. THGBM1GxDxEBAIx has an industry standard MMC protocol for easy use.

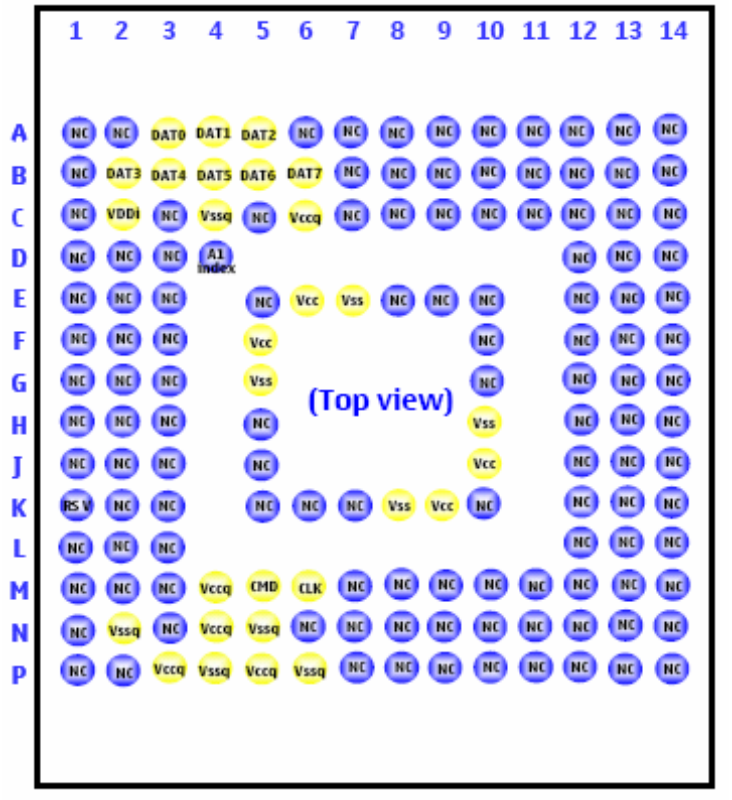
FEATURES

THGBM1GxDxEBAIx Series Interface

THGBM1GxDxEBAIx has the-MMCA 4.3 interface with either 1-I/O, 4-I/O and 8-I/O mode support.

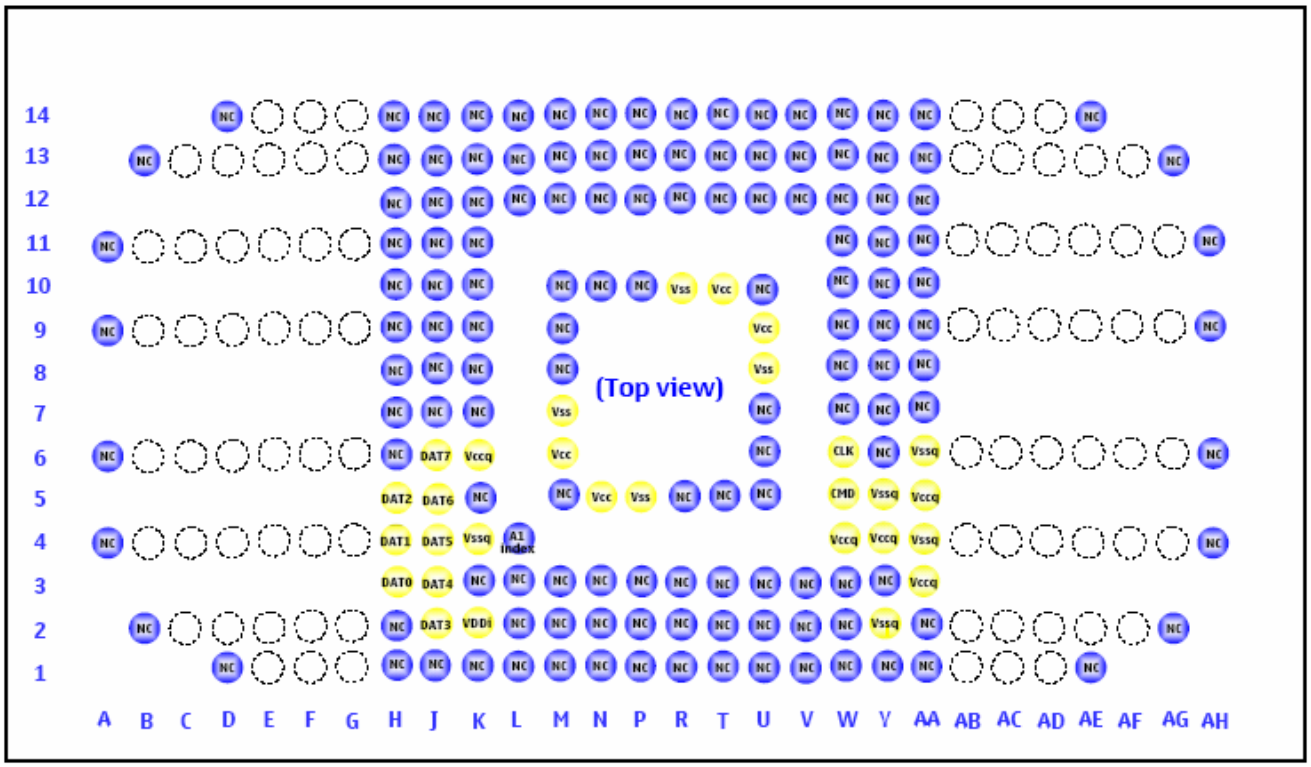
Pin Connection

11.5mm x 13.0mm x 1.2mm(max) Package



Pin Number	Name	Pin Number	Name
A3	DAT0	H10	Vss
A4	DAT1	J10	Vcc
A5	DAT2	K8	Vss
B2	DAT3	K9	Vcc
B3	DAT4	M4	VccQ
B4	DAT5	M5	CMD
B5	DAT6	M6	CLK
B6	DAT7	N2	VssQ
C2	VDDi	N4	VccQ
C4	VssQ	N5	VssQ
C6	VccQ	P3	VccQ
E6	Vcc	P4	VssQ
E7	Vss	P5	VccQ
F5	Vcc	P6	VssQ
G5	Vss		

12.0mm x 16.0mm x 1.3mm(max) Package
12.0mm x 18.0mm x 1.3mm(max) Package
12.0mm x 18.0mm x 1.4mm(max) Package
14.0mm x 18.0mm x 1.4mm(max) Package



Pin Number	Name	Pin Number	Name
H3	DAT0	R10	Vss
H4	DAT1	T10	Vcc
H5	DAT2	U8	Vss
J2	DAT3	U9	Vcc
J3	DAT4	W4	VccQ
J4	DAT5	W5	CMD
J5	DAT6	W6	CLK
J6	DAT7	Y2	VssQ
K2	VDDi	Y4	VccQ
K4	VssQ	Y5	VssQ
K6	VccQ	AA3	VccQ
M6	Vcc	AA4	VssQ
M7	Vss	AA5	VccQ
N5	Vcc	AA6	VssQ
P5	Vss		

Part Numbers

Available e-MMC Module Products – Part Numbers

TOSHIBA Part Number	Density	Package Size	NAND Flash Type	Weight
THGBM1G3D1EBAI8	1-GBytes	11.5mm x 13.0mm x 1.2mm(max)	1 x 8Gbit MLC 43nm	TBD
THGBM1G4D1EBAI7	2-GBytes	12.0mm x 16.0mm x 1.3mm(max)	1 x 16Gbit MLC 43nm	TBD
THGBM1G5D2EBAI7	4-GBytes	12.0mm x 16.0mm x 1.3mm(max)	2 x 16Gbit MLC 43nm	0.41g typ.
THGBM1G6D4EBAI4	8-GBytes	12.0mm x 18.0mm x 1.3mm(max)	4 x 16Gbit MLC 43nm	0.45g typ.
THGBM1G7D8EBAI0	16-GBytes	12.0mm x 18.0mm x 1.4mm(max)	8 x 16Gbit MLC 43nm	0.51g typ.
THGBM1G7D4EBAI2	16-GBytes	14.0mm x 18.0mm x 1.4mm(max)	4 x 32Gbit MLC 43nm	TBD
THGBM1G8D8EBAI2	32-GBytes	14.0mm x 18.0mm x 1.4mm(max)	8 x 32Gbit MLC 43nm	0.60g typ.

Operating Temperature and Humidity Conditions

-25°C to +85°C, and 0%RH to 95%RH

Performance

52MHz / x8 mode / Sequential access

TOSHIBA Part Number	Density	NAND Flash Type	Min Performance [MB/sec]	
			Read	Write
THGBM1G3D1EBAI8	1-GBytes	1 x 8Gbit MLC 43nm	20 (Target)	10 (Target)
THGBM1G4D1EBAI7	2-GBytes	1 x 16Gbit MLC 43nm	20 (Target)	10 (Target)
THGBM1G5D2EBAI7	4-GBytes	2 x 16Gbit MLC 43nm	20 (Target)	10 (Target)
THGBM1G6D4EBAI4	8-GBytes	4 x 16Gbit MLC 43nm	20 (Target)	10 (Target)
THGBM1G7D8EBAI0	16-GBytes	8 x 16Gbit MLC 43nm	20 (Target)	10 (Target)
THGBM1G7D4EBAI2	16-GBytes	4 x 32Gbit MLC 43nm	25 (Target)	20 (Target)
THGBM1G8D8EBAI2	32-GBytes	8 x 32Gbit MLC 43nm	25 (Target)	20 (Target)

Power Supply

V_{CC} = 2.7V to 3.6V
VccQ = 1.7V to 1.95V / 2.7V to 3.6V

Operating Current (RMS)

Operating : 100mA max (without Interleave operation)
150mA max (with Interleave operation)

The measurement for max RMS current is done as average RMS current consumption over a period of 100ms

Sleep Mode Current

TOSHIBA Part Number	Density	NAND Flash Type	Iccqs [uA]		Iccqs+Iccs [uA]	
			Typ. *1	Max. *2	Typ. *1	Max. *2
THGBM1G3D1EBAI8	1-GBytes	1 x 8Gbit MLC 43nm	50	100	80	150
THGBM1G4D1EBAI7	2-GBytes	1 x 16Gbit MLC 43nm	50	100	80	150
THGBM1G5D2EBAI7	4-GBytes	2 x 16Gbit MLC 43nm	50	100	100	200
THGBM1G6D4EBAI4	8-GBytes	4 x 16Gbit MLC 43nm	50	100	150	300
THGBM1G7D8EBAI0	16-GBytes	8 x 16Gbit MLC 43nm	50	100	200	450
THGBM1G7D4EBAI2	16-GBytes	4 x 32Gbit MLC 43nm	50	100	150	300
THGBM1G8D8EBAI2	32-GBytes	8 x 32Gbit MLC 43nm	50	100	200	450

*1 : The conditions of typical values are 25°C and VccQ = 3.3V or 1.8V.
*2 : The conditions of maximum values are 85°C and VccQ = 3.6V or 1.95V.

Product Architecture

The diagram in Figure 1 illustrates the main functional blocks of the THGBM1GxDxEBAIx series.

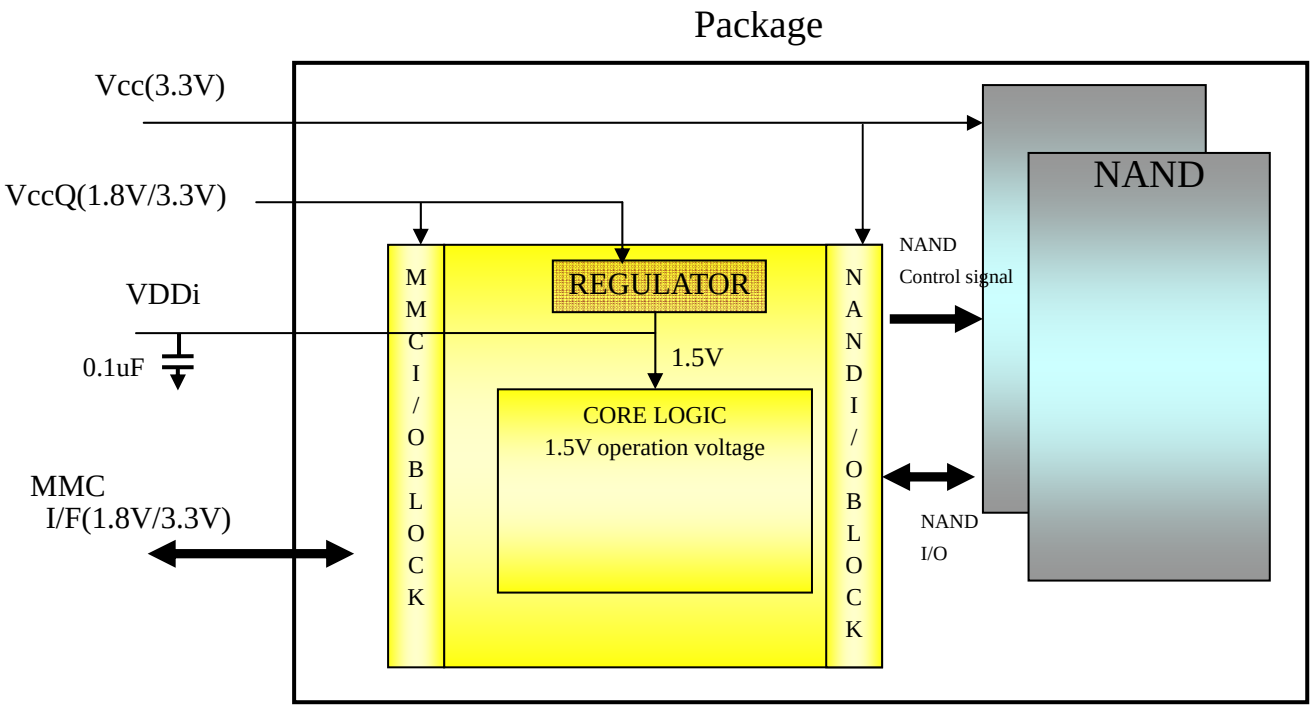


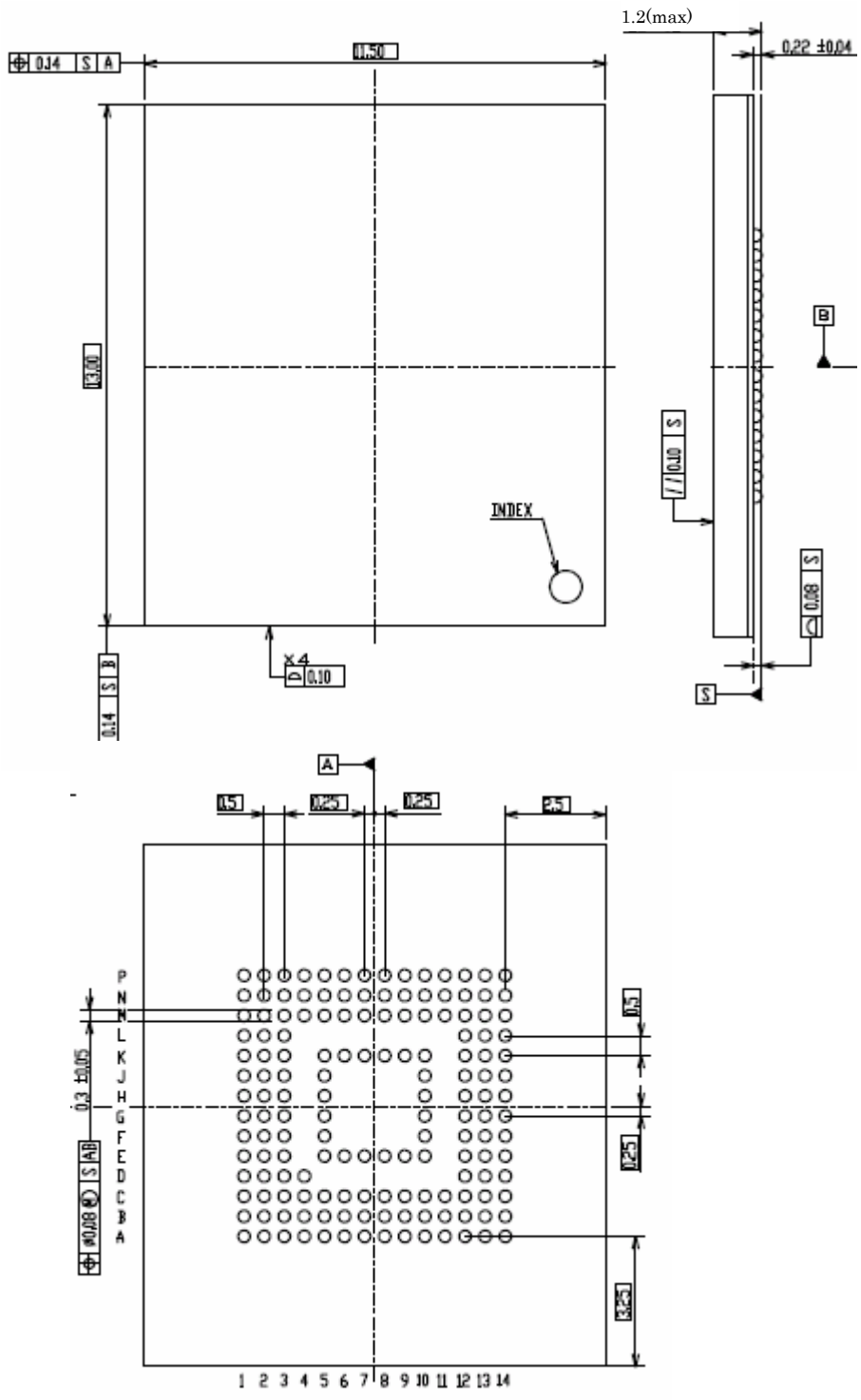
Figure 1 THGBM1GxDxEBAIx series Block Diagram

PRODUCT SPECIFICATIONS

Package Dimensions

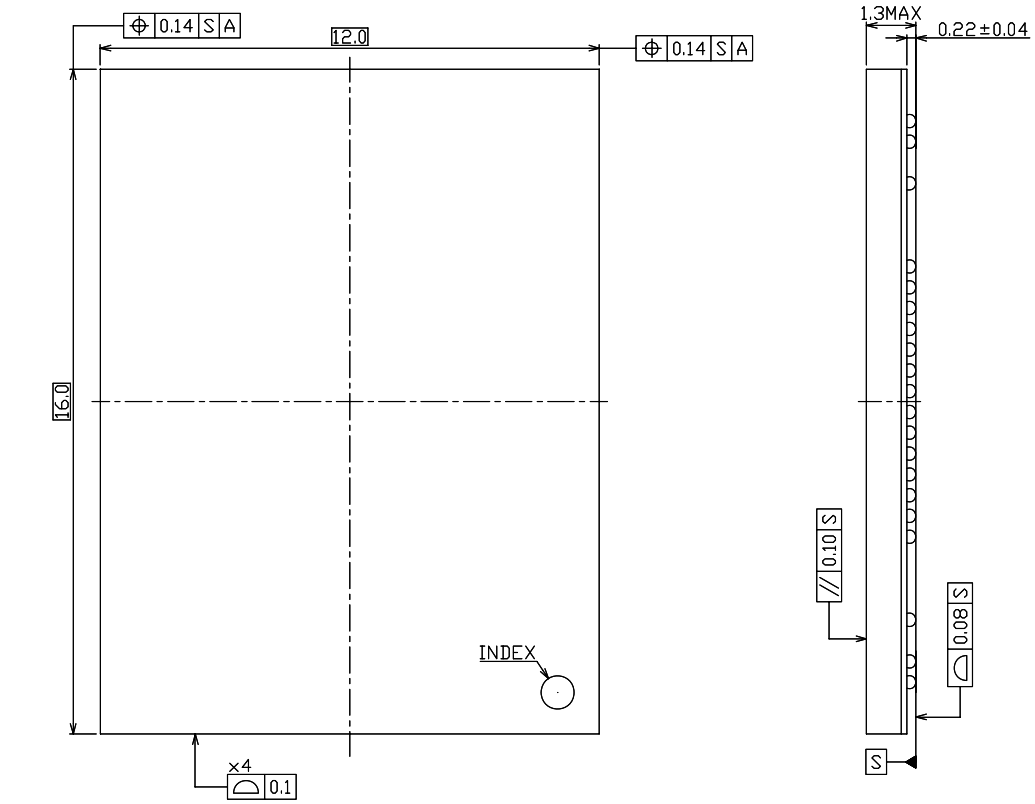
11.5mm x 13mm x 1.2mm(max)

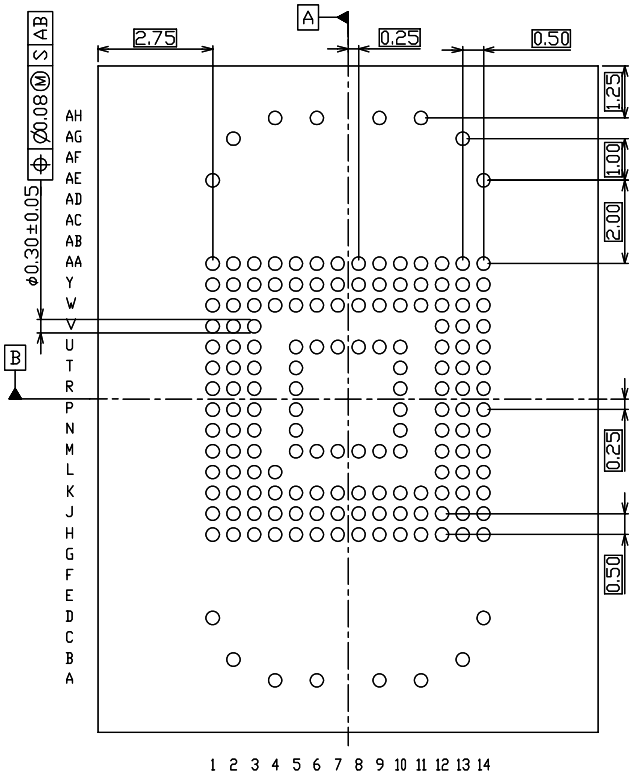
Unit: mm
Tolerance: ±0.1 mm



12mm x 16mm x 1.3mm(max)

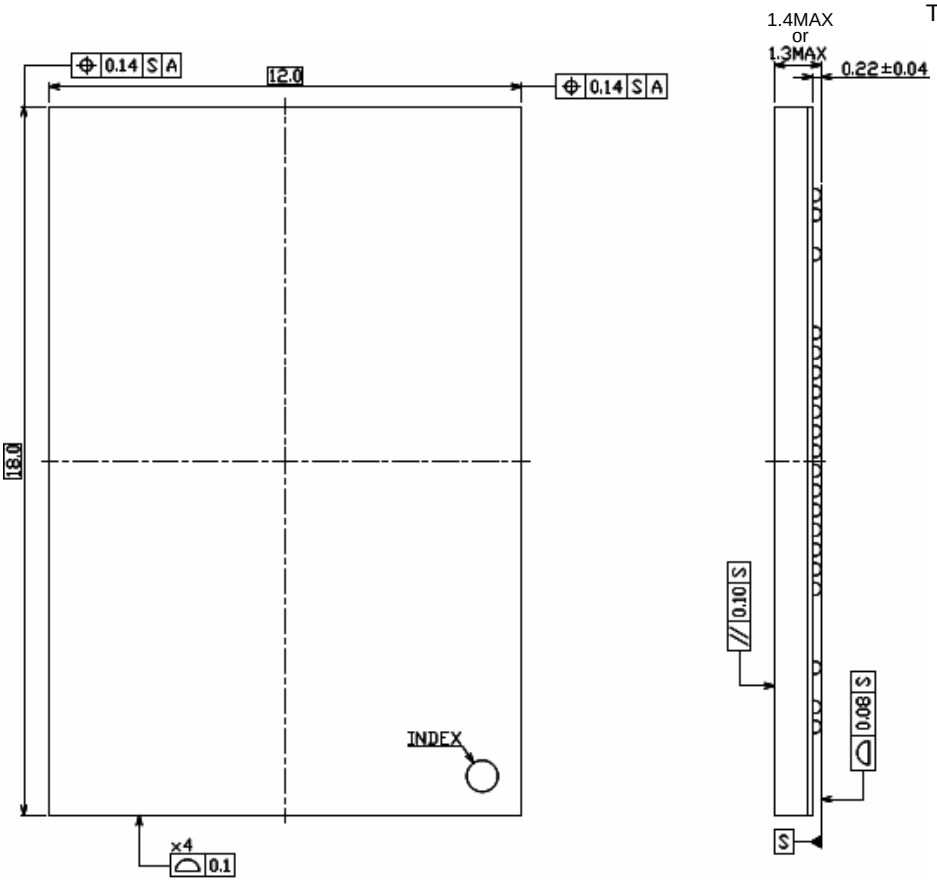
Unit: mm
Tolerance: ±0.1 mm

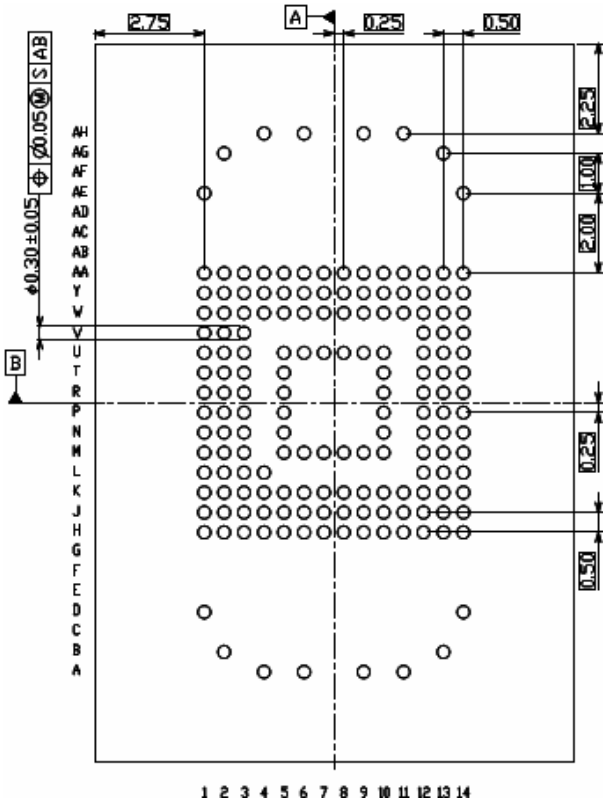




12mm x 18mm x 1.3mm(max)
12mm x 18mm x 1.4mm(max)

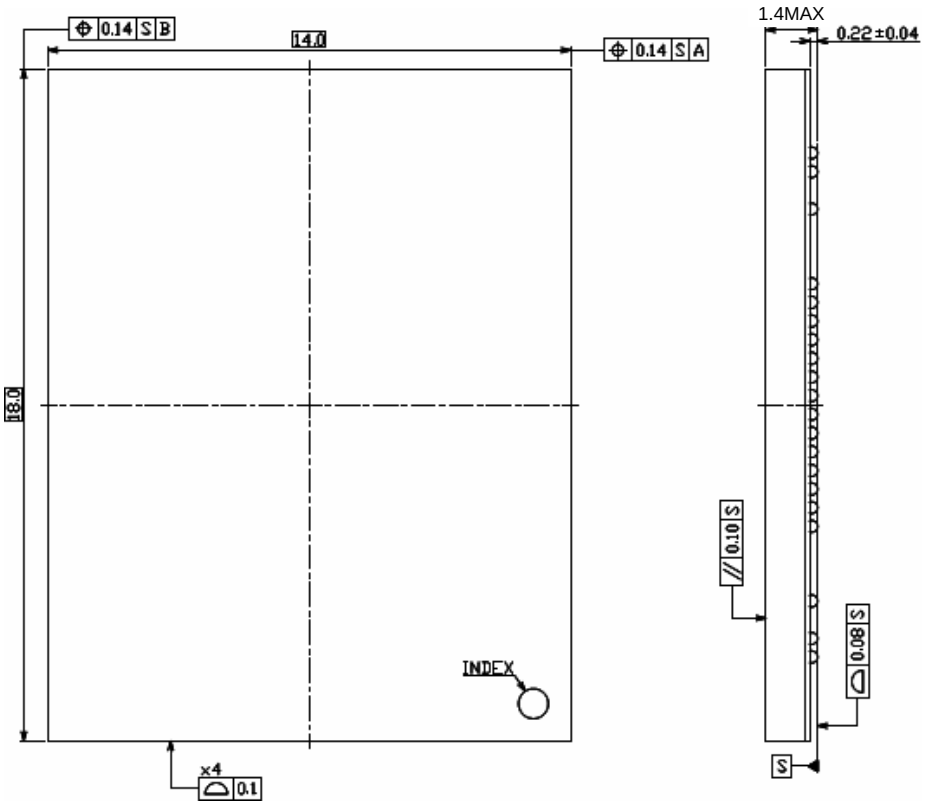
Unit: mm
Tolerance: ±0.1 mm

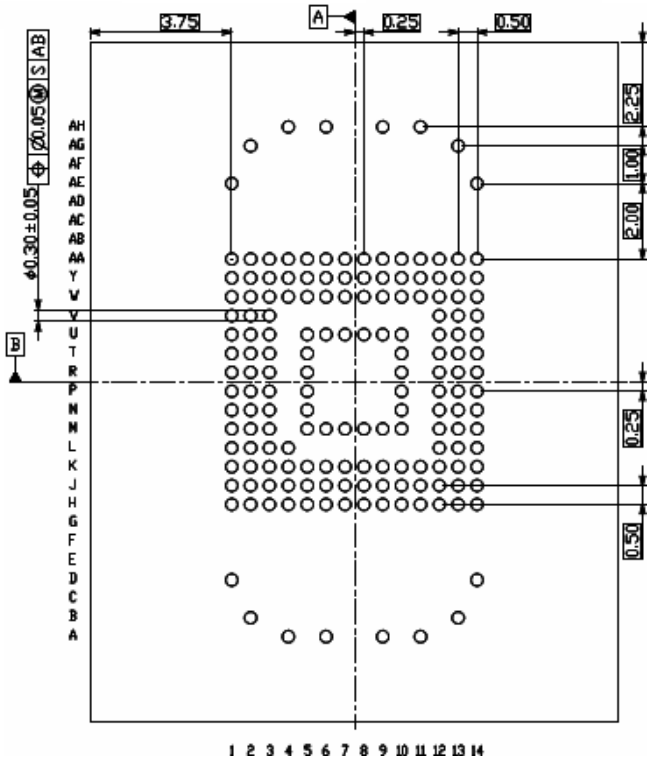




14mm x 18mm x 1.4mm(max)

Unit: mm
Tolerance: ±0.1 mm





Density Specifications

THGBM1GxDxEBAIx series Densities

Parameter	1GByte	2GByte	4Gbyte	8GByte	16Gbyte	32Gbyte
User area density	TBD	TBD	4,001,366,016	8,006,926,336	16,007,561,216	32,015,122,432
SEC_COUNT in Extended CSD	TBD	TBD	0x00774000	0x00EEA000	0x01DD1000	0x3BA2000

Register Informations

OCR Register

OCR bit	VDD Voltage window	Value
[6:0]	Reserved	000 000b
[7]	1.70-1.95	1b
[14:8]	2.0-2.6	000 000b
[23:15]	2.7-3.6	1 1111 1111b
[28:24]	Reserved	0 0000b
[30:29]	Access Mode	10b [2]
[31]	(card power up status bit (busy))[1]	

1) This bit is set to LOW if the card has not finished the power up routine.
2) In THGBM1G3D1EBAI8(1GB) and THGBM1G4D1EBAI7(2GB) case, the value is 00b.

CID Register

CID bit	Name	Field	Width	Value
[127:120]	Manufacturer ID	MID	8	0001 0001b
[119:114] *	Reserved	-	6	0b
[113:112] *	Card/BGA	CBX	2	01b
[111:104] *	OEM/Application ID	OID	8	0b
[103:56]	Product name	PNM	48	see product name table
[55:48]	Product revision	PRV	8	0000 0001b
[47:16]	Product serial	PSN	32	Serial number
[15:8]	Manufacturing date	MDT	8	see-MMCA Specification
[7:1]	CRC7 checksum	CRC	7	CRC7
[0]	Not used, always '1'	-	1	1b

Product name table (In CID Register)

Part number	Product name in CID Register	Density
THGBM1G3D1EBAI8	0x4D4D43303147 (MMC01G)	1-GBytes
THGBM1G4D1EBAI7	0x4D4D43303247 (MMC02G)	2-GBytes
THGBM1G5D2EBAI7	0x4D4D43303447 (MMC04G)	4-GBytes
THGBM1G6D4EBAI4	0x4D4D43303847 (MMC08G)	8-GBytes
THGBM1G7D8EBAI0	0x4D4D43313647 (MMC16G)	16-GBytes
THGBM1G7D4EBAI2	0x4D4D43313647 (MMC16G)	16-GBytes
THGBM1G8D8EBAI2	0x4D4D43333247 (MMC32G)	32-GBytes

CSD Register

CSD bit	Name	Field	Width	Cell Type	Value					
					1GB	2GB	4GB	8GB	16GB	32GB
[127:126]	CSD Structure	CSD_STRUCTURE	2	R	10b					
[125:122]	System specification version	SPEC_VERS	4	R	0x4					
[121:120]	Reserved	-	2	R	00b					
[119:112]	Data read access-time 1	TAAC	8	R	0x0E					
[111:104]	Data read access-time 2 in CLK cycles (NSAC * 100)	NSAC	8	R	0x00					
[103:96]	Max. bus clock frequency	TRAN_SPEED	8	R	0x32					
[95:84]	Card command classes	CCC	12	R	0x0f5					
[83:80]	Max. read data block length	READ_BL_LEN	4	R	0x9	0xA*	0x9	0x9	0x9	0x9
[79:79]	Partial blocks for read allowed	READ_BL_PARTIAL	1	R	0b					
[78:78]	Write block misalignment	WRITE_BLK_MISALIGN	1	R	0b					
[77:77]	Read block misalignment	READ_BLK_MISALIGN	1	R	0b					
[76:76]	DSR implemented	DSR_IMP	1	R	0b					
[75:74]	Reserved	-	2	R	00b					
[73:62]	Device size	C_SIZE	12	R	TBD	TBD	0xFFF	0xFFF	0xFFF	0xFFF
[61:59]	Max. read current @ VDD min.	VDD_R_CURR_MIN	3	R	111b					
[58:56]	Max. read current @ VDD max.	VDD_R_CURR_MAX	3	R	111b					
[55:53]	Max. write current @ VDD min.	VDD_W_CURR_MIN	3	R	111b					
[52:50]	Max. write current @ VDD max.	VDD_W_CURR_MAX	3	R	111b					
[49:47]	Device size multiplier	C_SIZE_MULT	3	R	0x7					
[46:42]	Erase group size	ERASE_GRP_SIZE	5	R	0x1F					
[41:37]	Erase group size multiplier	ERASE_GRP_MULT	5	R	0x1F					
[36:32]	Write protect group size	WP_GRP_SIZE	5	R	0x03					0x07
[31:31]	Write protect group enable	WP_GRP_Enable	1	R	1b					
[30:29]	Manufacturer default ECC	DEFAULT_ECC	2	R	00b					
[28:26]	Write speed factor	R2W_FACTOR	3	R	0x5					
[25:22]	Max. write data block length	WRITE_BL_LEN	4	R	0x9					
[21:21]	Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	0b					
[20:17]	Reserved	-	4	R	0x0					
[16:16]	Content protection application	CONTENT_PROT_APP	1	R	0b					
[15:15]	File format group	FILE_FORMAT_GRP	1	R	0b					
[14:14]	Copy flag (OTP)	COPY	1	R	0b					
[13:13]	Permanent write protection	PERM_WRITE_PROTECT	1	R	0b					
[12:12]	Temporary write protection	TMP_WRITE_PROTECT	1	R	0b					
[11:10]	File format	FILE_FORMAT	2	R	00b					
[9:8]	ECC code	ECC	2	R	00b					
[7:1]	CRC	CRC	7	R	CRC					
[0]	Not used, always ‘1’	-	1	-	1b					

* READ_BL_LEN has to be equal to WRITE_BL_LEN in the Specification. However, Exception to this rule is the 2GB of density device that should indicate 1KB access size in READ_BL_LEN, and this device does not support 1KB access size.

Extended CSD Register

CSD-slice	Name	Field	Size (Bytes)	Cell Type	Value	
[511:505]	Reserved	-	7	-	All '0'	
[504]	Supported Command Sets	S_CMD_SET	1	R	0x00	
[503:229]	Reserved	-	275	-	All '0'	
[228]	Boot information	BOOT_INFO	1	R	0x01	
[227]	Reserved	-	1	R	All '0'	
[226]	Boot partition size	BOOT_SIZE_MULTI	1	R	0x04	
[225]	Access size	ACC_SIZE	1	R	0x07*	0x06
[224]	High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	0x08**	0x04
[223]	High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	0x01	
[222]	Reliable write sector count	REL_WR_SEC_C	1	R	0x10***	
[221]	High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	0x01	
[220]	Sleep current (Vcc)	S_C_VCC	1	R	0x09	
[219]	Sleep current (VccQ)	S_C_VCCQ	1	R	0x07	
[218]	Reserved	-	1	-	All '0'	
[217]	Sleep/awake timeout	S_A_TIMEOUT	1	R	0x10	
[216]	Reserved	-	1	-	All '0'	
[215:212]	Sector Count	SEC_COUNT	4	R	see Capacity Specification table	
[211]	Reserved	-	1	-	All '0'	
[210]	Minimum Write Performance for 8bit @ 52MHz	MIN_PERF_W_8_52	1	R	0x00	
[209]	Minimum Read Performance 8bit @ 52MHz	MIN_PERF_R_8_52	1	R	0x3C	
[208]	Minimum Write Performance for 8bit @ 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	1	R	0x00	
[207]	Minimum Read Performance for 8 bit @ 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	1	R	0x3C	
[206]	Minimum Write Performance for 4bit @ 26MHz	MIN_PERF_W_4_26	1	R	0x00	
[205]	Minimum Read Performance for 4bit @ 26MHz	MIN_PERF_R_4_26	1	R	0x1E	
[204]	Reserved	-	1	-	All '0'	
[203]	Power Class for 26MHz @ 3.6V	PWR_CL_26_360	1	R	0x02****	0x00
[202]	Power Class for 52MHz @ 3.6V	PWR_CL_52_360	1	R	0x02****	0x00
[201]	Power Class for 26MHz @ 1.95V	PWR_CL_26_195	1	R	0x06****	0x00
[200]	Power Class for 52MHz @ 1.95V	PWR_CL_52_195	1	R	0x06****	0x00
[199:197]	Reserved	-	3	-	All '0'	
[196]	Card Type	CARD_TYPE	1	R	0x03	
[195]	Reserved	-	1	-	All '0'	
[194]	CSD Structure Version	CSD_STRUCTURE	1	R	0x02	
[193]	Reserved	-	1	-	All '0'	
[192]	Extended CSD Revision	EXT_CSD_REV	1	R	0x03	
[191]	Command Set	CMD_SET	1	R/W	Can be set	
[190]	Reserved	-	1	-	All '0'	
[189]	Command Set Revision	CMD_SET_REV	1	RO	0x00	
[188]	Reserved	-	1	-	All '0'	
[187]	Power Class	POWER_CLASS	1	R/W	Can be set	

[186]	Reserved	-	1	-	All ‘0’
[185]	High Speed Interface Timing	HS_TIMING	1	R/W	Can be set
[184]	Reserved		1	-	All ‘0’
[183]	Bus Width Mode	BUS_WIDTH	1	WO	Can be set
[182]	Reserved	-	1	-	All ‘0’
[181]	Erased Memory Content	ERASED_MEM_CONT	1	RO	0x01
[180]	Reserved	-	1	-	All ‘0’
[179]	Boot configuration	BOOT_CONFIG	1	R/W	Can be set
[178]	Reserved	-	1	-	All ‘0’
[177]	Boot bus width	BOOT_BUS_WIDTH	1	R/W	Can be set
[176]	Reserved	-	1	-	All ‘0’
[175]	High-density erase group definition	ERASE_GROUP_DEF	1	R/W	Can be set
[174:0]	Reserved	-	175	-	All ‘0’

(Note)

*ACC_SIZE

THGBM1G7D4EBAI2(16-GBytes) and THGBM1G8D8EBAI2(32-GBytes) case, the values are 0x07

**HC_ERASE_GRP_SIZE

THGBM1G7D4EBAI2(16-GBytes) and THGBM1G8D8EBAI2(32-GBytes) case, the values are 0x08

***REL_WR_SEC_C

Reliable write address for 8Kbyte data size, should be aligned on the boundary of 8Kbytes.

****PWR CL

THGBM1G7D4EBAI2(16-GBytes) and THGBM1G8D8EBAI2(32-GBytes) case, the values are 0x02

ELECTRICAL CHARACTERISTICS

DC Characteristics

General

Parameter	Symbol	Test Conditions	Min	Max	Unit
Peak voltage on all lines			-0.5	VccQ+0.5	V
All Inputs					
Input Leakage Current (before initialization sequence[1] and/or the internal pull up resistors connected)			–100	100	μA
Input Leakage Current (after initialization sequence and the internal pull up resistors disconnected)			–10	10	μA
All Outputs					
Output Leakage Current (before initialization sequence)			-100	100	μA
Output Leakage Current (after initialization sequence)			-10	10	μA

1) Initialization sequence is defined in Section 12.3 of JEDEC/MMCA Standard 4.3

Power Supply Voltage

Parameter	Symbol	Test Conditions	Min	Max	Unit
Supply voltage 1	V_{CC}		2.7	3.6	V
Supply voltage 2	VccQ		1.7	1.95	V
			2.7	3.6	V

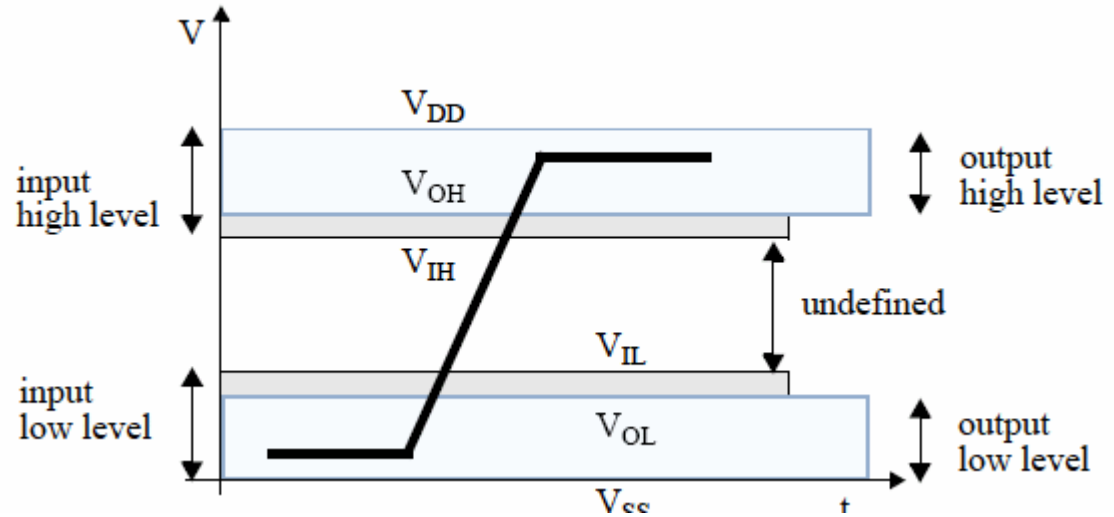
Supply Current

Parameter		Symbol	Test Conditions	Min	Max	Unit
Operation (RMS)	Read	I_{ROP}		—	100	mA
	Write	I_{WOP}		—	100	mA

Internal resistance and Device capacitance

Parameter	Symbol	Test Conditions	Min	Max	Unit
Single device capacitance	C_{CARD}		—	12	pF
Internal pull up resistance DAT1 – DAT7	R_{INT}		50	150	kOhm

Bus Signal Levels



Open-Drain Mode Bus Signal Level

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output HIGH voltage	V_{OH}		VccQ - 0.2	—	V
Output LOW voltage	V_{OL}		—	0.3	V

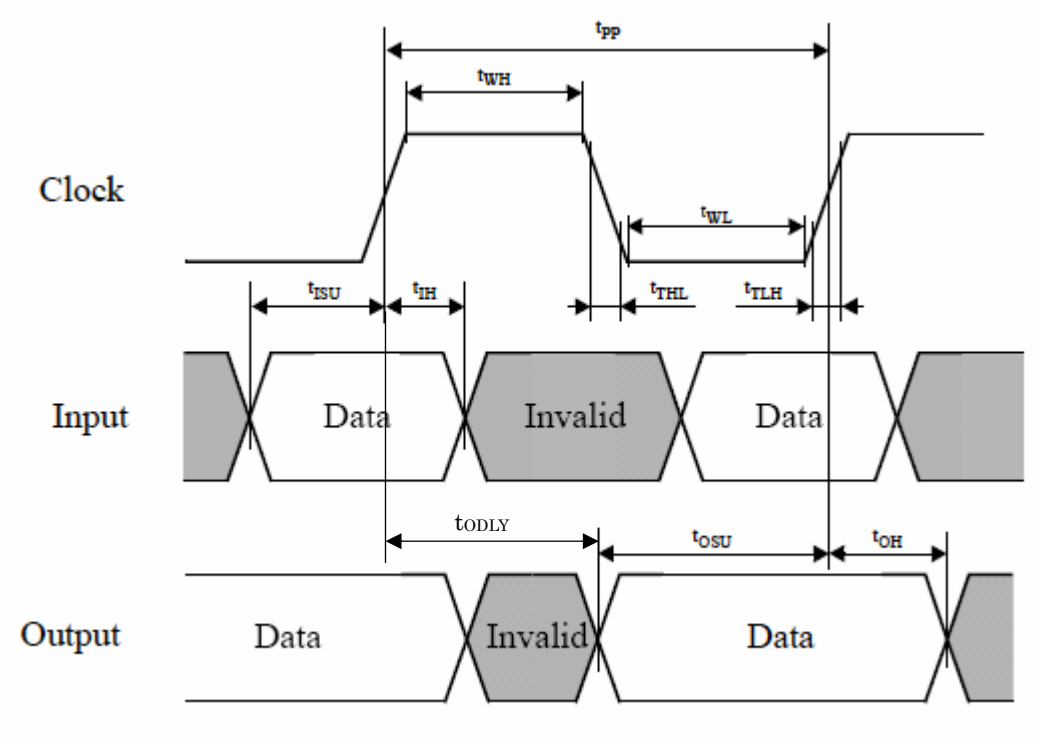
Push-Pull Mode Bus Signal Level (High-Voltage)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output HIGH voltage	V_{OH}	I_{OH} = -100µA @ $V_{DD\ min}$	0.75 * VccQ	—	V
Output LOW voltage	V_{OL}	I_{OL} = 100µA @ $V_{DD\ min}$	—	0.125 * VccQ	V
Input HIGH voltage	V_{IH}		0.625* VccQ	VccQ + 0.3	V
Input LOW voltage	V_{IL}		V_{SS} - 0.3	0.25 * VccQ	V

Push-Pull Mode Bus Signal Level (Low-Voltage)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output HIGH voltage	V_{OH}	I_{OH} = -100µA @ $V_{DD\ min}$	VccQ - 0.2	—	V
Output LOW voltage	V_{OL}	I_{OL} = 100µA @ $V_{DD\ min}$	—	0.2	V
Input HIGH voltage	V_{IH}		0.7 * VccQ	VccQ + 0.3	V
Input LOW voltage	V_{IL}		V_{SS} - 0.3	0.3 * VccQ	V

Bus Signal Levels



Card Interface Timings (High-speed interface timing)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Clock frequency Data Transfer Mode (PP)[2]	f_{pp}	C_L <= 30pF Tolerance: +100KHz	0	52	MHz
Clock frequency Identification Mode (OD)	f_{OD}	Tolerance: +20KHz	0	400	KHz
Clock low time	t_{WL}	C_L <= 30pF	6.5	—	ns
Clock rise time	t_{TLH}	C_L <= 30pF	—	3	ns
Clock fall time	t_{THL}	C_L <= 30pF	—	3	ns
Inputs CMD,DAT (referenced to CLK)					
Input set-up time	t_{ISU}	C_L <= 30pF	3	—	ns
Input hold time	t_{IH}	C_L <= 30pF	3	—	ns
Outputs CMD,DAT (referenced to CLK)					
Output Delay time during Data Transfer	t_{ODLY}	C_L <= 30pF	0	13.7	ns
Output hold time	t_{OH}	C_L <= 30pF	2.5	—	ns
Signal rise time [4]	t_{rise}	C_L <= 30pF	—	3	ns
Signal fall time	t_{fall}	C_L <= 30pF	—	3	ns

1) CLK timing is measured at 50% of VccQ
2) THGBM1GxDxEBAIx shall support the full frequency range from 0-26MHz, or 0-52MHz
3) e-MMC can operate as high-speed interface timing at 26MHz clock frequency.
4) CLK rise and fall times are measured by min(VIH) and max(VIL).
5) Inputs CMD,DAT rise and fall times area measured by min(VIH) and max(VIL), and outputs CMD, DAT rise and fall times are measured by min(VOH) and max(VOL).

Card Interface Timings (Backward-compatible interface timing)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Clock frequency Data Transfer Mode (PP)[2]	f_{pp}	C_L <= 30pF	0	26	MHz
Clock frequency Identification Mode (OD)	f_{OD}	Tolerance: +20KHz	0	400	KHz
Clock low time	t_{WL}	C_L <= 30pF	10	—	ns
Clock rise time	t_{TLH}	C_L <= 30pF	—	10	ns
Clock fall time	t_{THL}	C_L <= 30pF	—	10	ns
Inputs CMD,DAT (referenced to CLK)					
Input set-up time	t_{ISU}	C_L <= 30pF	3	—	ns
Input hold time	t_{IH}	C_L <= 30pF	3	—	ns
Outputs CMD,DAT (referenced to CLK)					
Output set-up time	t_{OSU}	C_L <= 30pF	11.7	—	ns
Output hold time	t_{OH}	C_L <= 30pF	8.3	—	ns

1) The e-MMC must always start with the backward-compatible interface timing. The timing mode can be switched to high-speed interface timing by the host sending the SWITCH command (CMD6) with the argument for high-speed interface select.

2) CLK timing is measured at 50% of VccQ

3) For compatibility with e-MMCs that support the v4.2 standard or earlier, host should not use >20MHz before switching to high-speed interface timing.

4) CLK rise and fall times are measured by min(VIH) and max(VIL).

Functional restrictions

TBD if necessary.

Reliability Guidance

This reliability guidance is intended to notify some guidance related to using raw MLC NAND flash. For detailed reliability data, please refer to TOSHIBA's reliability note. Although random bit errors may occur during use, it does not necessarily mean that a block is bad. Generally, a block should be marked as bad when a program status failure or erase status failure is detected. The other failure modes may be recovered by a block erase. ECC treatment for read data is mandatory due to the following Data Retention and Read Disturb failures.

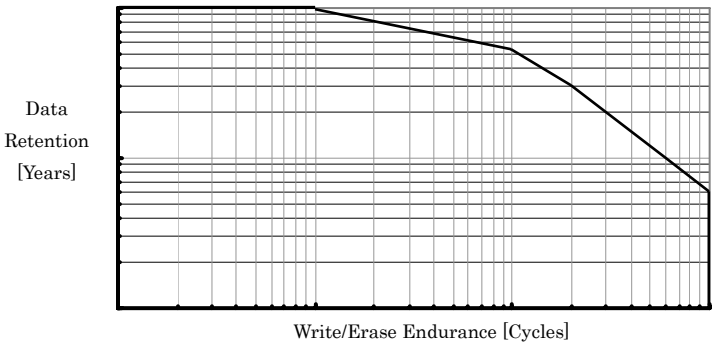
-Write/Erase Endurance

Write/Erase endurance failures may occur in a cell, page, or block, and are detected by doing a status read after either an auto program or auto block erase operation. The cumulative bad block count will increase along with the number of write/erase cycles.

-Data Retention

The data in memory may change after a certain amount of storage time. This is due to charge loss or charge gain. After block erasure and reprogramming, the block may become usable again.

Here is the combined characteristics image of Write/Erase Endurance and Data Retention.



-Read Disturb

A read operation may disturb the data in memory. The data may change due to charge gain. Usually, bit errors occur on other pages in the block, not the page being read. After a large number of read cycles (between block erases), a tiny charge may build up and can cause a cell to be soft programmed to another state. After block erasure and reprogramming, the block may become usable again.

Document Revision History

Rev1.0	May 9th, 2008	Released as an initial version
Rev1.1	Oct 24th, 2008	32Gbyte User area density is defined. Access size (ACC_SIZE), High-capacity area unit size (HC_ERASE_GRP_SIZE) and Power Class (PWR_CL) values are updated.
Rev1.2	Oct 31th, 2008	Product weight of 4GByte/8GByte/16GByte(8 x 16Gbit MLC)/32Gbyte are added.
Rev1.3	Nov 6th, 2008	A comment regarding reliable write is added
Rev1.4	Dec 8th, 2008	In Extended CSD register [208 : 207], 4bit at 52MHz expressions were added.

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070122EBA_R6

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