MOS INTEGRATED CIRCUIT
μPD9323

MOTION DETECTION LSI FOR THE IMPROVED DEFINITION TV

The μPD9323 is a motion detection processor (MDP) LSI for the improved definition TV (IDTV). This LSI detects whether the input signal represents a still picture part or a motion picture part, and generates motion signal adaptively to the magnitude of the motion.

In combination with five LSIs (YCS, YCP, YCI, CDU, and CKG), this LSI can configure an IDTV signal processing system.

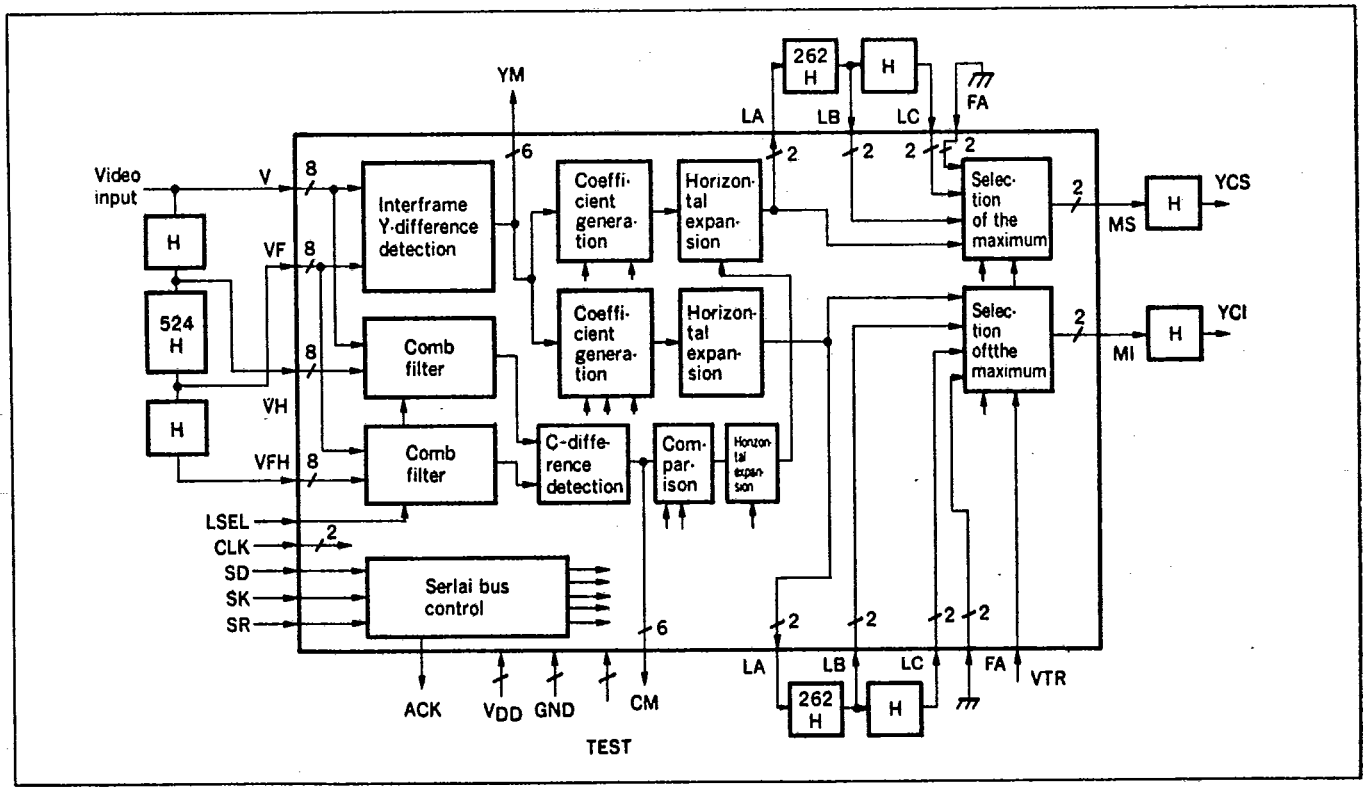
FEATURES

- Detects interframe luminance differencial signal.
- Capable of detecting the interframe color difference signal.
- Built-in motion signal expander: Horizontal, line, and field.
- Serial bus control
- +5 volts single power supply.
- Low-power consumption due CMOS circuiting.
- 100 PIN PLASTIC QFP

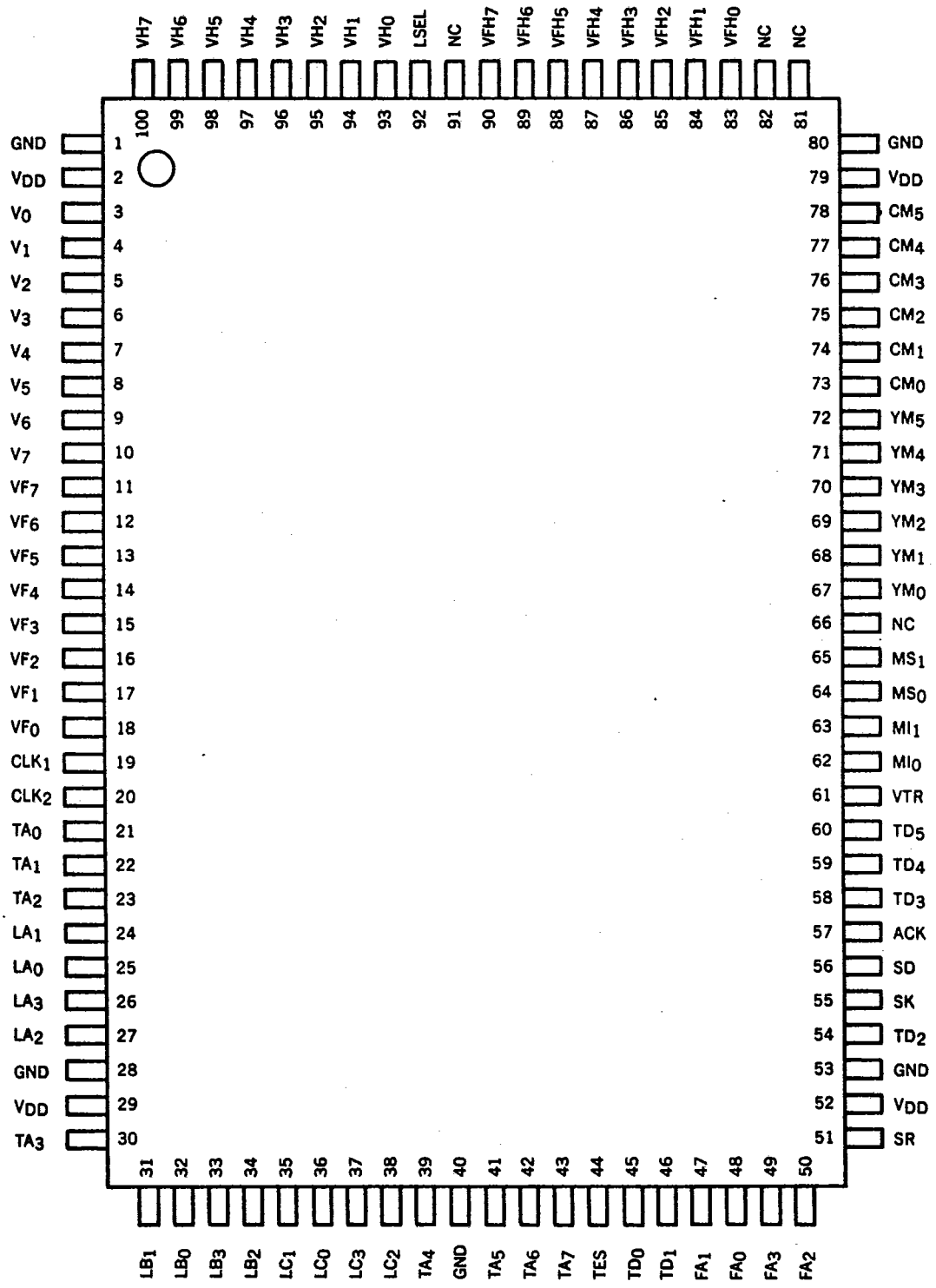
ORDERING INFORMATION

Part Number	Package
μPD9323GF-3BA	100 PIN PLSTIC QFP (14 x 20)

BLOCK DIAGRAM

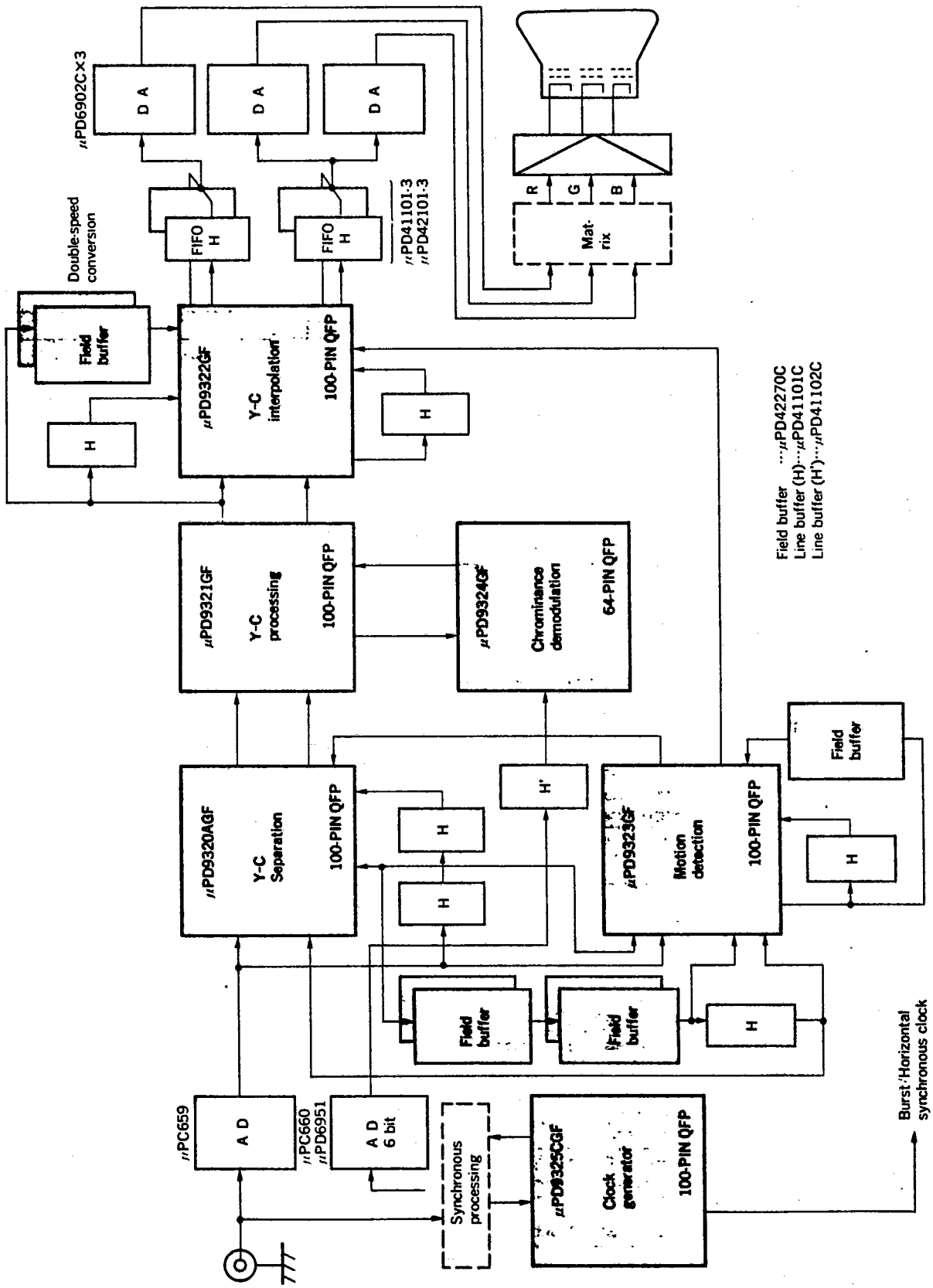


CONNECTION DIAGRAM (Top View)



LSI SYSTEM CONFIGURATION FOR THE 1DTV

T-77-07-09



T-77-07-09

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Source Voltage	V_{DD}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−0.5 to V_{DD} +0.5	V
Output Current	I_{OUT}	20	mA
Package Allowable Dissipation	P_D	400	mW
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = −20 to +75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Source Voltage	V_{DD}	4.5	5.0	5.5	V	
Low-Level Input Voltage	V_{IL}	0		0.3 V_{DD}	V	Input terminals: VTR, LSEL, and CLK (CMOS input)
High-Level Input Voltage	V_{IH}	0.7 V_{DD}		V_{DD}	V	
Low-Level Input Voltage	V_{IL}	0		0.8	V	Input terminals: V, VH, VF, VFH, LB, LC, and FA (TTL input)
High-Level Input Voltage	V_{IH}	2.4		V_{DD}	V	
High-Level Input Voltage	V_{IH}	1.8		4.0	V	Input terminals: SD, SK, and SR (Schmitt input)
Low-Level Input Voltage	V_{IL}	0.6		3.1	V	
Hysteresis Voltage	V_H	0.3		1.5	V	
Clock Frequency	F_{CLK}		14.3		MHz	

ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V ±10 %, T_a = −20 to +75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Current	I_{DD}		50		mA	
Low-Level Output Current	I_{OL}	4	11		mA	V_{OL} = 0.4 V
High-Level Output Current	$-I_{OH}$	4	8		mA	V_{OH} = V_{DD} − 0.4 V
Input Current	$\pm I_I$			10	μA	V_I = V_{DD} or GND
Input Current	I_I	25	80	260	μA	V_I = V_{DD} Pull-down resistor input
Output Delay Time	T_d		18		ns	
Input Terminal Capacitance	C_{IN}			10	pF	V_{DD} = V_I = 0 f = 1MHz
Output Terminal Capacitance	C_{OUT}			15	pF	

TERMINAL DESCRIPTION (MDP)

T-77-07-09

TERMINAL SYMBOL	TERMINAL NAME	TERMINAL NUMBER	FUNCTIONS	
V_0 to V_7	Video input	3 ~ 10	Input (TTL)	Inputs the A/D converted eight-bit video signal. (V_0: LSB, V_7: MSB)
VH_0 to VH_7	Video input (Delayed by 1H)	93 ~100	Input (TTL)	Input the 1H-delayed video signal. (VH_0: LSB, VH_7: MSB)
VF_0 to VF_7	Video input (Delayed) by one frame)	18 ~11	Input (TTL)	Inputs the one-frame (525H) delayed video signal. (VF_0: LS, VF_7: MSB)
VFH_0 to VFH_7	Video inputs (1F + 1H delayed)	80 ~ 90	Input (TTL)	Inputs the one-frame (526H) delayed video signal. (VFH_0: LSB, VFH_7: MSB)
MS_0 MS_1	YC separation motion output	64 65	Output (CMOS)	Delays the signal by 1H and outputs it to the YCS. This signal controls the adaptive selection of the YC separation process. Delayed by 15 clocks relative to the video input. (MS0: LSB, MS1: MSB)
MI_0 MI_1	Y interpolation motion output	62 63	Output (CMOS)	Outputs the 1H-delayed signal to the YCI. This signal controls the adaptive selection of Y interpolation. Outputs the signal 31 clocks after the video input. (MI0: LSB, MI1: MSB)
YM_0 to YM_5	Luminance motion output	67 ~ 72	Output (CMOS)	This terminal outputs the signal to the CKG. The signal is the one-frame difference luminance motion signal. (YM_0: LSB, YS_5: MSB)
CM_0 to CM_5	Chrominance motion output	73 ~ 78	Output (CMOS)	Outputs the one-frame difference chrominance motion signal. (CM_0: LSB, CM_5: MSB)
LA_0 LA_1	Expansion motion output (MS)	25 24	Output (CMOS)	This output is used to expand the YC separation motion signal. (LA_0: LSB, LA_1: MSB)
LA_2 LA_3	Expansion motion output (MI)	27 26	Output (CMOS)	This output is used to expand the Y interpolation motion signal. (LA_2: LSB, LA_3: MSB)
LB_0 LB_1	Expander motion input (MS: Delayed by 262H)	32 31	Input (TTL)	Inputs the one-field (262H) delayed LA output signal. This input is used to expand the YC separation motion signal.
LB_2 LB_3	Expander motion input (MI: Delayed by 262H)	34 33	Input (TTL)	Inputs the one-field (262H) delayed LA output signal. This input is used to expand the Y interpolation motion.
LC_0 LC_1	Expander motion input (MS: Delayed by 263H)	35 36	Input (TTL)	Inputs the one-field (263H) delayed LA output signal. This input is used to expand the YC separation motion signal.
LC_2 LC_3	Expander motion input (MI: Delayed by 263H)	38 37	Input (TTL)	Input the one-field (263H) delayed LA output signal. This input is used to expand the Y interpolation motion signal.
FA_0 FA_1	Expander motion input (MS)	48 47	Input (TTL)	This input is used to expand the YC separation motion signal. Connect this terminal to the GND terminal when not in use.
FA_2 FA_3	Expander motion input (MI)	50 49	Input (TTL)	This input is used to expand the Y interpolation motion signal. Connect this terminal to the GND terminal when not in use.
VTR	Forced motion input	61	Input Pull-down R	MI/MS output is made the motion mode signal (1, 1) when this terminal is set to "H".
LSEL	Color separation filter selection	92	Input Pull-down R	Selects the color separation filter for detecting the chrominance motion signal. Normally operated at "0". (0:1H comb filter, 1: BPF)
SD	Serial data	56	Input CMOS Schmitt	The data is input from the controller. Serves as the serial data line.
SK	Serial clock	55	Input CMOS Schmitt	The clock signal is input from the controller. Serves as the serial clock line.
SR	Serial reset	51	Input CMOS Schmitt	The signal is input from the controller. Serves as the serial bus set line.

T-77-07-09

TERMINAL SYMBOL	TERMINAL NAME	TERMINAL NUMBER	FUNCTIONS	
ACK	Acknowledge	57	Output (N-open)	Serial bus acknowledge output terminal. This terminal continues to output "L" level every ninth clock while its address is being selected.
CLK1 CLK2	Clock	19 20	Input (CMOS)	The clock is input from the CKG. Inputs the 4FSC (14.3 MHz) system clock.
TES	Test input	44	Input	Test input terminal. Connect this terminal to the GND terminal.
TA_0 to TA_7	Test input A	21 ~ 23 30 39 ~ 43	Input	Test input terminal. Connected to the GND terminal.
TD_0 to TD_7	Test input D	45 ~ 46 54 58 ~ 60	Input	Test input terminal. Connected to the GND terminal.
V_{DD}	Supply terminal	2 29 52 79		The supply input terminal. Apply +5 volts to this terminal.
GND	Grounding terminal	1 28 40 53 80		Grounding terminal.

DESCRIPTION OF FUNCTIONS

T-77-07-09

1. Motion Signal Detection

The μPD9323 has a built-in circuit to generate the motion signal to suit the motion of the picture parts detected by the signal difference in one frame in the unit of dot.

This LSI is composed of the following four circuit blocks:

(1) Y Difference Detection Circuit
Detects the luminance signal difference in one frame.

(2) Collor Difference Detection circuit
Detects the color signal difference in one frame.

(3) Coefficient Generator Circuit
Converts the Y-difference of the motion signal into two factors (two bits) for the YC separation and Y interpolation motion output data.

(4) Motion Signal Expander Circuit
Expands the factored motion signal in the horizontal line, vertical line, and time (field).

1-1 Y Difference Detection Circuit

This circuit detects the interframe luminance signal difference.

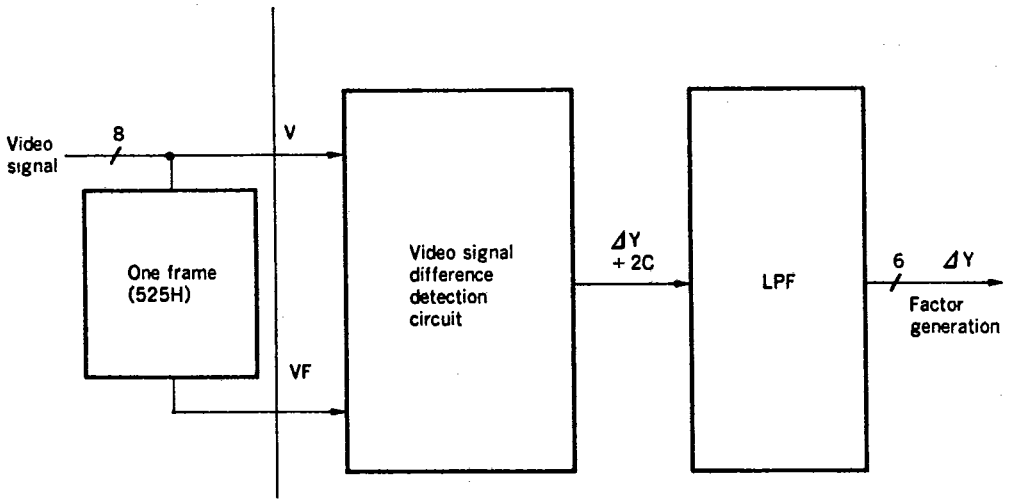
This circuit calculates the difference between the signal in the present frame and that in the one-frame delayed frame using the video signal difference detection circuit, and detects based on the difference the interframe luminance difference ΔY and the adder signal 2C of the color signal.

Interframe difference = interframe luminance difference (ΔY) + color signal (2C)

The LPF removes the color signal 2C and extracts the luminance interframe difference ΔY from the detected signal.

The most significant bits of ΔY are limited and output as the six-bit absolute signal for unit gain. Note that this signal is output to external terminals as the Y luminance output (YM_0 to YM_5).

Fig. 1 Y Difference Detection Circuit Block Diagram



T-77-07-09

1-2 Color Difference Detection Circuit

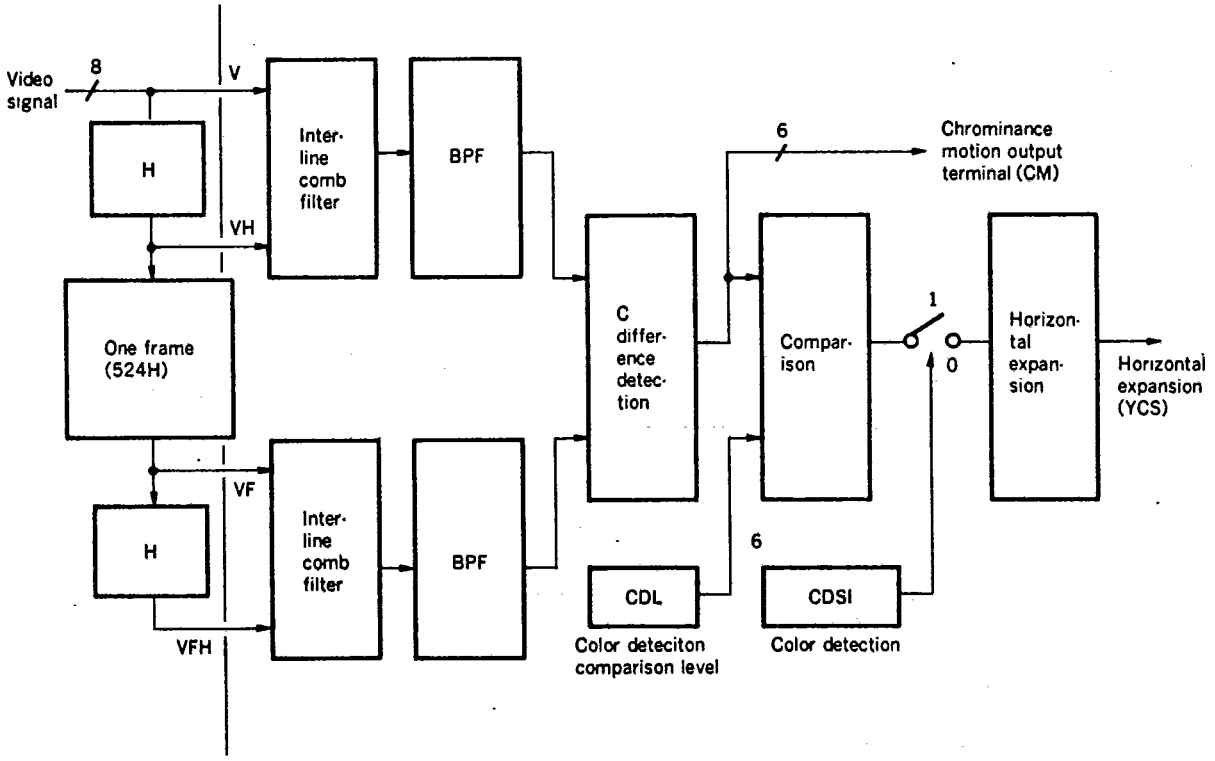
This circuit detects the interframe color signal difference.

Using the 1H form interline YC separation circuit and the BPF, this circuit cores the present video signal of the color signal. Using the 1H form interline YC separation circuit and the BPF, this circuit extracts the one-frame delayed color signal from the one-frame-delayed video signal.

These color signals are used by the C difference detection circuit to detect the interframe color signal difference. The output of this difference is compared with the six-bit data (0 to 63) of the color detection comparison level (CDL) input from the serial bus from the comparison detection circuit, and used to generate the signal showing whether there is motion in color or not. The output from the comparison circuit is horizontally expanded by the horizontal expansion circuit by one sample and output to the YC separation motion signal expander circuit. When motion in the color is detected in this process, the YC separation filter is separated into the in-the-field YC separation.

To inhibit color difference detection by this detection circuit, set the color detection bit (CDSI) to "1" using the serial bus.

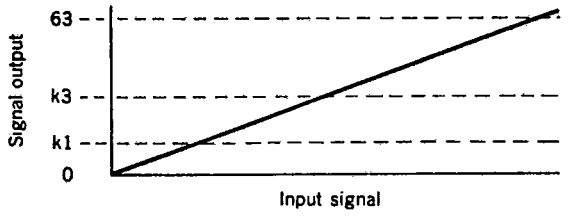
Fig. 2 Color Difference Detection Circuit



1-3 Factor Generation Circuit

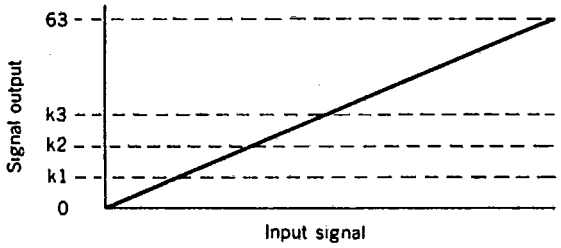
This circuit performs the YC separation of the Y difference in the motion signals and converts the difference into the Y interpolation motion signal output (two bits).

The luminance interframe difference signal ΔY in the six bits from the Y difference detection circuit is converted into two-bit outputs based on the two factors, "MSk1" and "MSk3" input from the serial bus, in the YC separation factors generation circuit.



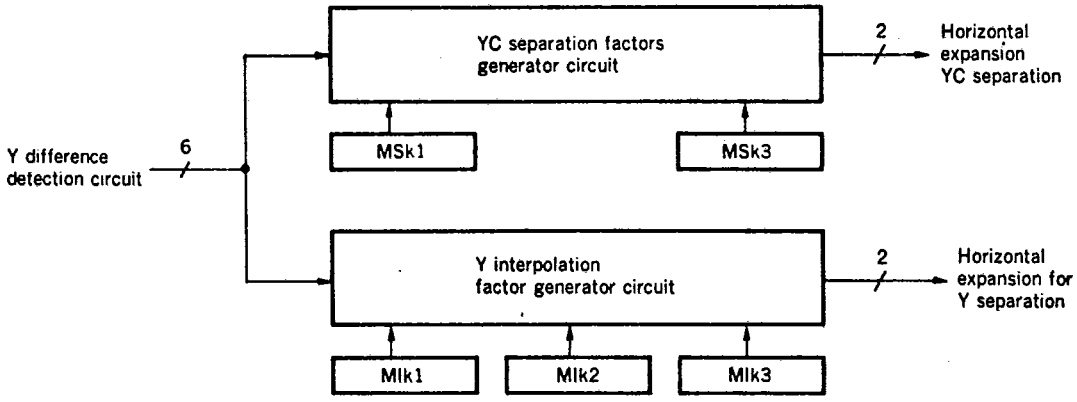
Input Signal					Output in the Factor Generator	
					MSB	LSB
0	<	MD	<	MSk1	0	0
MSk1	<	MD	<	MSk3	0	1
MSk3	<	MD	<	63	1	1

The interframe luminance signal ΔY is then converted into two-bit data using the three factors, "MSK1", "MSK2" and "MSK3" input through the serial bus, in the Y interpolation factor generator circuit.



Input Signal					Output from the Factor Generator	
					MSB	LSB
0	<	MD	<	MSk1	0	0
MSk1	<	MD	<	MSk2	0	1
MSk2	<	MD	<	MSk3	1	0
MSk3	<	MD	<	63	1	1

Fig. 3 Diagram of Factor Generator Circuit



T-77-07-09

1-4 Motion Signal Expansion Circuit

This circuit expands the factored motion signal in three dimensions: horizontal line, vertical line, and time (field).

The two-bit output signal from the YC separation factor generator circuit is horizontally expanded (in the left-right directions) by 210 ns in the horizontal expansion circuit and output to the expansion motion signal output terminals (LA_0, LA_1). At these terminals, the expanded signal is mixed with the output from the color difference detection circuit.

The maximum selection circuit selects and outputs the maximum of this mixed signal, expansion motion input (LB_0, LB_1), (LC_0, LC_1), and (FA_0, FA_1), and expands the selected motion signal in the vertical line and time (field) dimensions using the external delay line or field delay line.

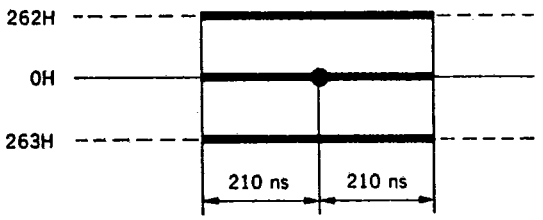
A similar operation will be carried out on the Y interpolation signal. The two-bit signal output from the Y interpolation factor generator circuit is horizontally expanded (to the left and right by 210 ns each) in the horizontal expansion circuit and output to the expansion motion output terminals (LA_2, LA_3).

The maximum selection circuit selects and outputs the maximum of this mixed signal, expansion motion input (LB_2, LB_3), (LC_2, LC_3), and (FA_2, FA_3), and expands the selected motion signal in the vertical line and time (field) dimensions using the external delay line or field delay line.

An example of the maximum selection is shown in Figures 4 and 5 below. In this example, the present signal is the maximum of the signals delayed by 262Hs and 263Hs.

Therefore, three lines of the 525 lines of the motion signal are expanded.

Fig. 4 Motion Signal Expansion Example



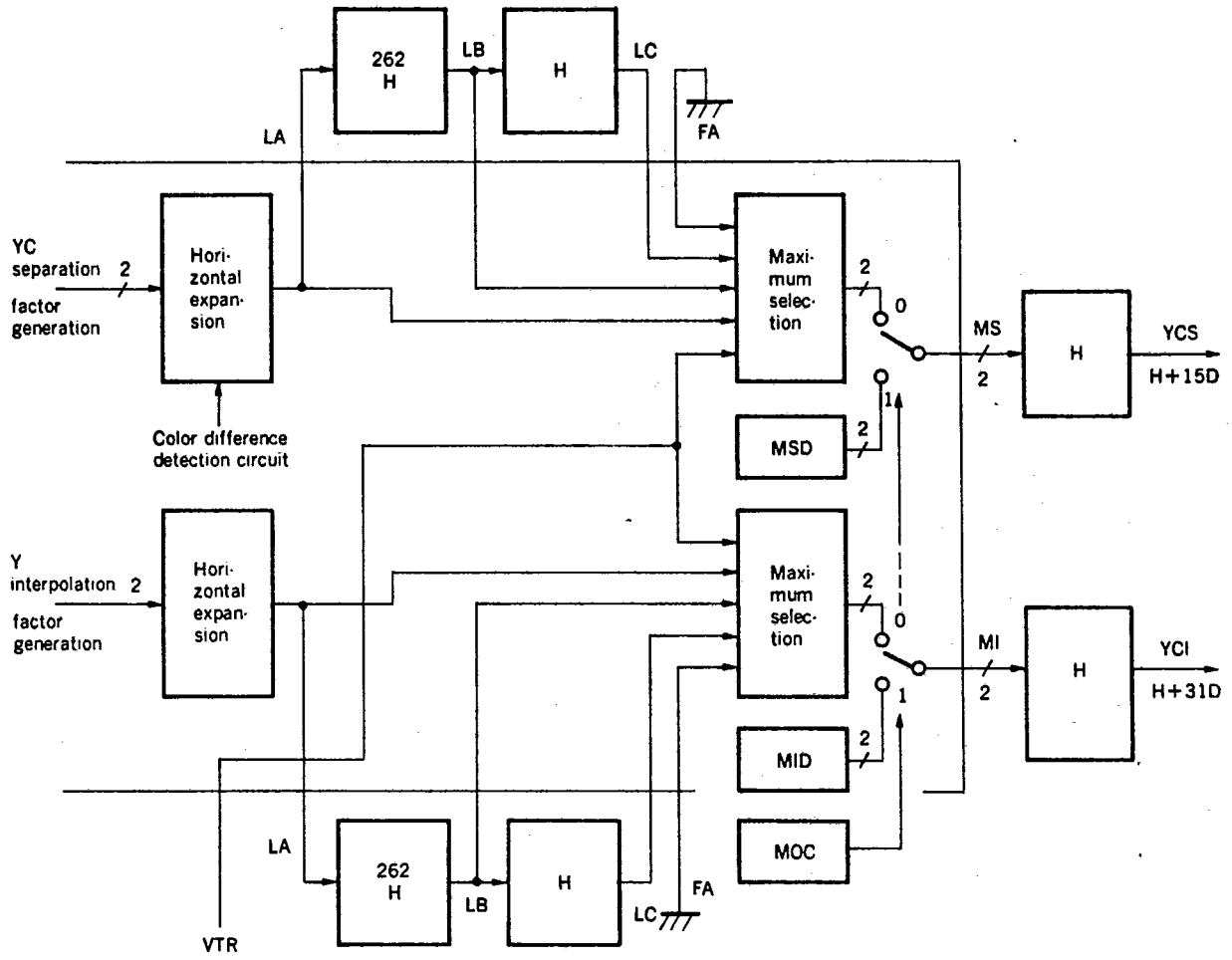
The forced motion signal input terminal (VTR) externally converts the output of the MS and MI into the motion mode. When this terminal inputs a nonstandard signal detection signal from the CKG, the YC separation and the Y interpolation are both processed in the field. To retain the Y interpolation signal in the adaptive processing, connect the VTR terminal to ground (GND terminal) and configure a system applying the nonstandard signal detection output and the OR circuit for the YC separation MS signal.

The YC separation motion output (MS) and the Y interpolation motion output (MI) can be directly controlled by the serial bus.

To control these outputs by the serial bus, set the MOC bit (SA_6, D_4) to "1" to directly obtain the data of the MSD (SA_6, D_0 to D_1) and the MID (SA_6, D_2 to D_3) bits. (Refer to the Description on the Serial Bus for details.)

Fig. 5 Motion Signal Expansion Circuit

T-77-07-09



2. Serial Bus

2-1 Hardware Configuration

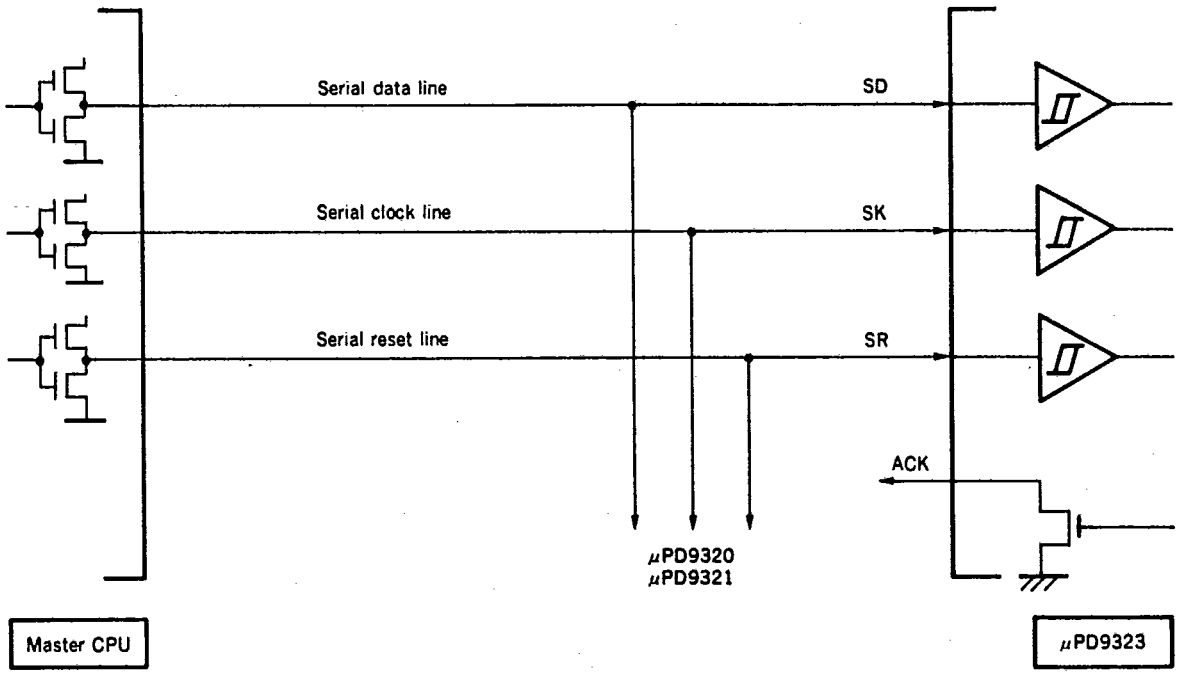
This IDTV system adopts a serial bus with a three-line address system to facilitate control over three LSIs (i.e., the μPD9320A (YCS), the μPD9321 (YCP), and the μPD9323 (MDP)).

The three lines comprising this serial bus are as follows:

- SD (Serial Data Line)
  The master CPU outputs serial data synchronized with the clock signal (SK). The μPD9323 fetches the data having its own address.
- SK (Serial Clock Line)
  The master CPU outputs the serial data clock through this line. The μPD9323 fetches the data based on this clock.
- SR (Serial Rest Line)
  The master CPU outputs signals to operate the bus through this line. When this signal becomes "1," the μPD9323 starts fetching the data. When it becomes "0," the μPD9323 forcefully rests the internal system to the initial state.

The μPD9320 has an additional terminal (ACK (acknowledge terminal)), which can be used to output the status of the internal operation.

Fig. 6 Serial Bus Connection Diagram



A CMOS Schmitt input system is adopted for the SD, SK, and SR, to reduce the fault operation generation rate. The ACK terminal is an N-ch open drain output, so connect a resistor to the power source, V_{DD} (5 volts), outside the system.

2-2 Software Specification

T-77-07-09

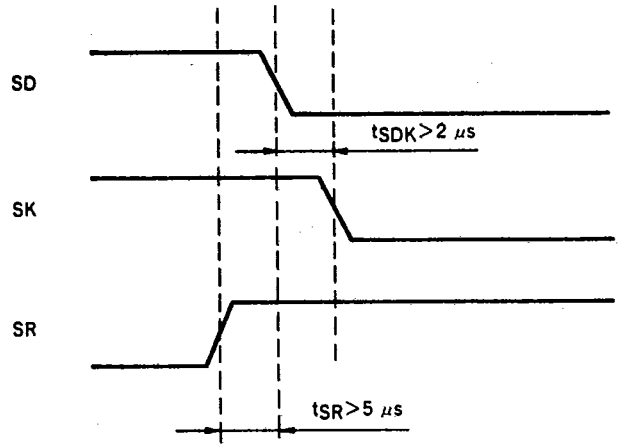
The section describes how the master CPU controls LSIs connected to this serial bus.

Start

To activate this bus, the master CPU raises the SR (Serial reset) line from "L" to "H." At this time, the SD (Serial data) line and SK (Serial clock) line are kept at "H". When the SR line is set to "L", the bus is forcefully reset.

When the SD and SK lines fall after start of the master CPU, the SD line must fall first.

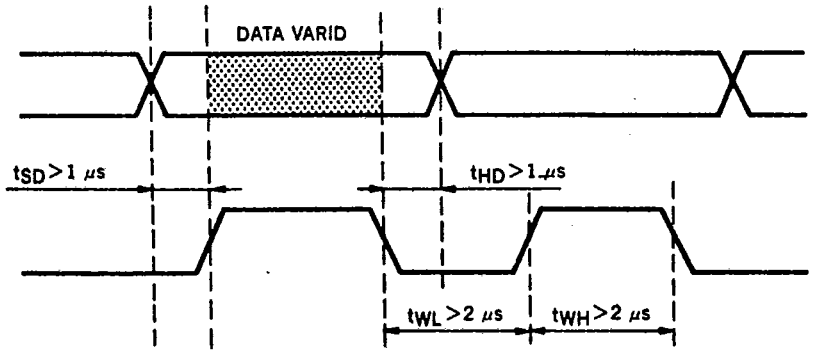
Fig. 7 Start



Data Fetch

The SD line data is fetched when the SK line is "H." Therefore, the master CPU must be switch the data when the SK line is "L."

Fig. 8 Data Fetch



T-77-07-09

Data Transfer

A byte is composed of eight bits of data and an acknowledge (ACK) bit.

To transfer one data byte to the master CPU, three bytes are required: the address byte, subaddress byte, and data byte. To send several data bytes consecutively, however, transfer data bytes only because this LSI has a built-in subaddress byte counter with auto-increment feature.

Address byte ..... Used by the master CPU to select the LSIs.
Subaddress byte ..... Selects the function address of the selected LSI.
Data byte ..... Data in the function address.

Address Byte Transmission

After being activated, the master CPU sends out the main address of the LSI whose data is to be transmitted. The address for the μPD9323, is selected with "8CH."

When the address sent is not its own, the CPU terminates fetching the data and stops internal operation until the next start. When the address is its own, it outputs the acknowledge signal to the acknowledge (ACK) terminal at the ninth clock.

It continues outputting the acknowledge signal to the ACK terminal every ninth clock time, which is the end of a byte, while it is selected.

A_7	A_6	A_5	A_4	A_3	A_2	A_1	-A	ACK
1	0	0	0	1	1	0	0	

ACK: Acknowledge

μPD9323 .... "8CH" Main address

Subaddress Byte Transmission

The byte following the address byte is the subaddress byte. This subbaddress byte selects the functional address in the LSI and serves as the data byte following it.

The μPD9323 has eight subaddresses which can be selected by the three least significant bits.

X	X	X	X	X	SA_2	SA_1	SA_0	ACK
0	0	0	0	0	0	0	0	"00H"
					⋮	⋮	⋮	⋮
0	0	0	0	0	1	1	1	"07H"

ACK: Acknowledge

Data Byte Transmission

The byte following the subaddress byte is the data byte. The address of this data byte is set with the subaddress data.

When transmitting a single byte, the three bytes shown in Figure 10 are sent to complete transfer of the data. Several data bytes can be transmitted consecutively. In initial data loading, for example, set the subaddress to "00" and consecutively transmit eight bytes of data to write in the required data consecutively.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	ACK

ACK: Acknowledge

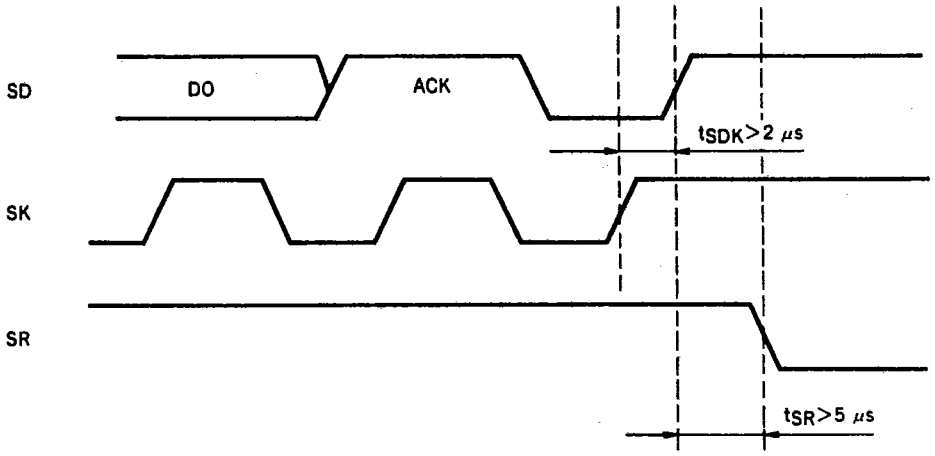
Termination

T-77-07-09

To terminate the operation of this bus, the master CPU turns the status of the SK line to "H" and lets the SR line fall from "H" to "L" to release the bus.

Be sure to make the SK line rise before the SD line.

Fig. 9 Termination



T-77-07-09

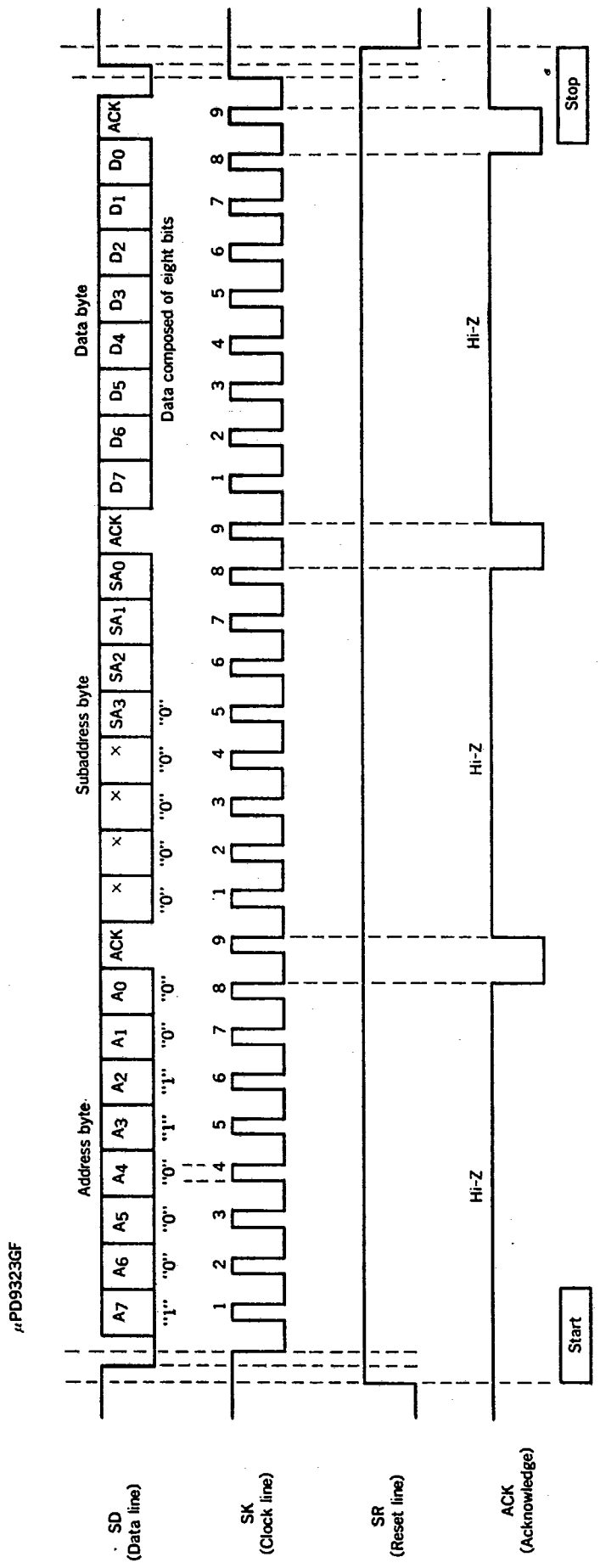


Fig. 10. Example of Writing A Single Byte Data
(The master CPU writes one byte of data to a slave IC.)

T-77-07-09

MDP Serial Bus Function List

Main address . . . "8CH"

Sub-address	Data							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SA_0	"0"	"0"		MSk1	YC separation comparison level < 0 to 63 >			k1
			D_5	D_4	D_3	D_2	D_1	D_0
SA_1	"0"	"0"		MSk3	YC separation comparison level < 0 to 63 >			k3
			D_5	D_4	D_3	D_2	D_1	D_0
SA_2	"0"	"0"		Mik1	YC separation interpolation level < 0 to 63 >			k1
			D_5	D_4	D_3	D_2	D_1	D_0
SA_3	"0"	"0"		Mik2	YC interpolation level < 0 to 63 >			k2
			D_5	D_4	D_3	D_2	D_1	D_0
SA_4	"0"	"0"		Mik3	YC interpolation comparison level < 0 to 63 >			k3
			D_5	D_4	D_3	D_2	D_1	D_0
SA_5	"0"	"0"		CDL	Chrominance detection comparison level < 0 to 63 >			
			CD_5	CD_4	CD_3	CD_2	CD_1	CD_0
SA_6	"0"	"0"	"0"	MOC Motion output control 1: Serial bus control 0: Internal control	MID		MSD	
					YCI motion data (MOC = 1)		YSC motion data (MOC = 1)	
					MID 1	MID 0	MSD 1	MSD 0
SA_7	"0"	"0"	"0"	"0"	"0"	"0"	CD1 Inter-polation color detection 1: Detects. 0: Inhibits.	CD0 Color detection 1: Inhibits. 0: Detects.

T-77-07-09

Description of the MDP Serial Bus

1. YC Separation Motion Detection Comparator Level (MSk1)

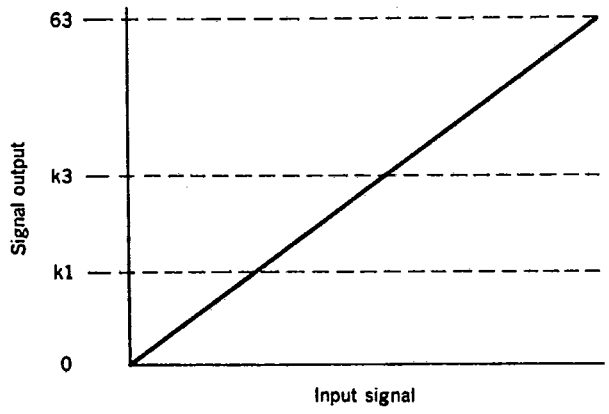
SA_0	"0"	"0"	5	4	3	2	1	0

MSk1 data is used to convert the Y motion detection signal (six bits) to the YC separation motion signal (two bits).
There are 64 levels ("0" to "63") that can be set.
The closer to "0" the set level is, the easier the motion signal is to detect.

2. YC Separation Motion Detection Comparator Level (MSk3)

SA_1	"0"	"0"	5	4	3	2	1	0

MSk3 data is used to convert the Y motion detection signal (six bits) to the YC separation motion signal (two bits).
There are 64 levels ("0" to "63") that can be set.
The closer to "0" the set level is, the easier the motion signal is to detect.



Input Signal	MS Output	
	MS1	MS0
0 < MD < k1	0	0
k1 < MD < k3	0	1
k3 < MD < 63	1	1

3. YC Interpolation Comparator Level (Mlk1)

T-77-07-09

SA_2	"0"	"0"	5	4	3	2	1	0

Mlk1 data is used to convert the Y motion detection signal (six bits) to the YC interpolation motion signal (two bits).
There are 64 levels ("0" to "63") that can be set.
The closer to "0" the set level is, the easier the motion signal is to detect.

4. YC Interpolation Comparator Level (Mlk2)

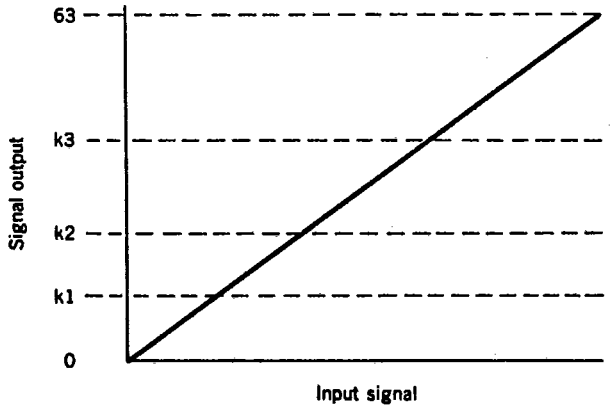
SA_3	"0"	"0"	5	4	3	2	1	0

Mlk2 data is used to convert the Y motion detection signal (six bits) to the YC interpolation motion signal (two bits).
There are 64 levels ("0" to "63") that can be set.
The closer to "0" the set level is, the easier the motion signal is to detect.

5. YC Interpolation Comparator Level (Mlk3)

SA_4	"0"	"0"	5	4	3	2	1	0

Mlk3 data is used to convert the Y motion detection signal (six bits) to the YC interpolation motion signal (two bits).
There are 64 levels ("0" to "63") that can be set.
The closer to "0" the set level is, the easier the motion signal is to detect.



Input Signal	MS Output	
	MI1	MI0
0 < MD < k1	0	0
k1 < MD < k2	0	1
k2 < MD < k3	1	0
k3 < MD < 63	1	1

6. C-Motion Detection Comparator Level (CDL)

SA_5	"0"	"0"	5	4	3	2	1	0

This data is used to convert the C-motion (color motion) detection signal (six bits) to the color motion signal (one bit). There are 64 levels ("0" to "63") that can be set.
The closer to "0" the set level is, the easier the motion signal is to detect.

7. Motion Output Control (MOC)

SA_6	"0"	"0"	"0"	4	X	X	X	X

The data is this bit is used as a switch to control the output of the motion output terminals (MS, MI) by the serial bus. When this bit is set at "1," the motion output is inhibited and the data from the serial bus (MSD, MID) is output to the motion output terminals (MS, MI)).

1: Serial bus (MSD, MID)
0: Internal output (standard operation)

8. Motion YCS Data (MSD)

T-77-07-09

SA_6	"0"	"0"	"0"	X	X	X	1	0

This data is output to the YC separation motion output terminal (MS).
This data can directly control the output at the YC separation motion output terminals (MS0, 1) when the motion output control bit (MOC) is set to "1."

MSD0 (D0) : Output terminal MS0
MSD1 (D1) : Output terminal MS1

Serial Bus Data		YCS Function	
MSD1	MSD0	Interline YC	Interframe YC
0	0	0	1
0	1	0.5	0.5
1	0	0.5	0.5
1	1	1	0

9. Motion YCI Data (MID)

SA_6	"0"	"0"	"0"	X	3	2	X	X

This data is output to the Y interpolation motion output terminal (MI).
Setting the motion output control bit (MOC) to "1" enables this output to directly control the output of the Y interpolation output terminals (MI0, 1).

MID0 (D2) : Output terminal MI0
MID1 (D3) : Output terminal MI1

Serial Bus Data		YCI Function	
MID1	MID0	Interline Interpolation	Interfield Interpolation
0	0	0	1
0	1	0.375	0.625
1	0	0.625	0.375
1	1	1	0

10. Color Detection (CDSI)
(C-Detect YCS, YCI)

SA_7	"0"	"0"	"0"	"0"	"0"	"0"	X	0

This bit controls the color motion signal detection.
When this bit is set to "1", the color motion signal detection is inhibited and only the Y motion signal is output.

1 : Color motion detection inhibited.
0 : Color motion detected.

11. Interpolation Color Detection (CDI)
(C-Detect YCI)

SA_7	"0"	"0"	"0"	"0"	"0"	"0"	1	X

This bit controls whether or not to use the color motion signal for the Y interpolation motion signal output.
When this bit is set to "0", the color motion signal detection is inhibited; when set to "1," the color motion is detected.

1 : Color motion signal detected.
0 : Color motion signal detection inhibited.

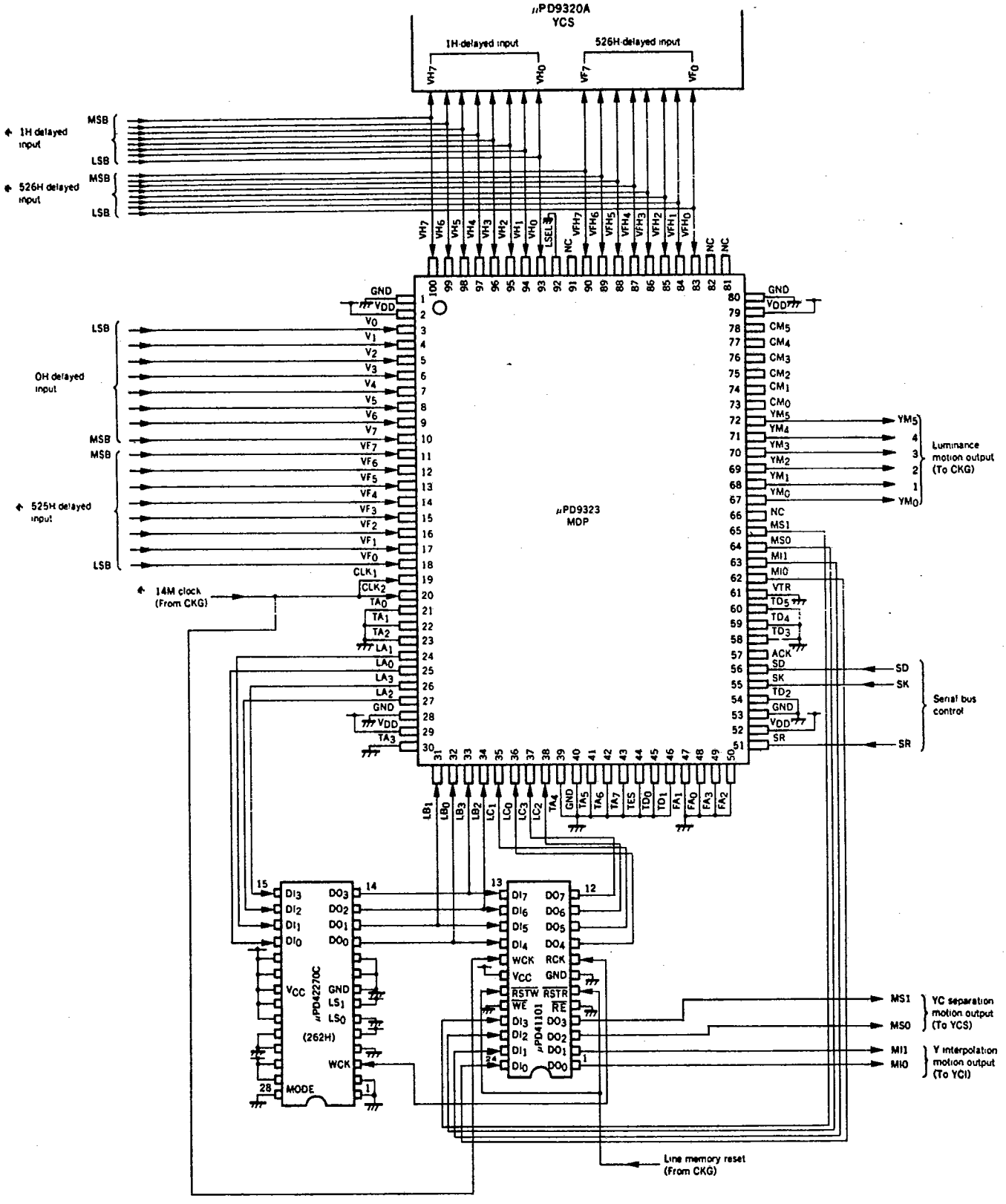
Reference data for evaluation

Following data is just for evaluation. For mass-production it's need fitting by evaluating screen condition:

SA_0 ..... 04_H
SA_1 ..... 07_H
SA_2 ..... 04_H
SA_3 ..... 08_H
SA_4 ..... $0A_H$
SA_5 ..... 10_H
SA_6 ..... 00_H
SA_7 ..... 00_H

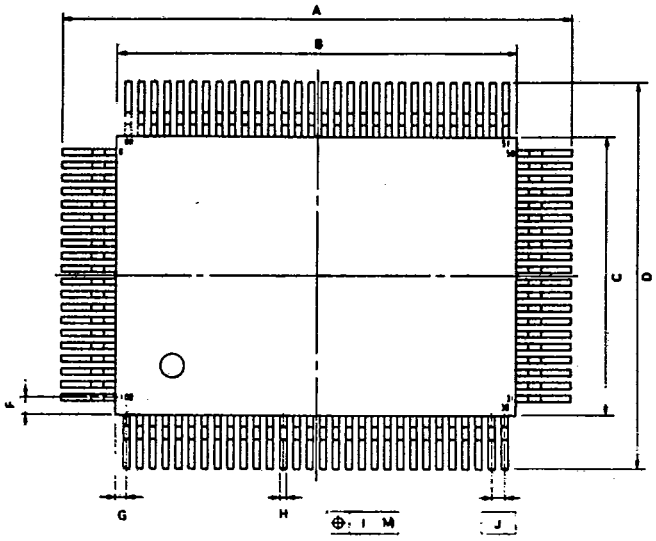
T-77-07-09

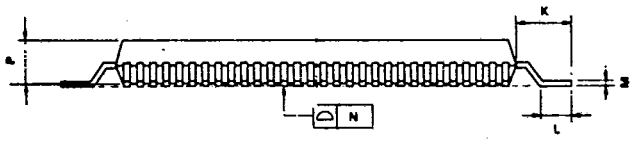
APPLICATION CIRCUIT EXAMPLE



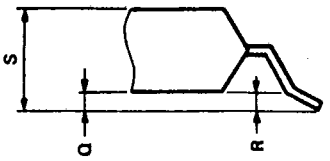
※ The clock of Field Buffer and Line Buffer which connected to $VF_{0\sim7}$, $VFH_{0\sim7}$, $VH_{0\sim7}$ must be delayed to this clock. (About 10 ns).

100PIN PLASTIC QFP (14×20)





detail of lead end



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

P100GF-65-3BA-1

ITEM	MILLIMETERS	INCHES
A	$23.6^{+0.4}$	$0.929^{+0.016}$
B	$20.0^{+0.2}$	$0.795^{+0.009}_{-0.008}$
C	$14.0^{+0.2}$	$0.551^{+0.009}_{-0.008}$
D	$17.6^{+0.4}$	$0.693^{+0.016}$
F	0.8	0.031
G	0.6	0.024
H	$0.30^{+0.10}$	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	$1.8^{\pm0.2}$	$0.071^{+0.008}_{-0.009}$
L	$0.8^{\pm0.2}$	$0.031^{+0.008}_{-0.009}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{\pm0.1}$	$0.004^{\pm0.004}$
R	$0.1^{\pm0.1}$	$0.004^{\pm0.004}$
S	3.0 MAX.	0.119 MAX.