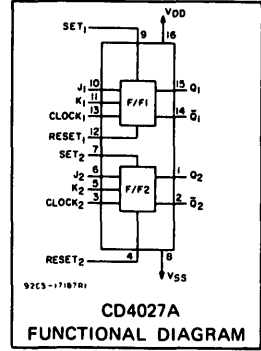


CD4027A Typ s

COS/MOS Dual J-K Master-Slave Flip-Flop

The RCA-CD4027A is a single monolithic chip integrated circuit containing two identical complementary-symmetry J-K master-slave flip-flops. Each flip-flop has provisions for individual J, K, Set, Reset, and Clock input signals. Buffered Q and \bar{Q} signals are provided as outputs. This input-output arrangement provides for compatible operation with the RCA-CD4013A dual D-type flip-flop.

The CD4027A is useful in performing control, register, and toggle functions. Logic levels present at the J and K inputs along with internal self-steering control the state of each flip-flop; changes in the flip-flop state are synchronous with the positive-going transition of the clock pulse. Set and reset functions are independent of the clock and are initiated when a high level signal is present at either the Set or Reset input.



These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

MAXIMUM RATINGS, Absolute-Maximum Values:

| | |
|---|---------------------------------------|
| STORAGE-TEMPERATURE RANGE (T_{stg}) | -65 to +150°C |
| OPERATING-TEMPERATURE RANGE (T_A): | |
| PACKAGE TYPES D, F, H | -55 to +125°C |
| PACKAGE TYPE E | -40 to +85°C |
| DC SUPPLY-VOLTAGE RANGE, (V_{DD}) | |
| (Voltages referenced to V_{SS} Terminal): | -0.5 to +15 V |
| POWER DISSIPATION PER PACKAGE (P_D): | |
| FOR $T_A = -40$ to +60°C (PACKAGE TYPE E) | 500 mW |
| FOR $T_A = +60$ to +85°C (PACKAGE TYPE E) | Derate Linearly at 12 mW/°C to 200 mW |
| FOR $T_A = -55$ to +100°C (PACKAGE TYPES D, F) | 500 mW |
| FOR $T_A = +100$ to +125°C (PACKAGE TYPES D, F) | Derate Linearly at 12 mW/°C to 200 mW |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR | |
| FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) | 100 mW |
| INPUT VOLTAGE RANGE, ALL INPUTS | -0.5 to $V_{DD} + 0.5$ V |
| LEAD TEMPERATURE (DURING SOLDERING): | |
| At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. | +265°C |

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

| CHARACTERISTIC | V_{DD} (V) | LIMITS | | | | UNITS |
|---|-----------------|---------------------|------------|--------------|---------|---------------|
| | | D, F, H PACKAGES | | E PACKAGE | | |
| | | MIN. | MAX. | MIN. | MAX. | |
| Supply-Voltage Range (For $T_A =$ Full Package-Temperature Range) | | 3 | 12 | 3 | 12 | V |
| Data Setup Time, t_S | 5 10 | 150 50 | — — | 200 75 | — — | ns |
| Clock Pulse Width, t_W | 5 10 | 330 110 | — — | 500 165 | — — | ns |
| Clock Input Frequency (Toggle Mode) f_{CL} | 5 10 | dc | 1.5 4.5 | dc | 1 3 | MHz |
| Clock Rise or Fall Time, t_{rCL} , t_{fCL} | 5 10 | — — | 15 5 | — — | 15 5 | μs |
| Set or Reset Pulse Width, t_W | 5 10 | 200 80 | — — | 300 120 | — — | ns |

*If more than one unit is cascaded in a parallel clocked operation, t_{CL} should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

Features:

- Set-Reset capability
- Static flip-flop operation—retains state indefinitely with clock level either "high" or "low"
- Medium-speed operation—10 MHz (typ.) clock toggle rate at 10V
- Quiescent current specified to 15 V
- Maximum input leakage of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications

- Registers, counters, control circuits

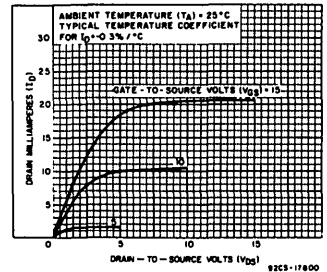


Fig. 1 - Typical n-channel drain characteristics.

CD4027A Typ s

STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTICS | CONDITIONS V _O (V) V _{IN} (V) V _{DD} (V) | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | | UNITS |
|--|--|------|-------|---------------------------------------|-------|-------|--------|-----------|------|-------|-------|-------|
| | | | | D, F, H PACKAGES | | | | E PACKAGE | | | | |
| | | | | -65 | +25 | | +125 | -40 | +25 | | +85 | |
| | | TYP. | LIMIT | | | TYP. | LIMIT | | | | | |
| Quiescent Device Current, I _L Max. | | | 5 | 1 | 0.005 | 1 | 60 | 10 | 0.01 | 10 | 140 | μA |
| | | | 10 | 2 | 0.005 | 2 | 120 | 20 | 0.05 | 20 | 280 | |
| | | | 15 | 25 | 0.5 | 25 | 1000 | 250 | 2.5 | 250 | 2500 | |
| Output Voltage: Low Level, V _{OL} | - | 0.5 | 5 | 0 Typ., 0.05 Max | | | | | | | | V |
| | - | 0.10 | 10 | 0 Typ., 0.05 Max | | | | | | | | |
| High Level V _{OH} | - | 0.5 | 5 | 5 Typ., 4.95 Min | | | | | | | | V |
| | - | 0.10 | 10 | 10 Typ., 9.95 Min | | | | | | | | |
| Noise Immunity: Inputs Low, V _{NL} | 4.2 | - | 5 | 2.25 Typ., 1.5 Min | | | | | | | | V |
| | 9 | - | 10 | 4.5 Typ., 3 Min | | | | | | | | |
| Inputs High V _{NH} | 0.8 | - | 5 | 2.25 Typ., 1.5 Min. | | | | | | | | V |
| | 1 | - | 10 | 4.5 Typ., 3 Min. | | | | | | | | |
| Noise Margin: Inputs Low, V _{NML} | 4.5 | - | 5 | 1 Min | | | | | | | | V |
| | 9 | - | 10 | 1 Min. | | | | | | | | |
| Inputs High, V _{NMH} | 0.5 | - | 5 | 1 Min | | | | | | | | V |
| | 1 | - | 10 | 1 Min. | | | | | | | | |
| Output Drive Current: N Channel (Sink), I _{DN} Min. | 0.5 | - | 5 | 0.65 | 1 | 0.5 | 0.35 | 0.35 | 1 | 0.3 | 0.24 | mA |
| | 0.5 | - | 10 | 1.25 | 2.5 | 1 | 0.75 | 0.72 | 2.5 | 0.6 | 0.5 | |
| P-Channel (Source), I _{DP} Min. | 4.5 | - | 5 | -0.31 | -0.5 | -0.25 | -0.175 | -0.17 | -0.5 | -0.14 | -0.12 | mA |
| | 9.5 | - | 10 | -0.8 | -1.3 | -0.65 | -0.45 | -0.4 | -1.3 | -0.33 | -0.27 | |
| Input Leakage Current, I _{IL} , I _{IH} | Any Input | | 15 | ±10 ⁻⁵ Typ., ±1 Max | | | | | | | | μA |

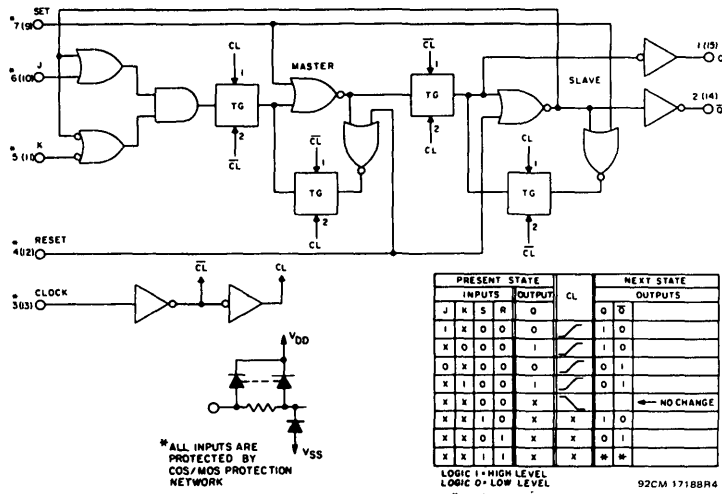
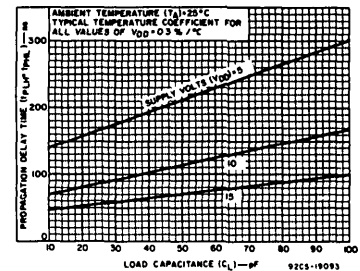
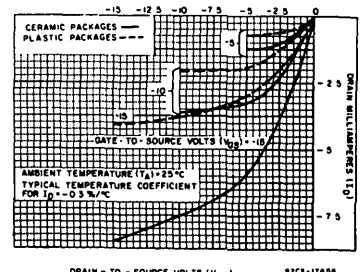
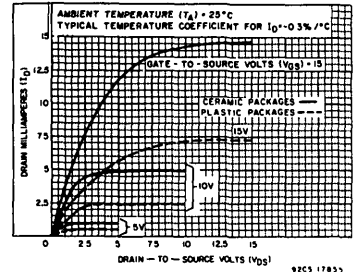
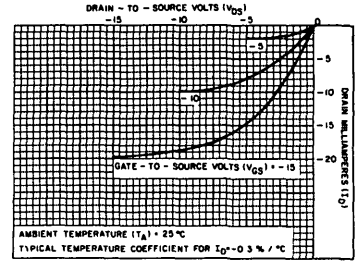


Fig. 2 - Logic diagram & truth table for CD4027A (one of two identical J-K flip flops).

Fig. 6 - Typical propagation delay time vs. C_L.

CD4027A Typ s

DYNAMIC ELECTRICAL CHARACTERISTICS

at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20\text{ ns}$, $C_L = 15\text{ pF}$, $R_L = 200\text{ k}\Omega$

| CHARACTERISTIC | V_{DD} (V) | LIMITS | | | | | | UNITS |
|---|-----------------|---------------------|------------|------------|--------------|-----------|------------|-------|
| | | D, F, H PACKAGES | | | E PACKAGE | | | |
| | | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | |
| Propagation Delay Time: Clock to Q or \bar{Q} Outputs t_{PHL}, t_{PLH} | 5 10 | - - | 200 100 | 400 200 | - - | 150 75 | 400 150 | ns |
| Set to Q or Reset to \bar{Q} , t_{PLH} | 5 10 | - - | 175 75 | 225 110 | - - | 175 75 | 350 150 | ns |
| Set to \bar{Q} or Reset to Q, t_{PHL} | 5 10 | - - | 175 75 | 225 110 | - - | 175 75 | 350 150 | ns |
| Transition Time t_{THL}, t_{TLH} | 5 10 | - - | 75 50 | 125 70 | - - | 75 50 | 250 140 | ns |
| Maximum Clock Input Frequency (Toggle Mode) f_{CL} | 5 10 | 1.5 4.5 | 3 8 | - - | 1 3 | 3 8 | - - | MHz |
| Minimum Clock Pulse Width, t_W | 5 10 | - - | 165 65 | 330 110 | - - | 165 65 | 500 165 | ns |
| Minimum Set or Reset Pulse Width, t_W | 5 10 | - - | 125 50 | 200 80 | - - | 125 50 | 300 120 | ns |
| Minimum Data Setup Time, t_S | 5 10 | - - | 70 25 | 150 50 | - - | 70 25 | 200 75 | ns |
| Clock Rise or Fall Time, t_{rCL}, t_{fCL} | 5 10 | - - | - - | 15 5 | - - | - - | 15 5 | us |
| Average Input Capacitance, C_I | Any Input | - | 5 | - | - | 5 | - | pF |

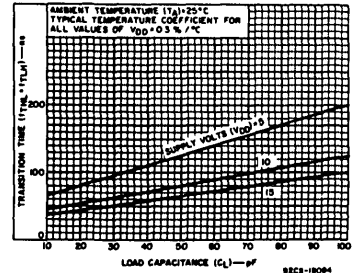


Fig. 7 - Typical transition time vs. C_L .

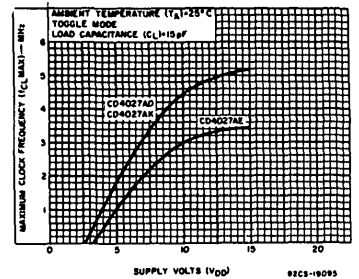


Fig. 8 - Typical maximum clock input frequency vs. supply voltage.

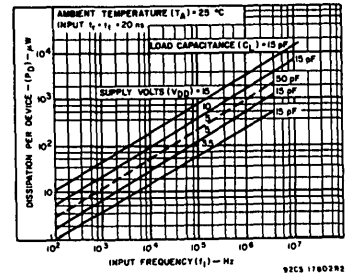


Fig. 9 - Typical dissipation characteristics.

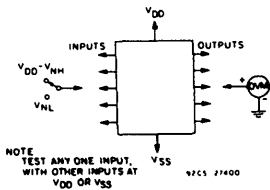


Fig. 10 - Noise immunity test circuit.

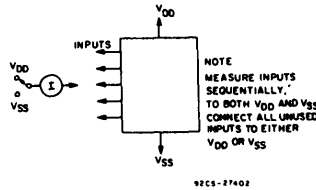


Fig. 11 - Input leakage current test circuit.

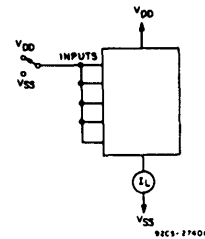


Fig. 12 - Quiescent device current test circuit.