CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CMX990

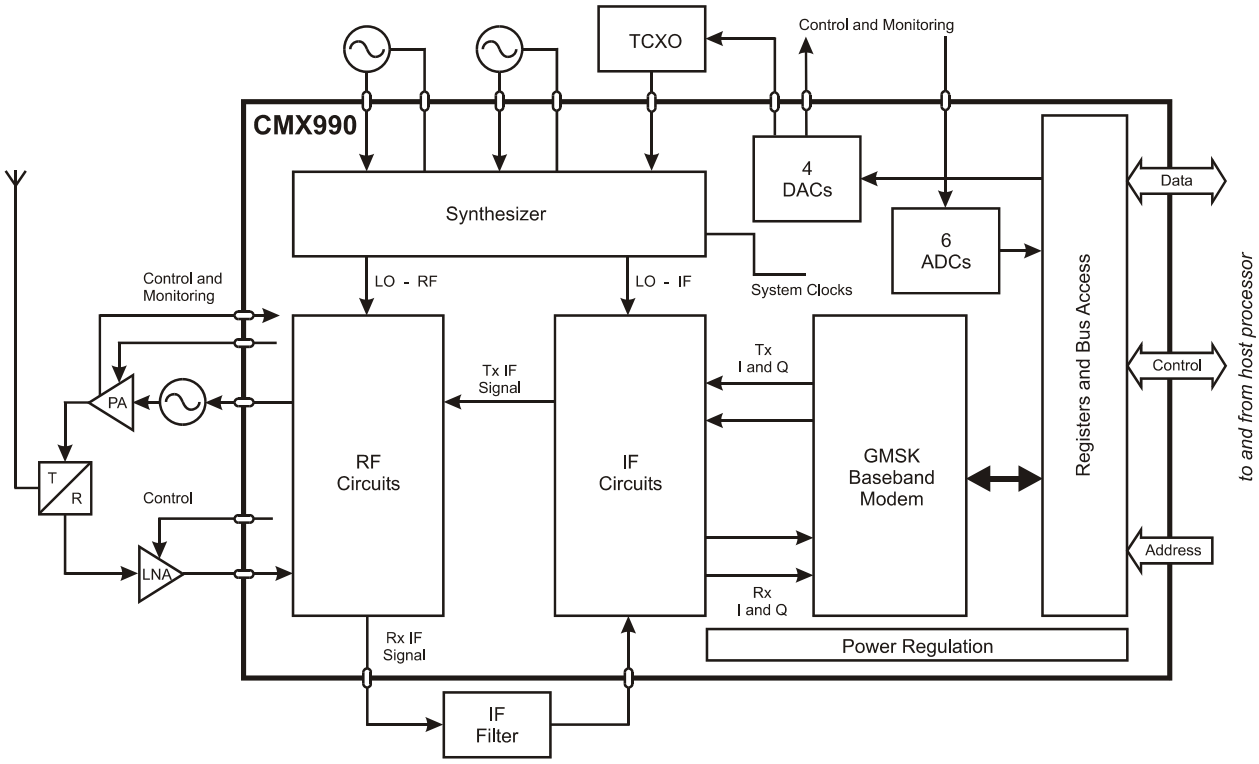
GMSK Packet Data Modem and RF Transceiver

D/990/6 April 2008

Provisional Issue

Features

- **Single Chip RF Transceiver and GMSK Modem**
- **IF, RF, Control and Synthesizer Stages**
- **Selectable B_t = 0.27, 0.3 or 0.5**
- **Receiver Sensitivity -116dBm at 8kbps**
- **Full Mobitex Compatibility**
- **Versatile Data Rates: 4kbps to 16kbps**
- **Packet and Freeformat (Raw) Data**
- **Low-Power, Low Profile, Low-Cost BOM**
- **400MHz - 1GHz Radio Data Systems**
- **Simple Parallel Interfacing**
- **AGC Algorithm**
- **RSSI Measurement**
- **Flexible System Clocks**
- **Suitable for EN 300 113, EN 300 220 and FCC CFR 47 Part 90**



1 Brief Description

A single-chip GMSK packet-data modem and RF transceiver, the CMX990 provides the majority of circuits and functions to implement a full-feature 'wireless modem' subsystem. The CMX990 can operate in RF ranges of 400MHz to 1GHz at data rates of 4 to 16 kbps and is fully Mobitex compatible.

With a minimum of external components and circuits, this half-duplex device provides on-chip: a flexible, formattable GMSK packet and free-format modem, a dual synthesiser, IF and RF stages for both Rx and Tx modes, and auxiliary ADCs and DACs for system control and monitoring.

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This versatile GMSK modem is programmable to both packet and free-format data operations via an efficient task-oriented Rx and Tx format and command structure, which is combined with data scrambling, interleaving and FEC and CRC capabilities. Rx data acquisition, extraction and tracking abilities, allied with Rx data quality feedback, allow the CMX990 to operate seamlessly in varying signal environments.

Tx includes an internal vector modulator to accurately generate the modulation. This is then translated to the final frequency using an offset-phased locked loop. In the Rx path an image-reject mixer is provided to minimise external RF filtering requirements. The output of the mixer goes off-chip to allow the circuit designer flexibility in the choice of IF filter. The CMX990 then provides AGC functions and I/Q mix down to generate baseband signals for the modem. Significant Rx selectivity is provided using internal I/Q baseband filters.

Comprehensive internal and external system control and monitoring is provided by the 8-bit host interface registers and the on-chip ADCs and DACs. Requiring a power supply input in the range 3.0 to 3.6 Volts, the CMX990 can be used in wireless products designed to comply with such standards as EN 300 113 and FCC CFR 47 Part 90. Operating over a temperature range of -40°C to +85°C, the CMX990 consolidates the core radio modem functions to enable a new generation of small, narrow-band wireless data modems. The CMX990 comes in a 64-pin low profile VQFN package.

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It is always recommended that you check for the latest product datasheet version from the Datasheets page of the CML website: [www.cmlmicro.com].

2 Block Diagram

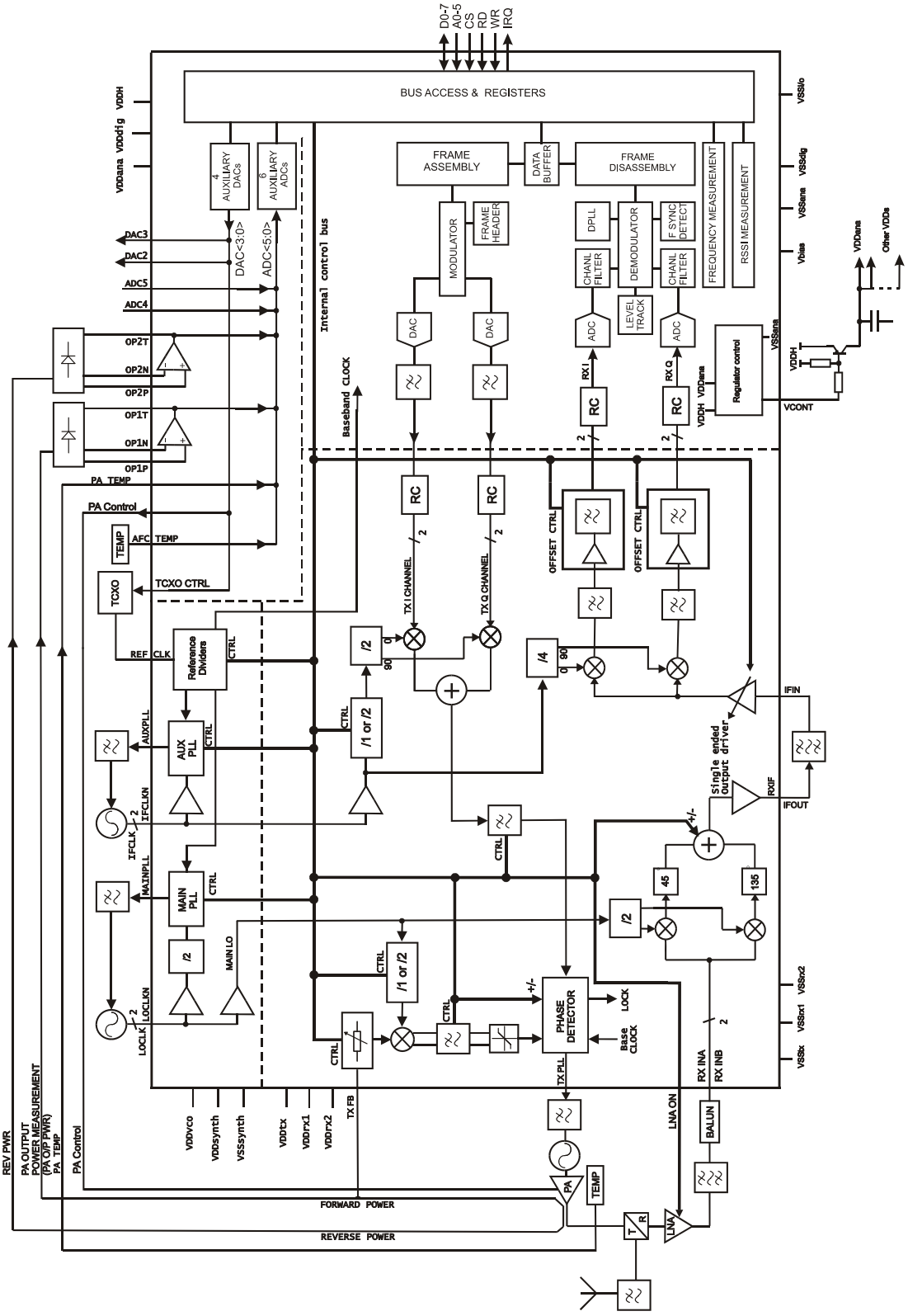


Figure 1 Block Diagram

3 Signal List

Package Q1	Signal		Description
Pin No.	**Name**	**Type**	
1	PA-CNTL	O/P	DAC0 output to control PA power.
2	TX FB	I/P	Tx feedback input signal.
3	-	NC	*do not make any connection to this pin*
4	V_{DD} Tx	Power	Power supply to Tx IF and RF circuits.
5	-	NC	*do not make any connection to this pin*
6	V_{SS} Tx	Power	Return for V_{DD} Tx, good decoupling required.
7	TXPLL	O/P	Tx Phase Detector output.
8	RF IN A	I/P	RF input A for received signal.
9	RF IN B	I/P	RF input B for received signal. (RF IN A and RF IN B are a differential input)
10	V_{DD} Rx1	Power	Power supply to Rx RF circuits.
11	IF OUT	O/P	Output to the external IF filter.
12	V_{SS} Rx1	Power	Return for V_{DD} Rx1, good decoupling required.
13	V_{SS} Rx2	Power	Return for V_{DD} Rx2, good decoupling required.
14	LNA ON	O/P	Digital output to turn on external LNA block.
15	V_{DD} Rx2	Power	Power supply to Rx IF circuits.
16	IF IN	I/P	Input from the external IF filter.
17	A5	I/P	Register address select logic inputs.
18	A4	I/P	"
19	A3	I/P	"
20	A2	I/P	"
21	A1	I/P	"
22	A0	I/P	"
23	V_{DD} Dig	Power	Power supply to base band digital circuits.
24	V_{DD} Ana	Power	Power supply to aux ADC, DAC, OP1/2 circuits.
25	V_{BIAS}	O/P	Output of internal bias generator, decouple to V_{SS} Ana.
26	V_{SS} Ana	Power	Return for V_{DD} Ana, good decoupling required.
27	V_{SS} Dig	Power	Return for V_{DD} Dig, good decoupling required.
28	V_{SS} H	Power	Return for V_{DD} H, good decoupling required.
29	RDN	I/P	Read. An active low logic level input used to control the reading of data from the modem into the controlling µC.

Package Q1	Signal		Description
30	WRN	I/P	Write. An active low logic level input used to control the writing of data into the modem from the controlling µC.
31	CSN	I/P	Chip Select. An active low logic level input used to enable a data read or write operation.
32	IRQN	O/P	A 'wire-ORable' output for connection to the host Interrupt Request input. This output has a low impedance pull down to VSS when active and is high impedance when inactive. An external pullup resistor is required.
33	V_{DD} H	Power	Power supply to host interface and 2.5V regulator circuit.
34	D7	BI	Tri-state µC interface data line.
35	D6	BI	"
36	D5	BI	"
37	D4	BI	"
38	D3	BI	"
39	D2	BI	"
40	D1	BI	"
41	D0	BI	"
42	V-CONT	O/P	Control signal for external regulating transistor.
43	DAC3	O/P	Aux. D/A 3 output.
44	DAC2	O/P	Aux. D/A 2 output.
45	ADC5	I/P	Aux. A/D 5 input.
46	ADC4	I/P	Aux. A/D 4 input.
47	OP2T	O/P	Uncommitted op-amp 2 output, internally connected to ADC3.
48	OP2N	I/P	Uncommitted op-amp 2 negative input.
49	OP2P	I/P	Uncommitted op-amp 2 positive input.
50	OP1T	O/P	Uncommitted op-amp 1 output, internally connected to ADC2.
51	OP1N	I/P	Uncommitted op-amp 1 negative input.
52	OP1P	I/P	Uncommitted op-amp 1 positive input.
53	REFCLK	I/P	Master clock input from external TCXO.
54	TCXO-CNTL	O/P	DAC1 output to control TCXO.
55	TCXO-TEMP	I/P	A/D input to measure TCXO temperature, internally connected to ADC1.
56	LOCLKN	I/P	Inverted input from the RF Oscillator circuit.
57	LOCLK	I/P	Input from the RF Oscillator circuit.

Package Q1	Signal		Description
58	IFCLKN	I/P	Inverting Input from IF Oscillator (if balanced input is used). If IFCLK is used as a single ended input this pin should be connected to the VCO ground. The pin is a.c. coupled.
59	MAINPLL	O/P	Main PLL output, connect to external filter.
60	V_{DD} VCO	Power	Power supply to the VCO charge pump.
61	AUXPLL	O/P	Aux PLL output, connect to external filter.
62	V_{DD} Synth	Power	Power supply to synthesiser circuits.
63	IFCLK	I/P	Input from the IF Oscillator circuit.
64	PA-TEMP	I/P	A/D input to measure PA temperature, internally connected to ADC0.
EXPOSED METAL PAD	SUB	Power	The Exposed Metal Pad must be electrically connected to Analogue Ground (V_{SS} Ana).

Total = 65 Pins (64 pins and central metal ground pad)

Notes:
I/P = Input
O/P = Output
BI = Bidirectional
T/S = 3-state Output
NC = No Connection

4 External Components

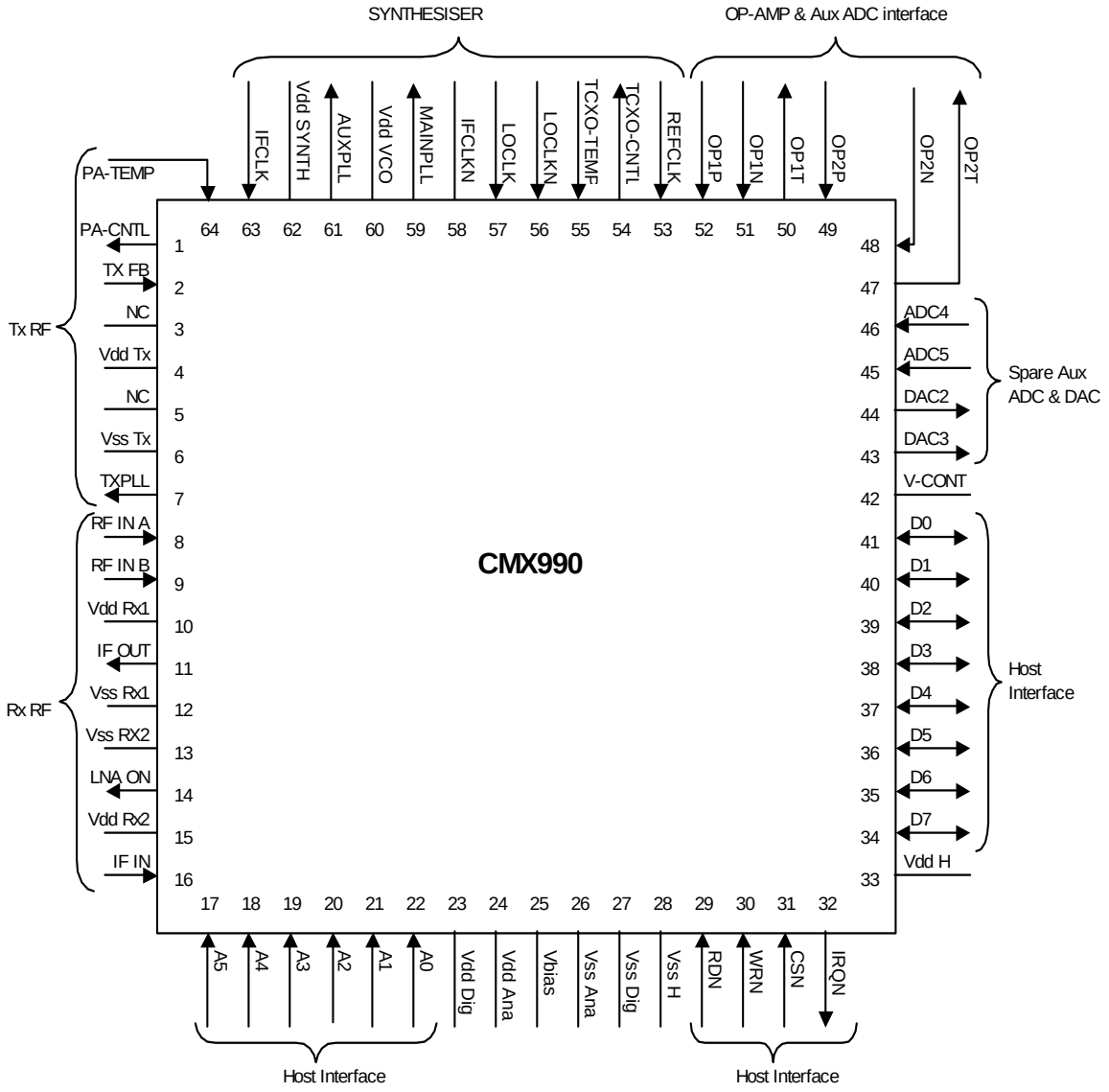


Figure 2 CMX990 Pin Overview

Note: In the following sections specified, component tolerances indicate a minimum requirement, components with better tolerances may be substituted.

4.1 Layout Recommendations

To achieve good noise performance, decoupling of V_{BIAS} and all supplies is very important as is protection of the receive path from extraneous in-band signals. It is recommended that the printed circuit board is laid out with a ground plane in the CMX990 area to provide a low impedance connection between the V_{SS} pins and all V_{DD} and V_{BIAS} decoupling capacitors. As shown in Figure 12 the ground for V_{SS} digital signals should be kept separate from that used for analogue / RF signals. The digital ground should be routed back to a suitable star point.

The CMX990 package has a metal area connected to ground under the main body of the IC. This pad should be connected to analogue ground. It will be noted that caution should be exercised over placing any tracks underneath the CMX990. Furthermore, any vias other than ground should be avoided under the device unless manufacturers can guarantee that the exposed ground pad on the CMX990 will not cause short circuits while a good electrical contact is maintained between the device and ground.

Apart from these recommendations normal RF layout practices should apply, such as keeping tracks as short as possible, equal track lengths on differential inputs, care with coupling between tracks etc.

4.2 Processor Interface

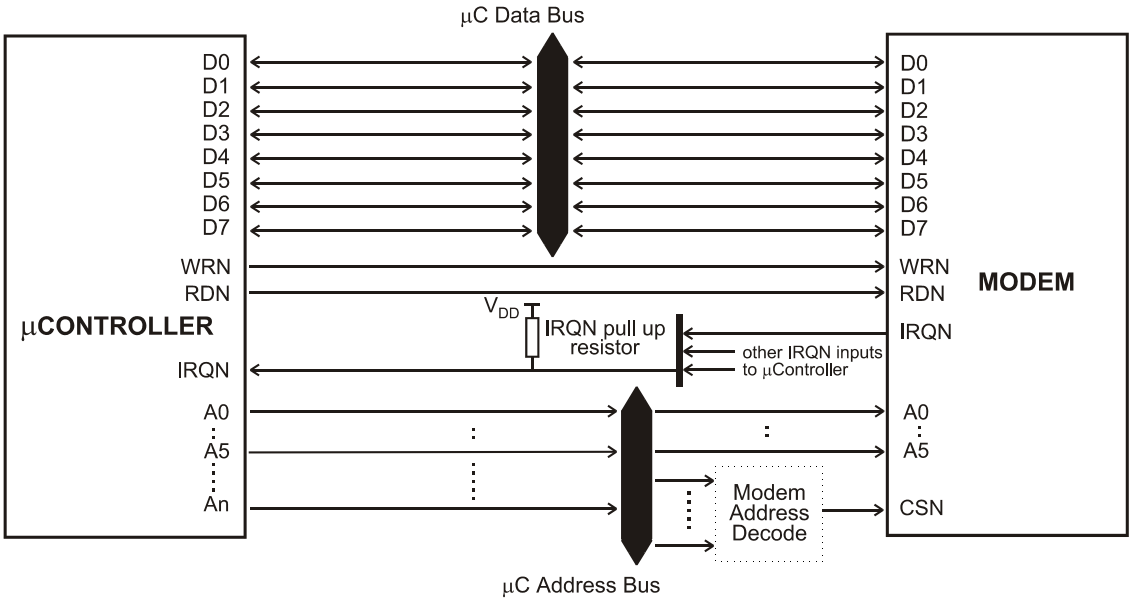


Figure 3 Recommended External Configuration - Processor Interface

The receiver circuits can be affected by digital noise from the host interface. Screening of RF circuits is recommended along with filtering of the digital lines. 100Ω series resistors with 56pF to ground on the CMX990 side of the resistor is suggested however designers are likely to find requirements will vary in individual designs depending on layout, screening arrangements and host. Care should be taken to ensure digital control lines A0-A5 are kept away from the IF input on pin 16 as these address lines are adjacent on pins 17-22.

4.3 Synthesiser and TCXO

The CMX990 synthesiser section provides two independent synthesisers. The PLLs implement a Type II loop with a phase / frequency phase detector providing an output of a charge pump current. Various types of loop filter can be used and should be optimised for VCO gain of a particular design. Figure 4 gives typical configuration and values.

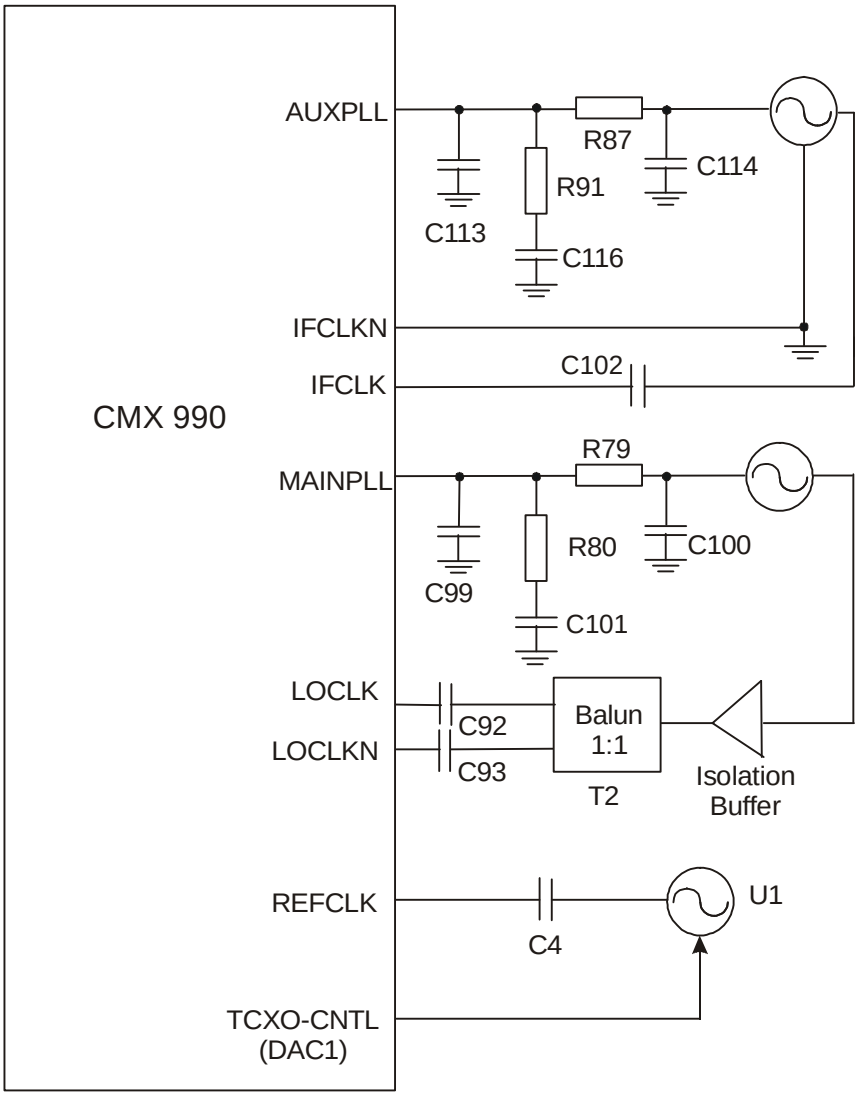


Figure 4 Recommended External Components – Synthesiser and TCXO

C4	1 nF	T2	TC1-1-13M+
C92	1 nF		
C93	1 nF	R79	470 Ω
C99	100 nF	R80	1.0 kΩ
C100	27 nF	R87	12 kΩ
C101	680 nF	R91	1.5 kΩ
C102	1 nF		
C113	22 nF		
C114	1 nF	U1	See notes
C116	150 nF		

Notes:
1 Resistors ±1%, capacitors ±5% unless otherwise stated.
2 For optimum lock time / phase noise it is recommended C113 and C116 use a low piezo type such as PPS film; optimum performance is not guaranteed with X7R or Y5V types.
3 U1 Should be a VCTCXO or TCXO depending on application requirements. A typical device is the Golledge GTXO-83. The CMX990 has a high impedance input suitable for use with oscillators with clipped sine wave output. An external DC blocking capacitor (as shown, C4) is required.
4 Ground currents on the board can result in contamination of the IFCLK signal, so for the best possible results use a balun to connect the differential inputs IFCLK and IFCLKN to the VCO. However, adequate elimination of ground noise may be achieved by connection of the IFCLKN to the ground of the VCO.
5 The IFCLK pin needs to be ac coupled. In the case of differential drive it is recommended that external dc-blocking capacitors for both IFCLK and IFCLKN be used so as to provide equal paths for both complementary signals.

4.4 Transmitter

The CMX990 transmitter uses an offset phase-locked loop to accurately modulate RF signals. Details are contained in subsequent sections of this document. The components used around the CMX990 will depend on application requirements however a typical configuration is shown in Figure 5.

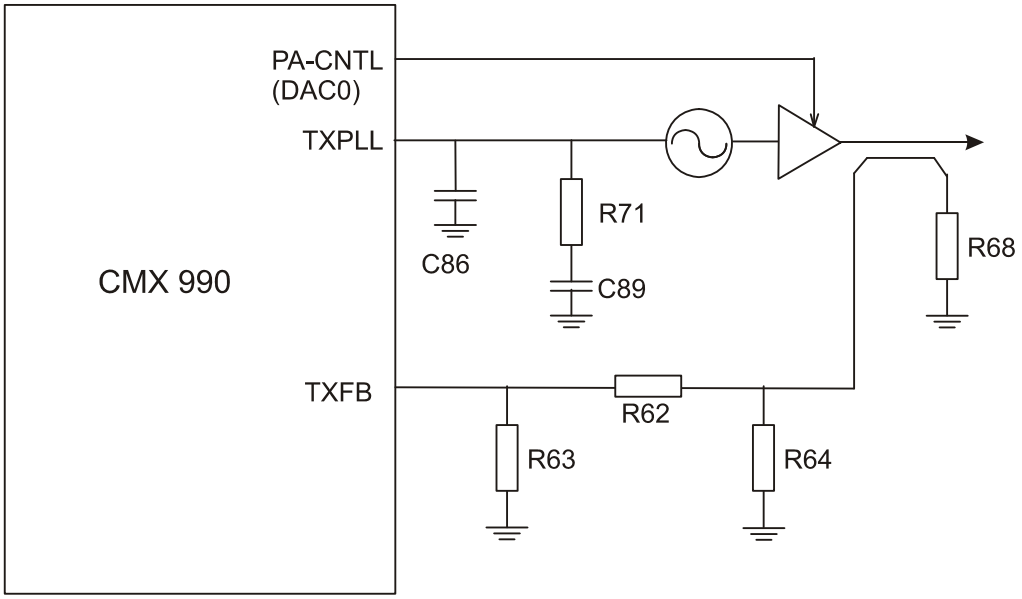


Figure 5 Recommended External Components - Transmit

C86	15 nF	R62	18 Ω
C89	68 nF	R63	270 Ω
		R64	270 Ω
		R68	47 Ω
		R71	36 Ω

Notes:
1 Resistors ±1%, capacitors ±5% unless otherwise stated.
2 The coupler may be a packaged type (e.g. 0869CP14A090 for 800MHz operation), a lumped element type or printed on the PCB; alternatively a sample of the output can be obtained with a resistive or capacitive tap.
3 Tx loop filter components need to be optimised for the selected VCO.

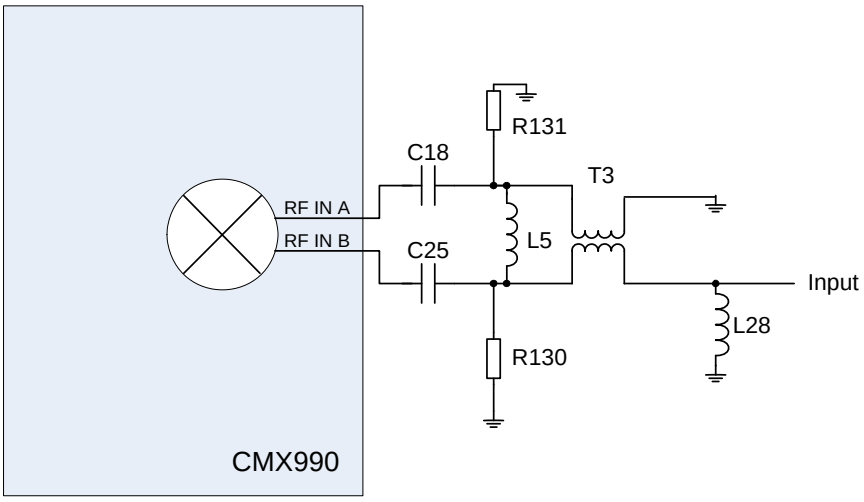
4.5 Receiver

The receiver relies on external LNA, filtering and T/R switch; details can be found in the following sections. The 1st mixer in the CMX990 has a differential input. To ensure optimum performance a balun is required when driving from typical single un-balanced LNAs or filters. The balun may be a transformer type or implemented using LC networks.

The input impedance to the CMX990 mixer is relatively high so suitable matching components around the balun should be selected for the desired operating frequency to provide a match to the desired impedance e.g. 50Ω. Figure 6 shows a typical configuration for 800 - 840MHz operation and Figure 8 for 360-490MHz operation.

Two matching configurations can be used for either best noise figure or best inter-modulation performance. In configuration 1 two 100ohm resistors are fitted (R131 and R130). These define the matching impedance but result in a small loss of signal although as the input is essentially a voltage swing the loss is not as much as might be expected. This configuration gives optimum inter-modulation performance. The alternative arrangement is to omit the resistors and match the impedance directly. This results in a small degradation in inter-modulation but provides an improved noise figure. Typical results for 800MHz operation are:

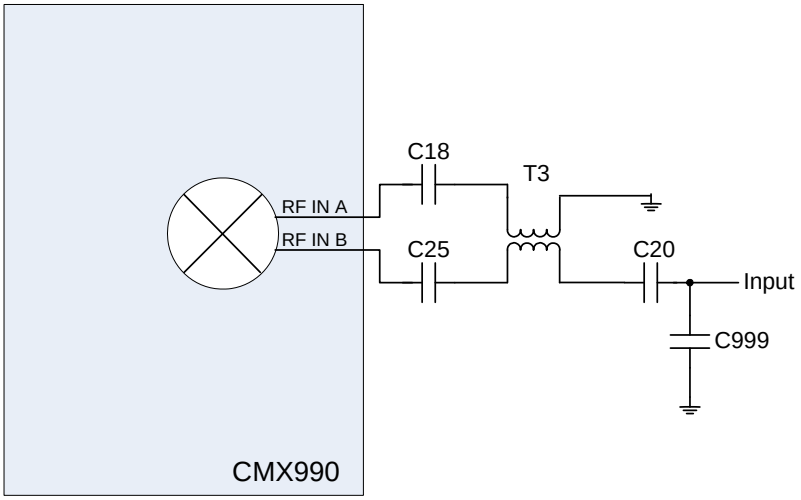
	Configuration 1	**Configuration 2**
Noise Figure (See Note 17 Section 7.1.3, page 91)	15dB	13dB
Input Third Order Intercept Point	+9.5dBm	+6.5dBm
1dB Compression point	-7dBm	-9.5dBm



C18	1 nF	L5	8.2 nH
C25	1 nF	L28	18 nH
		T3	TC1-1-13M+
R130	100 Ω	R131	100 Ω

Figure 6 Recommended External Components (800MHz) – Receive Mixer Configuration 1

Notes:
1 Resistors ±1%, capacitors and inductors ±5% unless otherwise stated.
2 Values for L5, L28 are typical matching values for 800MHz operation.

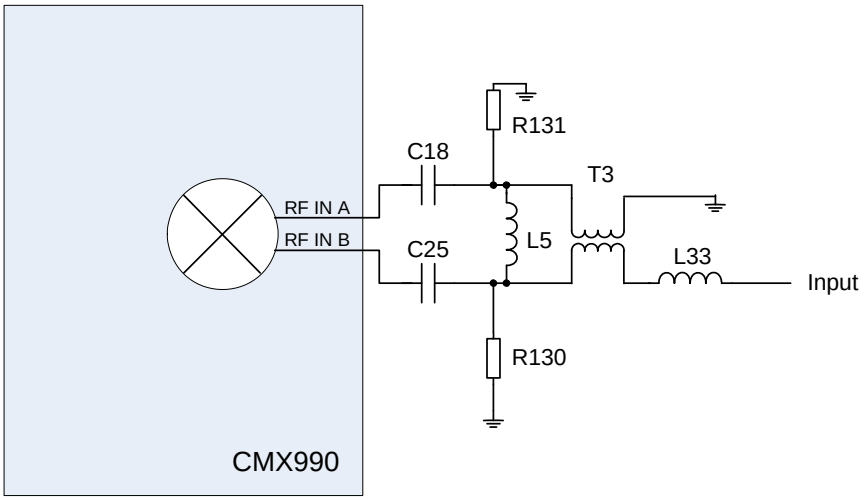


C18	1 nF	C20	4.7 pF
C25	1 nF	C999	2.2 pF
		T3	TC1-1-13M+

Figure 7 Recommended External Components (800MHz) – Receive Mixer Configuration 2

Notes:

1 Resistors ±1%, capacitors and inductors ±5% unless otherwise stated.
2 C20, C999 values are typical values for 800MHz operation.



C18	1 nF	L5	56 nH
C25	1 nF	L33	18 nH
R130	100 Ω	T3	TC1-1-13M+
R131	100 Ω		

Figure 8 Recommended External Components (400MHz) – Receive Mixer Configuration 1

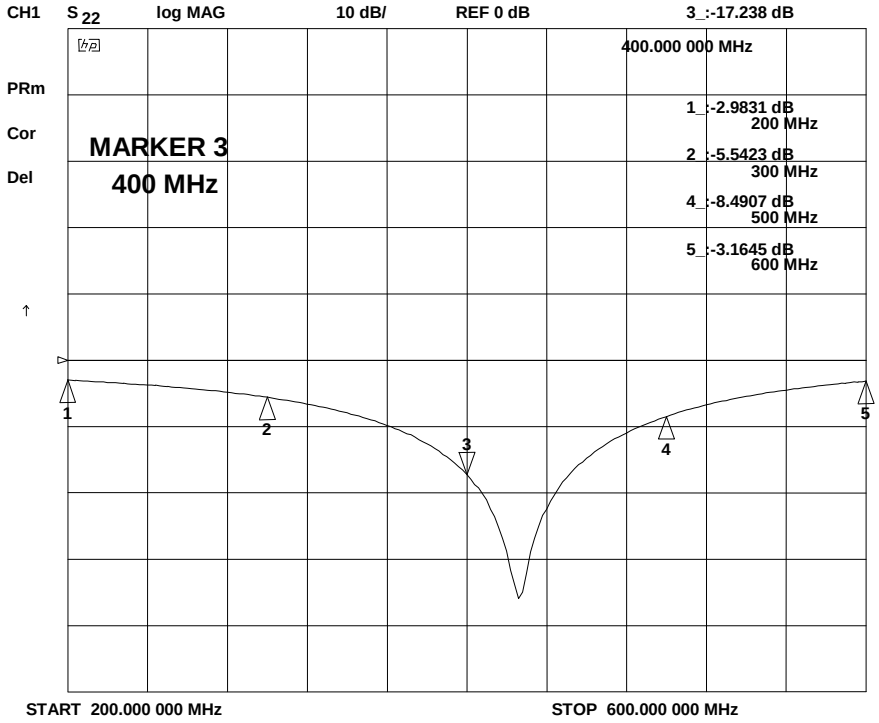
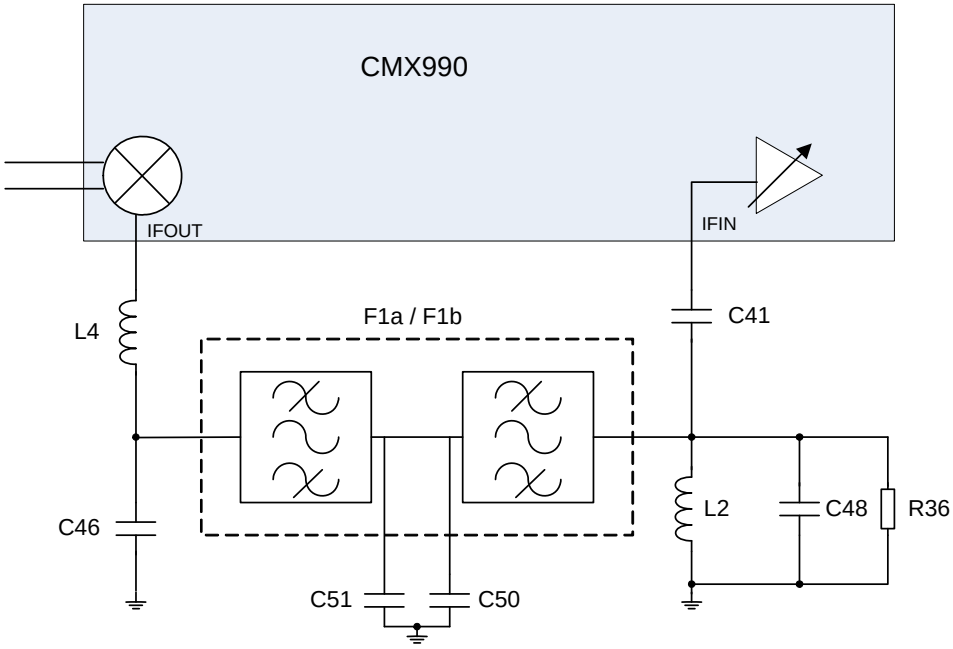


Figure 9 400MHz input match return loss with matching as Figure 8.

The output of the CMX990 first receive mixer should be at an IF in the range 44 to 46MHz. Only IF's in this range will benefit from the image reject functionality of the mixer. Between the mixer and IF amplifier stages a crystal filter is recommended. This filter is to protect the IF amplifier and subsequent stages from off-channel signals. Matching arrangements will vary, being dependant on the filter used, however an example of a typical configuration for a 45MHz IF is given in Figure 10.



C41	1 nF	L2	1.2 μH
C46	1 pF	L4	1.2 μH
C48	1 pF	R36	680 Ω
C50	4.7 pF	F1	MA08340
C51	5.6 pF		

Figure 10 Recommended External Components – Receive IF Section

Notes:

1 Resistors ±1%, capacitors and inductors ±5% or better unless otherwise stated.

2 F1 is a SMT 4 pole crystal filter implemented as a matched pair with a ±6kHz pass-band, load 500R//4pF, Cc = 13pF. The part is available from Golledge Electronics (www.golledge.com). Other parts may be equally suitable although matching arrangements will vary and different filters are recommended for different channel bandwidths and performance requirements. When selecting and matching a crystal filter care should be taken to ensure a flat pass-band and the performance should always be checked with a specific PCB layout. For further information on filter selection see section 6.5.1 and Table 3.

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4.6 Power Supply Decoupling and Layout

The CMX990 has dual supply voltages: a 3.3V supply is required for the PLLs and charge pump circuits and for the digital I/O pads, and a 2.5V supply (with separate decoupling) is required for the RF sections (Rx1, Rx2, Tx) as well as the baseband analogue and digital circuits.

The 3.3V supply must be provided by an external regulator circuit. The 2.5V supply may be provided by an external regulator, or alternatively may be derived from the 3.3V supply using an off-chip low saturation voltage transistor in conjunction with the on-chip control circuit (enabled by register PowerUp1 bit 5) - an example of this arrangement is shown in Figure 11. Whichever method is used to generate the 2.5V it is essential that all the circuits relying on this supply are powered down before this 2.5V source is turned off. The CMX990 will then allow the supply to drop to 2.0V, at which point it will be clamped by a separate on-chip micropower regulator. This is done so that the data in the on-chip registers and memories is not lost. The main 2.5V regulator circuit must be powered up again and allowed to settle before any RF or analogue circuitry, or the clock to the internal logic, is enabled. In other words, PowerUp1 ($04 - bits 7-6 and 4-0) and PowerUp2 ($05 - bits 7-4 and 0) must be set low whenever the 2.5V supply is unavailable.

The circuit shown in Figure 11 is an example, and will require that the 3.3V supply is regulated to within +/- 5%. This is necessary to ensure that the PNP transistor shown (TR3) does not enter saturation, taking worst case ambient conditions and bandgap / component tolerances into account.

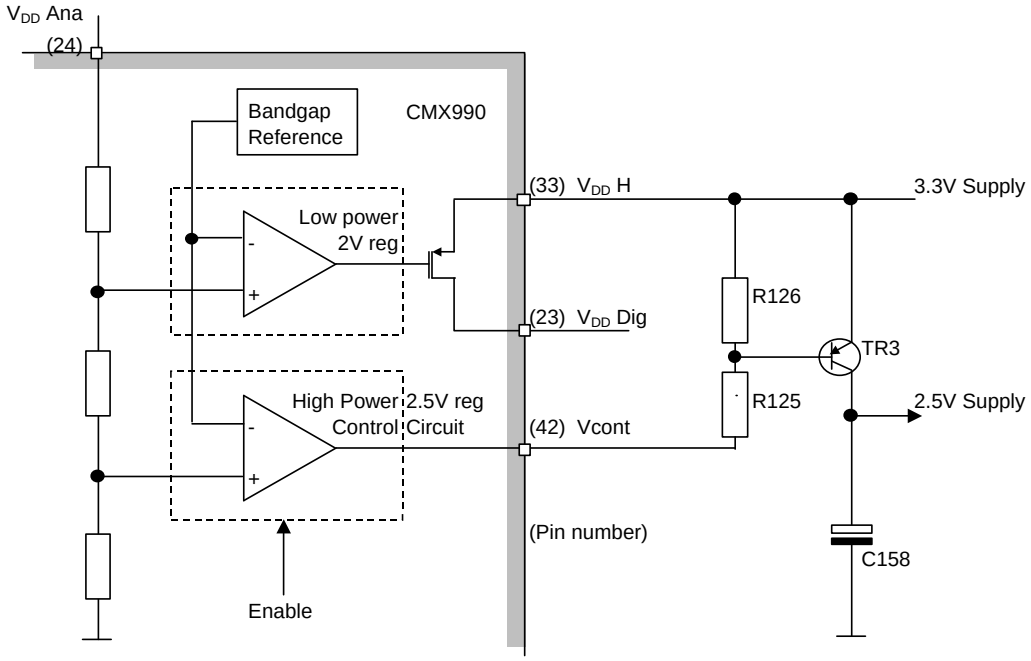

Figure 11 Voltage Regulator Connections

C158	100 µF	R125	330 Ω
TR3	PMBT4403	R126	47 kΩ

Resistors ±5%, capacitors ±20% or better.

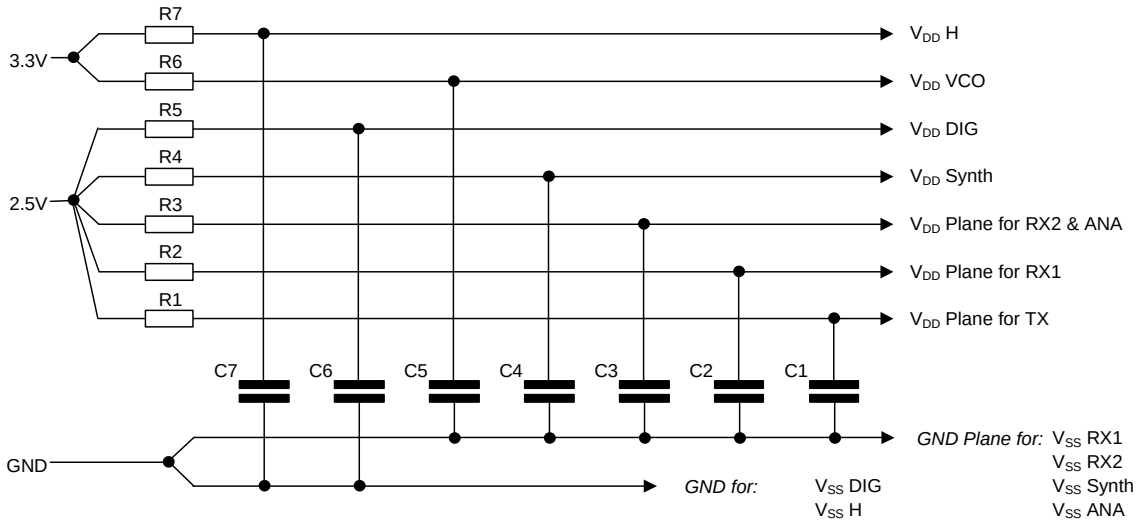

Figure 12 Power Supply Connections and De-coupling

C1	10 nF	R1	2.2 Ω
C2	10 nF	R2	2.2 Ω
C3	10 nF	R3	3.3 Ω
C4	10 nF	R4	10 Ω
C5	10 nF	R5	10 Ω
C6	10 nF	R6	10 Ω
C7	10 nF	R7	10 Ω

Resistors ±5%, capacitors ±20% unless otherwise stated.

Note:

It is expected that low frequency interference on the 3.3 Volt supply will be removed by active regulation; although a large capacitor is an alternative it may require more board space and so may not be preferred by the user. It is particularly important, however, to ensure that there is no interference from the V_{DD} H (which supplies the digital I/O) or from any other circuit that may use the 3.3V supply (such as a microprocessor) to sensitive analogue supplies like V_{DD} VCO or, importantly, the external RF VCO supplies.

The supply decoupling shown is intended for RF noise suppression only. It is necessary to have a small series impedance prior to the decoupling capacitor for the decoupling to work efficiently with physically small capacitors; this may be cost effectively done with the resistor and capacitor values shown. The use of resistors results in a small DC voltage drops (up to approx 0.1V). Choosing resistor values approximately inversely proportional to the DC current requirements of each supply, ensures the DC voltage drop on each supply are reasonably matched. The internal regulator uses V_{DD} ANA as its feedback, so this will compensate to reduce this voltage drop. In any case the DC voltage change that results is well within the design tolerance of the device. If higher impedance resistors are used (not recommended) then greater care will be needed to ensure the supply voltages are maintained within tolerance, even when individual parts of the device are enabled or disabled.

5 General Description

The CMX990 comprises a baseband modem and an associated RF section to provide a GMSK data modem including the ability to support the Mobitex air-interface. Device control and status is transferred via a set of memory mapped registers. An overview of the operation of the Modem is provided in section 5.1 and the RF / IF functions in section 5.2. These are followed by detailed description of the Host µC interface in section 5.3. Further application information is contained in section 6.

5.1 Baseband Modem

This section has been designed to be compliant with the appropriate sections of the "Mobitex Interface Specification" including Short Block Frame formatting for the extended battery saving protocol. References to 'data blocks' in this section apply to both the normal (18 byte) Data Block and the smaller (4 byte) Short Data Block.

The function of this section is further divided into Receive and Transmit sections that operate in half duplex.

In transmit mode the data may be encoded according to the Mobitex standard. This includes the calculation and appending of a Cyclic Redundancy Checksum (CRC) and Forward Error Correction (FEC), and Interleaving to reduce the effects of noise (note these functions can be bypassed if required). The subsequent NRZ data stream is then filtered digitally and the resulting digital data processed to produce an I and Q signal as the baseband form of the required FM signal. These are converted to analogue signals via D-A converters and passed to the RF section for subsequent transmission.

In receive mode, the analogue I and Q representations, at baseband, of the FM signal from the RF section are converted to digital signals via A-D converters. These signals are digitally filtered to suppress the adjacent channels and demodulated digitally. The resulting signal is then filtered, to optimise the signal to noise performance, before slicing to resolve into a digital bit stream. Mobitex specified error correction and de-interleaving can be applied and the resulting data is presented for transfer to an external processor.

5.1.1 Description of Blocks

Status and Data Quality Registers

8-bit registers which the µC can read to determine the status of the modem and the received data quality.

Command, Mode and Control Registers

The values written by the µC to these 8-bit registers control the operation of the modem.

Data Buffer

An 18-byte buffer used to hold receive or transmit data to or from the µC.

Frame Assembly / Disassembly

Each of these blocks consists of 4 circuits which generate (in transmit mode) or check (in receive mode) the bits of both short and normal Mobitex data blocks.

CRC Generator/Checker

A circuit which generates (in transmit) or checks (in receive) the CRC bits, which are included in transmitted Mobitex data blocks so that the receive modem can detect transmission errors.

FEC Generator/Checker

In transmit mode this circuit calculates and adds the FEC (4 bits) to each byte presented to it. In receive mode the FEC information is used to correct most transmission errors that have occurred in Mobitex data blocks or in the Frame Head control bytes.

Interleave/De-interleave Buffer

This circuit interleaves data bits within a data block before transmission and de-interleaves the received data block so that the FEC system is best able to handle short noise bursts or signal fades.

Scramble/De-scramble

This block may be optionally used to scramble/de-scramble the transmitted and received data blocks. It does this by modulating the data with a 511-bit pseudorandom sequence, as described in section 6.2.4. Scrambling improves the transmitted spectrum, especially when repetitive sequences are to be transmitted.

Frame Sync Detect

This circuit, which is only active in receive mode, is used to look for the user specified 16-bit Frame Synchronisation pattern which is transmitted to mark the start of every frame.

Tx Modulator and Low Pass Filter

The filter is used in transmit mode and is a low pass transitional Gaussian filter having a 3dB loss at 0.27, 0.3 or 0.5 times the bit rate (BT=0.27, 0.3 or 0.5). See Figure 13. This filter eliminates the high frequency components which would otherwise cause interference into adjacent radio channels. The BT=0.27 option is added as means of meeting the more stringent regulatory requirements for Adjacent Channel Power (for example EN 300 113).

The unmodulated baseband 'eye' diagrams of the transmitted signal is shown in Figure 14.

The Tx Modulator converts the baseband signal into an I and Q form which is passed to the Tx IF stage.

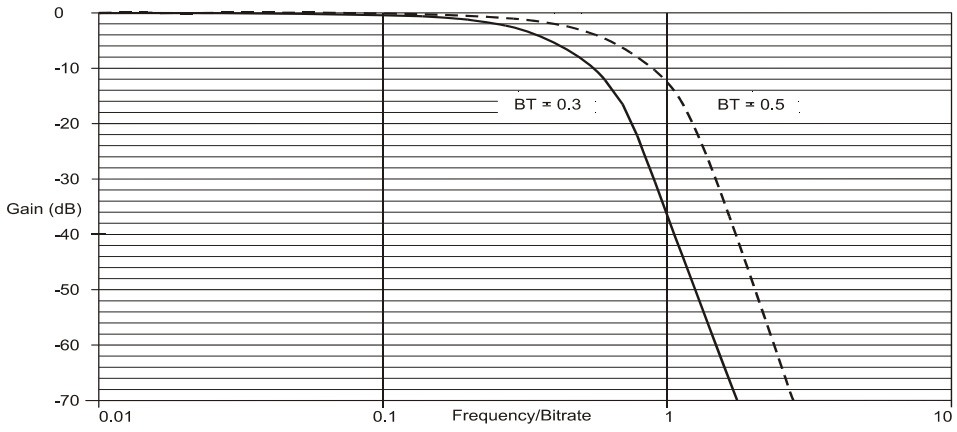

Figure 13 Typical Tx Baseband Filter Response

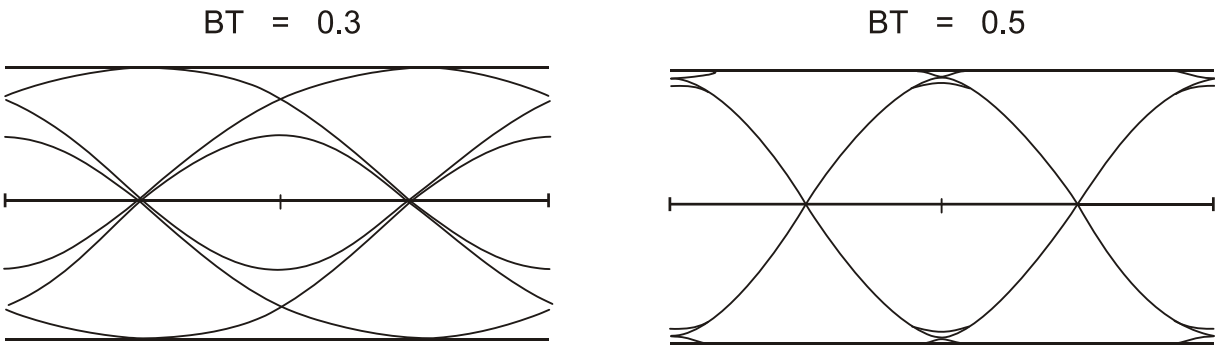

Figure 14 Baseband Transmitter Signal Eye Diagrams

Rx Low Pass Filter

This filter is a low pass transitional Gaussian filter having a 3dB loss at 0.56 times the bit rate (BT=0.56). It is used to reject HF noise to improve the BER.

Level Track and DPLL

These circuits, which operate only in receive mode, extract a bit rate clock from the received signal and measure the received signal amplitude and dc offset. This information is then used to extract the received bits and also to provide an input to the received Data Quality measuring circuit.

5.1.2 Modem - µC Interaction

In general, data is transmitted over air in the form of messages, or 'Frames', consisting of a 'Frame Head' optionally followed by one or more formatted data blocks. The Frame Head includes a Frame Synchronisation pattern designed to allow the receiving modem to identify the start of a frame. The following data blocks are constructed from the 'raw' data using a combination of CRC (Cyclic Redundancy Checksum) generation, Forward Error Correction coding, Interleaving and Scrambling. Details of the message formats handled by this modem are given in section 5.1.3 and further information is given in sections 6.2, 6.2.3, 6.2.4 and 6.3.

To reduce the processing load on the host µC, this modem has been designed to perform as much as possible of the computationally intensive work involved in Frame formatting and de-formatting and (when in receive mode) in searching for and synchronising onto the Frame Head. In normal operation the modem will only require servicing by the µC once per received or transmitted data block.

Thus, to transmit a block, the host µC has only to load the unformatted (raw) binary data into the modem's data buffer then instruct the modem to format and transmit that data. The modem will then calculate and add the CRC bits as required, encode the result with Forward Error Correction coding, interleave then scramble the bits before transmission.

In receive mode, the modem can be instructed to assemble a block's worth of received bits, de-scramble and de-interleave the bits, check and correct them (using the FEC coding) and check the resulting CRC before placing the received binary data into the Data Buffer for the µC to read.

The modem can also handle the transmission and reception of unformatted data, to allow the transmission of special Bit and Frame Synchronisation sequences, test patterns or custom data formats.

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5.1.3 Data Formats

Raw data
If required the user may transmit and receive raw data. This is transferred between the host and device a byte (8 bits) at a time.

Note that it is important to have established frame synchronisation before receiving data to enable the receiving device to decode synchronously. The user may add error detection and correction by way of algorithms performed on the host device.

General Purpose Formats
In a proprietary system the user may employ the data elements provided by this device to construct a custom, over-air data structure.

For example, 16 bits of bit sync + 2 bytes of frame sync + 4 bytes of receiver and sender address + n data blocks would be sent as:

TQB (bit and frame sync) + TQB (addresses) + (n x TDB) + TSB

And received as:

SFS + RSB + RSB + RSB + RSB + (n x RDB)

Mobitex Frame Structure
The Mobitex format for transmitted data is in the form of a Frame Head immediately followed by either 1 Short Data Block or a number of Data Blocks (0 to 32).

The Frame Head consists of 7 bytes:

2 bytes of bit sync:
1100110011001100 from base,
0011001100110011 from mobile
bits are transmitted from left to right

2 bytes of frame sync:
System specific.

2 bytes of control data.

1 byte of FEC code, 4 bits for each of the control bytes:
bits 7-4 (leftmost) operate on the first control byte.
bits 3-0 (rightmost) operate on the second control byte.

Each byte in the Frame Head is transmitted bit 7 (MSB) first to bit 0 (LSB) last.

The normal and short data blocks consist of:

18 bytes of data (Data Block) **OR** 4 bytes of data (Short Data Block).

2 bytes of CRC calculated from the data bytes.

4 bits of FEC code for each of the data and CRC bytes

The resulting data block bits are interleaved and scrambled before transmission.

Figure 15 shows how the over air signal is built up from Frame Sync and Bit Sync patterns, Control bytes and Data Blocks. The binary data transferred between the modem and the host µC is that shown enclosed by the thick dashed rectangles near the top of the diagram.

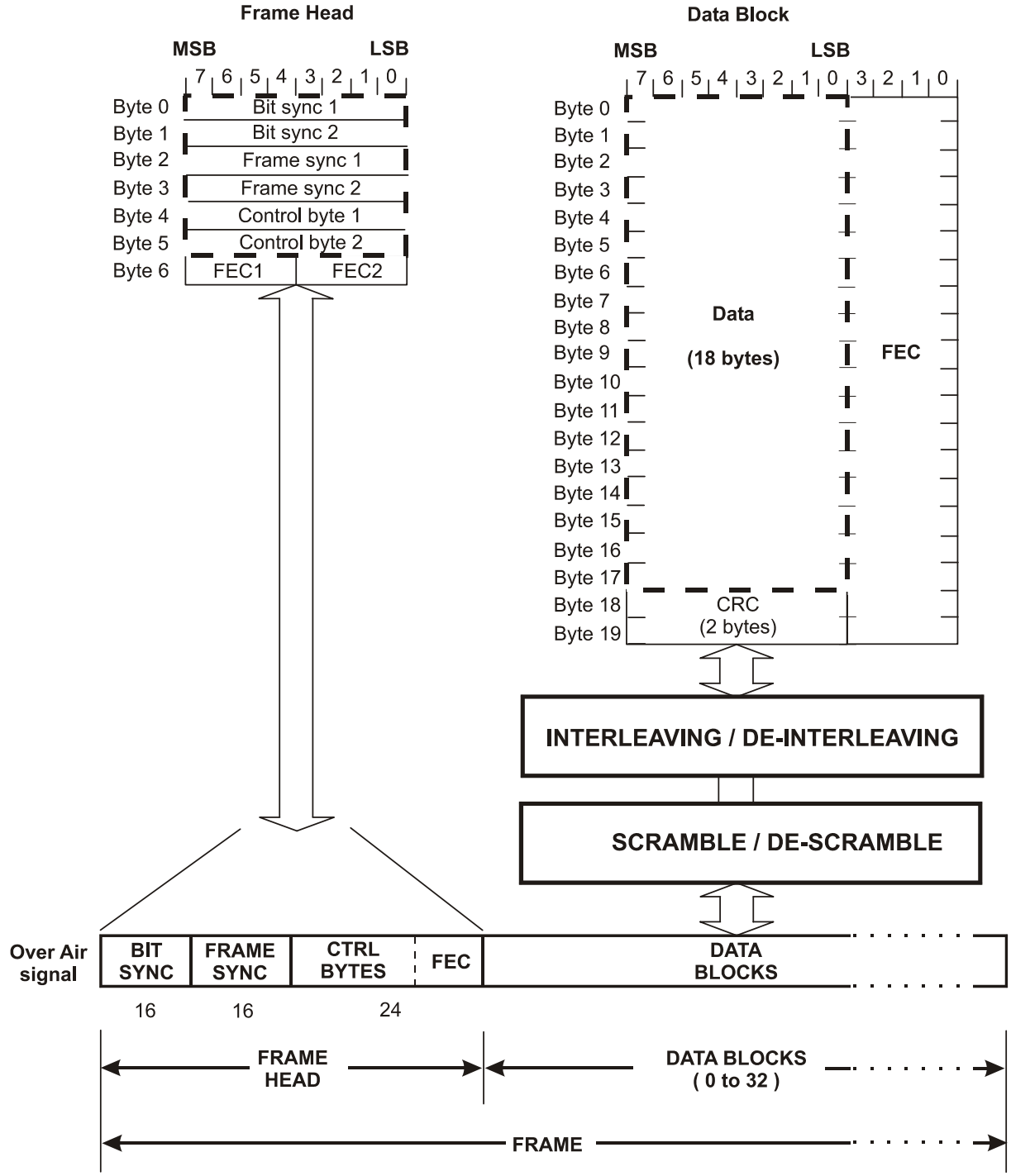

Figure 15 Mobitex Over Air Signal Format

5.1.4 Modem Interface

The data modem interfaces to the RF circuits using I and Q format for both transmit and receiver. Operation can be seen in Figure 1. On the transmitter the frame assembly block feeds data to the modulator which creates I and Q data streams for internal digital to analogue converters (DAC). The

output of the DAC is differential and is filtered to remove spurious responses before being passed to the analogue RF stages.

The input to the receiver section of the modem comes from the analogue receiver stages as a differential signal in I/Q format. Anti-alias filters are used prior to analogue to digital conversion (ADC). The analogue circuits include the ability to minimise DC offset errors, thus optimising the dynamic range of the signal. Further DC offset correction is applied in the signal processing after the ADC (for further details see section 6.5.2). Following the ADC FIR channel filters (see section 6.5.1) are applied prior to demodulation and associated timing recovery and synchronisation.

5.2 RF and IF

The CMX990 is a broadband RF modem system. The RF section can support transmission and reception between 400MHz and 1GHz.

The transmitter and receiver parts are designed for half duplex operation so should be operated mutually exclusively - normally the non-utilised part being powered down when not in use. For single antenna operation an external transmit/receive (T/R) switch is required.

The transmitter takes the baseband I and Q signals from the modem (See section 5.1 and Figure 1) and up-converts them via a quadrature modulator to a suitable Intermediate Frequency (IF). An offset PLL is then used to control an external VCO which translates the IF to the desired transmission frequency. The output of the VCO is sampled, usually after amplification, and mixed down to the IF; this mixed down signal is then phase/frequency compared with the IF signal from the quadrature modulator. The output of the phase comparator is fed to an external loop filter, which controls the VCO thereby closing the loop. The VCO output then will be an FM signal at the required RF frequency having a low out-of-band spurious response typical of VCO driven transmitters whilst guaranteeing a modulation index of exactly 0.5. The output of the VCO requires amplifying with an external PA (Power Amplifier).

The receiver requires use of an external LNA with some pre-filtering and an external balun. The differential output from the balun is down converted by an image reject mixer to a suitable IF (typically 45 MHz). The single ended IF signal is filtered with an external filter to remove spurious signals and this goes into an AGC stage with a gain control range of 45dB. The output of the AGC is mixed down to I and Q signals at baseband via quadrature mixers. The I and Q signals are amplified and filtered to remove any signals that may alias with the subsequent A-D sampling. The amplifier also has a coarse offset removal system to allow the approximate nulling of DC offsets developed in the circuits that may restrict the dynamic range in the subsequent processing.

As with any RF system care is required with frequency planning to minimise component count, avoid spurious responses etc. A examples of typical frequency planning is shown in Figure 17 and further discussion is given in section 6.5.1.

5.2.1 Transmitter Section

I and Q signals from the Modem block are base-band representations of the required modulated RF signal. These are up-converted by a quadrature modulator stage to a suitable IF. The summed output from this stage has the required modulation index but at a lower frequency (TXIF, typically 45MHz or 90MHz) than that required for transmission. The CMX990 provides either divide by 2 or divide by 4 from the programmed auxiliary local oscillator frequency to aid IF selection.

An Offset Phase Locked Loop (O-PLL) is used to translate this modulated TXIF signal to the appropriate carrier frequency. The O-PLL architecture is shown in Figure 16. The O-PLL works as a feedback loop with the TXIF signal as it's reference input. Considering the forward path the final frequency modulation is generated by a VCO which then drives a power amplifier to generate the required output level. The full power signal is sampled and then attenuated externally and / or on chip. For the signal sampling a directional coupler is recommended although a simple sample of the PA output can be used. The

attenuated signal is then down-mixed with the main LO signal to a frequency nominally the same as the TXIF value. The resulting signal is low-pass filtered to remove unwanted mixer products. This filter can be set to two values depending on the TXIF in use (section 5.3.11). A high gain limiting amplifier is then used to enable the loop to have a high dynamic range and to lock-in even when the transmitted signal is very small, e.g. when just starting to ramp up. The output of the limiting amplifier is then phase/frequency compared with the TXIF reference signal from the modulator, the charge pump output being passed off chip into a suitable loop filter. The filtered output controls the VCO with its nominal frequency set to the middle of the required transmission band. When the loop is locked, the VCO follows the frequency modulations of the reference signal so as to give an exact modulation index of 0.5 whilst having the low spurii in transmission typical of a VCO based system.

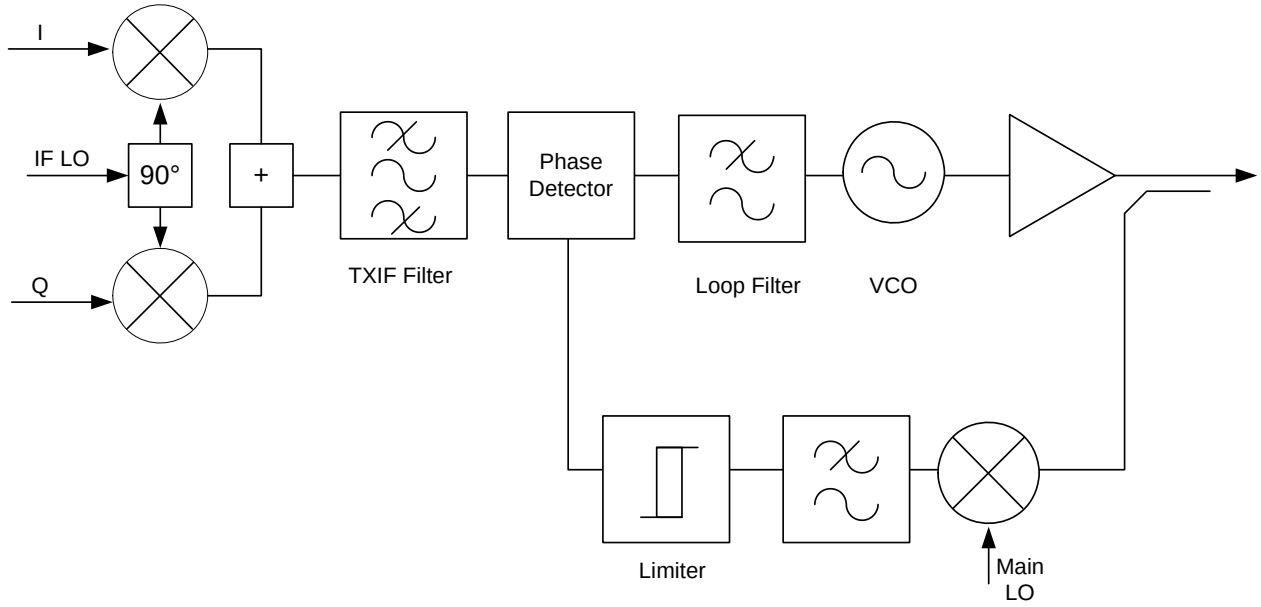

Figure 16 Block Diagram of Offset Phase Locked Loop Transmitter

As noted above, the output of the VCO is generally amplified with a Power Amplifier. A special feature of one of the Auxiliary D-A converters may be used to control the ramping of the power amplifier optimally should this be required. This feature is explained in section 5.3.6. The Auxiliary A-D section can also be used for sensing the forward and reverse power values, and the PA temperature should these features be required.

Further information on the transmitter operation can be found in section 6.4.

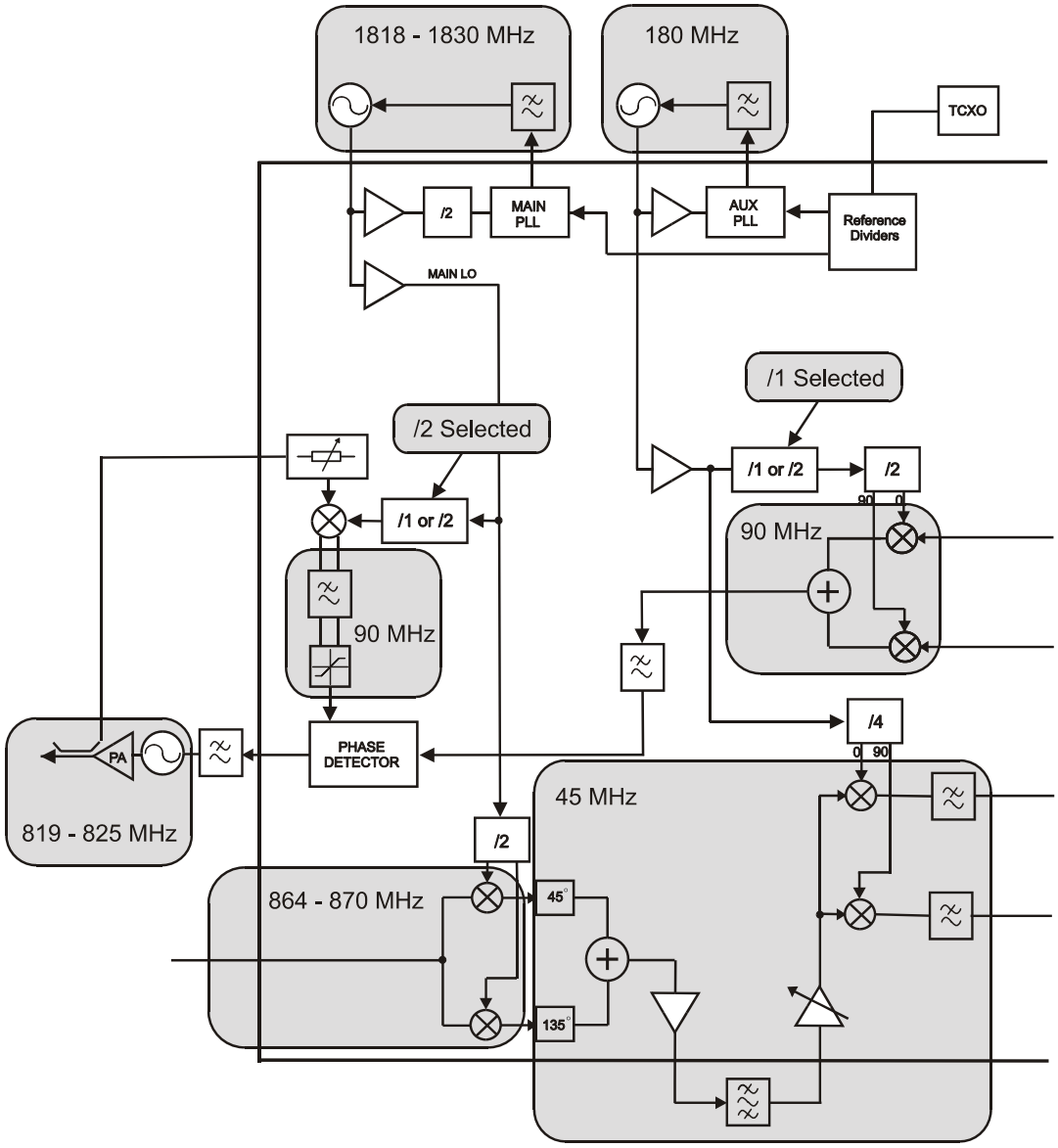

Figure 17 Simplified Block Diagram of CMX990 Showing Example Frequency Plan for 864-870MHz (Rx) / 819-825MHz (Tx) band

5.2.2 Receiver Section

It is expected that the signal from the T/R switch will be amplified via an external LNA. The use and positioning of an image reject filtering is up to the radio designer. As a guide, the Mobitex specification requires a minimum of 45dB of first image rejection of which at least 30dB will be provided by the on-chip image reject mixer stage. The design is optimised with an LNA gain of about 15dB. It has been assumed that there is some insertion loss prior to the LNA; but an overall noise figure of 4dB and gain of 10dB (approx.) is achieved by the circuits preceding the CMX990. A digital control signal is available from the chip which should be used to enable/disable the LNA. A balun must be used to produce a differential signal to the first mixer on the chip.

The Image Reject Mixer down-converts the signal to 45 MHz, although this frequency may be changed slightly if necessary, for example when used in regions where there may be conflicts with local broadcast transmissions. The resulting IF is then output from the chip as a single ended signal for filtering. A relatively low cost crystal filter can be used to remove signals outside the channel bandwidth. The specification of this filter will vary with the intented application. For detailed filter requirements see Table 3 (section 6.5.1).

The IF-signal from the filter is then taken back on chip to an amplifier stage which includes gain control, thus allowing Automatic Gain Control (AGC) to be implemented. The AGC is adjustable in steps of 15dB from -5dB to +40dB and can be adjusted automatically by the chip or may be controlled by instruction from the host processor.

The output from the AGC is then mixed down to baseband, by a quadrature mixer stage, to produce I and Q signals. These are then filtered, to remove unwanted mixer products, spurii and remaining blocking signals and at the same time amplified to a suitable level for subsequent A-D conversion. The filters also precondition the signal to prevent aliasing with the A-D sample frequency. Channel filtering is provided digitally in the baseband processing section (see section 6.5.1).

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5.3 Memory Map, Interface and Register Functions

The following is a summary of the internal registers as seen by the host, details of operation may be found in the relevant section.

Address	Read	Write
$00	Data Buffer (Rx)	Data Buffer (Tx)
$01	Status 1	Command
$02	Data Quality	Control
$03	Status 2	Mode
$04	Freq Offset	Power Up 1
$05	RSSI	Power Up 2
$08	Aux ADC 0 LSB	Aux DAC 0 LSB
$09	Aux ADC 0 MSB	Aux DAC 0 MSB
$0A	Aux ADC 1 LSB	Aux DAC 1 LSB
$0B	Aux ADC 1 MSB	Aux DAC 1 MSB
$0C	Aux ADC 2 LSB	Aux DAC 2 LSB
$0D	Aux ADC 2 MSB	Aux DAC 2 MSB
$0E	Aux ADC 3 LSB	Aux DAC 3 LSB
$0F	Aux ADC 3 MSB	Aux DAC 3 MSB
$10	Aux ADC 4 LSB	RAM DAC control
$11	Aux ADC 4 MSB	Aux ADC control 1
$12	Aux ADC 5 LSB	Aux ADC control 2
$13	Aux ADC 5 MSB	-
$14	-	Aux Ram Data1 LSB
$15	-	Aux Ram Data1 MSB
$16	-	Aux Ram Data2 LSB
$17	-	Aux Ram Data2 MSB
$18	Analogue Setup 1	Analogue Setup 1
$19	Analogue Setup 2	Analogue Setup 2
$1A	-	Special Command
$1B	Special Data0 LSB	Special Data0 LSB
$1C	Special Data0 MSB	Special Data0 MSB
$1D	Special Data1 LSB	Special Data1 LSB
$1E	Special Data1 MSB	Special Data1 MSB
$20	-	Main PLL M div LSB
$21	-	Main PLL M div MSB
$22	-	Main PLL N div LSB
$23	-	Main PLL N div NSB
$24	-	Main PLL N div MSB
$25	-	Aux PLL M div LSB
$26	-	Aux PLL M div MSB
$27	-	Aux PLL N div LSB
$28	-	Aux PLL N div MSB
$29	-	Clock Control
$3F	-	Test Output (see section 5.3.8.4)

Note: All unused addresses from $00 to $3F are reserved for future use.

5.3.1 Data Bus Buffers

The circuitry driving the D0-7 pins consists of 8 internal bidirectional 3-state logic level buffers between the internal registers and the external data bus lines.

5.3.2 Address and R/W Decode

Transfer of data bytes between the µC and the internal registers is controlled according to the state of the Write and Read Enable inputs (WRN and RDN), the Chip Select input (CSN) and the Register Address inputs A0 to A5.

The Data Bus Buffers, Address and R/W Decode blocks provide a byte-wide parallel µC interface, which can be memory-mapped, as shown in Figure 3.

5.3.3 Power-on and Reset

When the power is first applied to the device an internal circuit will reset internal registers to a known state and put all circuit blocks in an inactive and power saved state with the exception of the 'Enable Clock bit' in 'Power Up 1' register (section 5.3.5). This bit is set to '1' so that the device may respond to the TCXO clock which the reset task needs to complete its cycle.

The small current that this Clock enable circuit uses may be saved by writing all ‘0’s to the 'Power Up 1' register through the micro interface. Read bits will be reset to '0' - the inactive state. Counters / states will be reset to an inactive and known condition after a reset event - which can occur asynchronously.

Setting the RESET bit (Register $05, see section 5.3.5) to '1' is similar except the RESET bit does not control the 'V Reg”, 'Preserve registers' and 'Vbias' bits (shown in bold in the following register diagrams) and the ‘Clock Control Register’ ($29, see section 5.3.10), they will remain at the last programmed state. If minimum power is required and the ‘Clock Control register’ is using a value other than its default value of $18, it must be re-programmed with $18.

5.3.4 Modem Interface

The modem appears to the programmer as a series of 8-bit read and write registers, individual registers being selected by the A0 to A5 address pins. Most of the baseband control for formatting or decoding the data is controlled by the following registers:

Address	Write to Modem	Read from Modem
$00	Data Buffer	Data Buffer
$01	Command Register	Status 1 Register
$02	Control Register	Data Quality Register
$03	Mode Register	Status 2 Register

5.3.4.1 Data Buffer

Data Buffer $00 Write

Bit:	7	6	5	4	3	2	1	0
	Tx Data							

Data Buffer $00 Read

Bit:	7	6	5	4	3	2	1	0
	Rx Data							

This is an 18-byte read/write buffer which is used to transfer data (as opposed to command, status, mode, data quality and control information) between the modem and the host µC.

It appears to the µC as a single 8-bit register; the modem ensuring that sequential µC reads or writes to the buffer are routed to the correct locations within the buffer.

The µC should only access this buffer 2 µs after the Status Register BFREE (Buffer Free) bit is set to '1'.

The buffer should only be written to while in Tx mode and read from while in Rx mode (except when loading Frame Sync detection bytes while in Rx mode).

5.3.4.2 Command Register

Writing to this register tells the modem to perform a specific action or actions, depending on the setting of the TASK and acquire bits. The enable packet detect bit is used to indicate the presence of data signals in the receive path.

Command Register $01 Write

Bit:	7	6	5	4	3	2	1	0
	Acquire Bit Clock	Acquire I Q Offset	Acquire AFC	Enable packet detect	Task Control			

When it has no action to perform (but is not 'powersaved'), the modem will be in an 'idle' state. If the modem is in transmit mode the input to the Tx filter will be connected to a mid level. In receive mode the modem will continue to measure the received data quality and extract bits from the received signal, supplying them to the de-interleave buffer, but will otherwise ignore the received data.

Command Register B7: Acquire Bit Clock

This bit has no effect in transmit mode.

In receive mode, whenever a byte with the Acquire Bit Clock set to '1' is written to the Command Register, and TASK is not set to RESET, it initiates an automatic sequence designed to achieve bit timing synchronisation with the received signal as quickly as possible. This involves setting the Phase Locked Loop of the received bit timing extraction circuits to its widest bandwidth, then gradually reducing the bandwidth as timing synchronisation is achieved, until it reaches the 'normal' value set by the PLL Control bits of the Control Register.

Setting this bit to '0' (or changing it from '1' to '0') has no effect, however note that the acquisition sequence will be re-started every time that a byte written to the Command Register has the Acquire Bit Clock bit set to '1'. Details of the acquisition sequence are in section 5.3.4.3.

The Acquire Bit Clock will normally be set to '1' up to 12 bits before an SFS (Search for Frame Sync) or SFH (Search for Frame Head) task, however it may also be used independently to re-establish clock synchronisation quickly after a long fade. Alternatively, a SFS or SFH task may be written to the Command Register with the Acquire Bit Clock bit set to '0' if it is known that clock synchronisation does not need to be re-established. Details of the acquisition sequence are in section 5.3.4.3.

Command Register B6: Acquire I Q Offset

This bit has no effect in transmit mode.

In receive mode, when this bit is changed from a '0' to a '1' it initiates an automatic sequence designed to compensate the dc offset of the received I and Q signal. This sequence involves temporarily disabling the RF input and measuring dc offset and applying an appropriate correction. Once this has been completed the RF input will be reasserted and operation will then depending on the setting of bits 4 and 5 of the Control Register ($02). Details of the acquisition sequence are in section 5.3.4.3.

Changing this bit from '1' to '0' will terminate acquisition and the 'normal' value set by bits 4 and 5 of the Control Register ($02) will be carried out.

The Acquire I Q Offset bit will normally be set after changing or reacquiring a channel (e.g. after powering up from a sleep condition). This would normally be done so the acquisition sequence was completed before an SFS or SFH task is initiated. Alternatively, a SFS or SFH task may be written to the Command Register without previously setting the Acquire I Q Offset bit to '1' if it is known that there is no need to re-establish the received signal offsets, e.g. when receiving another message on the same channel in quick succession.

Note: SFH or SFS task should be set when the Acquire I Q Offset has completed and 12 bits after setting the Acquire Bit Clock sequence. For further discussion on I/Q offset correction see section 6.5.2.

Command Register B5: Acquire AFC

This bit has no effect in transmit mode.

In receive mode, when this bit is changed from a '0' to a '1' it initiates an automatic sequence designed to measure and compensate for small differences in the carrier frequencies of the transmitter and receiver. If the TCXO frequency is too far out the dc offset in the demodulated signal will become excessive and limit the decode performance of the device. In these cases the host must adjust the TCXO frequency via the on chip DAC based on the value read from the Frequency Offset register ($04).

In Mobitex systems the carrier frequencies of basestations are very accurate compared to the permitted tolerances of mobile units. Therefore once a mobile unit has set up it's local TCXO frequency it should be suitable for transmitting or receiving with any basestation. The Slow tracking mode should be sufficient to track any variations caused by environmental changes. Details of the acquisition sequence are in section 5.3.4.3.

Command Register B4: Enable packet detect

This bit has no effect in transmit mode.

In receive mode if this bit is set to '1' the device will monitor the demodulated waveform for signals likely to be valid data. The likely presence of valid data will be reported via bit 0 of Status Register 1. This information can assist in the timing of setting a SFS or SFH task. Note that some noise signals may appear in the baseband as valid data, the RSSI signal should be used to confirm that the received signal is suitable before relying on this signal, bearing in mind the RSSI averaging time, see section 5.3.8.6.

It is recommended that this bit is only set to '1' when searching for the start of a packet. Once a frame sync has been detected this bit should be set to '0' until the start of a new packet needs to be found.

Command Register B3, B2, B1, B0: Task

Operations such as transmitting a data block are treated by the modem as 'tasks' and are initiated when the µC writes a byte to the Command Register with the TASK bits set to one of the data handling commands (marked BOLD in the table below).

Mobitex modem tasks:

B3	B2	B1	B0	Receive Mode		Transmit Mode	
0	0	0	0	NULL		NULL	
0	0	0	1	**SFH**	Search for Frame Head	**T7H**	Transmit 7 byte Frame Head
0	0	1	0	**R3H**	Read 3 byte Frame Head		Reserved
0	0	1	1	**RDB**	Read Data Block	**TDB**	Transmit Data Block
0	1	0	0	**SFS**	Search for Frame Sync	**TQB**	Transmit 4 Bytes
0	1	0	1	**RSB**	Read Single Byte	**TSB**	Transmit Single Byte
0	1	1	0	**LFSB**	Load Frame Sync Bytes	**TSO**	Transmit Scrambler Output
0	1	1	1	RESET	Cancel any current action	RESET	Cancel any current action
1	0	0	1	**SFHZ**	SFH with zero errors		Reserved
1	0	1	1	**RSD**	Read Short Data Block	**TSD**	Transmit Short Data Block
1	1	0	0	**SFSZ**	SFS with zero errors		Reserved

Note: All other bit patterns are reserved.
Bold text indicates a 'data handling command'

The µC should not write a data handling command to the Command Register or write to or read from the Data Buffer when the BFREE (Buffer Free) bit of the Status 1 Register is '0'.

Different tasks apply in receive and transmit modes. Detailed timings for the various tasks are given in Figure 20 and Figure 21.

5.3.4.2.1 Transmit Operation

When the modem is in transmit mode, all data handling commands other than TSO instruct the modem to transmit data from the Data Buffer, formatting it as required. For these tasks the µC should wait until the BFREE (Buffer Free) bit of the Status 1 Register is '1', before writing the data to the Data Buffer. If more than 1 byte needs to be written to the Data Buffer, byte number 0 of the block should be written first. The host should then write the desired task to the Command Register.

Once the byte containing the desired task has been written to the Command Register, the modem will:

Set the BFREE (Buffer Free) bit of the Status 1 Register to '0'.

Take the data from the Data Buffer as quickly as it can - transferring it to the Interleave Buffer for eventual transmission. This operation will start immediately if the modem is 'idle' (i.e. not transmitting data from a previous task), otherwise it will be delayed until there is sufficient room in the Interleave Buffer.

Once all of the data has been transferred from the Data Buffer the modem will set the BFREE and IRQ bits of the Status 1 Register to '1', (causing the chip IRQN output to go low if the IRQ Enable bit of the Mode Register has been set to '1') to tell the µC that it may write new data and the next task to the modem.

In this way the µC can write a task and the associated data to the modem while the modem is still transmitting the data from the previous task. See Figure 18.

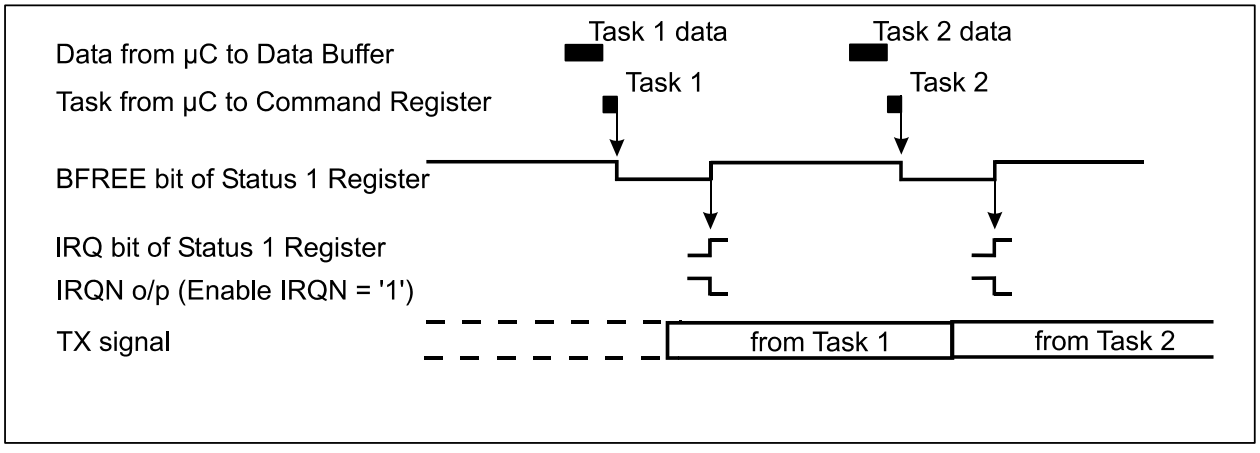

Figure 18 The Transmit Process

5.3.4.2.2 Receive Operation

When the modem is in receive mode, the µC should wait until the BFREE bit of the Status 1 Register is '1', then write the desired task to the Command Register.

Once the byte containing the desired task has been written to the Command Register, the modem will:

Set the BFREE bit of the Status Register to '0'.

Wait until enough received bits are in the De-interleave Buffer.

Decode them as needed, and transfer any resulting data to the Data Buffer.

Then the modem will set the BFREE and IRQ bits of Status 1 Register to '1', (causing the IRQN output to go low if the IRQ Enable bit of the Mode Register has been set to '1') to tell the µC that it may read from the Data Buffer and write the next task to the modem. If more than 1 byte is contained in the Data Buffer, byte number '0' of the data will be read first.

In this way the µC can read data and write a new task to the modem while the received bits needed for this new task are being stored in the De-interleave Buffer. See Figure 19.

The above is not true for loading the Frame Sync detection bytes (LFSB): the bytes to be compared with the incoming data must be loaded prior to the task bits being written.

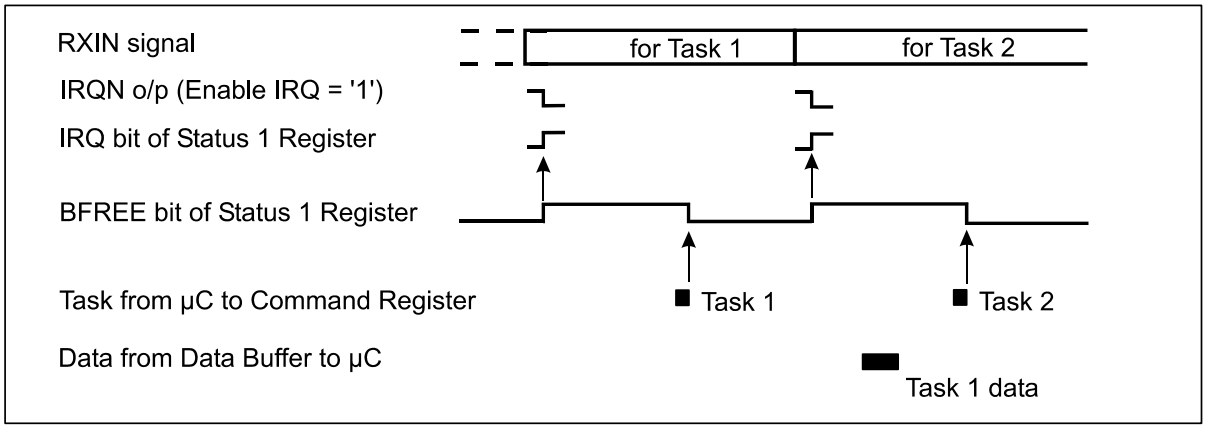

Figure 19 The Receive Process

Task Descriptions:

NULL - No effect

This task is provided so the acquisition commands can be issued without loading a new task.

SFH - Search for Frame Head

Causes the modem to search the received signal for a Frame Head. The Frame Head will consist of a 16-bit Frame Sync followed by control data (see Figure 15- Mobitex Over Air Signal). The search will continue until a Frame Head has been found, or until the RESET task is loaded.

The search is carried out by first attempting to match the incoming bits against the previously programmed (task LFSB) 16-bit Frame Sync pattern (allowing up to any one bit (of 16) in error). When a match has been found, the modem will read the next 3 received bytes as Frame Head bytes, these bytes will be checked, and corrected if necessary, using the FEC bits. The two Frame Head Data bytes are then placed into the Data Buffer.

The BFREE and IRQ bits of the Status 1 Register will then be set to a logic '1' to indicate that the µC may read the 2 Frame Head Data bytes from the Data Buffer and write the next task to the Command

Register. If the FEC indicates uncorrectable errors the modem will set the CRCFEC bit in the Status 1 Register to a logic '1'. The MOBAN bit (Mobile or Base) in the Status 1 Register will be set according to the polarity of the 3 bits preceding the Frame Sync pattern.

R3H - Read 3-byte Frame Head

This task, which would normally follow an SFS task, will place the next 3 bytes directly into the Data Buffer. It also causes the modem to check the 3 bytes as Frame Head control data bytes and will set the CRCFEC bit to a logic '1' (high) only if the FEC bits indicate uncorrectable errors. Note: This task will not correct any errors and, due to the Mobitex FEC specification, will not detect all possible uncorrectable error patterns. The BFREE and IRQ bits of the Status 1 Register will be set to '1' when the task is complete to indicate that the µC may read the data from the Data Buffer and write the next task to the modem's Command Register.

The CRCFEC bit in the Status 1 Register will be set according to the validity of the received FEC bits.

RDB - Read Data Block

This task causes the modem to read the next 240 bits as a Mobitex Data Block.

It will de-scramble and de-interleave the bits, FEC correct and CRC check the resulting 18 data bytes and place them into the Data Buffer, setting the BFREE and IRQ bits of the Status 1 Register to '1' when the task is complete to indicate that the µC may read the data from the Data Buffer and write the next task to the modem's Command Register. The CRCFEC bit will be set according to the outcome of the CRC check.

Note: in receive mode the CRC checksum circuits are initialised on completion of any task other than NULL.

SFS - Search for Frame Sync

This task, which is intended for special test and channel monitoring purposes, performs the first part only of a SFH task. It causes the modem to search the received signal for a 16-bit sequence which matches the Frame Synchronisation pattern with up to any 1 bit in error.

When a match is found the modem will set the BFREE and IRQ bits of the Status 1 Register to '1' and update the MOBAN bit. The µC may then write the next task to the Command Register.

RSB - Read Single Byte

This task causes the modem to read the next 8 bits and translate them directly (without de-interleaving or FEC) to a single byte which is placed into the Data Buffer (B7 will represent the earliest bit received). The BFREE and IRQ bits of the Status 1 Register will then be set to '1' to indicate that the µC may read the data byte from the Data Buffer and write the next task to the Command Register.

This task is intended for special tests and channel monitoring - perhaps preceded by an SFS task.

LFSB - Load Frame Sync Bytes

This task takes 2 bytes from the Data Buffer and updates the Frame Sync detect bytes. The MSB of byte '0' is compared to the first bit of a received Frame Sync pattern and the LSB of byte '1' is compared to the last bit of a received Frame Sync pattern. This task does not enable Frame Sync detection.

Unlike other Rx tasks, the data buffer must be loaded before the task is issued. This task must only be issued after a minimum of 4 bit times after a Command register Reset task. As Mobitex Frame Sync detect bytes are usually nationally or regionally set, this operation may easily be done after power up, or when changing channels.

Once the modem has read the Frame Sync bytes from the Data Buffer, the BFREE and IRQ bits of the Status 1 Register will be set to '1', indicating to the µC that it may write the next task to the modem.

SFHZ - Search for Frame Head with Zero Errors

This performs the same task as SFH task but allowing no bits to be in error over the 16-bit Frame Sync pattern.

RSD - Read Short Data Block

This task causes the modem to read the next 72 bits as a Mobitex Short Data Block.

It will de-scramble and de-interleave the bits, FEC correct and CRC check the resulting 4 data bytes and place them into the Data Buffer, setting the BFREE and IRQ bits of the Status 1 Register to '1' when the task is complete to indicate that the µC may read the data from the Data Buffer and write the next task to the modem's Command Register. The CRCFEC bit will be set according to the outcome of the CRC check.

Note: in receive mode the CRC checksum circuits are initialised on completion of any task other than NULL.

SFSZ - Search for Frame Sync with Zero Errors

This performs the same task as SFS task but allowing no bits to be in error over the 16-bit Frame Sync pattern.

T7H - Transmit 7-byte Frame Head

This task takes 6 bytes of data from the Data Buffer, calculates and appends 8 bits of FEC from bytes '4' and '5' then transmits the result as a complete Mobitex Frame Head.

Bytes '0' and '1' form the bit sync pattern, bytes '2' and '3' form the frame sync pattern and bytes '4' and '5' are the frame head control bytes. Bit 7 of byte '0' of the Data Buffer is sent first, bit 0 of the FEC byte last.

Once the modem has read the data bytes from the Data Buffer, the BFREE and IRQ bits of the Status 1 Register will be set to '1', indicating to the µC that it may write the next task and its data to the modem.

TQB - Transmit 4 Bytes

This task takes 4 bytes of data from the Data Buffer and transmits them, bit 7 first.

Once the modem has read the data bytes from the Data Buffer, the BFREE and IRQ bits of the Status 1 Register will be set to '1', indicating to the µC that it may write the next task and its data to the modem.

TDB - Transmit Data Block

This task takes 18 bytes of data from the Data Buffer, calculates and applies a 16-bit CRC and forms the FEC for the 18 data bytes and the CRC. This data is then interleaved and passed through the scrambler, if enabled, before being transmitted as a Mobitex Data Block.

Once the modem has read the data bytes from the Data Buffer, the BFREE and IRQ bits of the Status Register will be set to '1', indicating to the µC that it may write the next task and its data to the modem.

Note: In transmit mode the CRC checksum circuit is initialised on completion of any task other than NULL.

TSB - Transmit Single Byte

This task takes a byte from the Data Buffer and transmits the 8 bits, bit 7 first.

Once the modem has read the data byte from the Data Buffer, the BFREE and IRQ bits of the Status 1 Register will be set to '1', indicating to the µC that it may write the next task and its data to the modem.

TSO - Transmit Scrambler Output

This task, intended for channel set-up, enables the scrambler and transmits its output.

When the modem has started the task the Status 1 Register bits will not change and hence these will not raise an IRQ. The µC may write the next task and its data to the modem at any time and the scrambler output will stop when the new task has produced its first data.

TSD - Transmit Short Data Block

This task takes 4 bytes of data from the Data Buffer, calculates and applies a 16-bit CRC and forms the FEC for the 4 data bytes and the CRC. This data is then interleaved and passed through the scrambler, if enabled, before being transmitted as a Mobitex Data Block.

Once the modem has read the data bytes from the Data Buffer, the BFREE and IRQ bits of the Status 1 Register will be set to '1', indicating to the µC that it may write the next task and its data to the modem.

Note: In transmit mode the CRC checksum circuit is initialised on completion of any task other than NULL.

5.3.4.2.3 RESET - Stop any current action

This task takes effect immediately, and terminates any current task the modem may be performing and sets the BFREE bit of the Status 1 Register to '1', without setting the IRQ bit. It should be used when V_{DD} is applied to set the modem into a known state.

Note that due to delays in the internal circuitry, it will take approximately 3 bit times for any change to become apparent at the transmitter output.

5.3.4.2.4 Task Timings

The device should not write to the Command Register whenever the Enable Baseband bit is changed from '0' to '1' and for at least 2 bit times after the following:

Changing the Tx/Rx bit.

Resetting or after power is applied to the device.

This is to ensure that the internal operation of the device is initialised correctly for the new task. Note that this only applies to the Command Register, the other registers may be accessed as normal.

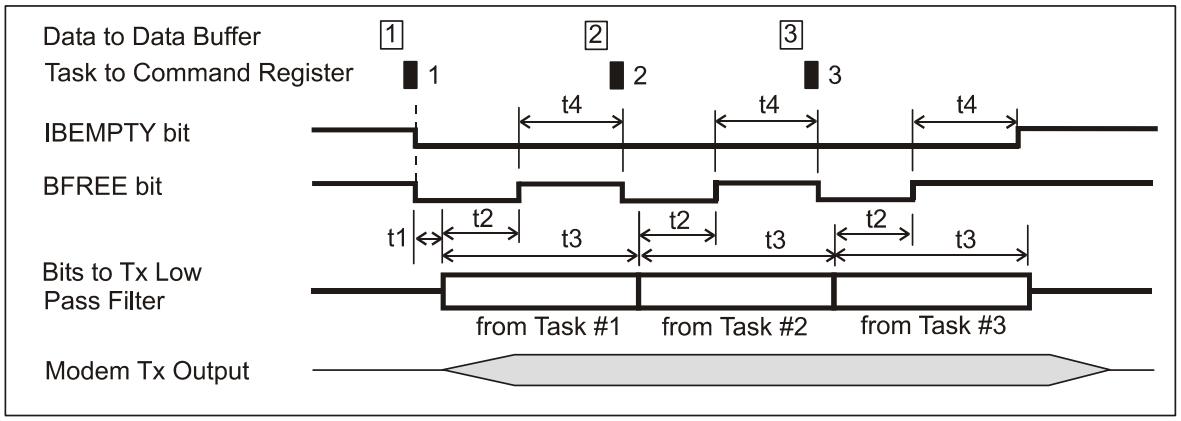

Figure 20 Transmit Mode Timing Diagram

		Task	Typical time (bit-times)
t1	Time from writing first task (modem in 'idle' state) to application of first transmit bit to Tx Low Pass filter	Any	1
t2	Time from application of first bit of task to Tx Low Pass filter until BFREE goes to a logic '1' (high)	T7H	36
		TQB	24
		TDB	20
		TSB	1
		TSD	6
t3	Time to transmit all bits of task	T7H	56
		TQB	32
		TDB	240
		TSB	8
		TSD	72
t4	Max time allowed from BFREE going to a logic '1' (high) for next task (and data) to be written to modem	T7H	18
		TQB	6
		TDB	218
		TSB	6
		TSD	64

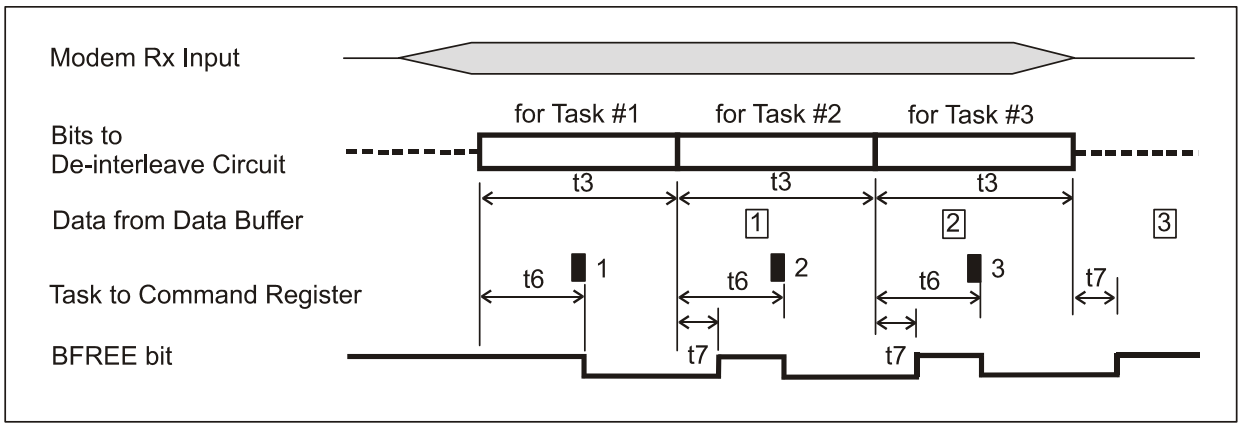

Figure 21 Receive Mode Timing Diagram

		Task	Typical time (bit-times)
t3	Time to receive all bits of task	SFH	56
		R3H	24
		RDB	240
		RSB	8
		RSD	72
t6	Maximum time between first bit of task entering de-interleave circuit and task being written to modem	SFH	14
		R3H	18
		RDB	218
		RSB	6
		RSD	64
t7	Time from last bit of task entering de-interleave circuit to BFREE going to a logic '1' (high)	Any	1

Tx and Rx Low Pass Filter Delay

The previous task timing figures are based on the signal at the input to the RF sections (in transmit mode) or the input to the de-interleave buffer (in receive mode). There is an additional delay of about 2 bit times in both transmit and receive modes due to the Tx/Rx filtering and RF circuitry, as illustrated in the figure below.

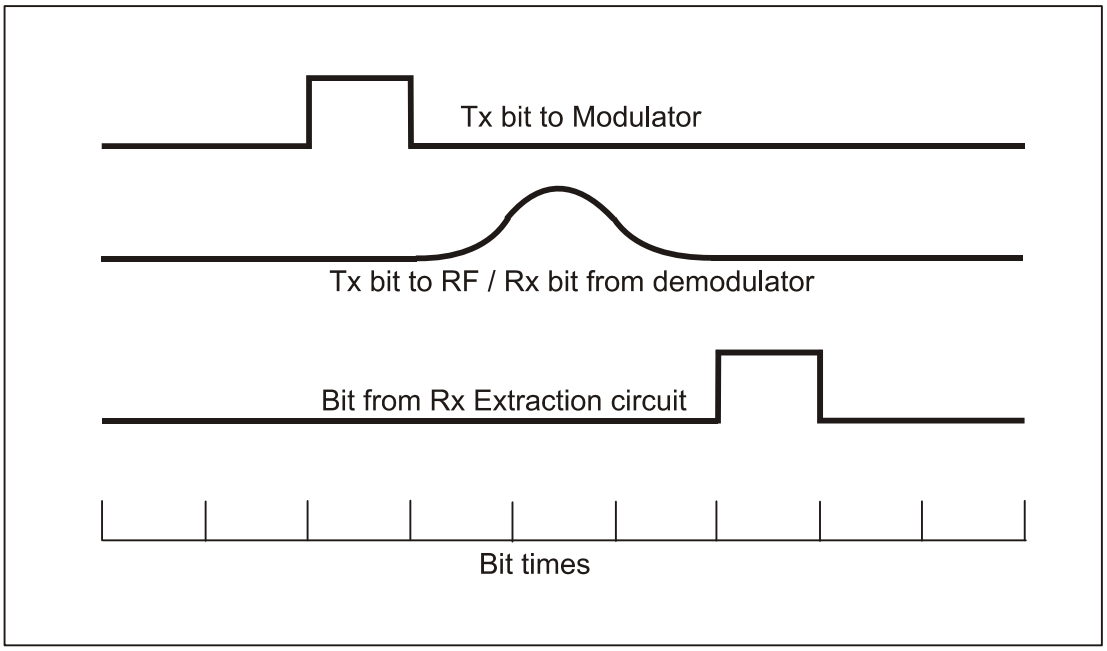

Figure 22 Low Pass Filter Delay

5.3.4.3 Control Register

This 8-bit write only register controls the response times of the receive clock extraction and signal level measurement circuits.

Control Register $02 Write

Bit:	7	6	5	4	3	2	1	0
	AGC Control		IQ Offset Control		Frequency tracking (AFC) Control		PLL Control	

The modem needs to make accurate measurements of the received signal level, dc offset, frequency offset and bit timing to achieve reasonable error rates. Accurate measurements, especially in the presence of noise, are best made by averaging over a relatively long time, however, in most cases the modem will be used to receive isolated messages from a distant transmitter and may be turned on for a very short time before the message starts

To cater for this situation acquire bits 7 to 5 are provided in the Command register ($01) which, when triggered, cause the modem to follow an automatic sequence designed to perform these measurements as quickly as possible. After these acquisition sequences have completed the circuits return to the mode as set in this register.

Control Register B7, B6: AGC Control

These two bits have no effect in transmit mode.

In receive mode these bits set the response of the AGC circuit. The 'Run' and 'Max Gain and Run' settings allow the circuit to acquire and track incoming signals.

B7	B6	Setting	Action
0	0	Max Gain and Hold	AGC set to maximum gain and held
0	1	Hold*	AGC gain not updated by internal circuit
1	0	Run	AGC tracks input signal
1	1	Max Gain and Run	AGC set to maximum gain and tracks input signal

* Host may override AGC setting by writing to $19 only when this setting is selected.

Control Register B5, B4: I/Q Offset Control

These two bits have no effect in transmit mode.

In receive mode, these set the 'normal' response of the I/Q offset measuring circuits. The offset control is in two sections, an analogue 'coarse' setting and a digital 'fine' setting. The host may read and directly overwrite the coarse setting via registers $18 and $19. The coarse and fine settings will be overridden by the Acquire I Q Offset command (bit 6 of Command register) which will go through a sequence of:

Reset (equivalent of RESET Task in command register)
Turn off Receiver 'front end'
Run with Tracking for 25 bits to correct I/Q offset errors
Turn on receiver 'front end' and apply offset
Revert to normal setting (hold / fine / coarse)

Further details can be found in section 6.5.2

B5	B4	Setting	Action
0	0	Reset and Hold	I/Q offset tracking reset and held
0	1	Hold*	I/Q offset tracking held at current setting
1	0	Fine Tracking*	I/Q fine offset tracking
1	1	Coarse Tracking	I/Q coarse offset tracking

* Host may override Coarse I/Q Offset by writing to registers $18 and $19 only when these settings are selected and bit 6 of Command register is = '0'.

Control Register B3, B2: Frequency tracking (AFC) Control

These two bits have no effect in transmit mode.

In receive mode, they set the 'normal' response of the frequency tracking circuits. This setting will be temporarily overridden by the Acquire AFC command (bit 5 of Command register) which will go through a sequence of:

Reset (equivalent of RESET Task in command register)
Run with Fast Tracking for 96 bits to correct frequency offset error
Run with Slow Tracking for 750 bits to follow any further frequency offsets
Revert to normal setting (hold / slow / fast)

B3	B2	Setting	Action
0	0	Reset and Hold	Frequency tracking reset and held
0	1	Hold	Frequency tracking held at current setting
1	0	Slow Tracking	Frequency slow tracking
1	1	Fast Tracking	Frequency fast tracking

For Mobitex systems, and most general purpose applications using the modem, these bits should normally be set to Slow Tracking after the host has activated the automatic sequence.

The Fast setting allows the modem to respond quickly without µC intervention - although at the cost of reduced Bit Error Rate versus Signal to Noise performance.

Note that the AFC measuring system requires '00' and '11' bit pairs to be received at reasonably frequent intervals. The AFC tracking will eventually fail if '1' or '0' is transmitted continuously.

Control Register B1, B0: PLL Control

These two bits have no effect in transmit mode.

In receive mode, they set the 'normal' bandwidth of the Rx clock extraction Phase Locked Loop circuit. This setting will be temporarily overridden by the Acquire Bit Clock command (bit 7 of Command register) which will go through a sequence depending if a frame sync is being searched for (SFH or SFS task is started within 14 bits):

Frame sync search:	*No frame sync search:*
Wide setting until Frame Sync is detected	16 bits of wide setting
30 bits of medium setting	30 bits of medium setting
Revert to normal setting	Revert to normal setting

B1	B0	PLL Bandwidth	Suggested use
0	0	Hold	Signal fades
0	1	Narrow	< ± 20ppm bit rate error systems
1	0	Medium	Wide bit rate error or long preamble acquisition
1	1	Wide	Quick acquisition

The 'hold' setting is intended for use during signal fades, otherwise the minimum bandwidth consistent with the transmit and receive modem bit rate tolerances should be chosen.

The wide and medium bandwidth settings allow the modem to respond rapidly to fresh messages and recover rapidly after a fade without µC intervention - although at the cost of reduced Bit Error Rate versus Signal to Noise performance.

Note that the clock extraction circuits work by detecting the timing of edges, i.e. a change from '0' to '1' or '1' to '0'. The clock extraction will eventually fail if '1' or '0' is transmitted continuously

5.3.4.4 Mode Register

The contents of this 8-bit write only register control the basic operating modes of the modem:

Mode Register $03 Write

Bit:	7	6	5	4	3	2	1	0
	IRQ Enable	INVBit	TxRxN	SCREn	En PLL Lock IRQ	Enable DQ IRQ	Enable Main ADC	Enable Main DAC

Mode Register B7: IRQ Enable - IRQN Output Enable

When this bit is set to '1' the IRQN chip output pin is pulled low (to V_{SS}) whenever the IRQ bit of the Status Register is a '1'.

Mode Register B6: INVBIT - Invert Bits

This bit controls inversion of transmitted and received data. This allows for frequency inversions in the RF chain and has the effect of swapping I and Q paths in both transmitter and receiver.

Mode Register B5: TXRXN - Tx/Rx Mode

Setting this bit to '1' puts the modem into Transmit mode, clearing it to '0' puts the modem into Receive mode. When changing from Rx to Tx there must be a 2-bit pause before setting a new task to allow the filter to stabilise. (See also Baseband Enable bit, section 5.3.5).

Note that changing between receive and transmit modes will cancel any current task. Note also that this bit does not enable Tx or Rx sections of the CMX990 which must be enabled by separate control bits.

Mode Register B4: SCREn - Scramble Enable

The scrambler only takes effect during the transmission or reception of a Mobitex Data Block, Short Data Block and during a TSO task. Setting this bit to '1' enables scrambling, clearing it to '0' disables scrambling.

The scrambler is only operative, if enabled by this control bit, during TSO, RDB, RSD, TSD or TDB, it is held in a reset state at all other times.

This bit should not be changed while the modem is decoding or transmitting a Mobitex Data Block.

Mode Register B3: En PLL Lock IRQ - Enable Phase Lock Loop lost IRQ

Setting this bit to '1' causes the IRQ bit of the Status 1 Register to be set to '1' whenever The PLL Lock lost bit is set to 1. (The Phase Lock lost bit of Status 2 Register will also be set to '1' at the same time.)

Mode Register B2: Enable DQ IRQ - Enable Data Quality IRQ

In receive mode, setting this bit to '1' causes the IRQ bit of the Status 1 Register to be set to '1' whenever a new Data Quality reading is ready. (The DQRDY bit of the Status 1 Register will also be set to '1' at the same time.)

In transmit mode this bit has no effect.

Mode Register B1 - 0: Enable Main ADC / Enable Main DAC

When the respective bit is set to '1' the main ADC and DAC are enabled, power may be saved by setting these bits to '0' when the ADC or DAC are not needed. Bit '0' would normally only be set to '1' when bit 5 is set to '1'. Bit '1' would normally only be set to '1' when bit 5 is set to '0'.

5.3.4.5 Status Registers

Two status registers indicate events that may require action by the host. Those marked as bold in the diagrams below will cause bit 7 of Status1 (IRQ) to go high when they change from a 0 to 1. Interrupts are enabled by setting bit 7 of the Mode register ($03) to '1', the IRQN pin will then be pulled low whenever the IRQ bit goes high. If the IRQN line to the host is pulled low or if the host is polling for interrupts then Status Register 1 should be read first then optionally followed by reading Status Register 2. The IRQ bit will be cleared to a '0' when the status register containing the interrupt(s) is read.

Status1 $01 Read

Bit:	7	6	5	4	3	2	1	0
	IRQ	**BFREE**	**IBEMPTY**	**DIBOVF**	CRCFEC	**DQRDY**	MoBaN	**Packet Detect**

Status2 $03 Read

Bit:	7	6	5	4	3	2	1	0
	PLL Lock lost	Main PLL in lock	Aux PLL in lock	Tx PLL in lock	**SPC command complete**	**Aux ADC conversion complete**	**Freq offset error**	**IQ offset complete**

Status 1 Register, B7: IRQ - Interrupt Request

This bit is set to '1' by:

The Status 1 Register BFREE bit going from '0' to '1', unless this is caused by a RESET task or by a change to the Mode Register Enable Baseband or TXRXN bits.

or The Status 1 Register IBEMPTY bit going from '0' to '1', unless this is caused by a RESET task or by changing the Mode Register Enable Baseband or TXRXN bits.

or The Status 1 Register DQRDY bit going from '0' to '1' (If DQEN = '1').

or The Status 1 Register DIBOVF bit going from '0' to '1'.

or The Status 1 Register Packet Detect bit going from '0' to '1' if the Enable Packet Detect bit is set in the Command Register.

or The Status 2 Register bits 7, 3, 2, 1 or 0 going from '0' to '1'.

The host must read Status 1 Register first after detecting or looking for an interrupt condition. The IRQ bit is cleared to '0' immediately after a read of the Status Register that caused the interrupt. In the case where 1 or more bits in Status 2 Register cause an interrupt the IRQ bit is only cleared after reading Status 2 Register.

If the IRQEN bit of the Mode Register is '1', then the chip IRQN output will be pulled low (to Vss) whenever the IRQ bit is '1'.

Status 1 Register, B6: BFREE - Data Buffer Free

This bit reflects the availability of the Data Buffer and is cleared to '0' whenever a task other than NULL, RESET or TSO is written to the Command Register.

In transmit mode, the BFREE bit will be set to '1' (also setting the Status 1 Register IRQ bit to '1') when the modem is ready for the µC to write new data to the Data Buffer and the next task to the Command Register.

In receive mode, the BFREE bit is set to '1' (also setting the Status 1 Register IRQ bit to '1') by the modem when it has completed a task and any data associated with that task has been placed into the Data Buffer. The µC may then read that data and write the next task to the Command Register.

The BFREE bit is also set to '1', but without setting the IRQ bit, by a RESET task or when the Mode Register Enable Baseband or TXRXN bits are changed.

Status 1 Register, B5: IBEMPTY - Interleave Buffer Empty

In transmit mode, this bit will be set to '1', also setting the IRQ bit, when less than two bits remain in the Interleave Buffer. Any transmit task written to the modem after this bit goes to '1' will be too late to avoid a gap in the transmit output signal.

The bit is also set to '1' by a RESET task or by a change of the Mode Register TXRXN or Enable Baseband bits, but in these cases the IRQ bit will not be set.

The bit is cleared to '0' by writing a task other than NULL, RESET or TSO to the Command Register.

Note: When the modem is in transmit mode and the Interleave Buffer is empty, a mid-level voltage (V_{BIAS}) will be applied to the Tx low pass filter.

In receive mode this bit will be '0'.

Status 1 Register, B4: DIBOVF - De-Interleave Buffer Overflow

In receive mode this bit will be set to ‘1’ (also setting the IRQ bit) when a task is written to the Command Register too late to allow continuous reception.

The bit is cleared to ‘0’ by reading the Status 1 Register or by writing a RESET task to the Command Register or by changing the Enable Baseband or TXRXN bits of the Mode Register.

In transmit mode this bit will be ‘0’.

Status 1 Register, B3: CRCFEC - CRC or FEC Error

In receive mode this bit will be updated at the end of a Mobitex Data Block task, after checking the CRC, and at the end of receiving Frame Head control bytes, after checking the FEC. A ‘0’ indicates that the CRC was received correctly or the FEC did not find uncorrectable errors, a ‘1’ indicates that errors are present.

The bit is only cleared to ‘0’ by a RESET task or by changing the Enable Baseband or TXRXN bits of the Mode Register.

In transmit mode this bit will be ‘0’.

Status 1 Register, B2: DQRDY - Data Quality Reading Ready

In receive mode, this bit is set to ‘1’ whenever a Data Quality reading has been completed.

The bit is cleared to '0' after reading the Data Quality Register.

Immediately after a RESET task, or a change in the Enable Baseband or TXRXN bits to ‘0’, the DQRDY bit may be set and generate an interrupt. The value in the Data Quality Register will not be valid in this case.

Status 1 Register, B1: MOBAN - Mobile or Base Bit Sync Received

In receive mode this bit is updated at the end of the SFS and SFH tasks. This bit is set to ‘1’ whenever the 3 bits immediately preceding a detected Frame sync are ‘011’ (received left to right), with up to any one bit in error. The bit is set to ‘0’ if the bit pattern is ‘100’, again with up to any one bit in error. Thus, if this bit is set to ‘1’ then the received message is likely to have originated from a Mobile and if it is set to ‘0’ from a Base Station.

In transmit mode this bit is a logic ‘0’.

Status Register 1, B0: Packet Detect

This bit indicates the status of the Packet Detect circuit and will be set to '0' when a packet is not present, as described in the description for Command Register bit B4.

In transmit mode this bit will be ‘0’.

Status 2 Register, B7: PLL Lost Lock

'PLL Lock lost' bit will be set to '1' whenever bits 4, 5 or 6 go from '1' to '0' since that bit was read as a '1' from Status Register 2, i.e. PLL Lock lost bit is only set if lock has been gained, the host has read the register to confirm this and that bit subsequently goes from a '1' to a '0'. This will cause bit 7 of Status1 to be set to '1' only if bit 3 of the Mode register ($03) is set to '1'. This bit will be cleared to ‘0’ immediately after reading the Status 2 register.

Status 2 Register, B6-B4 PLL in Lock (Main / Aux / Tx)

Bits 6 to 4 represent the lock status for the corresponding PLL at the time of the read of Status 2 register. A '1' indicates the PLL is in lock, a '0' indicates that the PLL is not in lock. Buffer circuitry will prevent changes in the lock status being lost while this register is being read.

Status 2 Register, B3: Special Command Complete

When operating a special command the 'SPC command complete' bit will be set to '1' when a command has finished and any associated data can then be read out. The correct sequence to initiate a special command is to load any required data into the special data registers $1B to $1E then issue the special command by writing to the special command register $1A. Having issued a special command the host must not read or write to the special command or data registers ($1A to $1E) until it has completed. Reading register Status 2 will clear this bit to '0'.

Status 2 Register, B2: Aux ADC Conversion Complete

'Aux ADC conversion complete' bit will be set to '1' when all enabled ADC channels have been converted. This bit will not be set if continuous conversion is selected, the host may read the latest conversion for each channel as required. Reading register Status 2 will clear this bit to '0'.

Status 2 Register, B1: Frequency Offset Error

During Rx mode the CMX990 continuously compares the local reference clock frequency against the received RF signal frequency. If these two frequencies deviate by more than the limit set by the host (see section 5.3.8.3), the frequency offset error bit will be set to '1'. This bit will be cleared to '0' by reading register Status 2. By default the error limit is set so that this bit never gets set. This default value can be changed by issuing a special command to the CMX990 (see section 5.3.8). For further details on frequency measurements see section 5.3.12.1.

Status 2 Register, B0: IQ Offset Complete

'IQ offset complete' bit will be set to '1' when the sequence to estimate the IQ offsets of the receive channel has completed. During the offset acquisition sequence the received signal will be unreliable.

5.3.4.6 Data Quality Register

Data Quality Register $02 Read

Bit:	7	6	5	4	3	2	1	0
	Data Quality Reading (0-255)							

This is intended to indicate the quality of the receive signal during a Mobitex Data Block or 30 single bytes. In receive mode, the modem measures the 'quality' of the received signal by comparing the actual received zero crossing time against an internally generated time. This value is averaged over 240 bits and at the end of the measurement the Data Quality Register and the DQRDY bit in the Status 1 Register is updated. Note: An interrupt will only occur at this time if the Enable DQ IRQ bit = '1'.

To provide synchronisation with Data Blocks, and hence ensure the Data Quality Register is updated in preparation to be read when the RDB task finishes, the measurement process is reset at the end of tasks SFH, SFS, RDB and R3H.

In transmit mode all bits of the Data Quality Register will be '0'.

Figure 23 shows how the value (0-240) read from the Data Quality Register varies with received signal to noise ratio. Note that the Signal-to-Noise ratio show is the post detection signal to noise and that this is different from the S/N measured in the RF section.

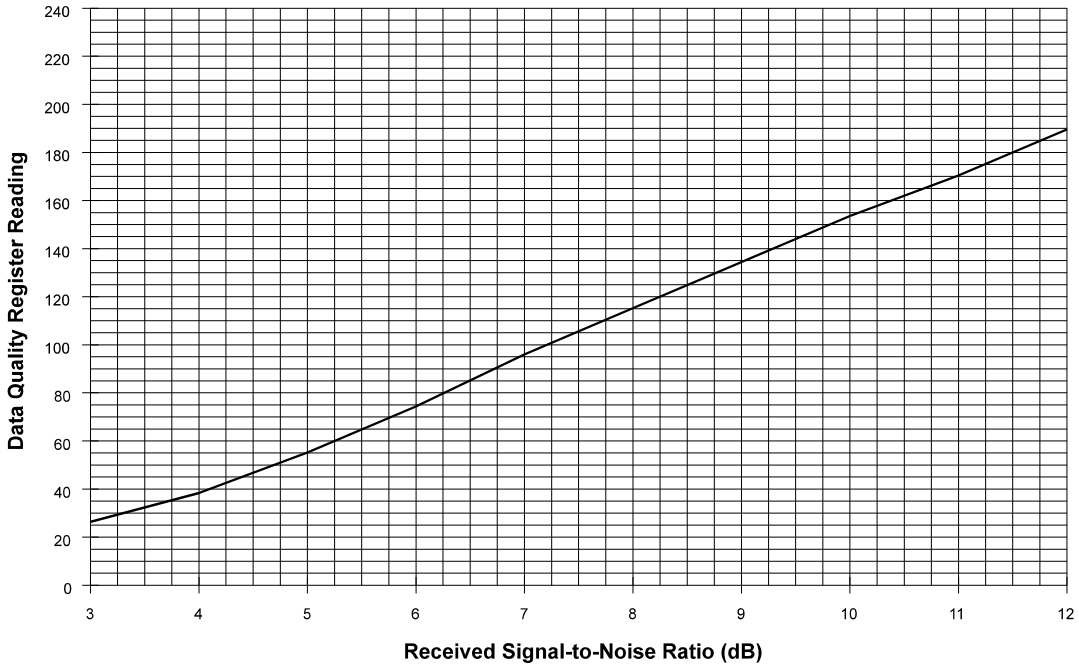

Figure 23 Typical Data Quality Reading (after 240 bits) vs baseband S/N (noise in bit rate bandwidth)

5.3.5 Power control

The following registers control individual power-up state of the indicated blocks. Note: Other sections of the device have the power control bits included in the control registers for those blocks. Blocks are disabled and in the zero power state when the associated control bit is '0'.

Power Up 1 $04 Write

Bit:	7	6	5	4	3	2	1	0
	Enable Clock	Enable Baseband	**V Reg**	Enable OP1 OP2	Rx IF	Rx RF1	Rx RF2	Tx RFIF

If the Enable Clock is set to '0' the on chip clock buffer will be disabled, the clock buffer must be enabled if setting RESET (bit 3 of $05) or if any of the internal circuits are powered up apart from those controlled by the 'V Reg', 'Vbias' and 'OP1 OP2' bits.

When the clock enable bit is changed from 0 to 1, the clock is enabled directly, which may cause erroneous operation if REFCLK (pin 53) is changing at the same time. This problem will not happen if the clock PLL is being used (i.e. the 'Clock Control Register' has a value other than $18). If not using the default value it is recommended that the required value is written to the 'Clock Control Register' before the 'Enable Clock Bit' is set. Alternativly if $18 is to be used a RESET command should be written ($05, bit 3) following the 'Enable Clock Bit'. It will be noted that the RESET does not effect the 'Enable Clock' bit or the 'Clock Control Register' (see section 5.3.3).

The Enable Baseband bit controls the data packeting and clock extraction circuits, this must be set to '1' before writing to any other register.

If V Reg bit is set to '0' an internal circuit will hold the nominal 2.5V supply pins at approximately 2V for data retention only. For normal operation the host must set this bit to '1' before enabling any other circuitry. If an external supply provides the nominal 2.5V then the V Reg bit should be set to '0'. See section 4.5 for more details.

When the OP1 OP2 bit is low both OP 1 and OP 2 amplifiers are disabled the OP1T and OP2T pins will become high impedance inputs to ADC2 and ADC3 respectively. When set to '1' both op-amps are enabled.

Rx IF bit enables the circuitry from the IF IN pin to the differential I and Q outputs to the baseband.

Rx RF1 bit enables the circuitry from the RF IN A and RF IN B pins to the output of the 1st mixers.

Rx RF2 bit enables the circuitry from the output of the 1st mixers to the IF OUT pin.

Tx RFIF bit enables all the transmit RF and IF circuits from the differential I and Q inputs to the Tx RF interface pins.

Power Up 2 $05 Write

Bit:	7	6	5	4	3	2	1	0
	AUX DAC3	AUX DAC2	AUX DAC1	AUX DAC0	RESET	LNA ON (External)	**Preserve Registers**	**Vbias**

The Vbias control bit must be enabled early enough so that the output is stable before any of the other circuit blocks are enabled as this circuit takes some time to stabilise after being enabled. Setting the RESET bit to '1' will not change the Vbias bit.

If set to '1' the Preserve Registers bit will preserve most user settings programmed via the Special Command register, e.g. Rx channel filter coefficients and non assigned memory. In Rx mode the AGC, offsets and timing estimates of the received signal will be lost after a RESET event.

LNA ON bit directly controls the LNA ON pin and does not control any internal analogue circuitry. Any time delay for the external circuitry to stabilise must be taken into account when controlling this bit. This control bit will be cleared to '0' after a power on reset or if the RESET bit is set to '1'.

Whenever a '1' is written to the RESET bit all registers will be cleared to '0' apart from the Clock Control register, bit 7 of the Power up register will be set to 1. Bit 5 of the Power Up 1 register and bits 1 and 0 of the Power Up 2 register will remain in their previous state. This will put all internal circuits in an inactive and power saved state except for the 'clock enable' buffer which remains at '1' so that the device may respond to the TCXO clock. The 'V Reg', 'Preserve registers' and 'Vbias' bits will be unchanged. To ensure a clean exit from the RESET condition the RESET bit should be set to '0' before any other circuitry is enabled. i.e. To enter RESET write '000010xx' to $05. To exit RESET write '000000xx' then 'xxxx0xxx', where 'x' is the desired condition for the Aux DACs, LNA ON, 'Preserve registers' and 'Vbias' bits. The host may then program the rest of the device to the desired configuration.

The AUX DAC0-3 bits control the relevant auxiliary DAC.

5.3.6 Auxiliary DAC and ADC

5.3.6.1 Aux DAC 0-3 $08-0F Auxiliary DAC Data Registers (Write only)

$08-09	Aux DAC 0	Auxiliary DAC 0 Data Register	LSB - MSB
$0A-0B	Aux DAC 1	Auxiliary DAC 1 Data Register	LSB - MSB
$0C-0D	Aux DAC 2	Auxiliary DAC 2 Data Register	LSB - MSB
$0E-0F	Aux DAC 3	Auxiliary DAC 3 Data Register	LSB - MSB

$08, $0A, $0C, $0E

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	DAC Data [1:0]	

$09, $0B, $0D, $0F

Bit	7	6	5	4	3	2	1	0
	DAC Data [9:2]							

There are two input registers for each of the four auxiliary DACs. Writing to the LSB register writes the two least significant bits of DAC data. Writing to the MSB register writes the eight most significant bits of DAC data and then passes all ten bits to the appropriate DAC input. If the MSB register is written while the LSB register is left constant, the converter may be treated as an 8-bit DAC.

5.3.6.2 RamDac Control $10 Auxiliary RAM DAC Control Register

Bit:	7	6	5	4	3	2	1	0
	Inc Aux RAM address	En Aux RAM access	RAM DAC scan rate [0-7 = /1024 to /8]			Scan direction	En auto cycle	En RAM DAC

Setting bit 7 high will cause read operations to the auxiliary DAC RAM to increment the address pointer. Setting this bit low causes write operations to increment the address pointer.

Bit 6 enables access to the auxiliary DAC RAM. Setting bit 6 low resets the RamDac address pointer.

Bits 5 to 3 control the rate at which the RAM DAC address pointer changes:

Bit 5	Bit 4	Bit 3	Rate of change
0	0	0	BCLK/1024
0	0	1	BCLK/512
0	1	0	BCLK/256
0	1	1	BCLK/128
1	0	0	BCLK/64
1	0	1	BCLK/32
1	1	0	BCLK/16
1	1	1	BCLK/8

Note: BCLK = Base-band clock, see section 5.3.10.

Bit 2 controls the direction of the memory scan operation. Setting this bit high will cause the memory address pointer to increment to the top location, setting this bit low will cause the memory address pointer to decrement to the bottom location. If this bit is changed while the memory is being scanned, the current scan will complete before the new state of this bit takes effect.

When bit 1 is set high, the memory address pointer continuously increments to the top location and then decrements to the bottom location.

Bit 0 controls whether DAC0 is driven by the RAM (when set high) or the Aux DAC 0 register (when set low).

5.3.6.3 AuxRamData1/2 $14-17 Auxiliary DAC Memory I/O Access Addresses

$14

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	RAM data [1:0]	

$15

Bit	7	6	5	4	3	2	1	0
	RAM data [9:2]							

$16

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	RAM data [1:0]	

$17

Bit	7	6	5	4	3	2	1	0
	RAM data [9:2]							

These four address locations allow access to the 64 x 10-bit RAM. The contents of this RAM can be pre-loaded with a table of values that can be automatically sent to the auxiliary DAC0 in either a single cycle or continuous mode. Therefore the RAM can be used in conjunction with DAC0 to enable user defined profile power ramping of an external RF power transmitter stage.

The RAM contents are addressed incrementally by first setting bit 6 of RamDac Control register. While this bit is low, the RAM address pointer is held reset. The first two data words are written by writing to addresses $14 to $17 in order. Accessing location $17 post-increments the address pointer. Bit 7 of the RamDac Control register determines whether a read or write operation will increment the RAM address pointer. Further write operations to addresses $14 to $17, will load the next two locations.

All locations are accessed incrementally; further accesses to this port while bit 7 of the RamDac Control register is active are not valid and may cause data loss.

5.3.6.4 Aux ADC 0-5 Data Registers $08-13 Read

$08-09	Aux ADC 0	Auxiliary ADC 0 Data Register	LSB - MSB
$0A-0B	Aux ADC 1	Auxiliary ADC 1 Data Register	LSB - MSB
$0C-0D	Aux ADC 2	Auxiliary ADC 2 Data Register	LSB - MSB
$0E-0F	Aux ADC 3	Auxiliary ADC 3 Data Register	LSB - MSB
$10-11	Aux ADC 4	Auxiliary ADC 4 Data Register	LSB - MSB
$12-13	Aux ADC 5	Auxiliary ADC 5 Data Register	LSB - MSB

$08, $0A, $0C, $0E, $10, $12

Bit	7	6	5	4	3	2	1	0
	X	X	X	X	X	X	ADC Data [1:0]	

$09, $0B, $0D, $0F, $11, $13

Bit	7	6	5	4	3	2	1	0
	ADC Data [9:2]							

These registers enable the user to inspect the conversion value for each of the six auxiliary ADCs. There are two read registers per ADC, one to obtain the two least significant bits of the data, the other for the eight most significant bits. Reading these registers does not affect the ADC conversion cycle. Reading the MSB register directly reads the ADC output and simultaneously causes the two bits in the LSB register to be written to a holding register. This holding register is read when the LSB register is read. This mechanism is necessary to allow the user to read MSB and LSB data from the same ADC conversion cycle. If only the MSB register is read, the converter can be considered as an 8-bit ADC. If a 10-bit conversion is required, the MSB register must be read first.

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5.3.6.5 Aux Control1 $11 Write

Bit:	7	6	5	4	3	2	1	0
	0	0	Enable ADC 5	Enable ADC 4	Enable ADC 3	Enable ADC 2	Enable ADC 1	Enable ADC 0

This register controls which ADC channels are converted. These bits may be changed at any time, but will only update the active state of the ADC channel for the next time it is converted.

5.3.6.6 Aux Control2 $12 Write

Bit:	7	6	5	4	3	2	1	0
	DAC RAM Polarity	Reset DAC RAMs	0	0	0	Conversion rate	Enable cont conversion	Start conversion

If bit 6 is set to '1' the RAM associated with DAC 0 is reset, if bit 7 is high the RAM is reset to all 1's, if bit 7 is low the RAM is reset to all 0's. This feature can be used to avoid programming every RAM location when short ramp profiles are required.

Bit 2 selects the conversion rate of the auxiliary ADC. If set low, the ADC will be clocked at (Base-band clock/16), giving a conversion time of 176 Base-band clock periods per enabled channel. Setting this bit high halves the ADC clock rate and doubles the conversion time. The first sample after enabling an auxiliary A/D sequence will take 3 conversion times to complete, each subsequent conversion will take 1 conversion period. For Base-band clock control - see section 5.3.10.

Setting bit 1 high will cause each enabled ADC channel to be converted continuously. Setting bit 0 high will cause a single conversion of all enabled ADC channels. This bit is automatically set low when the ADC conversion has been completed. Note that bit 0 only has an effect when bit 1 is set low.

5.3.7 Analogue Setup

Analogue Setup 1 $18 Write

Bit:	7	6	5	4	3	2	1	0
	Set Tx attenuation: '11' = 0dB, '10' = 10dB '01'= 20dB, '00'= 20dB		Coarse Rx I offset, '10000' = Mid value '00000' = Max -ve offset, '11111' = Max +ve offset					

Analogue Setup 2 $19 Write

Bit:	7	6	5	4	3	2	1	0
	Set Rx AGC: '11'= 40dB, '10'= 25dB '01 =10dB, '00' = -5dB		Coarse Rx Q offset, '10000' = Mid value '00000' = Max -ve offset, '11111' = Max +ve offset					

See section 5.3.11 for description of Tx attenuation.

The Rx AGC may be controlled by the host if the AGC Control ($02, B7-B6) is set to 'Hold' mode. In this mode the RSSI value calculated by the CMX990 will assume the last value of AGC calculated by the CMX990. If the host writes a new value the CMX990 RSSI circuits are not aware of this value and the host must apply an appropriate correction to the RSSI reported by the CMX990. Note that the state of the AGC can be read from $19, B7-B6 (see below). A possible sequence for manual updating the AGC could be:

i. Set AGC 'Hold' mode ($02 B7-B6 = '01')
ii. Read Analogue Setup 2 and store AGC value
iii. Write new AGC value to Analogue Setup 2
iv. Read RSSI.
v. If new value of AGC is different from the stored value apply appropriate correction to RSSI value
vi. Repeat steps iii to v as required.

The Rx I and Q offsets are the values applied to the hardware to correct for DC offsets. The offset can be measured automatically by the CMX990 (see sections 5.3.4.2 and 5.3.4.3). Analogue setup registers allow the offset values to be read or written by the host. Note that writing to these registers is only possible in certain conditions. An overview of DC calibration is given in section 6.5.2

Analogue Setup 1 $18 Read

Bit:	7	6	5	4	3	2	1	0
	X	Channel filter overflow	Coarse Rx I offset, '10000' = Mid value '00000' = Max -ve offset, '11111' = Max +ve offset					

Bit 6 is set to '1' when the receive channel filters have a numerical overflow. This bit is reset to '0' after this register is read. This bit does not generate an interrupt and is intended for test purposes only for evaluating custom receive filter coefficients (see section 5.3.8.1). Bits 5 to 0 indicate the current coarse offset correction in the receive I path.

Analogue Setup 2 $19 Read

Bit:	7	6	5	4	3	2	1	0
	AGC setting 0-3		Coarse Rx Q offset, '10000' = Mid value '00000' = Max -ve offset, '11111' = Max +ve offset					

Bits 7 to 6 indicate the current gain setting of the AGC circuit. Bits 5 to 0 indicate the current coarse offset correction in the receive Q path.

5.3.8 Special Command Functions

Special Command (SPC) $1A Write

Bit:	7	6	5	4	3	2	1	0
	Special Command							

Special Data0 $1C-1B Read and Write

Bit:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	MSB Data								LSB Data							

Special Data1 $1E-1D Read and Write

Bit:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	MSB Data								LSB Data							

The 8-bit value written to the Special Command (SPC) register instructs the modem to perform special tasks such as loading coefficients or reading receive values. When executing a special task that requires input data, the data should be loaded into the Special Data 0/1 registers before writing the Special Command. When the Special Command has completed, the 'SPC command complete' bit will be set to '1' and the host can read out any reply data from the Special Data 0/1 registers. If the internal circuits

read the SPC register as a non-zero value, they will try to complete the task when there is a gap in processing.

Function	Cmd No. (Hex)	Input Data		Returned Data		Notes
		Data 0 $1C $1B MSB LSB	Data 1 $1E $1D MSB LSB	Data 0 $1C $1B MSB LSB	Data 1 $1E $1D	
Null	00	-	-	-	-	No command - do nothing
Set address	01	address	-	-	-	address1 = address
Set tx filter	09	-	-	-	-	address1 = tx filter address
Set rx channel filter	0A	-	-	-	-	address1 = rx channel filter address
Set rx gauss	0B	-	-	-	-	address1 = rx gauss filter address
Poke(addr)	0C	address	data	-	-	*address=data
User channel filter	15	-	-	-	-	Loads rx channel filter from data at address1
Set BT	1A	data	-	-	-	Set BT BT = 0.3 is default setting
Set BT = 0.5	1B	-	-	-	-	Tx and Rx with BT = 0.5
Set AFC limit	1C	Limit	-	-	-	
View Rx Eye	1D	-	-	-	-	For RF test set up
Set Decode Threshold	18	Offset	-	-	-	Set data decode threshold level. Default = 2400
Set RSSI averaging	1F	data	-	-	-	Set N and f values see sections 5.3.8.6 and 5.3.12.2

Notes: *address = data in memory pointed to by 'address'.

5.3.8.1 Alternative Channel Filters

It is possible to load alternative filters in the CMX990. The Transmit data filter, the receiver channel filter and receiver data filter are all programmable. For further details contact techsupport@cmlmicro.com.

5.3.8.2 Transmitter BT Options (Special Command $1A, $1B)

In addition to the ability to completely re-program the filters three pre-programmed filters are available in the CMX990 offering BT = 0.27, BT = 0.3 or BT = 0.5.

The default operation of the CMX990 is BT=0.3. This can be changed using special command $1A which should have data in Data 0 ($1C, $1B). The following setting are allowed:

Data 0 Value	Result
0	BT = 0.3
1	BT = 0.5
2	BT = 0.27

A simplified command to select BT = 0.5 is special command $1B which does not require a data value.

5.3.8.3 AFC Limit (Special Command $1C)

This special command allows the limit at which a frequency error measurement will trigger an interrupt. For more details see section 5.3.12.

5.3.8.4 View Rx Eye (Special Command $1D) - Receiver set-up

To assist in evaluating the performance of the RF and IF circuits the user can enable a special test mode to observe the base-band eye from the receiver. This gives a good measure of the overall receiver performance and can be useful to give a rapid visual indication of the effects of disturbing factors such as frequency offset, IF filter changes, RF levels etc. The ideal Rx eye patterns are shown in Figure 14.

During 'view Rx eye' mode pins 45 and 46 temporarily become outputs and are driven by the receive eye signal differentially. These 2 pins should have an external RC filter of 100kOhm and 33pF on each line to analogue ground for operation at 8kb/s (scale the capacitor values inversely with bit rate).

To enter the 'view Rx eye' mode, first set up the transmit and receive paths as required, ensure that auxiliary ADC4 and ADC5 are powered down (these functions normally use pins 45 and 46), then write the following to the CMX990 receiving the signal:

Address	Data	
$03	xx0xxx11	Enable main ADC and main DAC
$3F	11101010	Enable routing to pins 45 and 46
$1A	00011101	Start special command $1D

Where 'x' represents the user's preferred settings.

The oscilloscope or other instrument displaying the received eye may need a trigger signal synchronised to the data, especially in degraded signal conditions. Ideally this should be taken from the device generating the transmitted signal, however this is sometimes not available (e.g. when receiving a signal remote from the transmitting system). In this case the IRQ from the CMX990 can be used while it carries out successive RSB tasks on the received data.

To exit the 'view Rx eye' mode the CMX990 should be reset.

5.3.8.5 Set Decode Threshold (Special Command $18)

This a threshold within the decoder which optimises performance of the receiver for a particular BT. The required threshold is set for a particular level of data filtering. As can be seen in Figure 14 with a BT=0.3 significant Inter-Symbol-Interferene (ISI) is introduced causing a closing of the data ‘eye’. The amount of this ‘eye’ closing is compensated with this threshold. The default threshold (2400-decimal) is optimal for BT=0.3. Increasing BT will require a lower threshold, e.g. with BT=0.5 a threshold of 1500 (decimal) is recommended.

5.3.8.6 RSSI Averaging

This command sets the amount of averaging used in calculating the RSSI measurement (see section 5.3.12.2). The $1F command offers the following averaging options:

Data 0 Value	N and f values	Averaging Time
0	N=2048,f=16	64ms
1	N=1024,f=32	32ms
2	N=512,f=64	16ms
3	N=256,f=128	8ms
4	N=128,f=256	4ms
5	N=64,f=512	2ms
6	N=32,f=1024	1ms
7	N=16,f=2048	0.5ms

5.3.9 Local Oscillator Synthesisers

Two integer-N synthesisers are provided, one as the main RF synthesiser (Main PLL), which provides the tuneable frequency to enable channel selection, and the other (Aux PLL) for the generation of lower

frequency for mixing to / from IF and baseband. These two synthesisers are fully programmable, via the processor interface, to any frequency in the range 600 MHz to 2 GHz and 150 MHz to 250 MHz respectively. Both the synthesised frequencies are internally divided down. The main RF frequency is divided by two for use in the offset loop in the transmitter and also for the image reject mixer in the receiver. Note that, in order to obtain quadrature signals for the image reject mixer, both the rising and falling edges of the VCO generated signal are used; it is important, therefore, that the VCO produce a waveform that is as close as possible to a mark to space ratio of one. The second synthesiser is optionally divided by 2 or 4 for the transmitter and divided by 4 for the receiver.

Both synthesisers are phase locked loops (PLLs) and utilise external VCOs and loop filters. The phase noise of the VCOs should be adequate for the application with particular attention paid to the performance of the main VCO. It will be noted that as the CMX990 includes an internal divide-by-two in the LO path the PLL phase noise will be improved by approximately 6dB. The loop filters will need to be designed as required based on switching bandwidths, VCO gain etc. The CMX990 phase detectors are of the phase-frequency type with a high impedance charge pump output requiring just passive components in the loop filter. As a result standard design equations for a type II PLL can be used to select loop filter components. Lock detect functions are built in to each synthesiser and the status reported to the host processor. In particular, a transition to out-of-lock can be detected and communicated via an interrupt to the processor if required; this can be important to ensure that the transmitter cannot falsely transmit into other bands in the event of a fault condition arising.

The minimum step size is programmable by setting the reference division ratio; to minimise the effects of phase noise this should be kept as high as possible, particularly on the main RF synthesiser. For Mobitex, the maximum this can be set to is 25 kHz as this is governed by the 12.5 kHz channel spacing and the subsequent divide-by-2 of the generated frequency. Note that if it is required to select a frequency that is 6.25 kHz offset from a convenient division of the main frequency (although still with 12.5 kHz channel spacings), it is better to keep the step size at 25 kHz but slightly offset the reference oscillator. In this way the phase noise and lock time performance will not be compromised.

Each synthesiser is set up using two registers, an ‘M’ register that sets the division value of the input reference frequency to the comparison frequency (step size), and an ‘N’ register that sets the division of the required synthesised frequency from the external VCO to the comparison frequency.

In the main PLL the VCO frequency is pre-scaled by 2 prior to being divided by N, therefore there is a factor of 2 in the formula that yields a required synthesised frequency. The equations for the main and auxiliary synthesisers are:

$F_{MAIN} = (2 \times N_{MAIN} / M_{MAIN}) \times F_{REF}$ $N_{MAIN} > 1023$ $M_{MAIN} > 1$

$F_{AUX} = (N_{AUX} / M_{AUX}) \times F_{REF}$ $N_{AUX} > 7$ $M_{AUX} > 1$

Where F_{REF} is the reference oscillator frequency REF CLK.

Main and Aux PLL and RF set up

Input

The main and aux PLL circuits have control registers as listed below. Writing to the least significant 8 bits will trigger the circuit to update the dividers with the new multi byte value. Whenever the enable bit is low the divider circuit will be in the inactive 'zero power' (ZP) mode. To enter normal operation from ZP mode the MSB (including the enable bit) is written, the LSB would be written last, this would simultaneously enable the PLL and load the divider ratio - lock may take longer when exiting ZP mode. To enter ZP mode only the MSB need be written, double buffering will not be used for this control line - a simple SET / RESET latch will store the 'Enable' value, SET from the output of the 2nd buffer, RESET from the inverted output of the 1st buffer. The main and aux PLL will control their outputs to the required quiescent value when shutting down.

Output

One buffered digital output line from each PLL will indicate when the relevant PLL is in lock, this output is not synchronised. '1' = PLL enabled and in lock, '0' = all other conditions (including disabled ZP state).

These lock outputs are available in the status register in the host interface block and can optionally cause an external interrupt to occur. See section 5.3.4.5 for a description of interrupt operation.

Main PLL M divider $21-20 Write

Bit:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	Main PLL Enable	Tx LO DIV	Tx Mix Filter	MSB					LSB							

Tx LO DIV controls a divide by 2 stage in the Tx LO clock path, '1' = div by 1, '0' = div by 2.
Tx Mix Filter controls the post Tx mixer filter response, '1' = Hi (118MHz), '0' = Low (83MHz).
See also section 5.3.11.

NOTE: When writing synthesiser divider values the LSB must be written last to trigger the update.

Main PLL N divider $24-23-22 Write

Bit:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	Sign	0	0	Tx VCO charge	MSB				NSB								LSB							

In Rx 'Sign' controls the polarity of the Rx IF summer which is part of the image reject mixer in the receiver, a '0' = summation, '1' = subtraction. This allows the image reject mixer to be used for high-side or low-side injection.
In Tx 'Sign' controls the slope of the Tx PLL, '0' for a positive slope, '1' for negative slope.
Tx VCO charge controls the Tx VCO charge circuit, '1' = charge to 1/2 Vdd, '0' = no charge.
See also section 5.3.11.

NOTE: When writing synthesiser divider values the LSB must be written last to trigger the update.

Aux PLL M divider $26-25 Write

Bit:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	Aux PLL Enable	Tx IF Filter		MSB					LSB							

NOTE: When writing synthesiser divider values the LSB must be written last to trigger the update.

The 'Tx IF Filter' bits control the Tx IF filter frequency:
(See also section 5.3.11.)

Bit 6	Bit 5	Tx IF filter setting
0	0	90 MHz
0	1	80 MHz
1	0	45 MHz
1	1	40 MHz

Aux PLL N divider $28-27 Write

Bit:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	Tx IF DIV	0	MSB						LSB							

The 'Tx IF DIV' bit controls a divide by 2 stage in the Tx IF clock path, '0' = divide by 1, '1' = divide by 2.

NOTE: When writing synthesiser divider values the LSB must be written last to trigger the update.

5.3.10 Clock Control

This register controls the Reference Dividers block. The clock input to the REF CLK pin can be used to give a variety of bit rates from common clock rates, see examples given in the tables below. The clock control architecture is shown in Figure 24.

REF CLK (MHz)	**A**, Ref clock divider	Base freq (MHz)
4.8	2	2.4
12	5	2.4
16.8	7	2.4
19.2	8	2.4
21.6	9	2.4
14.4	5	2.88

Base freq (MHz)	VCO freq (MHz)	**B**, Base-band divider	Base-band clock	Bit rate
2.4	76.8	8	9.6	4000
2.4	76.8	4	19.2	8000
2.4	76.8	2	38.4	16000
2.88	92.16	8	11.52	4800
2.88	92.16	4	23.04	9600

Notes:
1. Bit rate = (REF CLK) / (75 x A x B). Bit rate should only be set from 4kb/s to 16kb/s.
2. The frequency of the signal at the REF CLK pin must be in the range 3.8MHz to 24MHz.
3. The Base frequency resulting from the division of the REF CLK signal must be in the range 1.9MHz to 3.0MHz.
4. The clock rate to the synthesizers is always the frequency of the signal at the REF CLK pin.

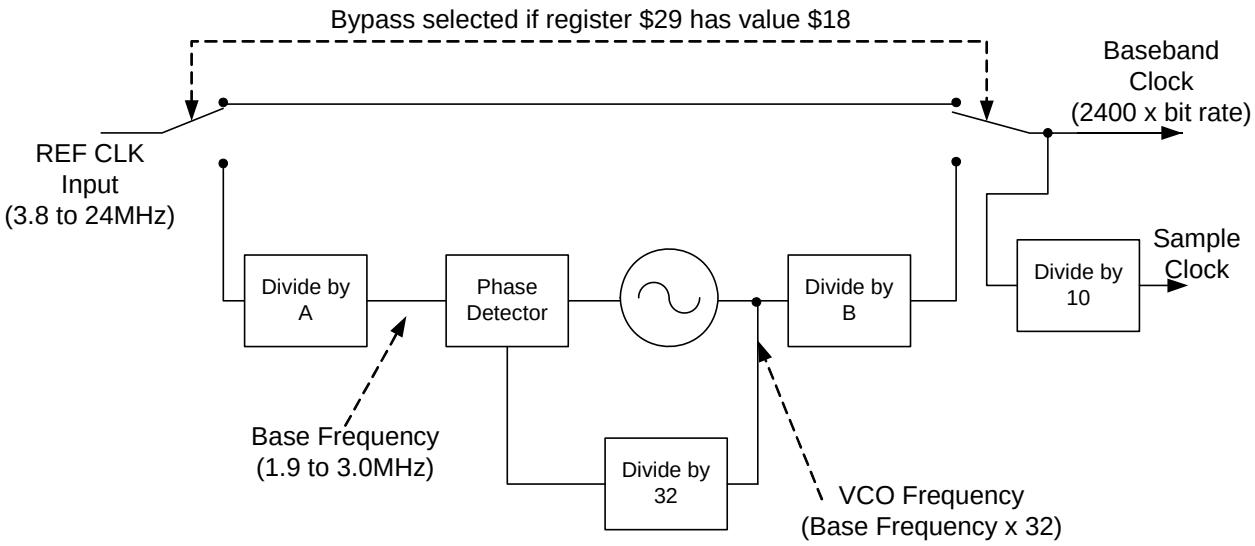

Figure 24 Programmability of Clock Circuits

Clock Control $29 Write

Bit:	7	6	5	4	3	2	1	0
	B, Base-band divider, 2 - 15 (0000 = illegal state, 0001 = See note 3)				**A**, Ref Clock divider, 1 - 15 (0000 = illegal state, 1000 = See note 3)			

Notes:
1. The value '0000' should not be programmed for 'A' or 'B'.
2. After power-up this register will be reset to $18.
3. If the REF CLK is 19.2MHz and the required bit rate is 8000b/s then the clock control register can be programmed with $18. 'B' should only be set to '0001' for this condition. This is the default state of this register and is also the minimum power condition.

5.3.11 Transmitter Control Bits

Various control bits for the O-PLL transmitter are included in several diverse registers. Details of their operation is included in this section so all related function can be seen together.

The input to the O-PLL mixer contains a variable attenuator. B7 and B6 in Analogue Setup 1 ($18, section 5.3.7) control the setting of the attenuator. Steps available are 0dB, -10dB and –20dB. The attenuator is designed to allow the mixer to be operated in it's linear range (therefore minimising spurious output) during normal operation. To allow locking of the loop at minimum output power the attenuator can be switched to the 0dB setting thereby providing maximum sensitivity.

The 'Tx IF DIV' bit (B7, $28, Section 5.3.9) controls the divider providing the local oscillator to the I/Q modulator section. Typical operation of the CMX990 uses a 180MHz Aux local oscillator. This will be divided by two to give a 90MHz TXIF if 'Tx IF DIV'=0. If 'Tx IF DIV'=1 a further division is applied to achieve a TXIF of 45MHz. This 'Tx IF DIV' therefore effectively selects the Tx mode (45MHz or 90MHz) for the Tx operation of the CMX990. Note that this bit does not effect the receiver I/Q demodulator which has a fixed divide by 4 between the Aux LO and the I/Q demodulator.

The 'Tx VCO Charge' bit (B4, $24, section 5.3.9) allows the loop filter of the O-PLL to be pre-charged to Vdd/2 through a resistive divider network of 10kΩ. This overcomes potential problem of the O-PLL locking to an image of the TXIF if the VCO used in the O-PLL has a wide tuning range. Further details can be found in section 6.4.1.

The TX Mix Filter (B5, $21, section 5.3.9) controls the filter following the O-PLL mixer. This filter can be set for cut-off frequencies of 83MHz for TXIF around 45MHz or 118MHz for TXIF around 90MHz. In practice the roll-off of this filter is quite slow and the loop will lock successfully with either filter selected for either 45MHz or 90MHz TXIF operation (note this very different from the case with the 'Tx IF Filter' discussed below) .

The 'Tx IF Filter' bits (B6 B5, $26, section 5.3.9) allow the selection of a filter between the output of the I/Q modulator and the O-PLL phase detector. Selecting the correct bandwidth is very important for correct operation of the loop. For TXIF around 90MHz the '90MHz' filter should be used, for TXIF around 45MHz the '45MHz' filter should be used. The '40MHz' and '80MHz' settings are provided if a little bit more rejection is required or a slightly different IF is used (i.e. just below 45MHz or 90MHz). If the 90MHz filter is selected when using the IC in 45MHz mode the modulation spectrum will be severely degraded. This is due to harmonics of the TXIF signal getting into the phase detector. If the 45MHz filter is used with the IC in 90MHz mode then it is likely that the O-PLL will not lock to the desired output frequency. This is because the loop reference frequency (in this case 90MHz) is not present as it has been filtered out prior to the phase detector input.

The 'Sign' bit (B7, $24, section 5.3.9) controls the slope of the TxPLL charge pump output. With 'Sign' = '0' the VCO should have a positive slope (i.e. a increase in charge pump voltage results in an increase in frequency). With the 'Sign' bit set to '1' the VCO slope should be negative. Note that this bit also controls the polarity of the image reject mixer in the receiver so in some circumstance might need to be changed between Tx and Rx operation. Also it should be noted that the operation is dependant on the frequency change present to the phase detector input and this might be inverted by the offset mixing operation. This happens in the case of high-side frequency conversion in the O-PLL. Consider the case of Figure 17, specifically a transmission of 819MHz with a 90MHz TXIF. In this case the LO is 1818MHz, which after the divide by 2 is 909MHz applied to the O-PLL mixer. So the offset mixer performs 909-819=90MHz. Now consider the case that VCO frequency changes due to an increase in the VCO tuning voltage, just for explanation of the effect, to 820MHz. It this case the VCO follows the normal characteristic of an increase in tuning voltage resulting in an increase in the frequency (i.e. positive slope). Now the O-PLL mixer performs subtraction of 909-820=89MHz. So 89MHz appears at the phase detector not the expected 91MHz. In this case the effective slope of the VCO is changed by the action of the mixer and negative polarity must be selected – even though the VCO itself is positive polarity.

A further degree of flexibility is offered by the 'INVbit' (B6, $03 section 5.3.4.4). This bit allows the polarity of the data to be inverted so that the correct polarity of modulation is always achieved, i.e a data '1' can be set as a positive frequency shift or a negative frequency shift as the application requires. Note that the 'INVbit' also affects the receiver so may need to be changed between Tx and Rx in some circumstances.

The 'TX LO DIV' (B6, $21, section 5.3.9) enable the divide by two in the Tx LO path (see Figure 1). Normal operation is with the divider active so the Tx LO matches the Rx LO which always has the divide by 2 active as this is part of the image reject mixer structure. The ability to switch off the divide by two is useful if an external mixer is used in the receiver. In this case the input to the Rx mixer is likely to be at the desired mixing frequency (i.e. not twice that frequency) so it is helpful to be able to select this operation in the O-PLL loop. This is discussed further in section 6.5.3.

5.3.12 Other Transceiver Functions

5.3.12.1 Frequency Offset

Frequency Offset $04 Read

Bit:	7	6	5	4	3	2	1	0
	Rx measured RF frequency offset (-64 to 63)							Good Data

The 2's complement number read from bits 7 to 1 represents the estimate of the frequency error between the transmitter and receiver carriers. This value is only valid if bit 0 = '1'. If bit 0 = '0' the RF frequency offset will not be computed and bits 7 to 1 will hold the last value calculated. The scaling of this value alters with selected bit rate. With 8kbps the scale is 19Hz per bit, for 4kbps 38Hz per bit and 16kbps 9.5Hz per bit. Intermediate values can be calculated by interpolating between the above values.

The measured frequency offset can be less accurate when receiving a modulated signal with a large offset between the Tx and Rx frequencies as it becomes distorted by the band edges of the IF filter. In this case, the reading may be approximately 10% in error. This error is less pronounced when receiving a carrier only with the same Tx / Rx frequency offset error.

5.3.12.2 Signal Strength

Signal Strength $05 Read

Bit:	7	6	5	4	3	2	1	0
	Rx measured signal strength RSSI (0-255)							

The value read from this register represents the latest estimate of the RSSI as the number of dB above a level of approximately -150 dBm. The absolute scaling of this will vary depending on gain of external components and input matching arrangements. The absolute scaling should be evaluated for a particular design however the RSSI is designed to work over at least –113dBm to –63dBm with typical external gains.

The RSSI value is averaged over a number of samples of the received data. This is to reduce variability due to noise and achieve a result with less fluctuation. Thus the RSSI algorithm computes the sum of N values, where each value is pre-multiplied by a factor f. To obtain the same measured RSSI value presented in this register for different values of N, the user must ensure that N/f is a constant. Default values of N and f are N=2048 and f=16. These values of N and f can be changed using special command $1F (see section 5.3.8.6).

The sample rate is 32kHz so one sample is 1/32000=31.25μs. Thus with N=2048 the averaging time is 2048*(1/32000)=64ms and the minimum averaging time is 16*(1/32000) = 0.5ms (see section 5.3.8.6 for a full table of values).

The RSSI algorithm runs continuously while the receiver is operating. The register is updated each time the specified number of averages has been completed. The register is updated within 31.25µs after the last data sample. The new averaging period starts 31.25µs after the end of the pervious averaging period. This is shown graphically in Figure 25. During the update period of 31.25µs the precise time the data is updated is not defined however the CMX990 ensures the data will always be valid (i.e. it will not produce erroneous values during an update). With the CMX990 operating in a particular state the update point will generally be the same so sampling RSSI at the maximum rate for a particular sample window will always provide the next sample. For example with N=64 the update rate is (64+1) * 1/32000 = 2.03125ms. Reading the register at this rate will always provide the next value.

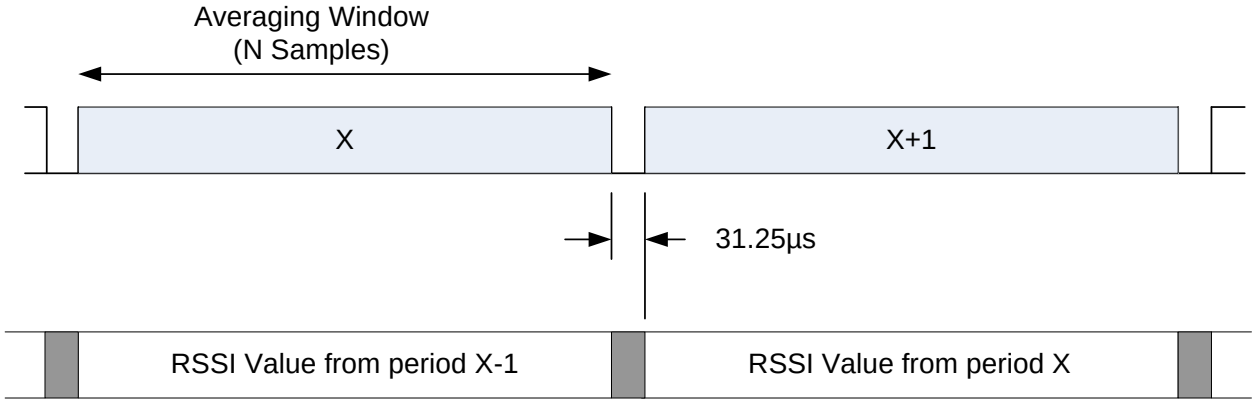

Figure 25 RSSI Timing

See also section 6.5.6.

6 Application Notes

6.1 General

The CMX990 chip is a modem and RF system designed for wireless data modem applications. The chip addresses the needs of various data systems, both product standards and regulatory requirements, including:

- Mobitex Interface Standard (MIS)
- European R&TTE (based on EN 300 113 or EN 300 220)
- FCC Limits (47 CFR Parts 2 and 90)

Details of techniques to meet these requirements can be found in following sections along with general discussion of how to design with the CMX990. The first sections (6.2, 6.2.3, 6.2.4 and 6.3) detail the data formatting offered by the CMX990. Operation is compliant with the Mobitex system however the CMX990 is configurable and the data format can be usefully used for many packet data modems.

Sections 6.4 and 6.5 focus on aspects of the RF operation of the CMX990.

6.2 CRC, FEC, Interleaving and Scrambling Information:

6.2.1 CRC

This is a 16-bit CRC code used in both the Mobitex Data Block and Short Data Block. In transmit it is calculated by the modem from the data block bytes using the following generator polynomial:

$$g(x) = x^{16} + x^{12} + x^5 + 1$$

i.e. CRC from CCITT X.25.

This code detects all (single) error bursts of up to 16 bits in length and about 99.998% of all other error patterns.

The CRC register is initialised to all ‘1s’ and the CRC is calculated octet by octet starting with the least significant bit of ‘byte 0’. The CRC calculated is bit-wise inverted and appended to the data bytes with the most significant bit transmitted earliest.

In receive mode, a 16-bit CRC code is generated from the data bytes of each Mobitex Data Block or Short Data Block as above and the bit-wise inverted value is compared with the received CRC bytes. If a mis-match is present, then an error has been detected.

6.2.2 FEC

In transmit mode, during T7H, TSD and TDB, the modem generates a 4-bit Forward Error Correction code for each coded byte. The FEC is defined by the following H matrix:

$$H = \begin{matrix} 7\_\_\_\_\_0 & 3\_\_\_0 \\ 11101100 & 1000 \\ 11010011 & 0100 \\ 10111010 & 0010 \\ 01110101 & 0001 \end{matrix}$$

Generation of the FEC consists of logically ANDing the byte to be transmitted with bits 7 to 0 of each row of the H matrix. Even parity is generated for each of the 4 results and these 4 parity bits, in the positions indicated by the last 4 columns of the H matrix, form the FEC code.

In checking the FEC, the received 12-bit word is logically ANDed with each row of the H matrix (earliest bit received compared with the first column). Again even parity is generated for the 4 resulting words and these parity bits form a 4-bit nibble. If this nibble is all zero then no errors have been detected. Other results 'point' to the bit in error or indicate that uncorrectable errors have occurred.

This code can correct any single error that has occurred in each 12-bit (8 data + 4 FEC) section of the message.

Example:
If the byte to be coded is '00101100' then the FEC is derived as follows:

H matrix row:	1	2	3	4
A	11101100	11010011	10111010	01110101
B	00101100	00101100	00101100	00101100
A AND B	00101100	00000000	00101000	00100100
Even Parity:	1	0	0	0

where A is bits 7 - 0 of one row of the H matrix and B is the byte to be coded. The even parity bits apply to the result of 'A AND B'.

So the word formed will be: '00101100 1000' sent left to right

When the same process is carried out on these 12 bits as above, using all 12 bits of each H matrix row, the resulting 4 parity bits will be '0000'.

6.2.3 Interleaving

All the bits of transmitted Mobitex Data Blocks and Short Data Blocks are interleaved by the modem to give protection against noise bursts and short fades. Interleaving is not performed on any bits in the Mobitex Frame Head.

In the Mobitex Data Block case, considering the 240 bits to be numbered sequentially before interleaving as 0 to 239 ('0' = bit 7 of byte 0, '11' = bit 0 of FEC for byte 0, ... , '239' = bit 0 of FEC for byte 19 - see Figure 15), then they will be transmitted as shown in Figure 26. The Mobitex Short Data Block is interleaved in a similar way; referring to Figure 15 consider bytes 4 and 5 as the CRC data and ignore bits 72 to 239 in the lower part of the diagram. i.e. the last bit to be transmitted will be '71'.

The modem performs the inverse operation (de-interleaving) in receive mode on both Mobitex Data Blocks and Short Data Blocks.

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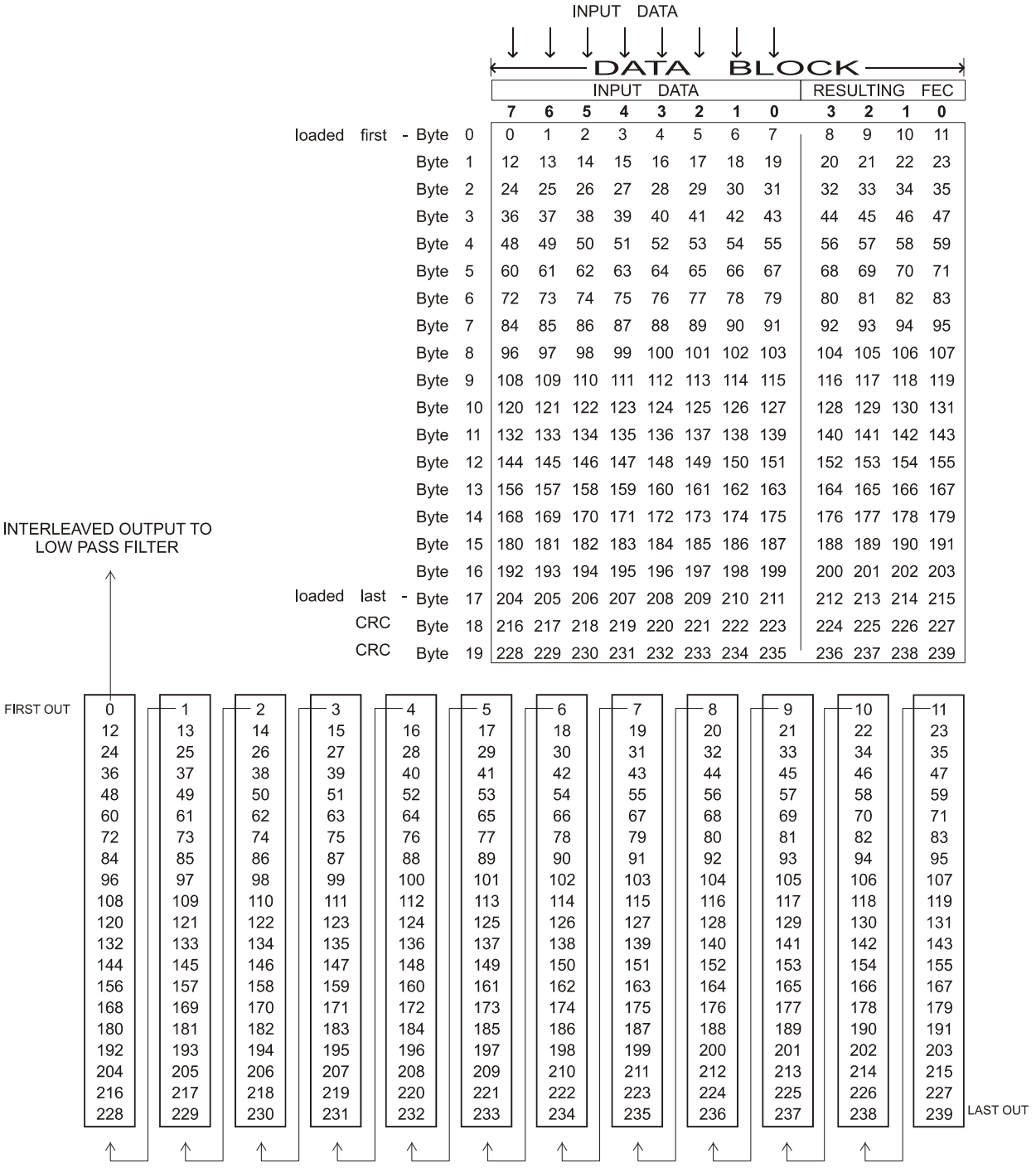


Figure 26 Interleaving - Input/Output

6.2.4 Scrambling

All formatted bits of both Mobitex Data Blocks and Short Data Blocks are XORed with the output of a 9-bit scrambler. This scrambler is initialised at the beginning of the first data block in every Frame. The 511-bit sequence is generated with a 9-bit shift register with the output of the 5th and 9th stages XOR'ed and fed back to the input of the first stage. The scrambler is disabled during all other tasks, apart for TSO.

6.3 Modem Application Examples

6.3.1 Transmit Frame Example

If the device is required to send a Mobitex Frame the following control signals and data should be issued to the modem, assuming the device is not starting from a powersave state, TXRXN is set to '1' and that the relevant control bits have been set as required after power was applied to the device:

1. 6 bytes forming the Frame Head are loaded into the Data Buffer, followed by a 2-bit pause to let the filter stabilise, followed by setting T7H task.
2. Device interrupts host µC with IRQN when the 6th byte is read from the Data Buffer.
3. Status Register is read and 18 bytes are loaded, followed by setting TDB task.
4. Device interrupts host µC with IRQN when 18th byte is read from the Data Buffer.
5. Status 1 Register is read, host may load data and set next task as required:

   GOTO '1' if the last Data Block for this Frame has been transmitted and another Frame is to be immediately transmitted
   GOTO '3' if another Data Block in this Frame is to be transmitted
   GOTO '6' if no more data is to be immediately sent

6. 1 byte representing the 'hang byte' is loaded into the Data Buffer, followed by setting the TSB task.

If the 'hang byte' has been transmitted and no more data is to be sent then a new task need not be written and the µC can wait for the IBEMPTY interrupt when, after a few bits to allow for the Tx filter delay, it can shut down the Tx RF circuits.

A top level flowchart of the transmit process is shown in Figure 27.

Hang Byte

The filtering required to reduce the transmitted bandwidth causes energy from each bit of information to be smeared across 3 bit times. To ensure that the last bit transmitted is received correctly it is necessary to add an 8-bit 'hang byte' to the end of each message. Thus the tasks required to transmit an isolated Mobitex frame are:

$$T7H + (n \times TDB) + TSB$$

When receiving this data, the extra byte can be ignored as its only function is to ensure integrity of the last bit and not to carry any information itself.

It is suggested that a '00110011' or '11001100' pattern is used for this 'hang byte'.

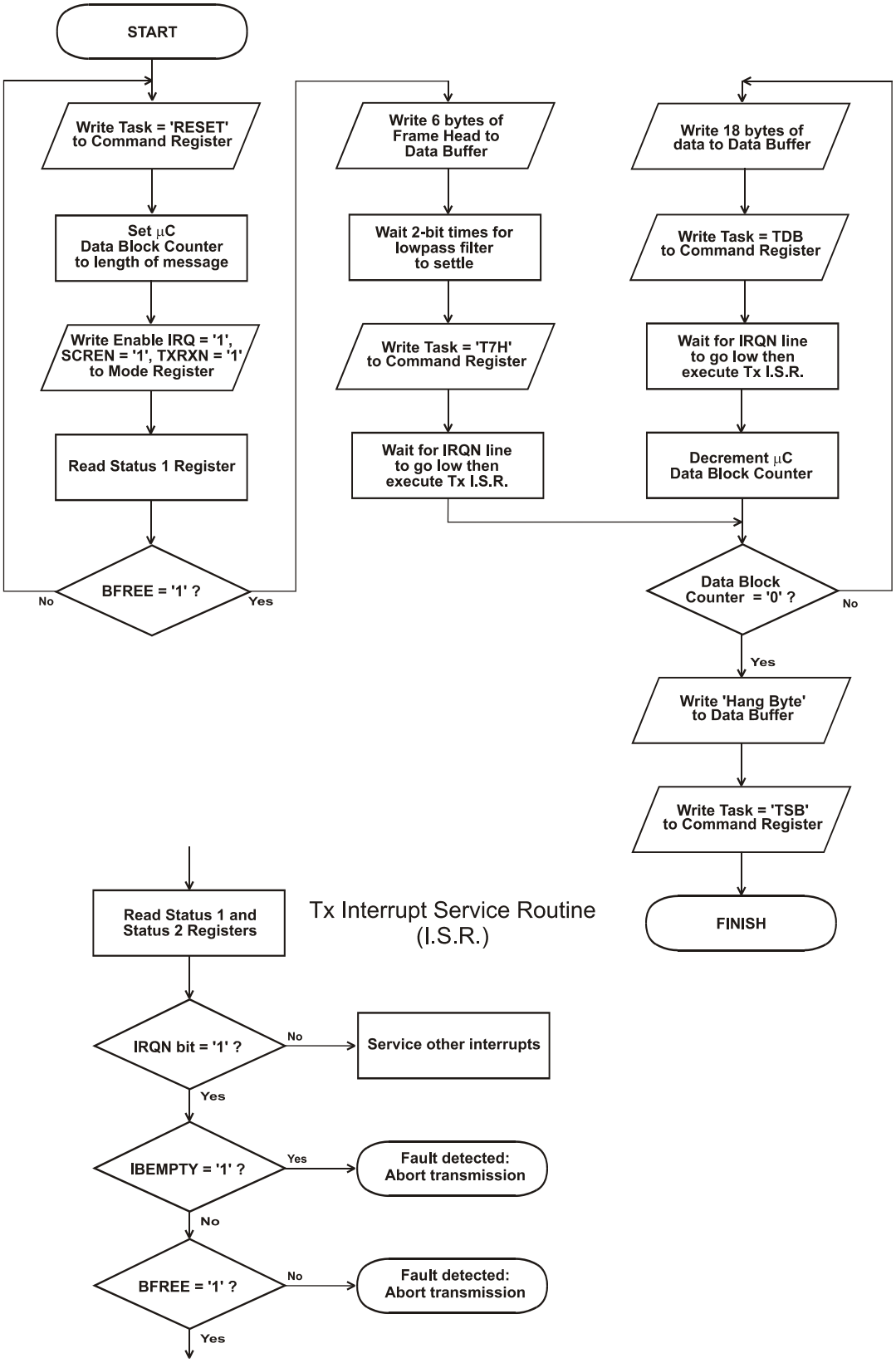


Figure 27 Transmit Process

6.3.2 Receive Frame Example

If the device is required to decode a Mobitex Frame the following control signals should be issued to the modem. The host should set the Control Register and activate the Acquire I Q Offset each time a new channel is selected. When the RSSI indicates a valid signal or carrier only is present the acquire AFC process should be activated (if required) before packets are decoded. This also assumes that the device is initially not in powersave, the correct Frame Sync bytes have been loaded, the SCREN is set as required, TXRXN bit is set to '0' and a Packet Detect event has occurred, or a Frame Head is imminently expected:

1. 2 bits after a carrier has been detected or a frame head is expected the Acquire Bit Clock bit is set to initiate the bit clock extraction sequence.
2. Wait 12 bits and set SFH task to search for a Mobitex Frame Head
3. Device will interrupt host µC with IRQN when valid Frame Sync is detected and header bytes decoded.
4. Host µC reads Status 1 Register, checks MOBAN and CRCFEC bit and reads out 2 Frame Head control bytes.
5. Host µC disables Packet Detect and sets the task to RDB to receive a Mobitex Data Block.
6. Device will interrupt host µC with IRQN when the Data Block has been received and the CRC has been calculated.
7. Host µC reads Status 1 Register, checks CRC validity and reads 18 Data Block bytes. The Data Quality Register can also be read to obtain the received S/N level.
8. Host µC sets task if more information is expected:

   GOTO '2' if last Data Block and another Frame Head imminently expected.
   GOTO '5' if another Mobitex Data Block expected.

If the last Data Block has been decoded and no more information is expected then the task bits need not be set as the device will automatically select the idle state.

A top level flowchart of the receive process is shown in Figure 28.

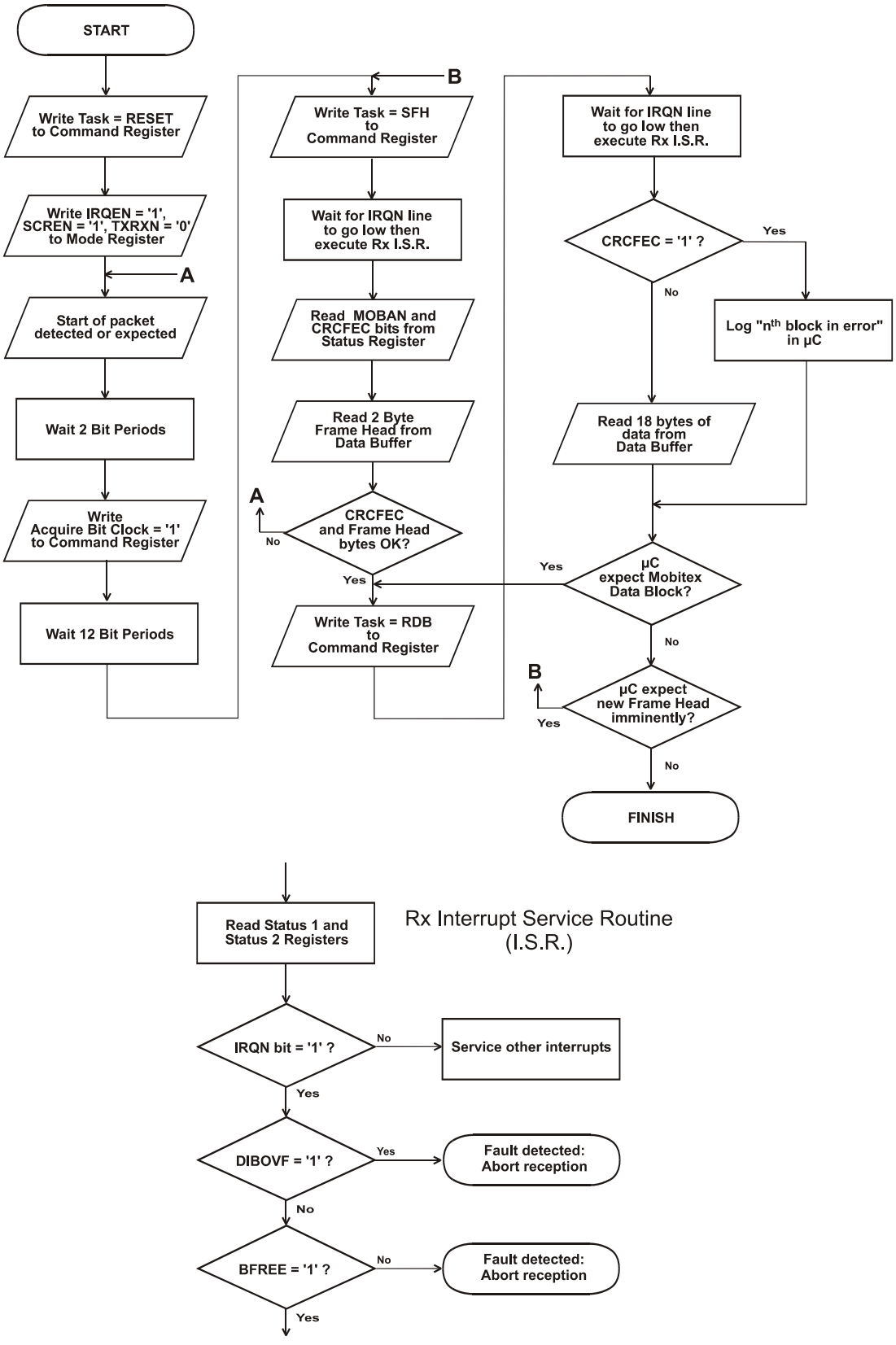


Figure 28 Receive Process

6.4 Transmitter

The transmitter architecture allows constant envelope phase/frequency modulation, typically GMSK or GFSK. The transmitter uses an offset phase locked loop (O-PLL) to generate the transmitted signal. This has the advantage of very low spurious output minimising the need for spurious response filtering, thus reducing the overall cost of the radio and maximising power efficiency due to reduced losses. A description of the O-PLL is given in sections 5.2 and 5.2.1.

Details of control of the transmitter are given in section 5.3. A particularly important section for transmitter operation is section 5.3.11 where a number of the transmitter control features are explained.

The following sections will now review a number of design consideration when developing a RF design using the CMX990.

6.4.1 Transmitter O-PLL Frequency Tuning Range Considerations

The O-PLL system is a phased locked loop so one aspect that needs to be considered in any design is the lock range, i.e. the band of frequencies over which the loop will correctly lock to the desired frequency.

There are a number of options available in using the Transmitter section and there are some constraints to the choices that need to be considered:

Transmit band required
Selection of the Intermediate Frequency (IF)
Selection of High side or Low side mixing
Selection of forward path “modulation” filter frequency
Selection of feedback path filter frequency

The Transmit Band is the range of frequencies over which the transmitter must be switchable. It is useful to define the highest required frequency as RFmax and the lowest required frequency as RFmin.

The IF selection and the choice of high side (LO>RF) or low side (LO<RF) mixing need to be considered along with the receiver operation as the choice is often governed by the need to minimise the time for switching between receive and transmit. Therefore it is desirable to minimise the difference between the Main Local Oscillator (MainLO) frequencies needed for transmit and receive. There are additional constraints on this choice, discussed below, governed solely by the need to control the offset loop. It is recommended that the IF be chosen at 40MHz, 45MHz, 80MHz or 90MHz although frequencies close to these values are also acceptable.

6.4.1.1 Filter Selection

The forward path ‘modulation’ filter, between the I/Q modulator and the phase detector, is designed to remove harmonics of the IF that are generated in the mixing process. There are four filter selections: one for each of the recommended IF frequencies (see section 5.3.11) If an IF is required that is not one of the recommended values, then it will be best to choose the filter frequency which is the nearest higher value. A nearest lower value will work if very close, but uses up the tolerances put into the filter design to allow for component value variation on-chip.

The choice of the filter value for the feedback path is more complicated. The purpose of the filter is to remove spurii that come out of the mixer in the feedback path of the offset PLL. These can result in unwanted spurs in the transmitted output or, in the extreme, prevent locking of the loop. To do this the filter needs to remove, to a sufficiently low level, the lowest frequency spurious signal that emerges from the transmit mixer. This lowest value spurious signal depends on whether high-side mixing or low-side mixing is used. Defining LO as the Local Oscillator frequency applied to the mixer (this is usually half the MainLO frequency):

- for low side mixing the minimum frequency to reject is 2LOmin - Rfmin
- for high-side mixing the minimum frequency to reject is RFmin

There are two choices of filter with guaranteed pass bands of 83MHz and 118MHz and with adequate stop bands above 300MHz and 425MHz respectively. It is necessary to select the filter to ensure the lowest unwanted frequency is rejected i.e. above the stated stop band value. (for detail of how to select the desired filter see section 5.3.11).

6.4.1.2 VCO Range

During the settling of the loop the VCO will produce frequencies that are different from the desired final value. Mixing an undesired VCO output frequency with the LO produces an IF which can be some way off from the required IF. This can result in the loop failing to converge for one of two reasons. Firstly, if the IF is sufficiently high that it is filtered by the feedback path filter; this essentially removes the feedback path and makes the feedback signal appear as a zero frequency (when it is in fact high). If this is allowed to happen the loop will drive the VCO away from the desired frequency rather than towards it. This means that the VCO must not be allowed to produce frequencies that cause the IF to exceed the minimum filter pass band value. This constrains the Tx VCO frequency prior to enabling Tx Offset PLL (VCOout) such that:

$VCOout_{max}$ < LOmin + Ffilter for Low-side mixing (Ffilter is 83MHz or 118MHz)

$VCOout_{max}$ must be in excess of the required RFmax if the frequency band is to be achieved

Or

$VCOout_{min}$ > LOmax – Ffilter for High-side mixing (Ffilter is 83MHz or 118MHz)

$VCOout_{min}$ must be below the required RFmin if the frequency band is to be achieved

Secondly, the loop may fail to converge if the RF signal from the VCO is allowed to move too far on the other side of the required frequency. In this region it is possible to produce an IF from the RF image frequency. As the RF frequency gets close to the LO value the IF approaches zero. As the IF is AC coupled internally, this may allow the subsequent limiter to self-oscillate and the loop may fail to converge. This constraint to the VCO is such that:

$VCOout_{min}$ > LOmax for Low-side mixing

$VCOout_{min}$ must be below the required RFmin if the frequency band is to be achieved

Or

$VCOout_{max}$ < LOmin for High-side mixing

$VCOout_{max}$ must be in excess of the required RFmax if the frequency band is to be achieved

All these conditions should ideally to be met for the loop to be guaranteed to converge correctly however the filters are not ‘brick wall’ so some operation beyond these limits is possible. Further the issue with a zero IF, noted above, will not necessarily cause a problem as the time constant of loop filter will usually mean that the VCO will transition through the zero point and continue to lock correctly.

The operation of these limits is shown in Figure 29. The upper diagram shows the frequency plan for the architecture of Figure 17. In this case high-side mix is used so the conditions given above are applied resulting in the conclusion that the minimum frequency the VCO can achieve should be in the range 796 – 819MHz and the Maximum frequency the VCO can achieve should be in the range 824MHz to 909MHz. These become constraints on the VCO design e.g. the VCO with V_{tune}=0V should be in the 796-819MHz range and with V_{tune}=V_{dd} should be in the range 824 to 909MHz. Also note that due allowance for tolerances and production variations should be made.

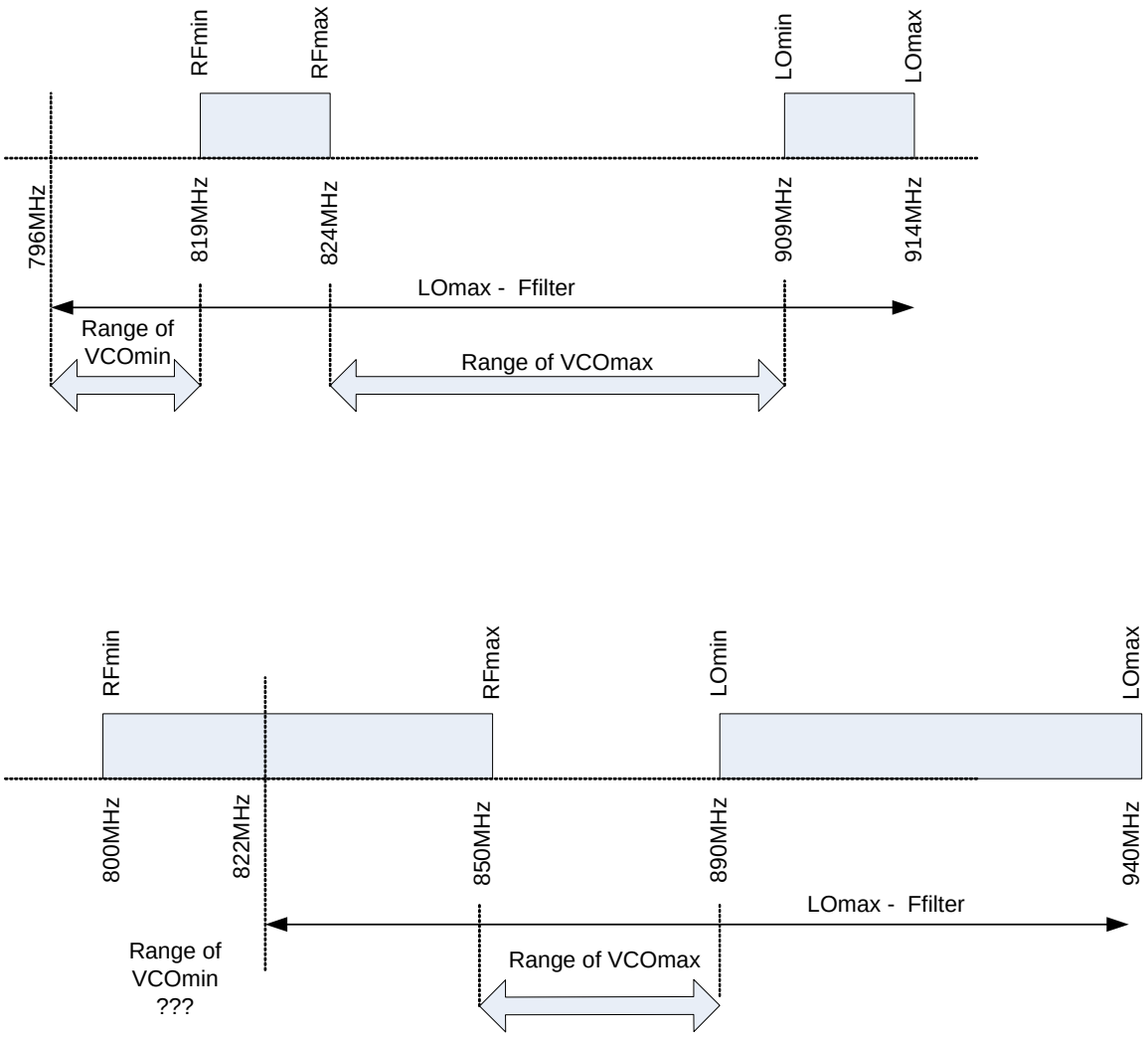


Figure 29 Allowed VCO Ranges

Considering now the lower diagram in Figure 29, here the required tuning band is 800MHz to 850MHz. In this case the LOmax – Ffilter comes above RFmin so it appears no VCOmin range is available for successful operation. Clearly VCOmin must be below Rfmin so the risk is the loop will not lock because the IF filter has removed the feedback signal. The solution is to use the pre-change facility of the CMX990 were the VCO loop filter can be pre-conditioned under user control to V_{DD}VCO/2 using the 'Tx VCO Charge bit (see section 5.3.11). Provided that the frequency that results from this is within the range 822MHz to 890MHz the loop will converge to the correct values.

6.4.2 Start Up

The timing of the turn-on of the transmitter needs careful control. A typical sequence is shown in Figure 30. The first step is to program the IF and RF synthesisers to the correct frequencies for the desired transmitter channel. When time has been allowed for the PLL's to lock the transmitter circuits (excluding the PA) should be enabled. In order for the O-PLL to function it is necessary to:

- Enable the TX DAC (bit 0 of register $03)
- Enable Tx mode (bit 5 of register $03)

This is because otherwise the input to the I/Q modulator is in a quiescent state with the result that the modulator does not produce significant output. As a result there is no reference signal for the O-PLL and hence it will not lock.

Depending on the leakage through the PA the O-PLL should start to lock up. The limiter has been designed to allow locking at low input levels so the loop will start to lock with a signal level of around -50dBm at the O-PLL mixer input (with 0dB attenuation). If leakage levels through the PA are particularly low it may be necessary to provide a small amount of bias (e.g. DAC0 control) to increase leakage to start locking. Typical levels are shown in Table 1.

Level at output of stage	PA 'Off'		PA 'On'	
	Feedback Path	Antenna Output	Feedback Path	Antenna Output
PA Output	-23dBm		+31.2dBm	
Coupler	-45dBm	-23.5dBm	+9.2dBm	+30.7dBm
TX Rx Switch		-43.5dBm		+30dBm
Attenuator	-48dBm		+6.2dBm	
CMX990 Attenuator	-48dBm (1)		-4.8dBm (2)	

Notes:

(1) CMX990 Attenuator setting: 0dB

(2) CMX990 Attenuator setting: –10dB

Table 1 Example Tx Loop Levels

Bit 4 in register $24 enables the pre-conditioning signal to the charge pump output TXPLL (see section 5.3.11). This will charge the loop filter components to V_{DD}VCO/2 through a resistive divider network of 10kΩ (note this is not shown in Figure 30). With typical loop filter values this will charge the loop filter in less than 5ms, however the user may control the amount of pre-charge by varying the time the pre-charge is enabled. The user should ensure that the pre-charge circuit is disabled when they wish locking of the transmitter offset PLL to commence. It should be noted that following enabling the TxRFIF bit (register $04, bit 0) there is a delay while data is clocked through the Tx DAC and filters. During this time the loop may not exhibit anticipated lock behaviour as the phase detector reference input has little or no signal.

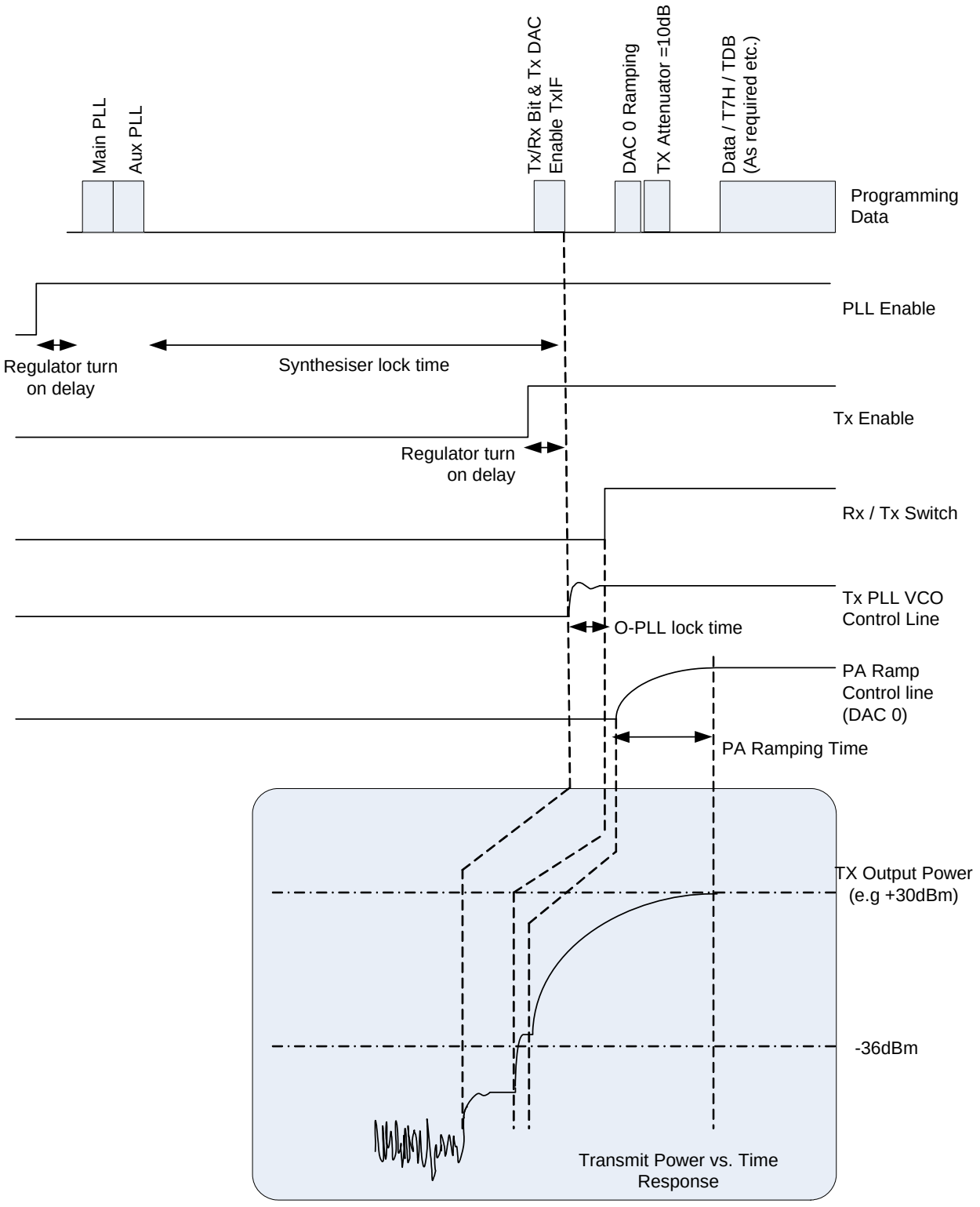


Figure 30 TX Timing Diagram (not to scale)

The time required for the O-PLL to lock will depend on a number of factors including the loop filter design. As a guideline typical lock-times are around 100-200µs. When observing lock time a number of factors

need considering, not just the generic lock time of the loop. Most important are the stability of the local oscillator sources. Pulling or pushing of the VCO during the PLL locking can cause a transient response in the PLL and typically this is much longer than that of the O-PLL. A buffer between VCO and CMX990 LO input is recommended to minimise this effect.

Another concern is power ramping. During this stage it is common that power supply transients will cause some pushing of the VCO. Furthermore, changes in impendence presented by the PA can cause pulling. These effects require the O-PLL to respond and stabilise the frequency (note: this is very much the same problem with traditional two-point FM VCO modulation). The effect is demonstrated in Figure 31 where the PA is ramped rapidly to full power and is a worst case test as no buffering is provided between PA and VCO; the transient in this case has decayed within about 8 symbols of 8kbit/s data (i.e. 1ms). Controlled power ramping can be used to optimise performance.

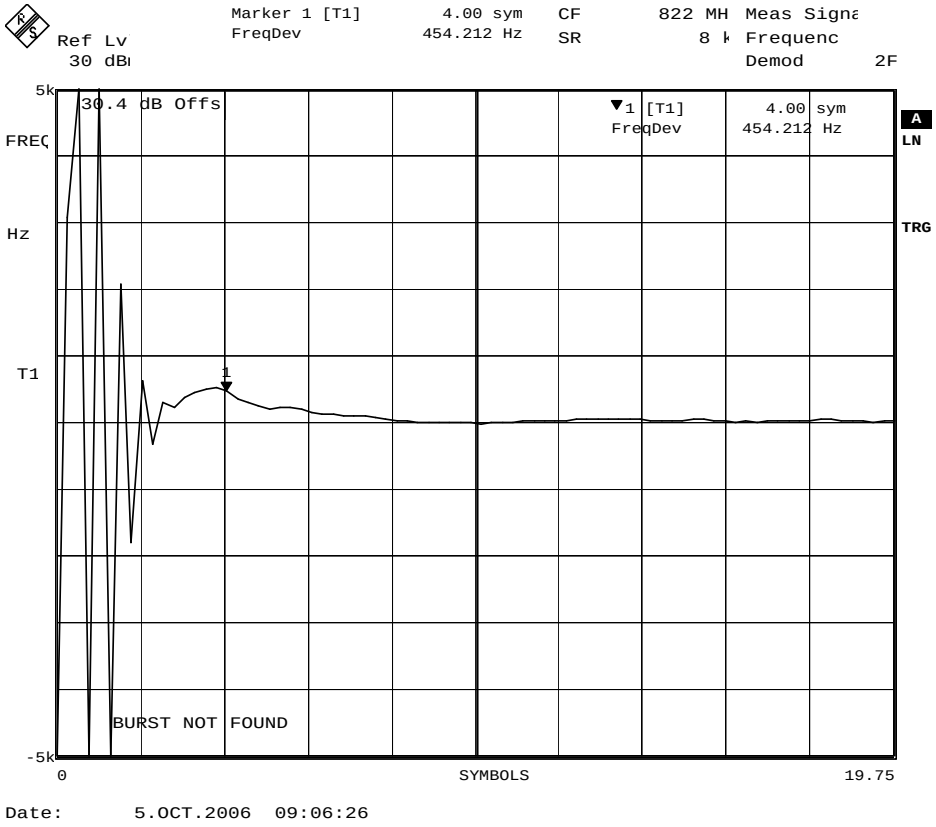


Figure 31 TX Loop transient caused by increasing PA output power from –10dBm to +30dBm; 90MHz IF, f_{tx} = 822MHz, external LO

At the end of a transmission, the various stages should be disabled / switched in reverse sequence to that shown in Figure 30.

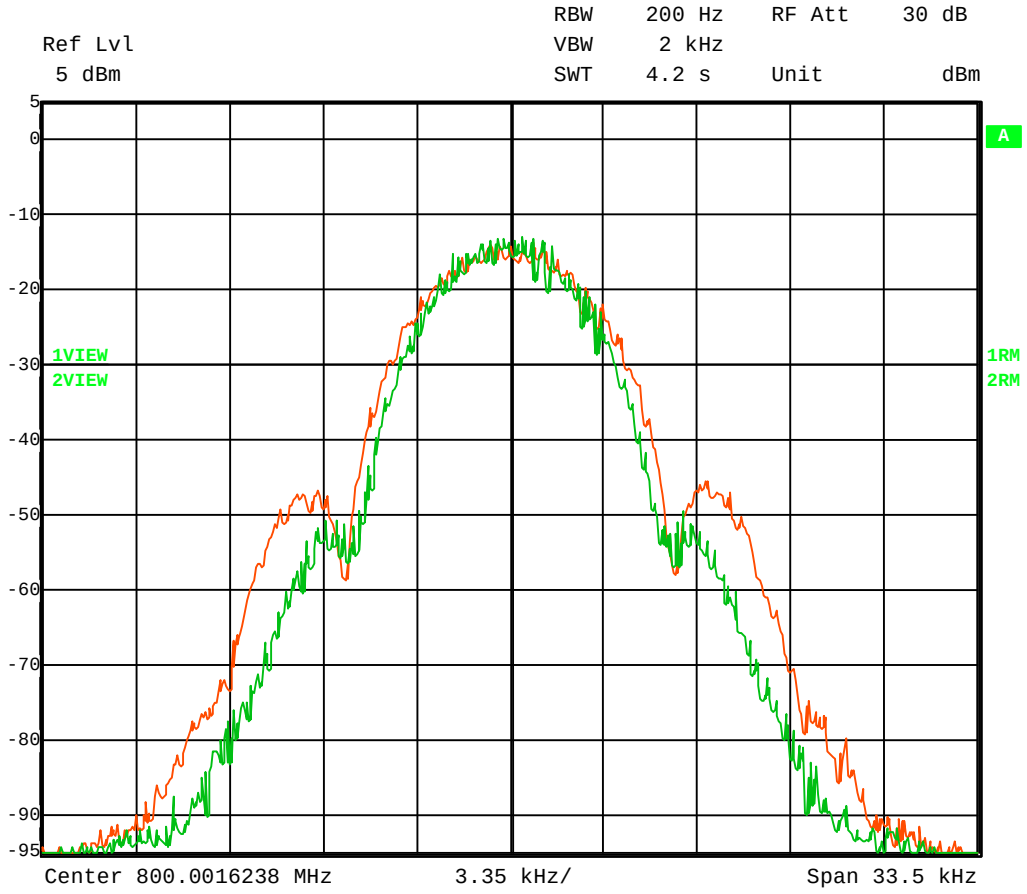
6.4.3 Spurious Emissions

The low level and small number of spurious emissions from the O-PLL transmitter are a major advantage of the technique. The major source of spurious signals is the power amplifier harmonics. The level of these will be set by the selected PA and a harmonic filter must be provided to remove these. The only significant spurious signals generated by the O-PLL transmitter is LO leakage from the offset mixer to the RF input port. The CMX990 mixer has been designed to have low local oscillator leakage meeting the typical requirements (e.g. -36dBm in Europe, -17dBm in USA). Performance is optimised by taking the O-PLL feedback signal from the PA output, thus amplification of the LO spurs is avoided.

The O-PLL loop can generate some spurs within the loop bandwidth. These spurs are generated by harmonics of LO signals and mixing products. As a result some care with frequency plans is required, for example operation on harmonics of the TXIF is problematic (e.g. 450MHz Tx with a 45MHz TXIF). These frequencies can be avoided by selecting a suitable IF that avoids such problems. For systems with a wide tuning range it may be necessary to use a slightly different IF for some frequencies, e.g a 46MHz IF for frequencies close to 450MHz.

6.4.4 Variable BT

The CMX990 offers the ability to select the BT factor in the transmit modulation. This allows characteristics to be optimised for a particular bit/rate channel bandwidth. Options of BT = 0.27, BT = 0.3 and BT = 0.5 are available (see section 5.3.8.2). Figure 32, Figure 33 and Figure 34 show the effect of changing BT.



Inner Trace is CMX990 with BT = 0.3 Outer Trace is CMX990 with BT = 0.5

Figure 32 Modulation spectrum of CMX990 at 8kbps with different BT

For BT=0.27 see Figure 37

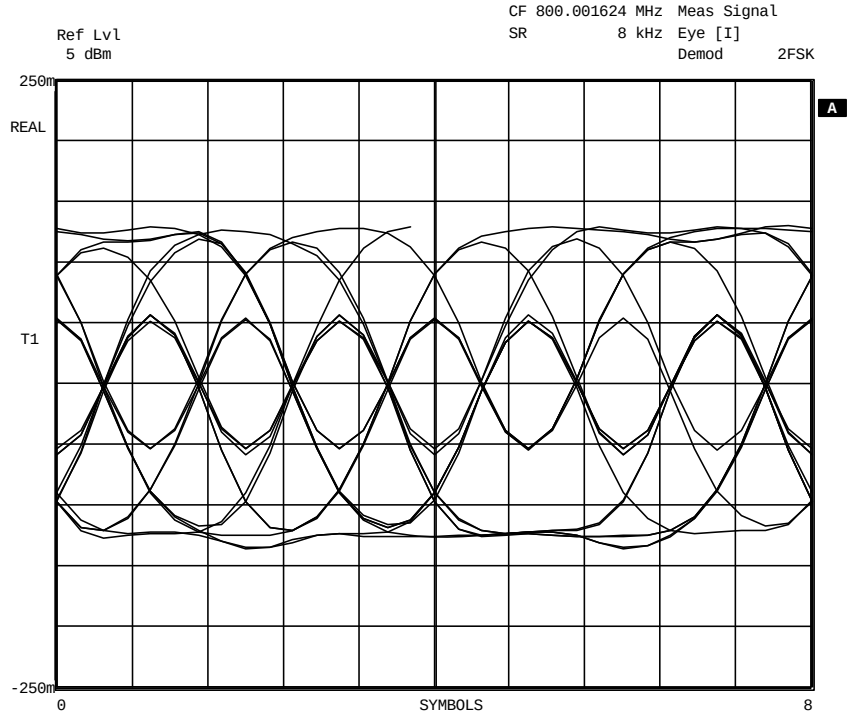


Figure 33 CMX990 modulation eye diagram at 8kbps with BT = 0.3 (Measurement filter BT=1)

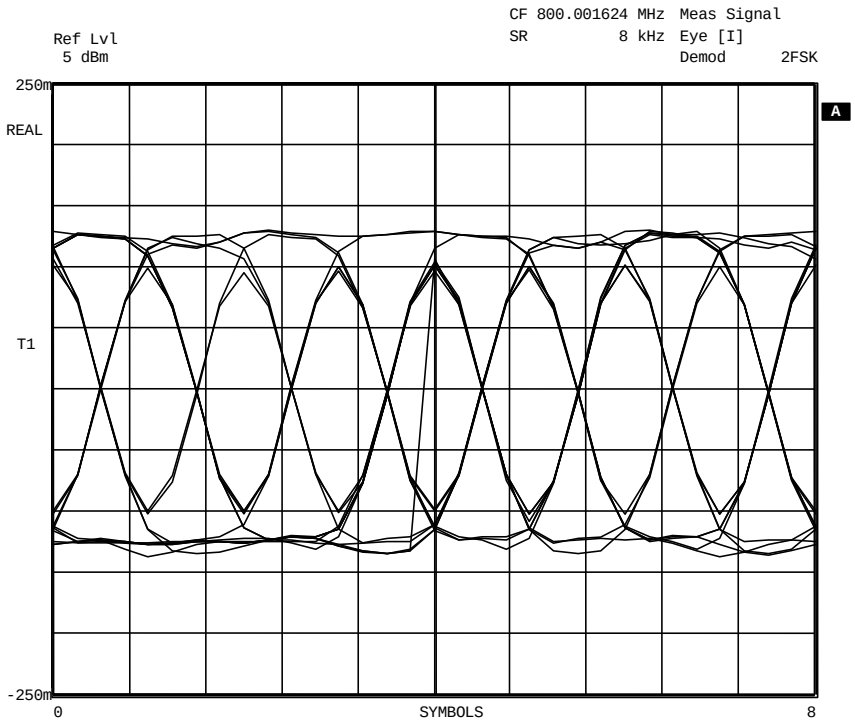


Figure 34 CMX990 modulation eye diagram at 8kbps with BT = 0.5 (Measurement filter BT=1)

6.4.5 Transmitter Performance

The modulation of the CMX990 is produced digitally, ensuring excellent accuracy and no need for alignment of deviation as might be required with an analogue modulator. The CMX990 is designed to meet the requirements of various international standards including EN 300 113 and EN 300 220 in Europe and 47 CFR 2.1049 & 90.210 (J) applicable in the USA (Figure 35).

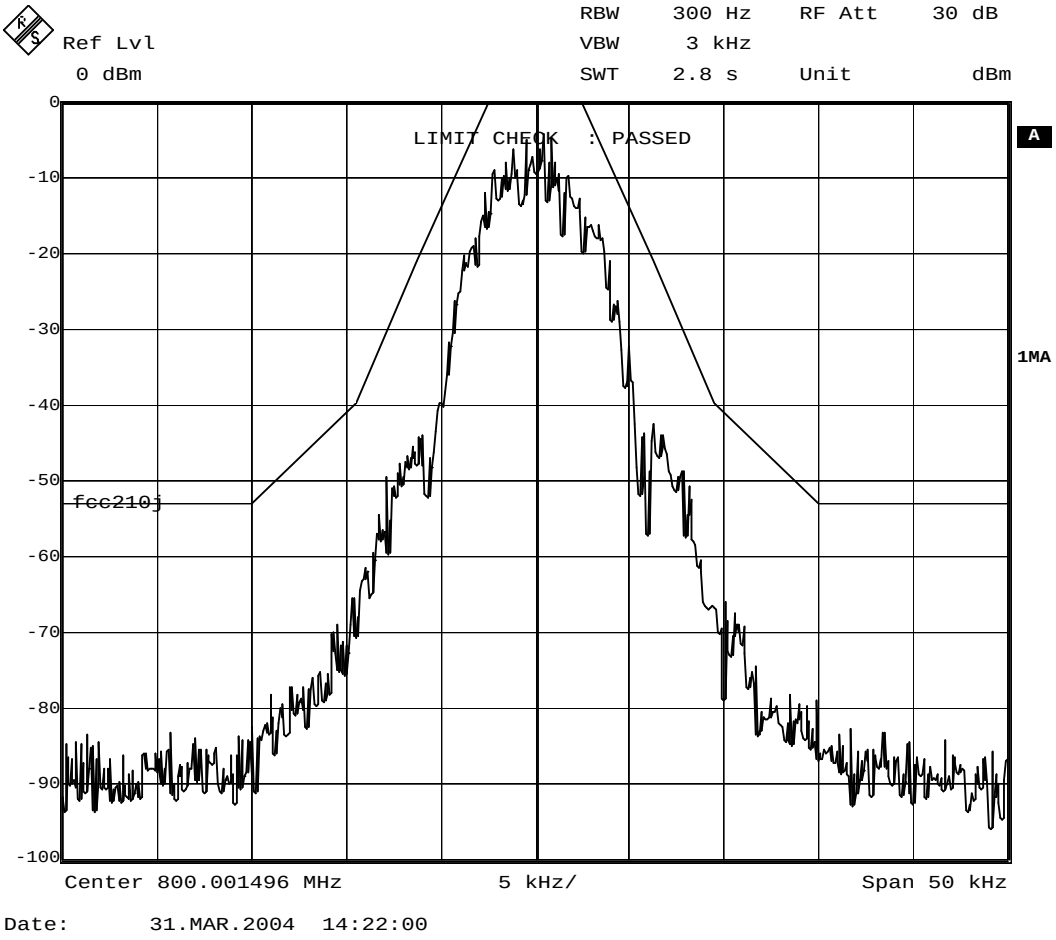


Figure 35 Modulation from CMX990 with 47 CFR 90.210 (J) emission mask

6.4.5.1 Adjacent Channel Power

The EN 300 113 requirements are the most demanding limits of those listed above, requiring -60dB adjacent channel power for 12.5kHz channelled systems and -70dB adjacent channel power for 25kHz channelled systems. These requirements can be met by the CMX990. Performance with a 25kHz system at 9600bps is shown in Figure 36.

For 12.5kHz channels a data rate of 8kbps per second is required for some standards with a nominal BT=0.3. Generating this modulation in an ideal case from a signal generator and measuring the Adjacent Channel Power (ACP) using the measurement bandwidth specified in EN 300 113 Annex B.1 suggests that meeting the –60dB limit is a significant challenge (see Table 2). For this reason a BT option of 0.27 has been included and using this setting the CMX990 achieves -62 or -63dB adjacent channel power (see

Figure 37). Interestingly, during development, tests were made with reduced deviation while maintaining a BT=0.3 during which it was found necessary to reduce the deviation substantially before the 60dB limit could be achieved. It was therefore concluded that the tighter filter (reduced BT) was the preferred option.

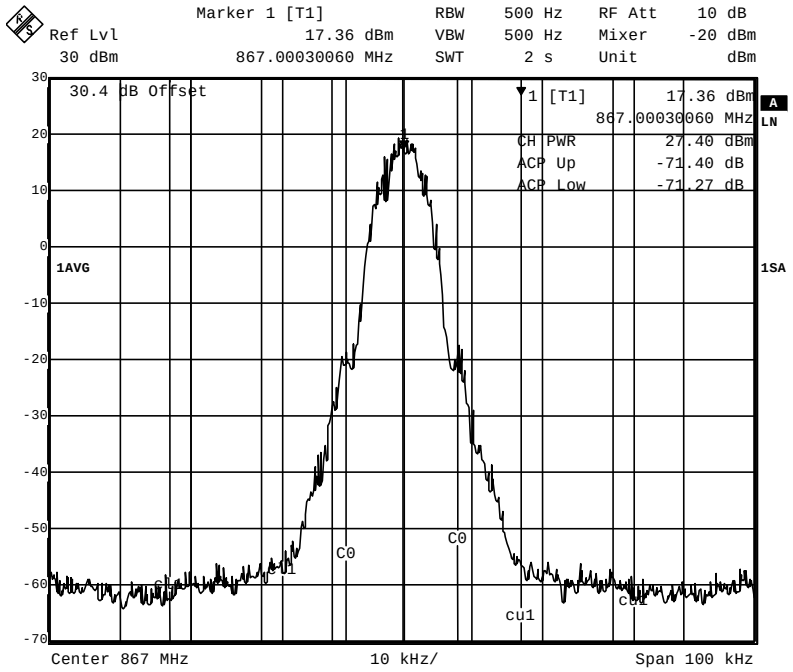


Figure 36 9.6kbps spectrum, 25kHz, +30dBm, BT=0.5

BT Product	Adjacent Channel Power (dBc)
0.25	-68
0.27	-63
0.28	-62
0.29	-61
0.30	-59
0.31	-57.5
0.32	-56.5

Table 2 ACP for 12.5kHz channel versus BT product for Digital Signal Generator (8kbps)

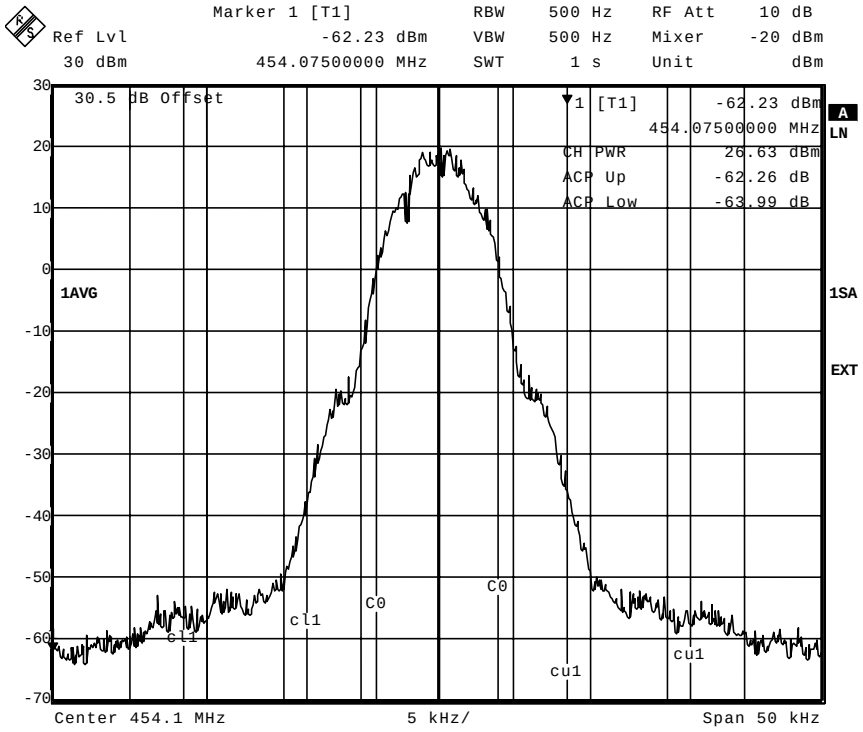


Figure 37 TX ACP of –62dBc (12.5kHz channel settings) at +30dBm carrier, 8kbps, BT = 0.27, IF 90MHz

A further issue to note concerning the adjacent channel power is that phase noise from both the main and aux local oscillators contribute to the adjacent channel power. The phase noise of the two local oscillators should be well below the adjacent channel power that is being sought. Note that a CW source which achieves –60dBc adjacent channel will be much worse than this when modulated. A further point to note is that phase noise is improved by the action of the LO dividers in the CMX990.

The phase noise of the VCO in the O-PLL is less significant when considering adjacent channel performance as the adjacent channel area is within the loop bandwidth. As a result the phase noise will reflect that of the reference source (aux LO) and any noise added in the feedback path (i.e. the main LO).

6.4.5.2 Wideband Noise

Wideband noise requirements vary between products and depending on particular international standards. A good guideline is CEPT/ERC/REC/74.01 which is based on ITU SM.329. This mask is required by EN 300 113 for example. As will be seem from Figure 38 the CMX990 comfortably meets the requirements for a 2W (+33dBm) transmitter.

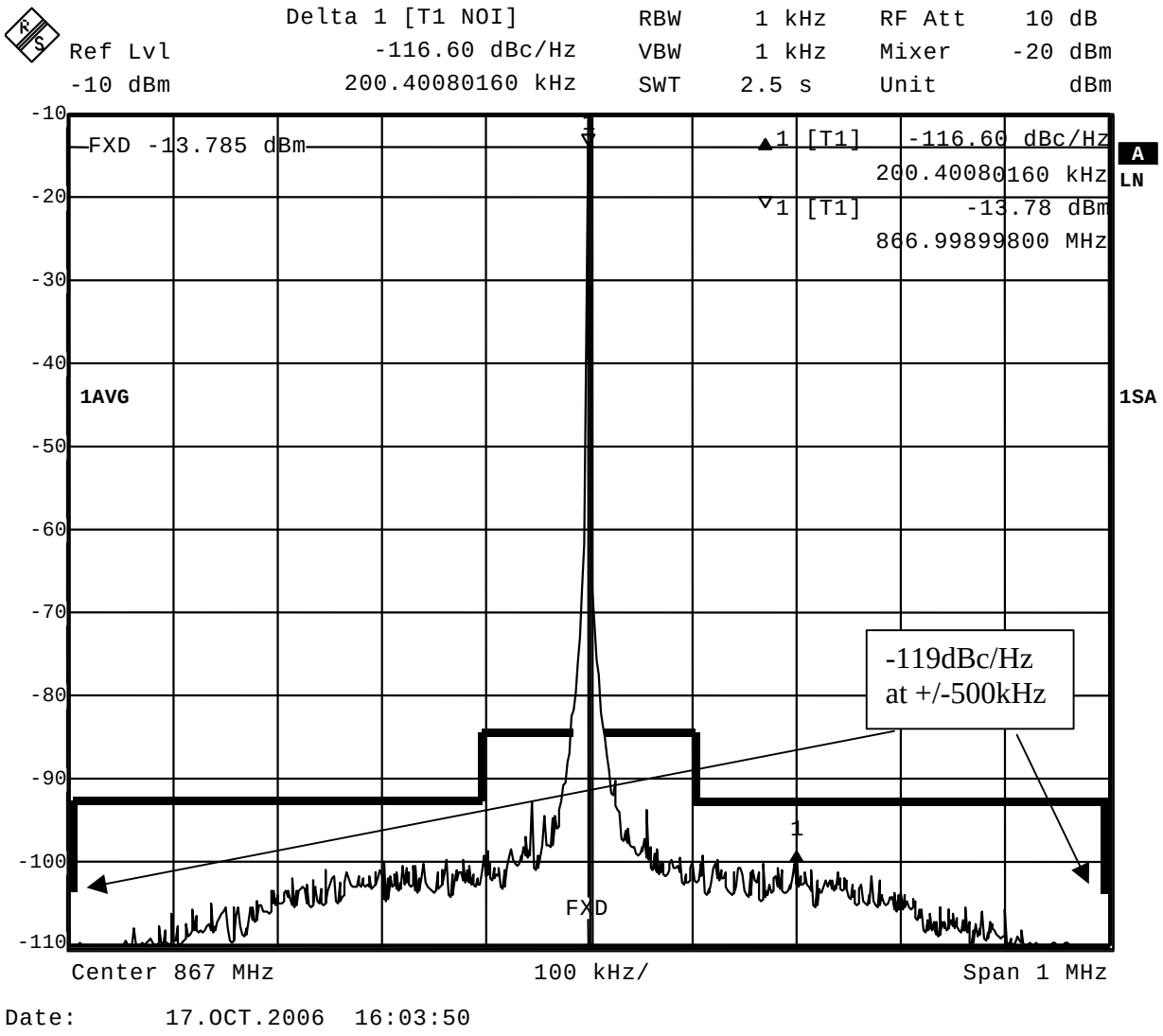


Figure 38 CMX990 Wideband noise performance showing CEPT/ERC/REC/74.01 emissions mask for a 2W (+33dBm) transmitter

6.5 Receiver

The design of the CMX990 is such as to allow receiver requirements of the Mobitex standard to be met. In addition the receiver is also capable of meeting the requirement of standards such as EN 300 113 and EN 300 220.

6.5.1 Architecture Overview

The receiver architecture is based on the classic superhetrodyne approach. The CMX990 provides the 1st mixer and IF stages with AGC followed by conversion to I/Q format baseband signals. These are then converted to digital signals in sigma-delta converters, which also provide adjacent channel filtering, before demodulation.

The first stage of the CMX990 receiver is a mixer intended to convert from RF to a 1st intermediate frequency (IF) of around 45MHz. The mixer is an image reject type thus minimising the external filters required before the mixer. The mixer would normally be preceded by input transmit/receive switch, low noise amplifier and a filter. A typical cascaded noise figure for these stages is around 4dB with a recommended gain of around 10dB. The noise figure of the mixers is very good for an image reject mixer circa 13dB to 15dB depending on configuration. This low noise performance allows the pre-gain required to achieve a reasonable overall noise figure to be minimised which has the benefit of making system intermodulation-performance better. It will be noted that the mixer is a Gilbert cell type therefore requires a differential input. This can be achieved with a narrow-band LC circuit or a balun transformer (see section 4.5).

The image reject network is selectable to permit high side or low side local oscillator injection (see 'sign' bit in register $24).

Following the 1st mixer the signal is passed off chip. A single ended output stage is used to ease connection to IF filter components. The 1st IF can be in the range 44-46MHz with 45MHz being a typical choice. Filtering is required at this point to achieve the typical performance requirements and the amount of selectivity can be tailored for a particular design. For example, Mobitex adjacent channel filtering can be met with digital filters at baseband alone, however the blocking signal test at 84dB puts severe demands on the dynamic range of the baseband sections so filtering at the IF is necessary; a 2-pole crystal filter is all that is required in this case. EN 300 113 has more severe adjacent channel requirements so reasonable adjacent channel selectivity at the 1st IF is recommended. A 4-pole crystal filter should be satisfactory. A summary of suggested filter requirements can be found in Table 3.

The output of the IF filter should be connected to IFIN pin which goes into a gain controlled low noise amplifier stage. 45dB of AGC range is available in 15dB steps. The output of the IF amplifiers passes to I/Q mixers which are fed a by a divide by 4 circuit from the IF local oscillator. The mixers include DC offset compensation (see section 6.5.2). Baseband amplifiers are then used to provide the correct input level to the ADC. The baseband amplifiers also include 55dB of rejection at 1.92MHz which is a typical ADC image frequency. This combined with at least 40dB of external rejection from the IF filter provides adequate rejection to meet blocking requirements. Please note that the ADC Image response frequency varies with the ADC clock frequency. The image response has a fixed relationship to the clocks i.e. Baseband Clock divided by 10 (see Figure 24); so for a 8kbit/s system the image response is at 1.92MHz but at 960kHz for a 4kbit/s system. For multi-rate systems care is required to ensure the blocking / spurious response rejection performance is met under all conditions.

Frequency Offset	**Radio Modem Mode** (2 Pole Filter Recommended)	**EN 300 113 Mode** (4 Pole Filter Recommended)
12.5 kHz	10dB	30dB
25 kHz	15dB	30dB
50 kHz	25dB	50dB
100 kHz	25dB	50dB
1 MHz to 10 MHz	40dB	50dB
Pass band ($\geq \pm$3.5 kHz)	3dB Typical	3dB Typical

Note: Attenuation relative to the pass band (with the exception of the pass band specification)

Table 3 IF Filter Requirements,12.5kHz channel spacing

The ADC are sigma delta types providing high dynamic range and adjacent channel rejection (see Figure 39). Internal DC offset correction is provided to maximise the useable range. After the ADC demodulation is provided along with RSSI/AGC algorithms. RSSI is available from a register. AGC can be controlled automatically or manually. The baseband section also provides AFC measurement. Results are available to the host and can be used (via Aux DAC 1) to control an external reference oscillator.

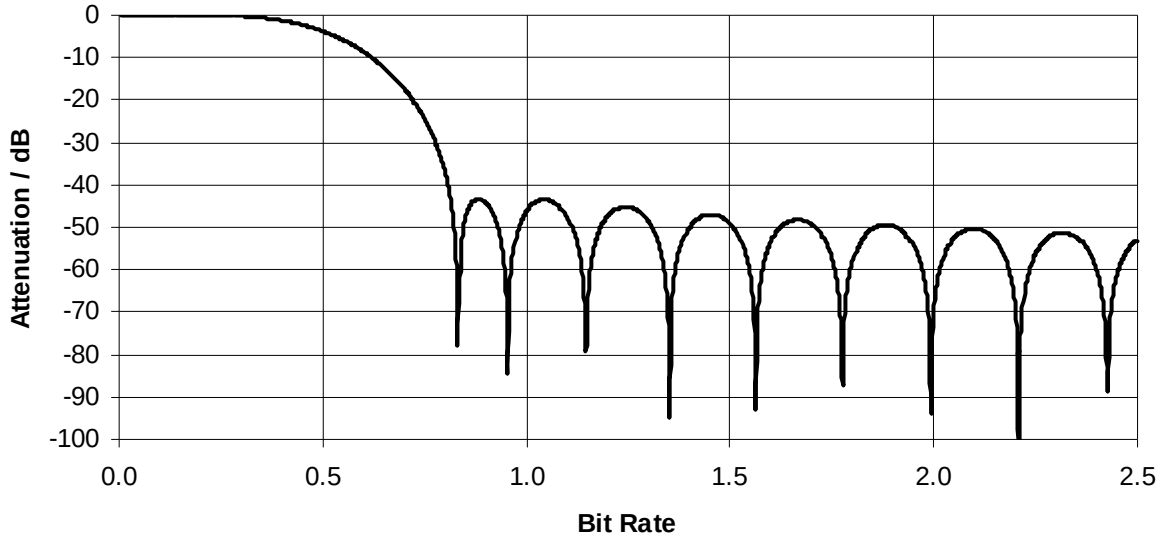


Figure 39 Baseband filter response scaled as a function of bit rate (e.g. for 8kbit/s 1.0 = 8kHz)

To design a complete receiver system using the CMX990 it is recommended that an analysis is made of receiver parameter such as overall noise figure, intermodulation performance etc. These factors need to be considered along with adjacent channel rejection, blocking and spurious responses discussed above. A typical gain, noise figure and intermodulation partition is shown in Table 4 which assumes the filter performance specified in Table 3. The partition uses suggested performance for external 'front end' stages. The calculated results show a noise figure of 8.3dB.

					CMX990 Stages				
		Switch & Filter	LNA	BPF	1st Mixer	IF Filter	AGC/iq	Digital Filter	Output
Stage specifications:									
Gain	(dB)	-1.8	15.0	-3.0	-1.4	-3.0	63.0	0.0	0.0
NF	(dB)	1.8	1.2	3.0	15.0	3.0	8.5	0.0	0.0
i/p IP	(dBm)	40.0	0.0	40.0	9.5	40.0	-44.0	99.0	99.0
i/p cp	(dBm)	30.0	-10.0	30.0	-7.0	30.0	-54.0	99.0	99.0
Cumulative response:									
preGain	(dB)	0.0	-1.8	13.2	10.2	8.8	5.8	68.8	68.8
Cum NF	(dB)	8.3	6.5	20.0	17.0	11.5	8.5	0.0	0.0
i/p Te	(%)	9.0	8.5	0.8	51.3	2.3	28.1	0.0	0.0
Cum IP	(dBm)	-1.3	-3.1	12.5	9.5	33.9	-44.0	97.5	99.0
i/p IM	(%)	0.0	24.0	0.0	76.0	0.0	0.0	0.0	0.0

Table 4 Typical Gain / Noise Figure / Intermodulation Partition for CMX990

Considering the detail of Table 4 the 'ip Te (%)' is the percentage of the overall receiver noise figure, calculated as a noise temperature, contributed by each stage. It will be seen that the largest contribution comes from the 1st mixer (51.3%). To improve sensitivity therefore increasing the gain before the 1st mixer will be very effective in reducing the overall receiver noise figure. Such a change will have a significant effect on the intermodulation performance however as the 'i/p IM (%)' shows that 76% of the intermodulation in the system is coming from the 1st mixer stage. The 'Cum IP (dBm)' is the third-order intercept point calculated for the input of each stage including the effect of all the following stages, so the

value in the 'Switch & Filter' column would be the value observed looking into the receiver; the value in the '1st mixer' column would be that measured looking into the CMX990. Note these values and calculations are only valid for the design based on the stage specifications given in Table 4 however they should give a useful indication of key areas that control the performance of the overall system.

Input level (dBm)	BER %
-107	0
-110	0.005
-113	0.16
-115	0.525
-116	0.98
-117	1.365

Table 5 Sensitivity Results for CMX990 System (8kbps)

6.5.1.1 Frequency Planning

Frequency planning for the CMX990 is a complex issue as requirements of both transmitter and receiver must be considered. The choice of IFs is limited however and this tends to reduce the options to a manageable number. A typical frequency plan is shown in Figure 17 and some further typical configurations in Table 6.

Rx band (MHz)		Tx band (MHz)		Rx IF	Sign	Rx LO (MHz)		Tx IF	IF Div	Tx LO (MHz)		LO Range
Bottom	Top	Bottom	Top	(MHz)	bit Rx	Bottom	Top	(MHz)	Setng	Bottom	Top	(MHz)
935	941	896	902	45	High	1960	1972	84	/2	1960	1972	12
864	870	819	825	45	High	1818	1830	90	/2	1818	1830	12
850	864	814	819	45	High	1790	1818	81-90	/2	1790	1818	28
426.6	429.5	416.6	419.5	45	Low	763.2	769	40	/4	753.2	759	15.8
453.1	453.4	459.6	459.9	45	High	996.2	996.8	40	/4	999.2	999.8	3.6

Table 6 Possible Frequency Plan for CMX990 in some common frequency bands

Some points to consider when choosing frequencies are:

- 45MHz Tx/Rx Offset: With a a 45MHz Tx/Rx offset transmit and receiver operation can be achieved without needing to re-tune the main local oscillator by using a 90MHz Tx IF (as shown in Figure 17).
- PLL Lock Range: It is often advisable to minimise main PLL tuning range (see section 6.5.1.2). One way of do this is to adjust the frequency of the IF PLL between Tx and RX (as suggested in Table 6). The IF PLL is usually less critical in terms of phase noise and can have a relatively high comparison frequency (e.g. 100kHz compared to 12.5kHz for the main PLL) making lock time and spurious performance easier to achieve.
- Tx Spurs: The O-PLL transmitter will generate spurs close to harmonics of it's IF, for example if 45MHz Tx IF is used operation close to 450MHz should be avoided.
- Rx Spurious Responses: Like all receivers the CMX990 will have some spurious responses, the most obvious being the image response but also half IF response, higher order LO / IF products etc. The designer must take care to evaluate and test responses for a particular frequency plan. One response that the CMX990 architecture avoids is the 2nd image response due to the use of 'zero IF' in the second conversion.
- The Receiver IF: The image reject mixer works best at 45MHz however due to spurious responses it is sometimes necessary to move this. Keeping the IF as close a possible to 45MHz is recommended. (Note: In some areas TV Carriers on 45MHz can be problematic, in these areas a move to 45.0125MHz IF has proved sufficient to avoid the interference).

6.5.1.2 Phase Noise

Like all radio designs the phase noise of the local oscillators plays an important role in the overall system performance with a CMX990 design. In order for the receiver to meet adjacent channel rejection requirements, the phase noise of the local oscillator in the adjacent channel must be better that the rejection requirement, by a reasonable margin, otherwise the process of reciprocal mixing will limit overall performance. The same process applies to spurious response rejection and blocking.

One factor to consider when calculating phase noise is the CMX990 main LO is divided by two prior to the mixer. This will provide a theoretical 6dB improvement in phase noise (the improvement in practice is close to this figure, typically in the range 5-6dB).

The phase noise requirements for the Aux LO are generally less stringent as the 1st IF filter provides protection. For a thorough receiver design a detailed partition of filtering requirements and phase noise is recommended, an example of which is shown in Table 7. A full explanation of this is beyond the scope of this datasheet however note that from the highlighted numbers the other values can be calculated. The effect of phase noise is observed by the fact the actual selectivity is much less than the amount of filtering provided in the receiver – the IF filter provided 30dB and the baseband 48dB (78dB total) however the signal to noise margin with a +60dB interferer (-47dBm to –107dBm) is only 0.8dB. Using this calculation method we find that with the given LO phase noises, the Adjacent channel rejection would be just over 62dB. This could be degraded further if intermodulation in the IF stages contributes to the total interference power. Some additional margin has been allowed as the Target S/N is quoted as 12dB wereas the actual limit of 1% BER is 11.5dB (section 6.5.5).

Specification Limit	-47.0	dBm
Wanted Signal Level	-107.0	dBm
Target S/N	12.0	dB
Normal S/N	17.0	dB
Noise Bandwidth	8000.0	kHz
Thermal Noise	-124.0	dBm
Relative Atteuatiuon Requirement	-72.0	dB
Selectivity at RF Input	-78.0	dB
RF Filter Relative Attenuation	0.0	dB
Selectivity at Mixer #1 Input	-78.0	dB
LO1 Phase Noise Margin	6	dB
LO1 Sideband Noise Ratio	-78.0	dB
LO1 SSB Phase Noise Density	-117.0	dBc/Hz
Total Noise at output of Mixer #1	-121.5	dBm
Selectivity at 1st IF Input	-78.0	dB
S/N at Mixer #1 Output	14.5	dB
1st IF Filter Selectivity	-30.0	dB
Selectivity at Mixer #2 Input	-48.0	dB
LO2 Phase Noise Margin	20	dB
LO2 Sideband Noise Ratio	-62.0	dB

LO2 SSB Phase Noise Density	-101.0	dBc/Hz
Selectivity at 2nd IF Input	-48.0	dB
Total Noise at output of Mixer #2	-121.4	dBm
Total Interference at output of Mixer #2	-125.0	dBm
S/N at Mixer #2 Output	12.8	dB
2nd IF Selectivity	0.0	dB
Baseband Digital Filter Attenuation	-48.0	dB
S/N Margin	**0.8**	**dB**

Table 7 Example Phase Noise Partition

6.5.2 DC Calibration

The signal levels in the receiver are small, typically only a few mV at sensitivity. For the demodulator algorithms to work correctly the DC offset must be reduced well below the level of the signal. To do this the CMX990 has two stages of DC correction. The first stage allows an analogue correction to be applied prior to the ADC (see Figure 40), the offset value being controlled from registers $18 and $19 (section 5.3.7). This allows the analogue signals prior to the ADC stage to have an error of less than 0.5mV. This maximises the dynamic range available from the ADC. The second element of DC offset correction is based on averaging the received signal. This is done as part of the demodulator section and the correction is applied by adding/subtracting the measured DC offset to the received data samples.

DC offsets can be corrected by turning off the 'front end' circuitry (Figure 40) and measuring the remaining signal then applying an appropriate correction. This process can be carried out automatically by the CMX990 via the Command register ($01, bit 6). An output control signal is provided from the chip to enable/disable the external LNA with appropriate timing. The disabling of the 'front end' is beneficial as it should ensure that no signal is present while DC offsets are being estimated. This is crucial in allowing a fast estimate of offsets as if signal is present the modulation can not be guaranteed not to have DC content, furthermore large signals introduce large potential errors when trying to estimate a precise DC value. By contrast noise, if measured over a suitable period, will have a mean value very close to the DC offset value. The result of any measurement of noise will vary somewhat: a longer measurement time will improve the accuracy. The CMX990 algorithm has been selected to give a good combination of speed and accuracy for typical bit rates. The automatic sequence is shown in section 5.3.4.3 (repeated below). During the 'Tracking' phase a first measurement of the error is taken and correction applied to the hardware 'Coarse Correction' registers. With this correction applied the fine correction is measured. After 25 bits the receiver 'front end' is enabled and the results of the calibration process are then used to correct the received signal prior to digital demodulation.

- Reset (equivalent of RESET Task in command register)
- Turn off Receiver 'front end'
- Run with Tracking for 25 bits to correct I/Q offset errors
- Turn on receiver 'front end' and apply offset
- Revert to normal setting (hold / fine / coarse)

On completion of the automatic sequence it is recommended that either the 'fine' or 'hold' modes are used. The 'hold' mode uses the measured calibration and does not update. This might be appropriate if the received data has extremely long sequences of 1's or 0's. Normally best results are achieved with the 'fine' tracking were the CMX990 will automatically measure and update the fine DC offset values. It should be noted that the algorithm used in 'fine' mode is intelligent and differentiates between signal and noise and applies an appropriate correction. The time constant of the algorithm is such that imbalanced data sequences should not effect the DC correction significantly.

When using the 'Coarse Tracking' mode the values of the 'Coarse Offset' registers are updated automatically while this mode is enabled. The 'Fine Offset' values are not updated during this mode, the algorithm resuming from it's last state when fine track is next enabled.

If no offset correction is required the 'Reset and Hold' mode should be used. This will set the 'Coarse' and 'Fine' offsets to zero.

The 'Coarse DC Offset' value can be read by the host and values can also be written by the host (see section 5.3.7) . This allows the host to 'remember' values for a particular hardware setting, for example a particular channel, which can then be written back to the CMX990 next time that setting is used. This allows operation on a channel without needing to run the full DC offset correction process. Access to the 'fine' offset values is not currently supported.

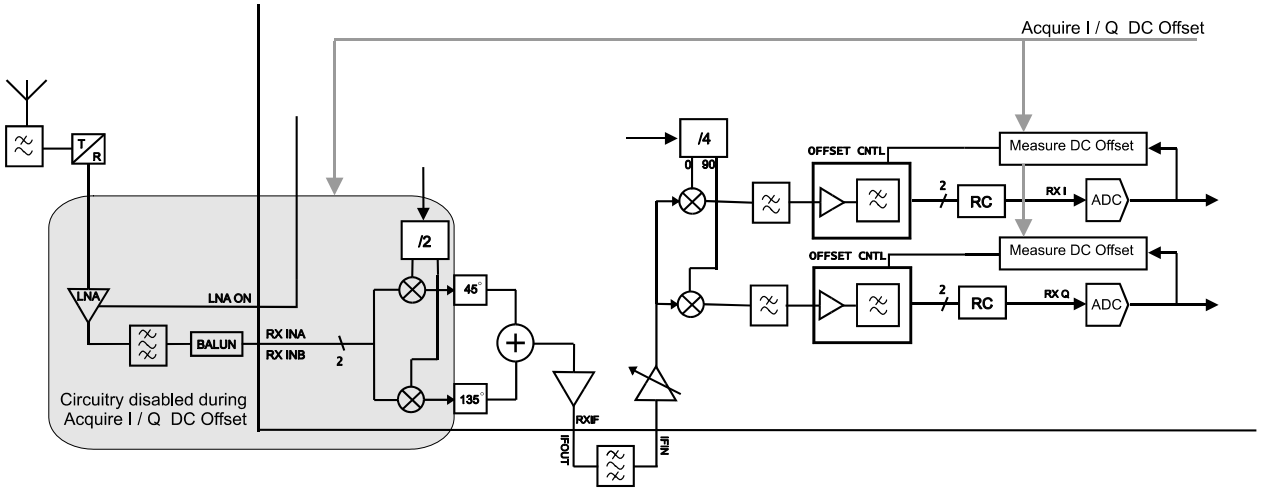


Figure 40 DC Offset Correction Scheme

6.5.3 Matching

Typical matching arrangements are given in section 4. This section gives some additional information that might be helpful to designers.

6.5.3.1 IF Output

Typical impedance of the IF output port is 290 – j138 Ω at 45MHz. A typical output match to 50Ω is shown in Figure 41.

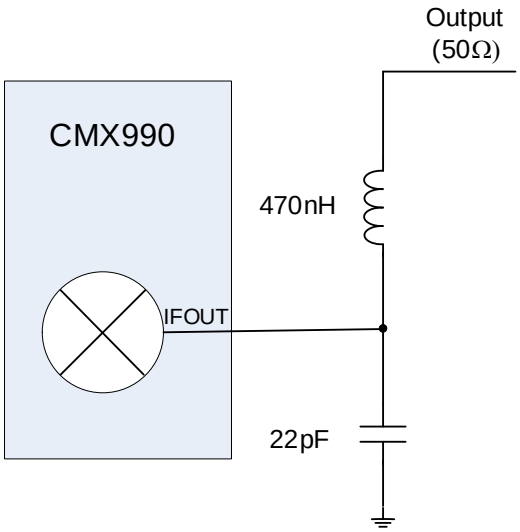


Figure 41 Mixer output (IFOUT) Matching

6.5.3.2 IF Input

Typical impedance of the IFIN port is approximately 4kΩ in parallel with 3.5pF at 45MHz. For test purposes it is useful to match the IFIN stages to 50Ω. This can be achieved with the match shown in Figure 42 IF Input Matching

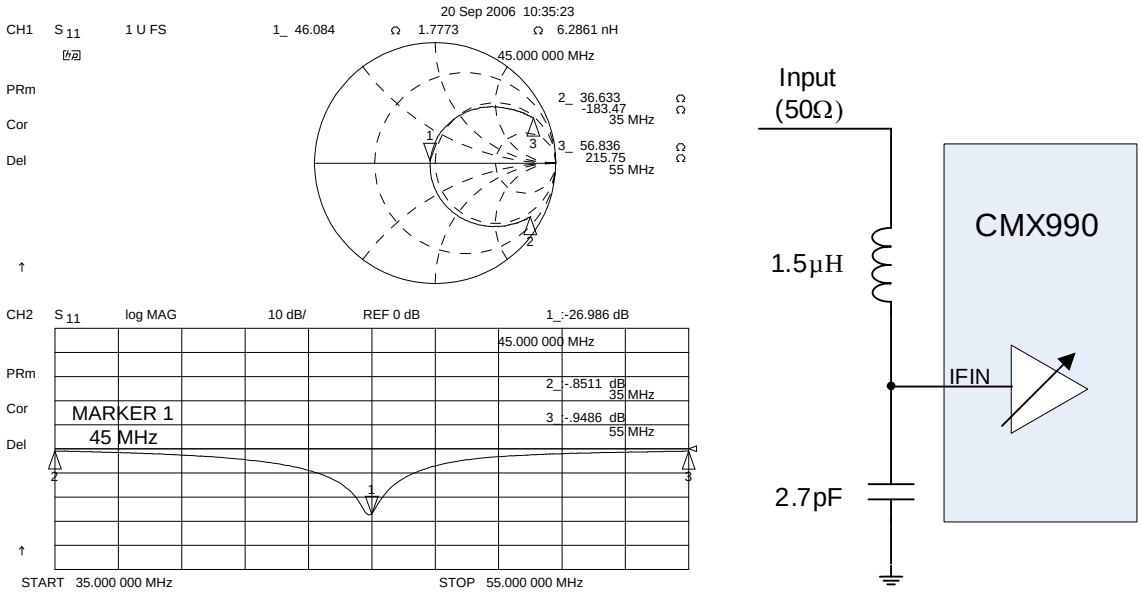


Figure 42 IF Input Matching

6.5.4 Rx Mixer Options

The receive mixer in the CMX990 is an image reject type allowing a reduction in external filtering thus allowing a minimum cost solution. Certain radio modem products may require better inter-modulation performance than can be achieved with the image reject architecture. In this case an external mixer is

recommended and to simplify external circuits the CMX990 incorporates a bypass switch for the transmit loop local oscillator divide-by-2. This allows the CMX990 transmit local oscillator to be re-used in an external mixer. When an external mixer is used, the power consumption can be reduced by disabling the circuits controlled by the RxF1 and RxF2 bits in the Power Up 1 register ($04). A typical configuration is shown in Figure 43.

In this mode the main LO and the Tx frequency are relatively close. Careful attention in the PCB design should be paid to isolation between LO and Tx sections to avoid interference between the two sections.

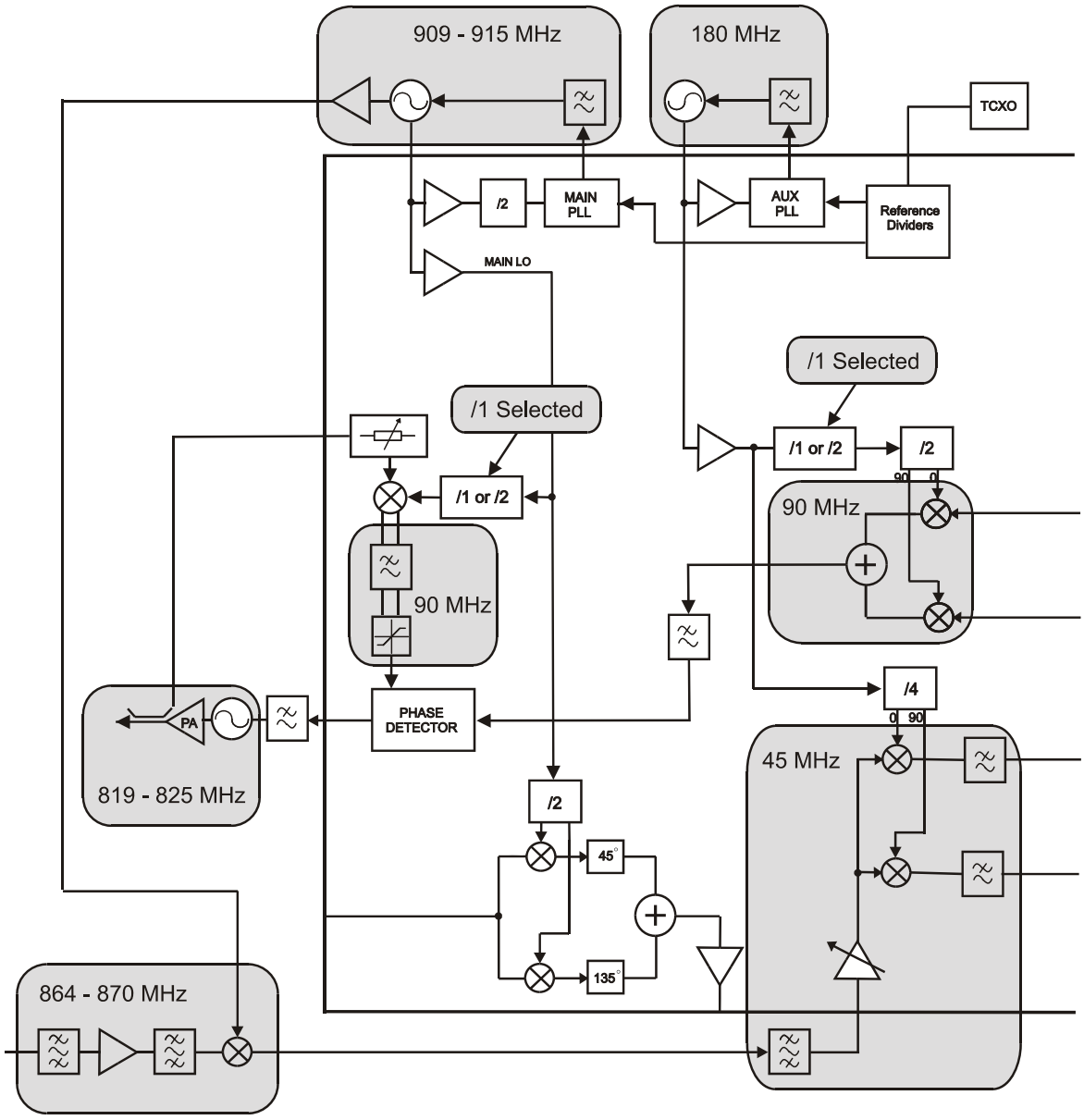


Figure 43 Block Diagram of CMX990 Showing use of External Receive Mixer

6.5.5 Signal to Noise

The performance of the receiver is based on the signal to noise performance of the demodulator. This achieves a bit error rate of 1 in 100 at 11.5dB signal-to-noise. Performance is shown in Figure 44 which also shows performance degrades a little with the addition of a crystal IF filter (dashed line).

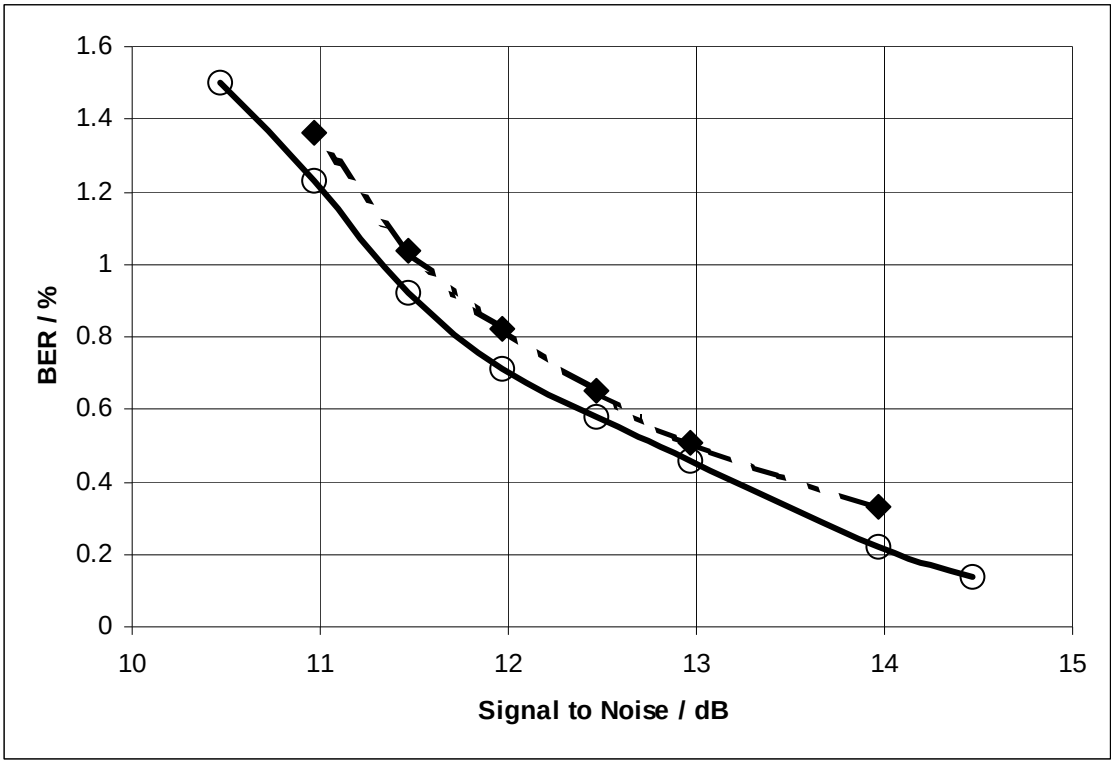


Figure 44 BER vs Signal-to-Noise for CMX990 with and without an IF Filter

6.5.6 Dynamic Range, RSSI and AGC

The CMX990 has a built in AGC algorithm. Programmable gain has 4 steps of 15dB (i.e -5dB, +10dB, +25dB and +40dB). It is beneficial to allow as large an operating window as possible as the AGC has a certain amount of hysteresis allowing the signal to rise more than 15dB before the gain is backed off.

The CMX990 measures the signal level in baseband. This information is used to control the AGC but is also available via the control interface. If AGC is being controlled by the host RSSI need to be correct as described in section 5.3.7. If AGC is being control by the CMX990 the value of the RSSI value reported is automatically corrected for the AGC value in use at the time.

Detail descriptions of the operation of the RSSI are given in sections 5.3.12.2 and 5.3.8.6.

6.5.6.1 Dynamic Range

The dynamic range of the receiver must be partitioned between various requirements. Key to this is the dynamic range of the ADC within IC that converts the I/Q signals into the digital domain. These converters have a dynamic range of at least 85dB. This must be partitioned between various factor such as filtering headroom, signal noise, quantisation noise margin etc. leaving an operating window. The proposed partition is shown in Figure 45. Other partitions are possible depending on adjacent channel requirements, external filtering, external gains etc.

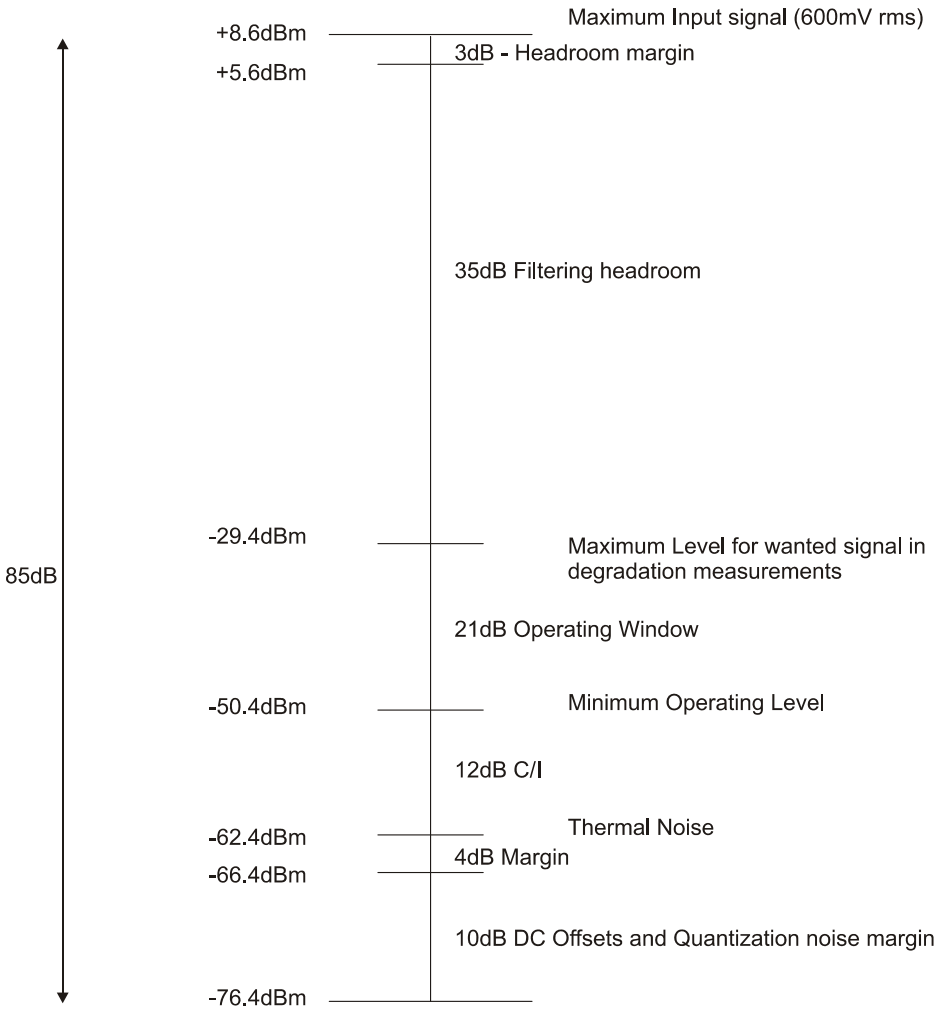


Figure 45 ADC Input Dynamic Range Partition

6.5.6.2 Listen Before Talk

A number of radio system use 'Listen Before Talk' (LBT) operation, for example this is specifically referenced in EN 300 220. Although LBT algorithms may take many forms EN 300 220 specifies specific listening periods and requirements. The minimum listening time is 5ms however the default averaging time for RSSI on the CMX990 is much longer than this (64ms). The averaging time can be reduced to 0.5ms (see section 5.3.8.6) which is convenient as the random part of the listing time if the channel is occupied, should be in 0.5ms steps.

6.5.7 Signal Processing

The CMX990 includes the demodulation functions, these are implemented digitally. Algorithms are consistent with Mobitex mobile burst timing structure and requirements. The received waveform can be inverted to allow high side or low side mixing in the receiver (see section 5.3.4.4, note this is separate and additional to the facility to invert the operation of the image reject mixer in the receiver section 5.3.9) It will be noted that when powered up, the CMX990 needs to acquire base channel. The baseband has been optimised to achieve this while also giving minimum power consumption in normal operation (i.e. maximum sleep times).

7 Performance Specification

7.1 Electrical Performance

7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Unit
Supply (V_{DDH} - V_{SSH} and V_{DDVCO} - V_{SSH} only)	-0.3	4.0	V
Supply (All other V_{DD} - V_{SS})	-0.3	3.0	V
Voltage on any pin to V_{SSH}	-0.3	V_{DD} + 0.3	V
Current into or out of any V_{DD} or V_{SS} pin	-100	+100	mA
Current into or out of any other pin	-20	+20	mA
Voltage between any two V_{SS} pins	-0.3	+0.3	V
Voltage between any two V_{DD} pins (except V_{DDH})	-0.3	+0.3	V

Q1 Package	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at T_{AMB} = 25 °C	–	3500	mW
... Derating above 70 °C	–	35.0	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

7.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DDH} - V_{SSH})		3.0	3.6	V
Supply (V_{DDVCO} - V_{SSH})		3.0	3.6	V
Supply (All other V_{DD} - V_{SSH})		2.25	2.75	V
Voltage difference between supplies:				
V_{DDH} to V_{DDVCO}		0	±0.2	V
Between all other V_{DD}		0	±0.2	V
All V_{SS} to V_{SSH}		0	±50	mV
Operating Temperature		-40	+85	°C
Clock Frequency	1	3.8	24	MHz
Bit rate	1	4000	16000	bits/sec

Notes: 1 Error in RF and IF frequencies and bit rate is directly related to the clock frequency.

7.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

Clock Frequency = 19.2MHz, Bit Rate = 8k bits/sec, Noise Bandwidth = Bit Rate,
V_{DDH} = V_{DDVCO} = 3.0V to 3.6V, all other supplies 2.25V to 2.75V, T_{AMB} = -40°C to +85°C.

	Notes	Min.	Typ.	Max.	Unit
DC Parameters					
I_{DD} (powersaved) at V_{DDH} = 3.3V	2	–	50	200	µA
Total Tx I_{DD} (V_{DDH} = 3.3V)	2,9	–	137	–	mA
Total Rx I_{DD} (V_{DDH} = 3.3V)	2,9	–	148	–	mA
Individual supply currents:					
V_{DD} VCO (synths in lock, RX mode)	2,7	–	1	–	mA
V_{DD} VCO (synths and TX loop in lock)	2,8	–	24	–	mA
V_{DD} ANA (in Rx mode)	2	–	8	–	mA
V_{DD} ANA (inTx mode)	2	–	5	–	mA
V_{DD} DIG (in Rx mode)	2,7,9	–	13	–	mA
V_{DD} DIG (in Tx mode)	2,8,9	–	7	–	mA
V_{DD} Synth	2,7,8	–	20	–	mA
V_{DD} Rx1	2	–	73	–	mA
V_{DD} Rx2	2	–	33	–	mA
V_{DD} Tx	2	–	81	–	mA
AC Parameters					
Clock Input					
'High' pulse width	3	20	–	–	ns
'Low' pulse width	3	20	–	–	ns
Signal amplitude		0.5	–	–	V p-p
Input impedance (at 19.2 MHz)		20	–	–	kΩ
µC Interface					
Input logic "1" level	4, 5	80%	–	–	V_{DDH}
Input logic "0" level	4, 5	–	–	20%	V_{DDH}
Input leakage current (Vin = 0 to V_{DDH})	2, 4, 5	-5.0	–	+5.0	µA
Input capacitance	4, 5	–	10	–	pF
Output logic "1" level (I_{OH} = 120 µA)	5	90%	–	–	V_{DDH}
Output logic "0" level (I_{OL} = 360 µA)	5, 6	–	–	10%	V_{DDH}
'Off' state leakage current (Vout = V_{DDH})	2, 6	–	–	10	µA

Notes:
2. Tamb = 25°C, not including any current drawn from the device pins by external circuitry.
3. Timing for the external input to the CLOCK pin.
4. WRN, RDN, CSN, A0 - A5 pins.
5. D0 - D7 pins.
6. IRQN pin.
7. For 420MHz Rx operation, main ADC and AuxDAC1 enabled, 14.4MHz reference.
8. For 425MHz TX operation, sending a PRBS sequence (TSO). Main DAC, AuxDAC0 and AuxDAC1 enabled, 14.4MHz reference.
9. For 9.6k bits/sec, BT=0.5 operation with a 14.4MHz clock (i.e. internal clock PLL enabled, see 5.3.10), using an EV9900A evaluation kit.

	Notes	Min.	Typ.	Max.	Unit
AC Parameters					
Rx 1st Mixer					
Input frequency range		200	–	950	MHz
Local oscillator frequency range	11	700	–	2000	MHz
IF output frequency		44	45	46	MHz
Gain	10	–	0.5	–	dB
Input third order intercept point		–	+8	–	dBm
Noise Figure	17,18		13		dB
Image rejection		–	33	–	dB
Output impedance		–	350 // 4.5	–	Ω / pF
Output noise voltage	13	–	4.9	–	nV/√Hz
Half IF Response	15	–	60	–	dB
Rx IF Stages					
Input frequency range		44	45	46	MHz
Input third order intercept (Max Gain)	16	–	-30	–	dBm
Input impedance		–	4000 / 3.7	–	Ω / pF
Noise figure		–	7	–	dB
Maximum gain (Max AGC)	16	–	63	–	dB
Minimum gain (Min AGC)	16	–	18	–	dB
AGC step size		–	15	–	dB
AGC step size accuracy		–	±1	–	dB
Selectivity at ±1 to 10 MHz		50	–	–	dB
Selectivity at ±1.92 MHz (ADC Alias)	12	65	–	–	dB
I/Q image rejection		–	30	–	dB
Local oscillator range	14	176	180	184	MHz
RSSI output			Digital		

Notes:
10. Gain shown is for a matched 50Ω source, however the input is high impedance and transformer or equivalent voltage step-up circuits can be used to achieve a higher gain figure. If such arrangements are used input third order intercept point will be degraded.
11. A divide by 2 is provided within the IC.
12. ADC Alias dependant on clock bit rate (see section 6.5.1).
13. Level predicted from simulation.
14. IC contains divide by 4.
15. Test with receiver frequency of 867MHz, IF of 45MHz giving half IF response at 889.5MHz (i.e. 867 + 22.5MHz).
16. Measured with 47 ohm resistor between pin IFIN and ground.
17. Noise Figure quoted is based on measured data when evaluated as a DSB noise figure however it will be noted that the input match provides a degree of selectivity so the result is something approaching the SSB noise figure of the mixer. The result is the correct (practical) value for use in most receiver designs.
18. Configuration as Figure 7.

	Notes	Min.	Typ.	Max.	Unit
AC Parameters (continued)					
Tx Offset Mixer					
Input frequency range		200	–	950	MHz
Local oscillator frequency range	24	700	–	2000	MHz
IF output frequency		40	–	90	MHz
Input level		-57	–	+10	dBm
Tx Limiter/Modulator/Phase Detector					
Input frequency range		40	–	90	MHz
Combined rms phase error		–	1.5	–	deg
Combined peak phase error		–	4.5	–	deg
Charge pump output current		–	±1.0	–	mA
Normal input level	22	-35	–	-10	dBm
Total limiting range	22	-91	–	-10	dBm
IF input frequency	23	160	–	180	MHz
Tx Offset-Phase Locked Loop					
Minimum input level 45MHz IF	20	–	-57	–	dBm
Minimum input level 90MHz IF	20	–	-57	–	dBm
Maximum input level		–	–	+10	dBm
Lock time	21	–	200	–	µs

Notes:
20. Input value at TX FB pin (TX O-PLL mixer input); Tx Attenuator setting = 0dB
21. Lock time depends on loop filter, Tx IF frequency, VCO tuning gain etc. Value stated measured for 45MHz with 250kHz Tx loop bandwidth.
22. Normal input level is the range over which phase error performance is specified. The total limiting range is an extended range, the lower end of which is intended to allow the Tx loop to “lock up” during power up.
23. TX LO chain has selectable divide by 2 or divide by 4.
24. A divide by 2 is provided within the IC.

	Notes	Min.	Typ.	Max.	Unit
Auxiliary ADC					
Resolution		–	10	–	bits
Input range	30	–	–	10 to 90	% V_{DD} Ana
Auxiliary DAC	31				
Resolution		–	10	–	bits
Output range		–	–	10 to 90	% V_{DD} Ana
Phase Locked Loop					
Reference Input					
Frequency	34	–	6 to 20	–	MHz
Level	32	0.5	–	–	Vp-p
Divide ratios	33	1	–	8192	
Main RF Synthesizer					
Comparison frequency		–	–	500	kHz
Input frequency range		600	–	2000	MHz
Input level		-20	–	-10	dBm
Divide ratios		1024	–	104857 5	
Charge pump current		–	±2.5	–	mA
Normalised SSB phase noise		–	-152	–	dBc/Hz
Aux IF Synthesizer					
Comparison frequency		–	100	600	kHz
Input frequency range		150	–	250	MHz
Input level		-20	–	-10	dBm
Divide ratios		2	–	16383	
Charge pump current		–	±2.5	–	mA
Normalised SSB phase noise		–	-144	–	dBc/Hz

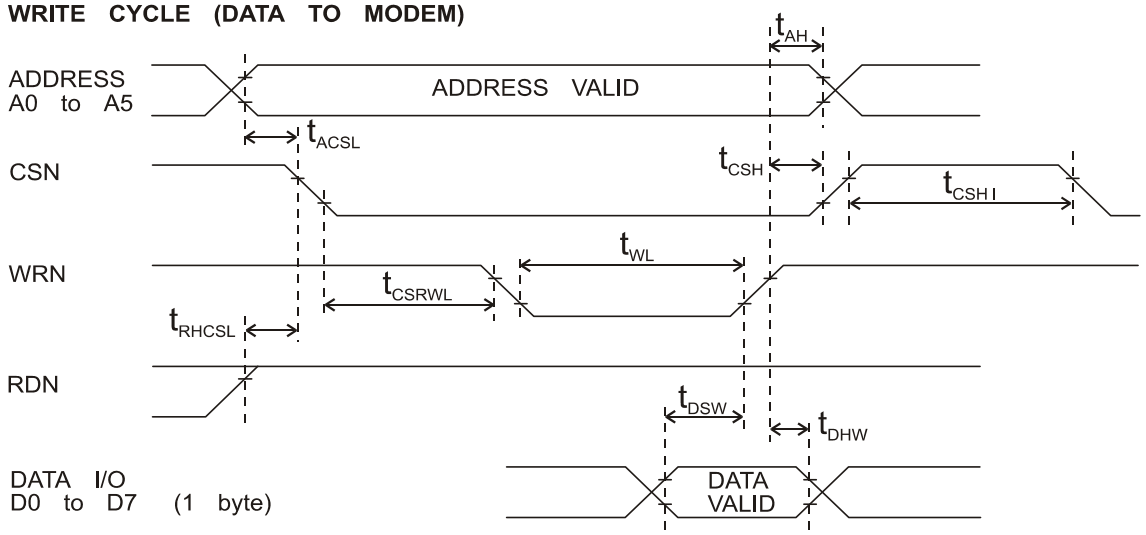
Notes:

30. Aux ADC 2 and 3 have uncommitted op-amps on the input.
31. Aux DAC 0 provides a power ramp for the PA, based on a user-programmable ramp table. Aux DAC 1 should be connected to VCXO (or VCTCXO) for AFC control.
32. Sine wave or clipped sine wave.
33. Separate dividers provided for RF and IF PLL's.
34. 14.4 MHz and 19.2 MHz are commonly used.

Operating Characteristics (continued)

Timing Diagrams

WRITE CYCLE (DATA TO MODEM)



READ CYCLE (DATA FROM MODEM)

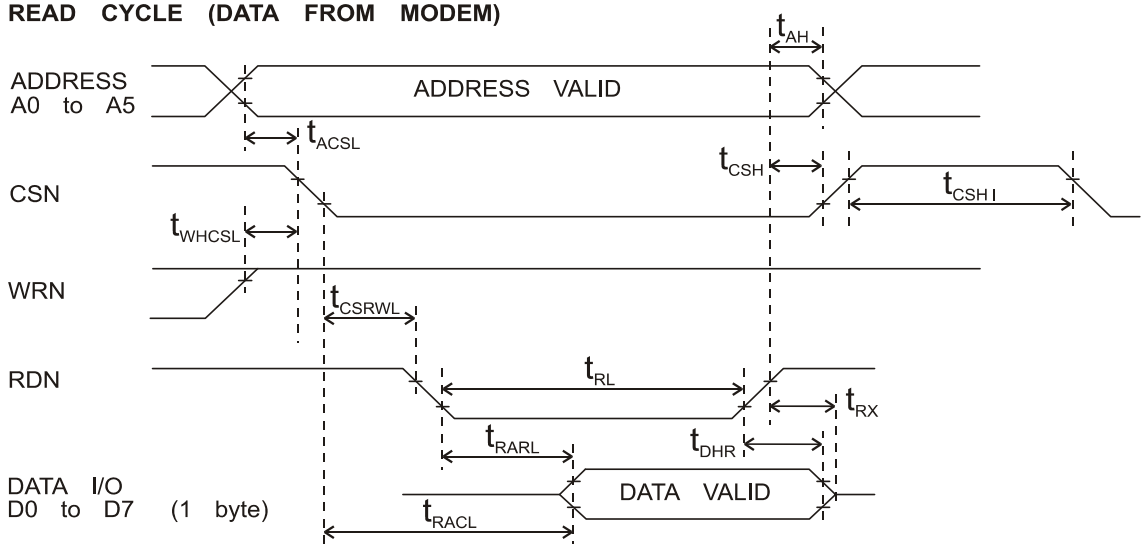


Figure 46 µC Parallel Interface Timings

For the following conditions unless otherwise specified:

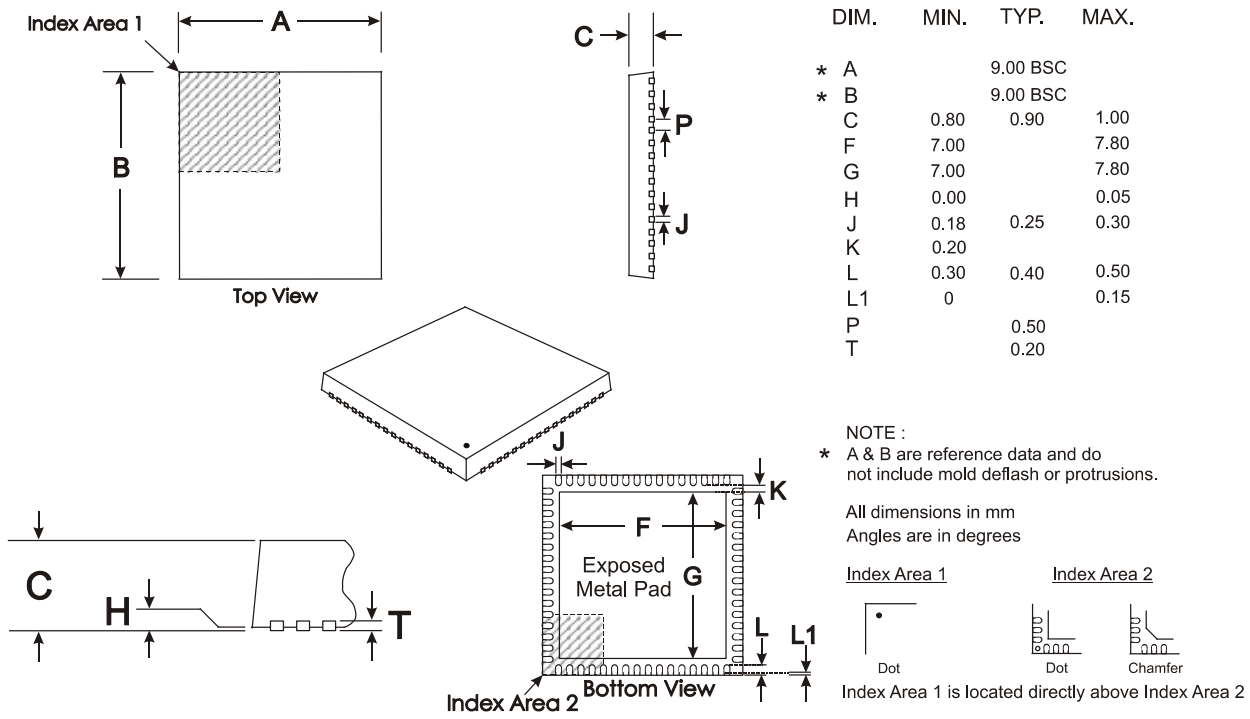
Clock Frequency = 19.2MHz, V_{DDH} = 3.0V to 3.6V, T_{AMB} = -40°C to +85°C.

		Notes	Min.	Typ.	Max.	Unit
Parallel Interface Timings (ref. Figure 46)						
t_{ACSL}	Address valid to CSN low time		0	–	–	ns
t_{AH}	Address hold time		10	–	–	ns
t_{CSH}	CSN hold time		0	–	–	ns
t_{CSHI}	CSN high time		6	–	–	clock cycles
t_{CSRWL}	CSN to WRN or RDN low time		0	–	–	ns
t_{DHR}	Read data hold time		0	–	–	ns
t_{DHW}	Write data hold time		0	–	–	ns
t_{DSW}	Write data setup time		90	–	–	ns
t_{RHCSL}	RDN high to CSN low time (write)		0	–	–	ns
t_{RACL}	Read access time from CSN low	40	–	–	175	ns
t_{RARL}	Read access time from RDN low	40	–	–	145	ns
t_{RL}	RDN low time		200	–	–	ns
t_{RX}	RDN high to D0-D7 3-state time		–	–	50	ns
t_{WHCSL}	WRN high to CSN low time (read)		0	–	–	ns
t_{WL}	WRN low time		200	–	–	ns

Notes:

40. With 30pF max to V_{SS} on D0 - D7 pins. Data valid at greater of: t_{RARL} + t_{CSRWL} or t_{RACL}.

7.2 Packaging



DIM.	MIN.	TYP.	MAX.
* A		9.00 BSC	
* B		9.00 BSC	
C	0.80	0.90	1.00
F	7.00		7.80
G	7.00		7.80
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30	0.40	0.50
L1	0		0.15
P		0.50	
T		0.20	

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Notes:

1. In this device, the underside of the Q1 package should be electrically connected to the analogue ground. The circuit board should be designed so that no unwanted short circuits can occur.
2. As package dimensions may change after publication of this datasheet, it is recommended that you check for the latest Packaging Information from the Datasheets page of the CML website: [www.cmlmicro.com].

Figure 47 Q1 Mechanical Outline: *Order as part no. CMX990Q1*

Handling precautions: This product includes input protection, however, precautions should be taken to prevent device damage from electro-static discharge. CML does not assume any responsibility for the use of any circuitry described. No IPR or circuit patent licences are implied. CML reserves the right at any time without notice to change the said circuitry and this product specification. CML has a policy of testing every product shipped using calibrated test equipment to ensure compliance with this product specification. Specific testing of all circuit parameters is not necessarily performed.

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