



T-58-11-31
CS-2842A/CS-3842A
CS-2843A/CS-3843A

CS-3842A/3843A SERIES

CURRENT MODE PWM CONTROL CIRCUIT

4

DESCRIPTION

The CS-3842A provides all the necessary features to implement off-line fixed frequency current-mode control with a minimum number of external components.

The CS-3842A family incorporates a new precision temperature-controlled oscillator with an internally trimmed discharge current to minimize variations in frequency. A precision duty-cycle clamp eliminates any need for an external oscillator when at, or near, a 50% duty-cycle condition. Duty-cycles greater than 50% are also possible. Special logic ensures that V_{ref} is stabilized before the output stage is enabled. Non-implant resistors provide tighter control of under-voltage lockout.

Other features include low start-up current, pulse-by-pulse current limiting, and a high-current totem pole output for driving capacitive loads, such as the gate of power MOSFET. The output is low in the off state, consistent with N-channel devices.

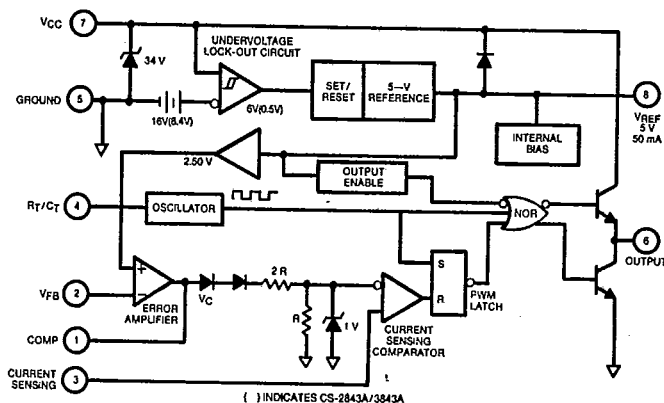
The CS-3842A series of current-mode control ICs are available in 14-pin and 16-pin "SO" package for surface mount applications as well as 8 pin PDIP and 8 pin CDIP.

ORDERING INFORMATION

PART NO.	0°C to 70°C	-25°C to 85°C	PACKAGE
CS-3842AN	*		8LP DIP
CS-3842AD	*		14LSO
CS-3842ADW	*		16L SO WIDE
CS-2842AJ	*		8LG DIP
CS-2842AN	*		8LP DIP
CS-2842ADW	*		16L SO WIDE

PART NO.	0°C to 70°C	-25°C to 85°C	PACKAGE
CS-3843AN	*		8LP DIP
CS-3843AD	*		14L SO
CS-3843ADW	*		16L SO WIDE
CS-2843AJ	*		8LG DIP
CS-2843AN	*		8LP DIP
CS-2843ADW	*		16L SO WIDE

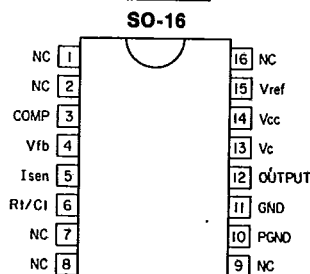
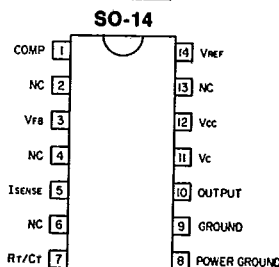
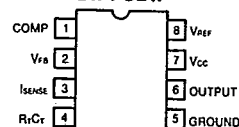
BLOCK DIAGRAM



FEATURES:

- Optimized for off-line control
- Internally trimmed temperature compensated oscillator
- Maximum duty-cycle clamp
- V_{ref} stabilized before output stage is enabled
- Low start-up current
- Pulse-by-pulse current limiting
- Improved U/V lockout
- Double pulse suppression
- 1% trimmed bandgap reference
- High current totem pole output

PIN CONNECTIONS



T-58-11-31

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($I_{CC} < 30\text{mA}$) Self Limiting
 Supply Voltage (Low Impedance Source) 30V
 Output Current $\pm 1\text{A}$

Output Energy (Capacitive Load) 5 μJ
 Analog Inputs (Pin 2, Pin 3) -0.3V to V_{CC}
 Error Amp Output Sink Current 10mA

ELECTRICAL SPECIFICATIONS: Unless otherwise stated, specifications apply for $-25 \leq T_A \leq 85^\circ\text{C}$
 for CS-2842A/2843A, $0 \leq T_A \leq 70^\circ\text{C}$ for CS-3842A/3843A. $V_{CC} = 15\text{V}$ (Note 1);
 $R_T = 680\Omega$, $C_T = 0.22\mu\text{F}$ for triangular mode, $R_T = 10\text{K}$, $C_T = 3.3\text{nF}$ for sawtooth mode (see Fig. 3)

PARAMETER	TEST CONDITIONS	CS-2842A CS-2843A			CS-3842A CS-3843A			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	

Reference Section

Output Voltage	$T_J = 25^\circ\text{C}$, $I_O = 1\text{mA}$	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	$12 \leq V_{IN} \leq 25\text{V}$		6	20		6	20	mV
Load Regulation	$1 \leq I_O \leq 20\text{mA}$		6	25		6	25	mV
Temp. Stability	(Note 2)		0.2	0.4		0.2	0.4	mV/ $^\circ\text{C}$
Total Output Variation	Line, Load, Temp. (Note 2)	4.90		5.10	4.82		5.18	V
Output Noise Voltage	$10\text{Hz} \leq f \leq 10\text{kHz}$, $T_J = 25^\circ\text{C}$ (Note 2)		50			50		μV
Long Term Stability	$T_A = 125^\circ\text{C}$, 1000 Hrs. (Note 2)		5	25		5	25	mV
Output Short Circuit	$T_A = 25^\circ\text{C}$	-30	-100	-180	-30	-100	-180	mA

Oscillator Section

Initial Accuracy	Sawtooth Mode (see Fig. 3), $T_J = 25^\circ\text{C}$	47	52	57	47	52	57	kHz
	Triangular Mode (see Fig. 3), $T_J = 25^\circ\text{C}$	47	52	57	44	52	60	kHz
Voltage Stability	$12 \leq V_{CC} \leq 25\text{V}$		0.2	1		0.2	1	%
Temp. Stability	Sawtooth Mode $T_{MIN} \leq T_A \leq T_{MAX}$ (Note 2)		5			5		%
	Triangular Mode $T_{MIN} \leq T_A \leq T_{MAX}$ (Note 2)		8			8		%
Amplitude	$V_{PIN 4}$ peak to peak		1.7			1.7		V
Discharge Current	$T_J = 25^\circ\text{C}$	7.8	8.3	8.8	7.4	8.3	9.2	mA
	$T_{MIN} \leq T_A \leq T_{MAX}$	7.5		9.0	7.2		9.4	mA

Error Amp Section

Input Voltage	$V_{PIN 1} = 2.5\text{V}$	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current			-0.3	-1		-0.3	-2	μA
A_{VOL}	$2 \leq V_{CC} \leq 4\text{V}$	65	90		65	90		dB
Unity Gain Bandwidth	(Note 2)	0.7	1		0.7	1		MHz
PSRR	$12 \leq V_{CC} \leq 25\text{V}$	60	70		60	70		dB
Output Sink Current	$V_{PIN 2} = 2.7\text{V}$, $V_{PIN 1} = 1.1\text{V}$	2	6		2	6		mA
Output Source Current	$V_{PIN 2} = 2.3\text{V}$, $V_{PIN 1} = 5\text{V}$	-0.5	-0.8		-0.5	-0.8		mA
V_{OUT} High	$V_{PIN 2} = 2.3\text{V}$, $R_L = 15\text{K}$ to ground	5	6		5	6		V
V_{OUT} Low	$V_{PIN 2} = 2.7\text{V}$, $R_L = 15\text{K}$ to Pin 8		0.7	1.1		0.7	1.1	V

Current Sense Section

Gain	(Notes 3 & 4)	2.85	3	3.15	2.85	3	3.15	V/V
Maximum Input Signal	$V_{PIN 1} = 5\text{V}$ (Note 3)	0.9	1	1.1	0.9	1	1.1	V
PSRR	$12 \leq V_{CC} \leq 25\text{V}$ (Note 3)		70			70		dB
Input Bias Current			-2	-10		-2	-10	μA
Delay to Output	$T_J = 25^\circ$ (Note 2)		150	300		150	300	ns

Output Section

Output Low Level	$I_{SINK} = 20\text{mA}$		0.1	0.4		0.1	0.4	V
	$I_{SINK} = 200\text{mA}$		1.5	2.2		1.5	2.2	V
Output High Level	$I_{SOURCE} = 20\text{mA}$	13	13.5		13	13.5		V
	$I_{SOURCE} = 200\text{mA}$	12	13.5		12	13.5		V
Rise Time	$T_J = 25^\circ\text{C}$, $C_L = 1\text{nF}$ (Note 2)		50	150		50	150	ns
Fall Time	$T_J = 25^\circ\text{C}$, $C_L = 1\text{nF}$ (Note 2)		50	150		50	150	ns
Output Leakage	$V_{CC} = 14\text{V}$, UVLO Active, $V_{PIN 8} = 0$		-0.01	-10		-0.01	-10	μA

Total Standby Current

Start-Up Current			0.5	1		0.5	1	mA
Operating Supply Current	$V_{PIN 2} = V_{PIN 3} = 0\text{V}$, $R_T = 10\text{K}$, $C_T = 3.3\text{nF}$		11	17		11	17	mA
V_{CC} Zener Voltage	$I_{CC} = 25\text{mA}$		34			34		V

Notes: 1. Adjust V_{CC} above the start threshold before setting at 15V.

2. These parameters, although guaranteed, are not 100% tested in production.

3. Parameter measured at trip point of latch with $V_{PIN 2} = 0$.

4. Gain defined as:

$$A = \frac{\Delta V_{PIN 1}}{\Delta V_{PIN 3}}; 0 \leq V_{PIN 3} \leq 0.8\text{V}.$$

T-58-11-31

ELECTRICAL SPECIFICATIONS

PARAMETER	TEST CONDITIONS	CS-2842A			CS-3842A			CS-2843A CS-3843A			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	

Under-Voltage Lockout Section

Start Threshold		15	16	17	14.5	16	17.5	7.8	8.4	9.0	V
Min. Operating Voltage	After Turn On	9	10	11	8.5	10	11.5	7.0	7.6	8.2	V

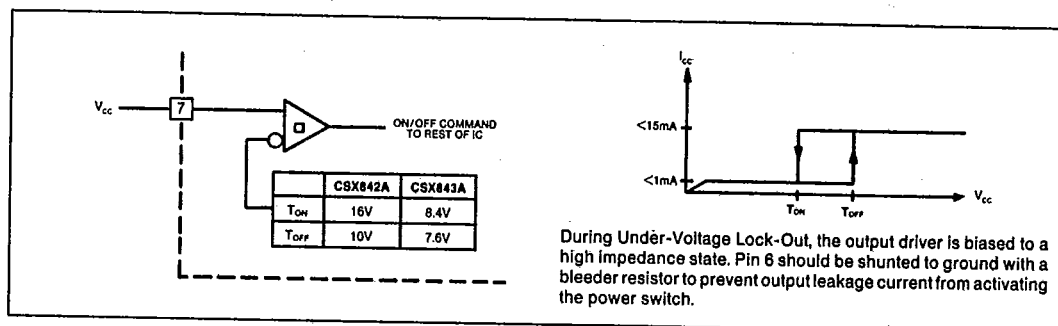


Fig. 1

3842A/3843A TIMING DIAGRAM

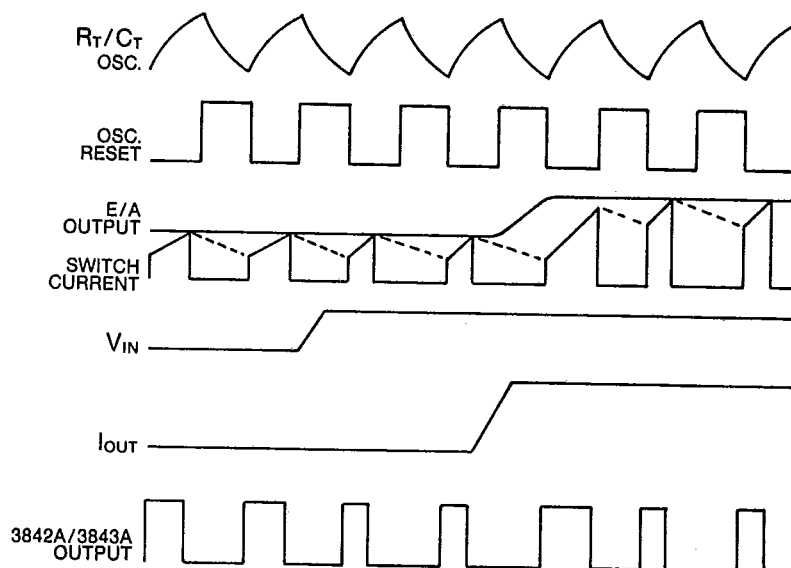


Fig. 2

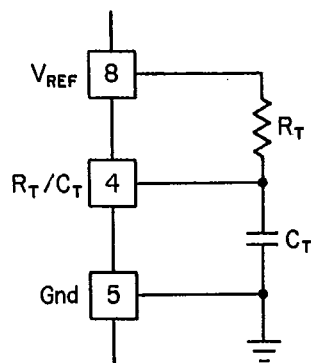
NOTES ON CS3842A/CS3843A TIMING DIAGRAM

To generate the PWM waveform, the control voltage from the error amplifier is compared to a current sense signal which represents the peak output inductor current. An increase in V_{IN} causes the inductor current slope to increase, thus reducing the duty cycle. This is an inherent feed-forward characteristic of current mode control, since the control voltage does not have to change during changes of input supply voltage.

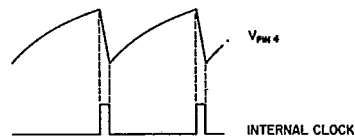
When the power supply sees a sudden large output current increase, the control voltage will increase allowing the duty cycle to momentarily increase. Since the duty cycle tends to exceed the maximum allowed, to prevent transformer saturation in some power supplies, the internal oscillator waveform provides the maximum duty cycle clamp as programmed by the selection of R_T/C_T components.

APPLICATIONS INFORMATION

T-58-11-31



Sawtooth Mode

LARGE R_T ($\approx 10K$)

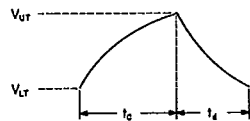
Triangular Mode

SMALL R_T ($\approx 700\Omega$)

Fig. 3

Oscillator timing capacitor, C_T , is charged by V_{REF} through R_T and discharged by an internal current source. During the discharge time, the internal clock signal blanks out the output to the LO

state, thus providing a user selected maximum duty cycle clamp. Charge and discharge times are determined by the general formulas:



$$t_C = R_T C_T \ln \left(\frac{V_{REF} - V_{LT}}{V_{REF} - V_{UT}} \right)$$

$$t_D = R_T C_T \ln \left(\frac{V_{REF} - I_D R_T - V_{UT}}{V_{REF} - I_D R_T - V_{LT}} \right)$$

Assuming typical values for the parameters in the above formulas:

$V_{REF} = 5.0V$, $V_{UT} = 2.7V$, $V_{LT} = 1.0V$, $I_D = 8.3mA$, then

$$t_C \approx .5534 R_T C_T$$

$$t_D \approx R_T C_T \ln \left(\frac{2.3 - .0083 R_T}{4.0 - .0083 R_T} \right)$$

The frequency and maximum duty cycle can be approximately determined from the following graphs

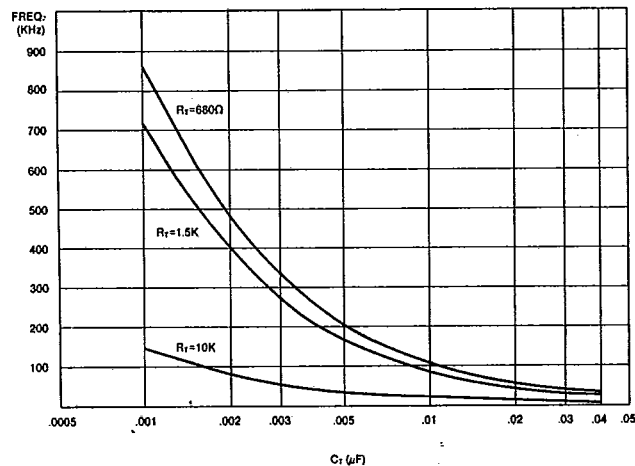
OSCILLATOR FREQUENCY VS. C_T 

Fig. 4

T-58-11-31

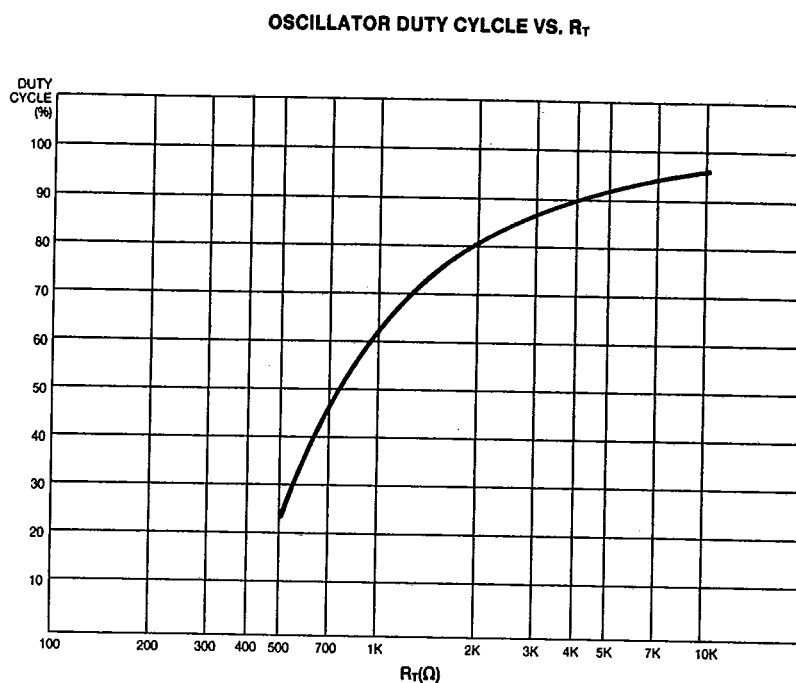
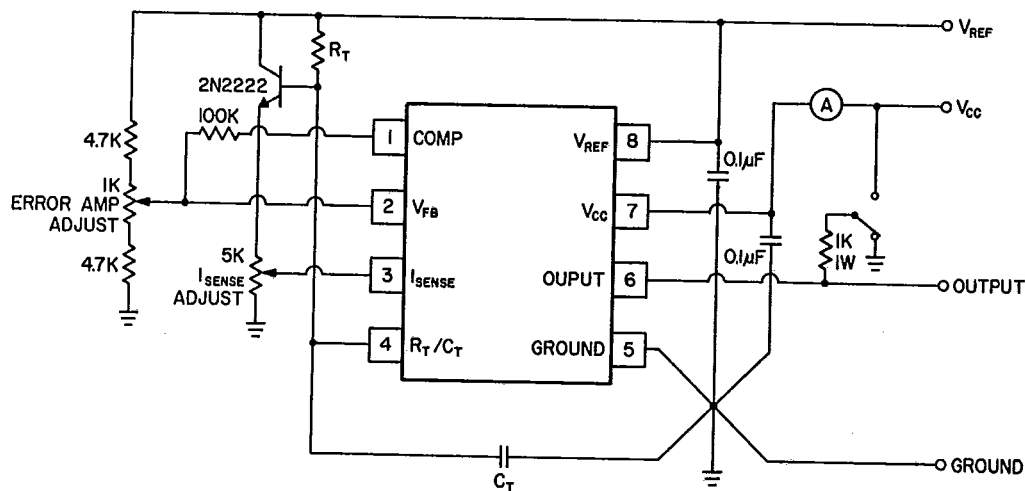


FIG. 5

OPEN-LOOP LABORATORY TEST FIXTURE



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground.

The transistor and 5K potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.