# THOMSON SEMICONDUCTORS

T-75-33-05

# EFB7510

## SINGLE CHIP ASYNCHRONOUS FSK MODEM

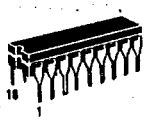
The EFB7510 is a single-chip asynchronous Frequency Shift Keying (FSK) voiceband modem.
Operating at rates up to 75, 150 or 1200 bits per second, it is compatible with the applicable Bell and CCITT recommended standards for 202 and V23 type modems.
This device provides the essential RS-232/CCITT V.24, V.25 and V.54 terminal control signal at TTL levels.

- Monolithic device includes both transmit and receive filters
- Standard low cost crystal (3.579 MHz)
- ± 5 % power supplies : + 5 V, - 5 V
- Separate analog and digital ground pins reduce system noise problems
- Available clock for UART (19.200 Hz)
- Reference voltage internally generated, to avoid noise and supply drift
- Back channel included
- 1.200 bauds, half-duplex two-wire operation or full-duplex four-wire operation
- Fixed compromise line equalizer
- No external precision component needed
- Low power consumption : 100 mW typical
- Direct interface to the THOMSON SEMICONDUCTORS EF6850, UART.

**CMOS**

**SINGLE CHIP ASYNCHRONOUS FSK MODEM**

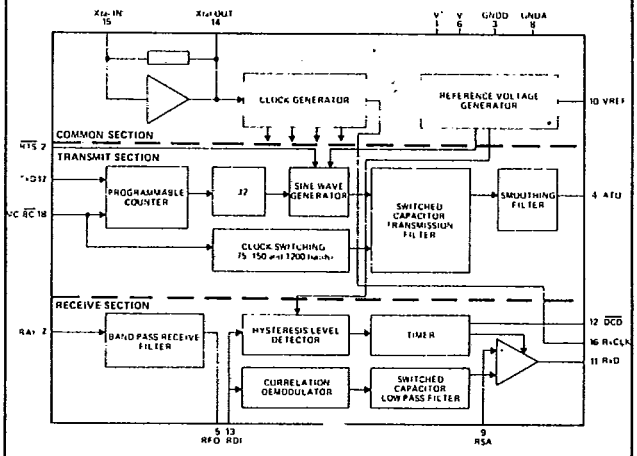
**CASE CB-181**



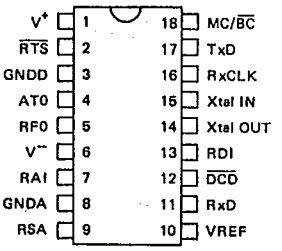

**J SUFFIX**
**CERDIP PACKAGE**

**C SUFFIX**
**CERAMIC PACKAGE**

## BLOCK DIAGRAM




## PIN ASSIGNMENT

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THOMSON COMPONENTS

## ABSOLUTE MAXIMUM RATINGS *

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply voltage | $V^+$ | + 7 V | V |
| Supply voltage | V – | – 7 V | V |
| Analog input range | $V_{in}$ | $V^- \leq V_{IN} \leq V^+$ | V |
| Digital input range (excepted MC/$\overline{BC}$) | $V_I$ | $GNDD \leq V_I \leq V^+$ | V |
| MC/$\overline{BC}$ input range | $V_I$ | $V^- \leq V_I \leq V^+$ | V |
| Operating temperature range | $T_A$ | 0 to 70 | °C |
| Storage temperature range | $T_{stg}$ | - 55 to+ 125 | °C |
| Pin temperature (Soldering, 10 s) | | 260 | °C |

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Standard CMOS handling procedures should be employed to avoid possible damage to device.

## ELECTRICAL OPERATING CHARACTERISTICS

| Parameter | Symbol | Min | Nominal | Max | Unit |
|---|---|---|---|---|---|
| Positive Supply Voltage | V+ | 4.75 | 5.0 | 5.25 | V |
| Negative Supply Voltage | V– | - 5.25 | - 5.0 | - 4.75 | V |
| $V^+$ Operating current | $I_{CC}$ | – | – | 10 | mA |
| $V^-$ Operating current | $I_{BB}$ | - 10 | – | – | mA |

## D.C. AND OPERATING CHARACTERISTICS

($T_A = 0°C$ to + 70°C, $V^+ = + 5\ V \pm 5\ \%$, $V^- = - 5\ V \pm 5\ \%$, GNDA = 0 V, GNDD = 0 V, unless otherwise noted).

### DIGITAL INTERFACE

| Parameter | Symbol | Min | Typ (1) | Max | Unit |
|---|---|---|---|---|---|
| Input Current ($V_{IL\ min} \leq V_I \leq V_{IH\ max}$) | $I_I$ | – | – | 1 | mA |
| Output low level current ( $V_{OL} = 0.4\ V$ ) | $I_{OL}$ | 1.6 | – | – | mA |
| Output high level current ( $V_{OH} = 2.8\ V$ ) | $I_{OH}$ | – | – | - 250 | µA |
| Input low voltage (except MC/$\overline{BC}$) | $V_{IL}$ | GNDD | – | 0.8 | V |
| Input high voltage (except MC/$\overline{BC}$) | $V_{IH}$ | 2.4 | – | $V^+$ | V |
| Input low voltage, MC/$\overline{BC}$ | $V_{IL}$ | $V^-$ | – | - 4 | V |
| Input intermediate voltage, MC/$\overline{BC}$ | $V_{II}$ | GNDD | – | GNDD + 0.8 | V |
| Input high voltage, MC/$\overline{BC}$ | $V_{IH}$ | 2.4 | – | $V^+$ | V |

Note : 1 – Typical values are for $T_A = 25°$ C and nominal power supply values.

**D.C. AND OPERATING CHARACTERISTICS (continued)**

($T_A$ = 0°C to + 70°C, $V^+$ = + 5 V ± 5 %, $V^-$ = 5 V ± 5 %, GNDA = 0 V, GNDD = 0 V, unless otherwise specified)

**ANALOG INTERFACE, RECEIVE FILTER**

| Parameter | | Symbol | Min | Typ (1) | Max | Unit |
|---|---|---|---|---|---|---|
| Input leakage current, (- 3 V < $V_{IN}$ < 3 V) | RAI | $T_{BRI}$ | - | ± 1 | ± 3 | µA |
| Input resistance, | RAI | $R_{IRI}$ | 1 | 3 | – | MΩ |
| Output offset voltage | RFO | $V_{OGSR}$ | – | – | ± 300 | mV |
| Output voltage swing, ($R_L$ ≥ 10 kΩ) | RFO | $V_{ORI}$ | – | – | ± 2 | V |
| Load capacitance, | RFO | $C_{LRI}$ | – | – | 20 | pF |
| Load resistance, | RFO | $R_{LRI}$ | 10 | – | – | kΩ |
| Input voltage swing | | $V_{IRI}$ | - 3 | – | + 3 | V |
| Signal frequency distortion products at maximum signal level | | $C_{DPR}$ | – | - 40 | – | dB |

**ANALOG INTERFACE RECEIVE DEMODULATOR INPUT (RDI)**

| Parameter | Symbol | Min | Typ (1) | Max | Unit |
|---|---|---|---|---|---|
| Input current | $I_{in}$ | -1 | – | 1 | µA |
| Maximum detection level to valid $\overline{DCD}$ output | $N_1$ | 1.1 | 1.3 | 1.5 | V |
| Minimum detection level to valid $\overline{DCD}$ output | $N_2$ | – | 0.92 | – | V |
| Hysteresis effect | N1/N2 | 1.26 | – | 1.6 | |
| | | 2 | 2.9 | 4 | dB |

**ANALOG INTERFACE, RECEIVE SLICER ADJUST (RSA)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input current | $I_{in}$ | - 1 | – | + 1 | µA |
| Input voltage | $V_I$ | $V_{REF}$ | $V_{REF}/2$ | GNDA | V |

**ANALOG INTERFACE, TRANSMIT OUTPUT (ATO)**

| Parameter | | Symbol | Min | Typ (1) | Max | Unit |
|---|---|---|---|---|---|---|
| Output DC offset, ($\overline{RTS}$ connected to $V_{DD}$) | | $V_{OS}$ | – | – | ± 250 | mV |
| Load capacitance | | $C_L$ | – | – | 20 | pF |
| Load resistance | | $R_L$ | 10 | – | – | kΩ |
| Output voltage swing ($R_L$ = 10 kΩ, $C_L$ = 20 pF) | 390 Hz | $V_O$ | 2 | 2.6 | 3.3 | $V_{PP}$ |
| | 450 Hz/390 Hz ampl. ratio | – | - 1 | 0.5 | + 1 | dB |
| | 490 Hz/390 Hz ampl. ratio | – | - 1 | - 0.7 | + 1 | dB |
| | 1300 Hz | $V_O$ | 2 | 2.8 | 3.6 | $V_{PP}$ |
| | 2100 Hz/1300 Hz ampl. ratio | – | - 2.3 | - 1.5 | - 0.7 | dB |
| $\overline{RTS}$ attenuation ratio efficiency | | – | 55 | – | – | dB |

(1) Typical values for $T_A$ = 25°C and nominal power supply values.

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### ANALOG INTERFACE, REGULATED VOLTAGE ($V_{REF}$)

| Parameter | Symbol | Min | Typ (1) | Max | Unit |
|---|---|---|---|---|---|
| Output voltage | $V_{OR}$ | - 2.5 | - 2 | - 1.5 | V |
| Load resistance | $R_{LR}$ | 10 | – | – | kΩ |
| Load capacitance | $C_{LR}$ | – | – | 20 | pF |

(1) Typical values for $T_A$ = 25°C and nominal power supplies values.

## DYNAMIC CHARACTERISTICS

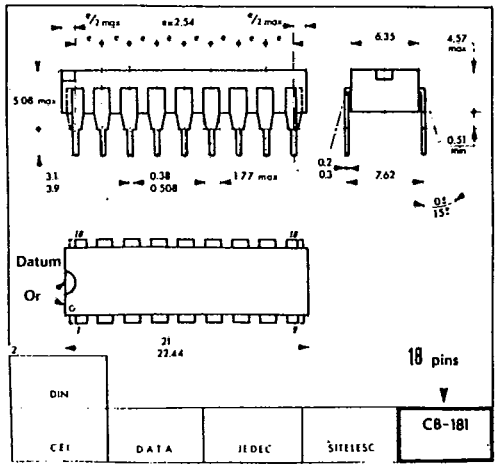
### RECEIVE FILTER TRANSFER CHARACTERISTICS

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Absolute passband gain at 2100 Hz ($V_{RFO}$, $R_L$ = ∞) | | $G_{AR}$ | - 3.2 | - 2.9 | - 2.6 | dB |
| Gain relative to gain at 2100 Hz - Maximum input signal | 380 Hz | $G_{RR}$ | – | - 65 | - 55 | dB |
| | 460 Hz | " | – | - 65 | - 55 | dB |
| | 1100 Hz | " | - 4.7 | - 4.4 | - 4.1 | dB |
| | 2800 Hz | " | - 23 | - 20 | - 17 | dB |
| | 10000 Hz | " | - 10 | - 8.5 | - 7 | dB |

### DIGITAL INTERFACE

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Capacitance | $C_{IB}$ | – | – | 10 | pF |
| Input rise-time, fall-time, measured between 0.8 V and 2.4 V | $t_{THL}$, $t_{TLH}$ | – | 20 | – | ns |
| Output rise-time, fall time between 0.4 V and 2.8 V (1) | $t_{THL}$, $t_{TLH}$ | – | 50 | – | ns |

(1) Driving one 74L or 74LS TTL load plus 30 pF.

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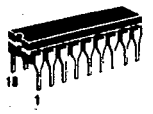

**J SUFFIX**
**CERDIP PACKAGE**

**C SUFFIX**
**CERAMIC PACKAGE**

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## PIN DESCRIPTION

### COMMON SECTION

| NAME | N° | FUNCTION | DESCRIPTION |
|---|---|---|---|
| $V^+$ | 1 | Positive power supply | + 5 V |
| $V^-$ | 6 | Negative power supply | - 5 V |
| GNDA | 8 | Ground | Pin 8 serves as the ground return for the analog circuits of the transmit and receive section. The analog ground is not internally connected to the digital ground. The digital and analog grounds should be tied together as close as possible to the system supply ground. |
| GNDD | 3 | Ground | Pin 3 serves as the digital ground return for the internal clock. The digital ground is not internally connected to the analog ground. The digital and analog grounds should be tied together as close as possible to the system supply ground. |
| Xtal IN | 15 | Oscillator input | This pin corresponds to the input of the inverter of the oscillator. It is normally connected to an external crystal, but may also be connected to a pulse generator. The nominal frequency of the oscillator is 3.579545 MHz. |
| Xtal OUT | 14 | Oscillator output | This pin corresponds to the output of an inverter with sufficient loop gain to start and maintain the crystal oscillating. |
| VREF | 10 | Regulated voltage | This output carries an internally regulated reference voltage. By means of an external potentiometer connected between VREF and GNDA, an adjustable reference voltage may be applied to RSA. The adjustment of RSA is to optimize the discrimination of high and low frequencies of the same channel. The voltage applied to RSA is approximately VREF/2. |

### TRANSMIT SECTION

| | | | |
|---|---|---|---|
| $\overline{RTS}$ | 2 | Request to send | When a low state is present on input $\overline{RTS}$, the EFB7510 delivers on output ATO a sinusoidal signal at a frequency which depends on input TXD. When a high state is present on input $\overline{RTS}$, output ATO is tied to the analog ground. |
| TxD | 17 | Transmit data | This input selects the high frequency or low frequency at the TRANSMITTED CARRIER output pin (ATO) :<br>• a high state selects the low frequency,<br>• a low state selects the high frequency.<br>For correct operation, inputs TxD and MC/$\overline{BC}$ must not be simultaneously low while power-on. |
| MC/$\overline{BC}$ | 18 | Main channel/ back channel | This input selects transmission on the main channel or back channel, and defines the modulation rate, according to European or American standards. (refer to functional description). |
| ATO | 4 | Analog transmit output | When a low state is present on $\overline{RTS}$, the EFB7510 delivers on output ATO a sinusoidal signal centered on the analog ground, with an amplitude of 2.8 V peak to peak. |

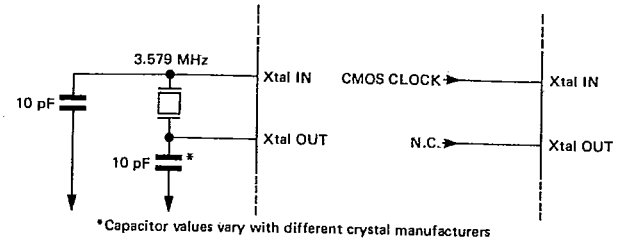
### RECEIVE SECTION

| | | | |
|---|---|---|---|
| RAI | 7 | Receive analog input | Input for analog signals of amplitude lower than 6 V peak to peak and centered on analog ground. |
| RFO | 5 | Receive filter output | This analog output must be connected to a high-pass filter and slicer, with sufficient gain to satisfy the level detection conditions. |

| NAME | N° | FUNCTION | DESCRIPTION |
|---|---|---|---|
| RDI | 13 | Receive demodulator input | This is the input of the demodulator. First, the analog signals are passed through level detection comparators and zero crossing detector. |
| RSA | 9 | Receive slicer adjust | Input of the decision comparator optimizing discrimination between high and low frequencies. |
| $\overline{DCD}$ | 12 | data carrier detect | This output is low when the EFB7510 receives on input RDI a sinusoidal signal with amplitude higher than N1.<br>This output is high when the EFB7510 receives on input RDI a sinusoidal signal with amplitude lower than N2. Within the N1 – N2 range, the detection system presents an hysteresis. |
| RxD | 11 | Receive data | This output is low when a high frequency signal is present on input RDI, and high when a low frequency signal is present on input RDI. Without CARRIER on pin RAI, this output is high. |
| RxCLK | 16 | Receive clock | This output delivers a clock signal, the frequency of which is 16 times of demodulation rate. |

## CLOCK GENERATION

Crystal :
NYMPH, NYP 035A-18




*Capacitor values vary with different crystal manufacturers

## FUNCTIONAL DESCRIPTION

With a minimum number of external components, the EFB7510 performs all the functions of modulation, demodulation and filtering necessary to meet the requirements of CCITT Recommendation V.23 and BELL Standard 202.

This circuit is in four parts :

- a modulator,
- a demodulator,
- a clock generator,
- a reference voltage generator.

Note : The description of the demodulator also covers a subsystem, external to the circuit proper and having the following functions :

- high-pass filter,
- amplification,
- slicer.

### MODULATOR

When input $\overline{RTS}$ is low, output ATO delivers a sinusoidal signal, the frequency of which depends on MC/$\overline{BC}$ and TxD.

### DEMODULATOR

When the analog signal on RDI conforms to certain criteria, output $\overline{DCD}$ detects it and output RxD delivers a digital signal, the logic state of which depends on the analog signal frequency.

### CLOCK GENERATOR

This part of the circuit generates from a 3.58 MHz crystal all the internal clocks necessary to the correct performance of the EFB7510 : ie clocks for the switched capacitor filters as well as those for the sinewave generator. The circuit also delivers on RxCLK a clock needed by the receive UART.

### REFERENCE VOLTAGE GENERATOR

This part of the circuit generates a regulated voltage on VREF which is used to adjust detection thresholds. It is independent of power supply values.

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## FUNCTIONAL CHARACTERISTICS

### MODULATOR

- Modulation conditions:

| $\overline{RTS}$ | ATO |
|---|---|
| "L" | FSK modulated signal |
| "H" | GNDA |

- Transmitted frequencies :
(for details of frequency selection see PIN DESCRIPTION - ATO)

| MC/$\overline{BC}$ | Modulation rate | TxD | R.35 and V.23 Recommendations (Hz) | Frequency generated from a 3.58 MHz crystal | Error (Hz) |
|---|---|---|---|---|---|
| GNDD | 75 bauds | "H"<br>"L" | 390 ± 2<br>450 ± 2 | 389.52<br>450.20 | −0.48<br>+0.20 |
| $V^-$ | 150 bauds | "H"<br>"L" | 390 ± 2<br>490 ± 2 | 389.52<br>489.39 | −0.48<br>−0.61 |
| $V^+$ | 1 200 bauds | "H"<br>"L" | 1 300 ± 10<br>2 100 ± 10 | 1 299.70<br>2 097.40 | −0.34<br>−2.61 |

### DEMODULATOR

- **Frequencies received on RDI**

Analog signals centered on analog ground are received on input RDI. The receive modulation rate is 1 200 bauds.

Frequencies to detect are as follows :

| Modulation rate | Frequencies (Hz) (Recommendation V.23) | Frequencies (Hz) (Recommendation BELL 202) |
|---|---|---|
| 1 200 bauds | 1 300 ± 16<br>2 100 ± 16 | 1 200 ± 16<br>2 200 ± 16 |

- **Level detection conditions**

Input RDI drives a signal detector the output of which ($\overline{DCD}$) is at logic "0" if the level of signal RDI is higher than N1. The output of this detector is at logic "1" if the level of signal RDI is lower than N2. This detector has a hysteresis effect : N1/N2.

- **Timing detection conditions**

The timing performance of the level detector ($\overline{DCD}$) conforms to CCITT Recommendation V.24.

Under normal working conditions, output $\overline{DCD}$ is :

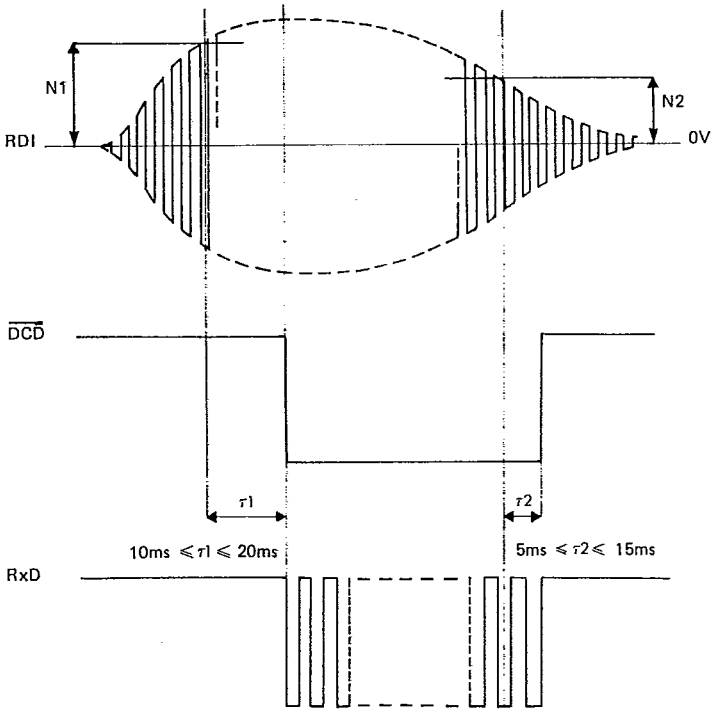
- low if signal RDI conforms to the level detection condition,
- high if signal RDI does not conform to the level detection conditions.

Output $\overline{DCD}$ goes from high to low when signal RDI conforms to the level detection conditions for 20 ms or more.

Output $\overline{DCD}$ does not go from high to low when signal RDI conforms to the level detection conditions for 10 ms or less.

Output $\overline{DCD}$ goes from low to high when signal RDI does not conform to the level detection conditions for 15 ms or more.

Output $\overline{DCD}$ does not go from low to high when signal RDI does not conform to the level detection conditions for 5 ms or less.




- **Demodulated signal**

Under normal working conditions, signal RxD conforms to the following table :

| Level received on RDI | $\overline{DCD}$ | Frequency received on RAI (Hz) | RxD |
|---|---|---|---|
| > N1 | "L" | 1 200 to 2 200 | "X" |
| < N2 | "H" | any | "H" |

- **Clock generator**

The clock generated by the EFB7510 and supplied on output RxCLK must have the following characteristics :

Frequency : 19 200 Hz (± 1 %)
Logic state duration : Compatible to the UART clock specification.

- **Reference voltage generator**

The VREF output carries a regulated reference voltage. An external potentiometer, connected between VREF and GNDA, can supply a regulated voltage to input RSA.

Adjustment of RSA optimizes the discrimination between the high and low frequencies.

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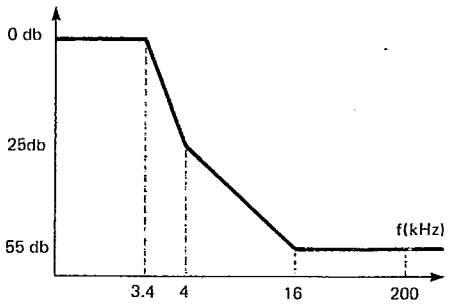
## TYPICAL PERFORMANCES

These typical performances are achieved with the environment described further. (See Annex II).

- **Transmitted spectrum**

The signal transmitted from output ATO conforms to the following specification, whatever the transmitted data:




- **Receiver**

**Measurement conditions**

Local transmit level : −2 dBm on 75 baud back channel. Receive level : −25 dBm, with 511 bit pseudo-random test pattern.

**Isochronous distortion**

Table below shows the typical isochronous distortion values obtained with the EFB7510, which conform to the CCETT specifications for videotex applications. The characteristics of CCETT lines used for measurements are given in Annex I.

| Line | Distortion |
|---|---|
| Line 1 (flat) | 10 % |
| Line 2 | 14 % |
| Line 3 | 12 % |
| Line 4 | 14 % |

**Bit error rate**

The typical bit error rates versus white noise are as follows.

| | S/N | BER |
|---|---|---|
| On line 1 | 6.4 dB | $2.10^{-3}$ |
| On line 2 | 5.5 dB | $2.10^{-3}$ |
| On line 3 | 6.8 dB | $2.10^{-3}$ |
| On line 4 | 6.5 dB | $2.10^{-3}$ |

## ENVIRONMENTAL FUNCTIONAL DESCRIPTION

(See diagram shown next page)

**Transmit section (A)**

The transmit section comprises a single operational amplifier capable of driving a load of 600 Ω, which can also be used to adjust the transmit level.

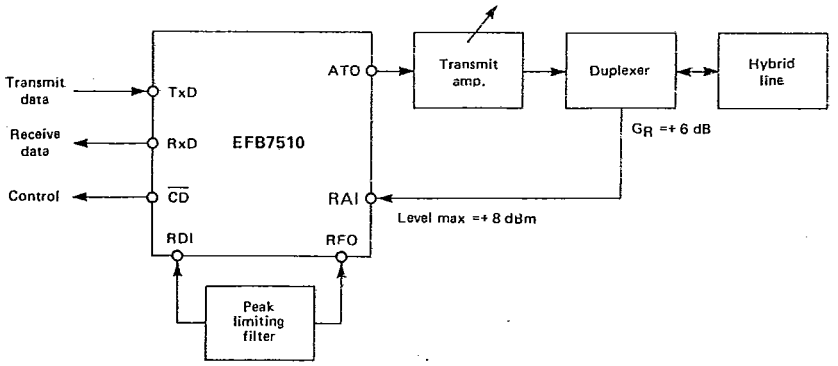
**Duplexer (A)**

This amplifier provides the 2 wire/4 wire separation function and enables a low cost standard non differential transformer (ratio 1:1) to be used. The duplexer principle provides a gain of 6 dB for the received signal.

**Peak-limiting filter**

This section is made of two operational amplifiers and performs three functions :

- peak-limiting amplifier, designed to meet the signal detector levels according to the signal received from the phone line.
- High-pass filter (12 dB per octave) to overcome the DC component of the signal to be demodulated.
- Low-pass filter to protect against the inherent noise of the receive filter.



## CALCULATION OF CIRCUIT ELEMENTS

The following factors must be considered in calculating the external components in the EFB7510 application :

- Signal attenation introduced by the receive filter is 3 dB.
- The maximum permissible level at RAI input is 6 Vpp (+ 8 dBm).

Note : the reference frequency is 2100 or 2200 Hz.

- A 2.5 dB hysteresis is introduced within the two signal detection level N1 and N2, in accordance with CCITT Recommendation V.23.

To be centered, the two limit values of the CARRIER DETECT signal are therefore :

- Upper : - 44.25 dBm, or 13.5 mVpp
- Lower : - 46.75 dBm, or 10 mVpp

- For a correct operation of the EFB7510 signal detector, the peak-limiting filter must remain linear up to - 44 dBm on line.
- At input RDI, the upper threshold level N1 of the signal detector is 3 Vpp (2.7 dBm), and must correspond to the minimum signal level received from the line transformer. With a duplexer reception gain of + 6 dB, the peak-limiting filter gain is defined by :

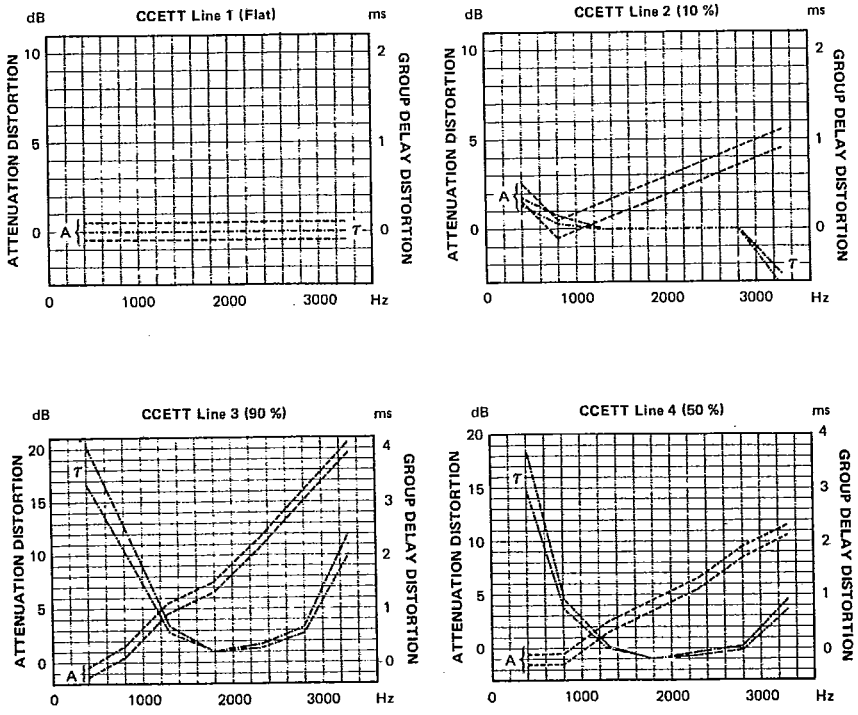
$$A = 44 - 6 + 3 + 2.7 = 43.7 \text{ dB (a ratio of 153)}$$

A typical application of the EFB7510 is shown next page.

Note : The peak-limiting filter gain must be adjusted according to the minimum level on line. With a minimum level of :

- - 38 dBm, A = 37.7 dB
- - 33 dBm, A = 32.7 dB.

## ANNEX I



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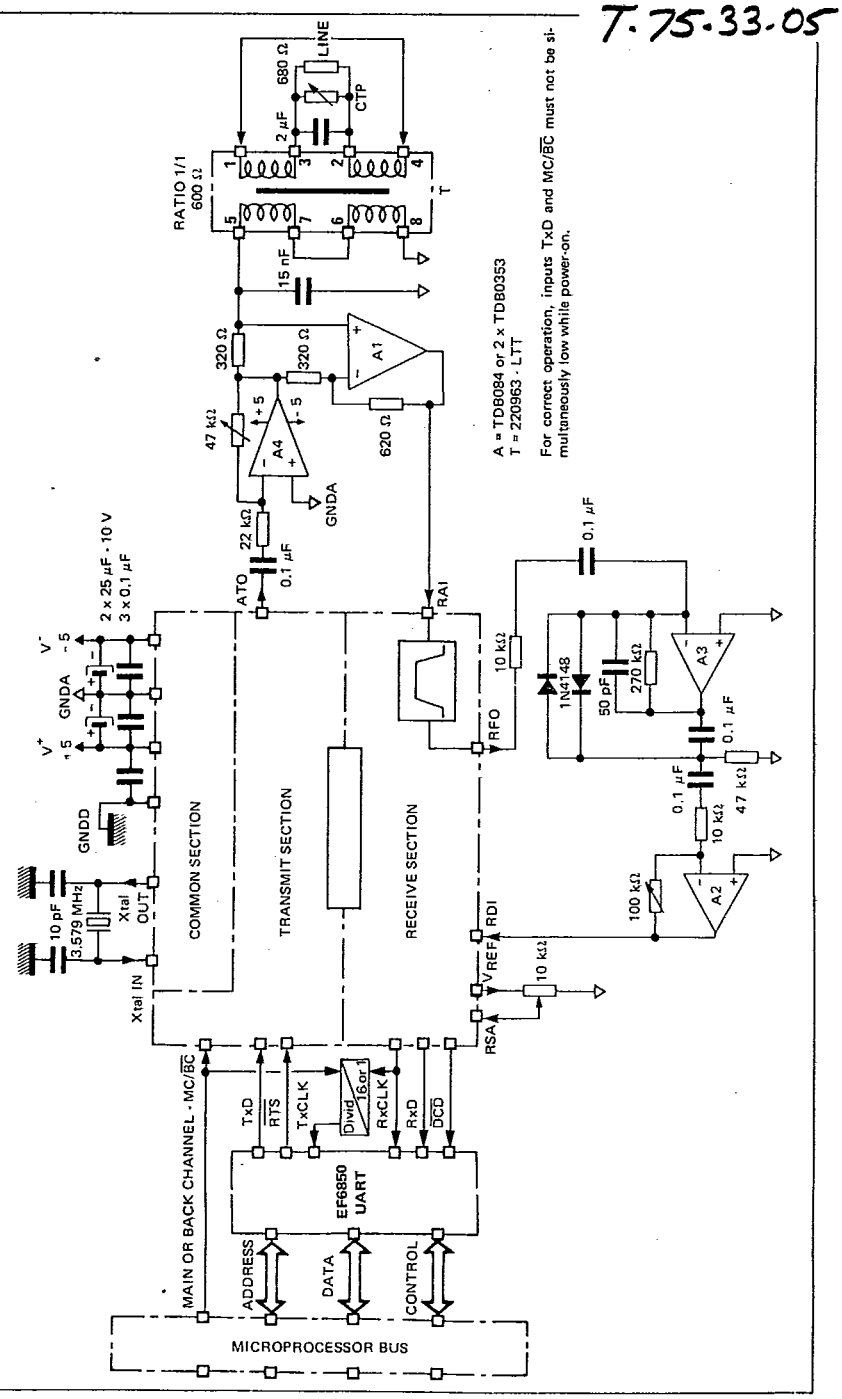
ANNEX II : TYPICAL APPLICATION OF EFB7510

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