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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

EOL product

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RENESAS

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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EOL Product

HD404344R Series/HD404394 Series

Rev. 7.0
Sept. 1999

EOL Product

Description

The HD404344R series and HD404394 series 4-bit microcomputers are products of the HMCS400 series, which is designed to make application systems compact while realizing higher performance and increasing program productivity.

Each microcomputer has an A/D converter, two timers and a serial interface. The HD404344R series includes the HD404344R with on-chip 4-kword ROM, HD404342R with 2-kword ROM, and HD404341R with 1-kword ROM. The HD404394 series includes the HD404394 with on-chip 4-kword ROM, HD404392 with 2-kword ROM, and HD404391 with 1-kword ROM.

The HD4074344 and HD4074394 are the PROM version ZTAT™ microcomputers. Programs can be written to the PROM by a PROM writer, which can dramatically shorten system development periods and smooth the process from debugging to mass production. (The PROM program specifications are the same as for the 27256.)

ZTAT™: Zero Turn Around Time ZTAT is a Trademark of Hitachi Ltd.

Features

- Input/output pins
  - HD404344R series, HD4074344: 22 pins
    (10pins: Large-current I/O pins)
  - HD404394 series: 21 pins
    (3 pins: intermediate-voltage NMOS open drain I/O; 5 pins: NMOS open drain I/O with 15-mA high-current driver)
- Two timer/counters
  - One timer output
  - One event counter input (with programmable edge detection)
- 8-bit clock-synchronous serial interface (1 channel)
- On-chip A/D converter
  - HD404344R series, HD4074344: 8 bit × 4 channel
  - HD404394 series: 8 bit × 3 channel (with V_{ref} pin)
- Built-in oscillator

— HD404344R Series
Ceramic oscillator, CR oscillation, External clock drive is also possible.
— HD404394 Series, HD4074344
Ceramic oscillator, External clock drive is also possible.

- Five interrupt sources
  — One by external source (with programmable edge detection)
  — Four by internal sources
- Subroutine stack
  — Maximum 16 levels including interrupts
- Two low-power dissipation modes
  — Standby mode
  — Stop mode
- One input signal to return from stop mode
- Instruction cycle time
  — 1 µs (f_{OSC} = 4 MHz)

EOL Product

Type of Products

Type	Product Name: HD404344R Series[*1]	Product Name: HD404394 Series	ROM (words)	RAM (digit)	Package
Mask ROM	HD404341RS	HD404391S	1,024	256	DP-28S
	HD40C4341RS				
	HD404342RS	HD404392S	2,048		
	HD40C4342RS				
	HD404344RS	HD404394S	4,096		
	HD40C4344RS				
	HD404341RFP	HD404391FP	1,024		FP-28DA
	HD40C4341RFP				
	HD404342RFP	HD404392FP	2,048		
	HD40C4342RFP				
	HD404344RFP	HD404394FP	4,096		
	HD40C4344RFP				
	HD404341RFT	HD404391FT	1,024		FP-30D
	HD40C4341RFT				
	HD404342RFT	HD404392FT	2,048		
	HD40C4342RFT				
	HD404344RFT	HD404394FT	4,096		
	HD40C4344RFT				
	HCD404344R	——	4,096		Chip[*3 *4]
	HCD40C4344R				
ZTAT™	HD4074344S	HD4074394S	4,096		DP-28S
	HD4074344FP	HD4074394FP			FP-28DA
	HD4074344FT	HD4074394FT			FP-30D

Note: 1. The HD404344R Series is available in a mask ROM version only.
2. ZTAT™ chip shipment is not supprted.
3. The specifications of shipped chips differ from those of the package product. Please contact our sales staff for details.

EOL Product

List of Functions

item		Mask ROM						
		HD404341R	**HD404342R**	**HD404344R**	**HCD404344R**	**HD40C4341R**	**HD40C4342R**	**HD40C4344R**
Operating voltage (V)		2.5 to 5.5	2.5 to 5.5	2.5 to 5.5	2.5 to 5.5	2.5 to 5.5	2.5 to 5.5	2.5 to 5.5
Instruction cycle time (typ.)		1 µs (f_{osc} = 4.0 MHz)	1 µs (f_{osc} = 4.0 MHz)	1 µs (f_{osc} = 4.0 MHz)	1 µs (f_{osc} = 4.0 MHz)	2 µs (R_f = 20 kΩ)	2 µs (R_f = 20 kΩ)	2 µs (R_f = 20 kΩ)
ROM (Words)		1,024	2.048	4,096	4,096	1,024	2,048	4,096
RAM (Digits)		256	256	256	256	256	256	256
I/O		22	22	22	22	22	22	22
	High-current I/O pins (Sink 15 mA max)	10	10	10	10	10	10	10
Timer functions	Free running timer	2	2	2	2	2	2	2
	Reload timer	2	2	2	2	2	2	2
	Event counter	1	1	1	1	1	1	1
	Watchdog timer	1	1	1	1	1	1	1
Serial interface		1	1	1	1	1	1	1
A/D converter		8bit × 4ch	8bit × 4ch	8bit × 4ch	8bit × 4ch	8bit × 4ch	8bit × 4ch	8bit × 4ch
Interrupt	External	1	1	1	1	1	1	1
	Internal	4	4	4	4	4	4	4
Low-power modes		2	2	2	2	2	2	2
	Stop mode	○	○	○	○	○	○	○
	Standby mode	○	○	○	○	○	○	○
Oscillator	Ceramic oscillation	○	○	○	○	—	—	—
	RC oscillation	—	—	—	—	○	○	○
Package		DP-28S FP-28DA FP-30D	DP-28S FP-28DA FP-30D	DP-28S FP-28DA FP-30D	Chip	DP-28S FP-28DA FP-30D	DP-28S FP-28DA FP-30D	DP-28S FP-28DA FP-30D
Guaranteed operation temperature (°C)		–20 to +75	–20 to +75	–20 to +75	+75	–20 to +75	–20 to +75	–20 to +75

EOL Product

List of Functions (cont)

item		Mask ROM HCD40C4344R	ZTAT™ HD4074344
Operating voltage (V)		2.7 to 5.5	2.7 to 5.5
Instruction cycle time (typ.)		2 µs (R_f = 20 kΩ)	1 µs (f_{osc} = 4.0 MHz)
ROM (Words)		4,096	4,096 PROM
RAM (Digits)		256	256
I/O		22	22
	High-current I/O pins (Sink 15 mA max)	10	10
Timer functions	Free running timer	2	2
	Reload timer	2	2
	Event counter	1	1
	Watchdog timer	1	1
Serial interface		1	1
A/D converter		8bit × 4ch	8bit × 4ch
Interrupt	External	1	1
	Internal	4	4
Low-power modes		2	2
	Stop mode	○	○
	Standby mode	○	○
Oscillator	Ceramic oscillation	—	○
	RC oscillation	○	—
Package		Chip	DP-28S FP-28DA FP-30D
Guaranteed operation temperature (°C)		+75	–20 to +75

EOL Product

List of Functions (cont)

		Mask ROM			ZTAT™
item		**HD404391**	**HD404392**	**HD404394**	**HD4074394**
Operating voltage (V)		2.7 to 5.5	2.7 to 5.5	2.7 to 5.5	2.7 to 5.5
Instruction cycle time (typ.)		1 µs (f_{osc} = 4.0 MHz)	1 µs (f_{osc} = 4.0 MHz)	1 µs (f_{osc} = 4.0 MHz)	1 µs (f_{osc} = 4.0 MHz)
ROM (Words)		1,024	2.048	4,096	4,096 PROM
RAM (Digits)		256	256	256	256
I/O		21	21	21	21
	intermediate-voltage NMOS open drain I/O	3	3	3	3
	NMOS open drain I/O (15 mA High current driver)	5	5	5	5
Timer functions	Free running timer	2	2	2	2
	Reload timer	2	2	2	2
	Event counter	1	1	1	1
	Watchdog timer	1	1	1	1
Serial interface		1	1	1	2
A/D converter		8bit × 3ch	8bit × 3ch	8bit × 3ch	8bit × 3ch
Interrupt	External	1	1	1	1
	Internal	4	4	4	4
Low-power modes		2	2	2	2
	Stop mode	○	○	○	○
	Standby mode	○	○	○	○
Oscillator	Ceramic oscillation	○	○	○	○
Package		DP-28S FP-28DA FP-30D	DP-28S FP-28DA FP-30D	DP-28S FP-28DA FP-30D	DP-28S FP-28DA FP-30D
Guaranteed operation temperature (°C)		–20 to +75	–20 to +75	–20 to +75	–20 to +75

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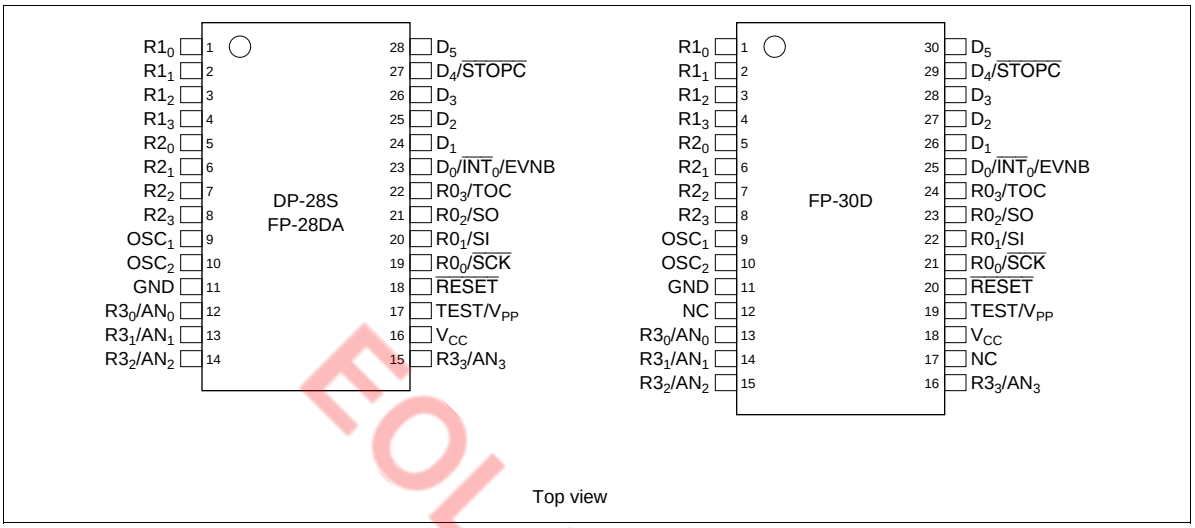
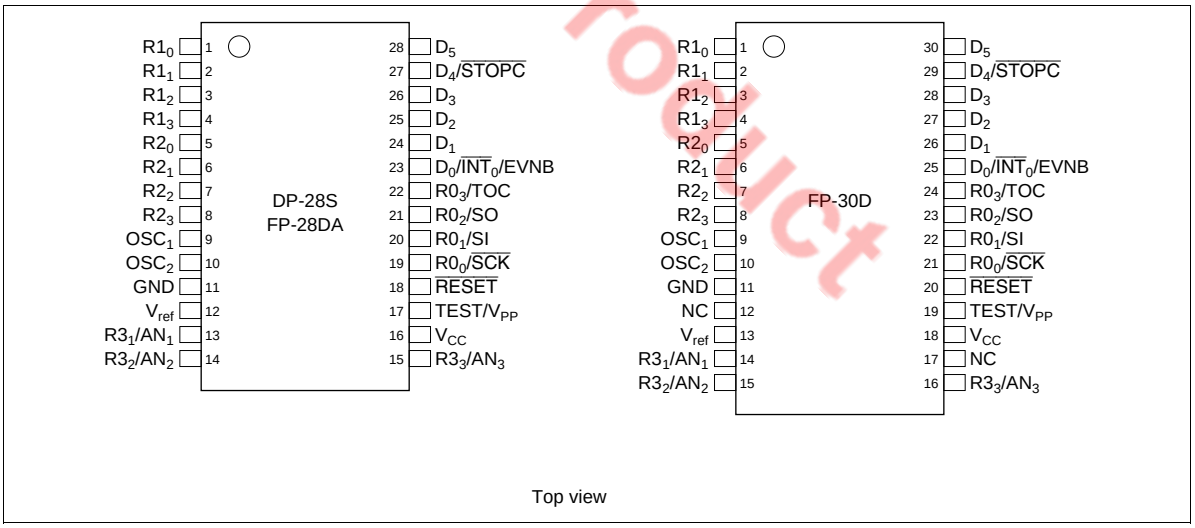
Pin Arrangement

HD404344R Series, HD4074344



HD404394 Series



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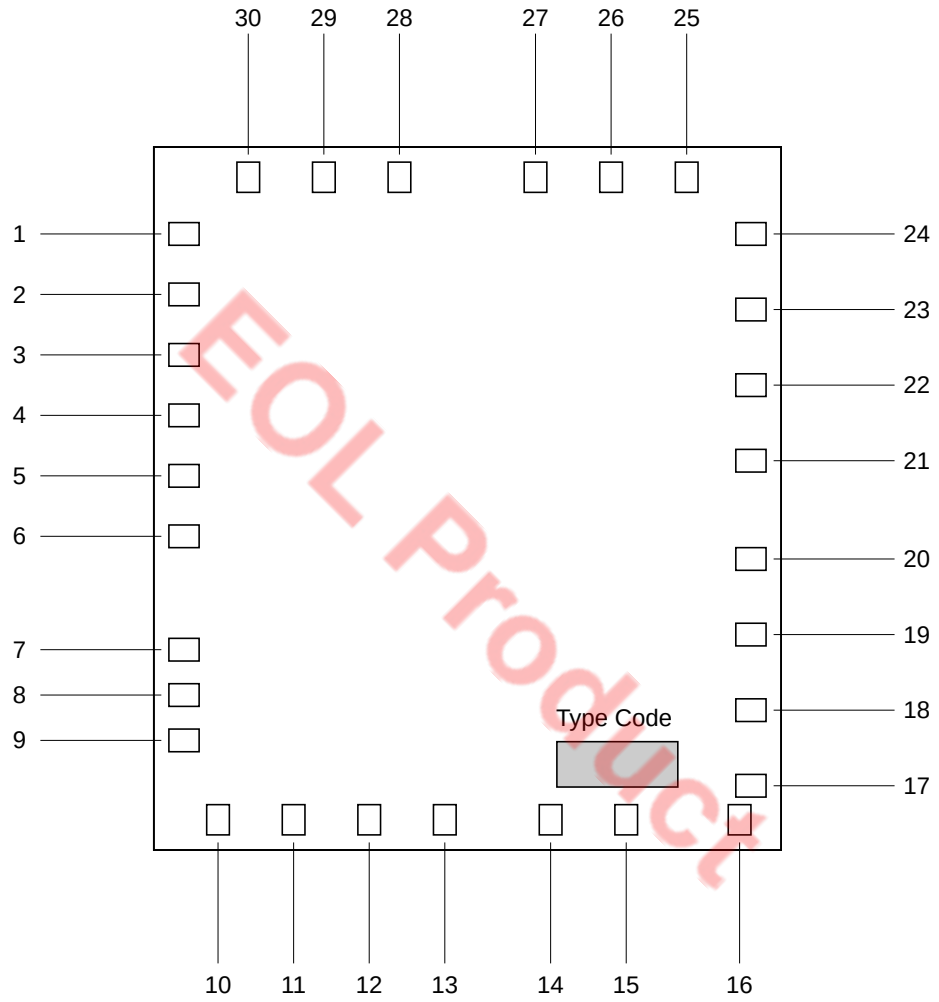
Pad Arrangement

HCD404344R, HCD40C4344R



Type Code: HD404344R (HCD404344R)
HD40C4344R (HCD40C4344R)

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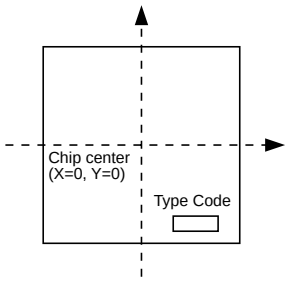
Bonding Pad Coordinates

HCD404344R, HCD40C4344R



Chip size (X × Y): 3.23 × 3.65 (mm)
Coordinates: Pad center
Home point position: Chip center
Pad size (X × Y): 90 × 90 (μm)
Chip thickness: 400 (μm)

Pad No.	Pad Name	Coordinates X (μm)	Coordinates Y (μm)	Pad No.	Pad Name	Coordinates X (μm)	Coordinates Y (μm)
1	R13	–1425	1370	16	TEST	1360	–1627
2	R20	–1425	1050	17	$\overline{\text{RESET}}$	1418	–1456
3	R21	–1425	732	18	R00	1418	–1072
4	R22	–1425	455	19	R01	1418	–690
5	R23	–1425	165	20	R02	1418	–306
6	OSC1	–1425	–115	21	R03	1418	312
7	OSC2	–1425	–732	22	D0	1418	694
8	GND	–1425	–997	23	D1	1418	1098
9	GND	–1425	–1244	24	D2	1418	1501
10	R30	–1257	–1627	25	D3	1075	1627
11	R31	–891	–1627	26	D4	693	1627
12	R32	–526	–1627	27	D5	309	1627
13	R33	–162	–1627	28	R10	–329	1627
14	V_{CC}	420	–1627	29	R11	–732	1627
15	V_{CC}	804	–1627	30	R12	–1135	1627

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Pin Description

HD404344R Series, HD4074344

Item	Symbol	Pin Number DP-28S/ FP-28DA	FP-30D	Chip	I/O	Function
Power supply	V_{CC}	16	18	14, 15		Applies power voltage
	GND	11	11	8, 9		Connects to ground
Test	TEST	17	19	16	I	Cannot be used in user applications. Connect this pin to GND.
Reset	$\overline{RESET}$	18	20	17	I	Resets the MCU
Oscillator	OSC_1	9	9	6	I	Input/output pins for the internal oscillator. Connect these pins to the ceramic oscillator, or OSC_1 to an external oscillator circuit.
	OSC_2	10	10	7	O	
Port	D_0–D_5	23–28	25–30	22–27	I/O	Input/output pins addressed individually by bits; pins D_1 and D_2 can sink 15 mA max.
	$R0_0$–$R0_3$, $R1_0$–$R1_3$, $R2_0$–$R2_3$, $R3_0$–$R3_3$	1–8, 12–15 19–22	1–8, 13–16, 21–24	18–21, 28–30, 1–5, 10–13	I/O	Four-bit input/output pins. Pins $R1_0$–$R2_3$ can sink 15 mA max.
Interrupt	$\overline{INT_0}$	23	25	22	I	Input pin for external interrupts
Stop clear	$\overline{STOPC}$	27	29	26	I	Input pin for transition from stop mode to active mode
Serial interface	$\overline{SCK}$	19	21	18	I/O	Serial interface clock input/output pin
	SI	20	22	19	I	Serial interface receive data input pin
	SO	21	23	20	O	Serial interface transmit data output pin
Timer	TOC	22	24	21	O	Timer output pin
	EVNB	23	25	22	I	Event count input pin
A/D converter	AN_0–AN_3	12–15	13–16	10–13	I	Analog input pins for the A/D converter

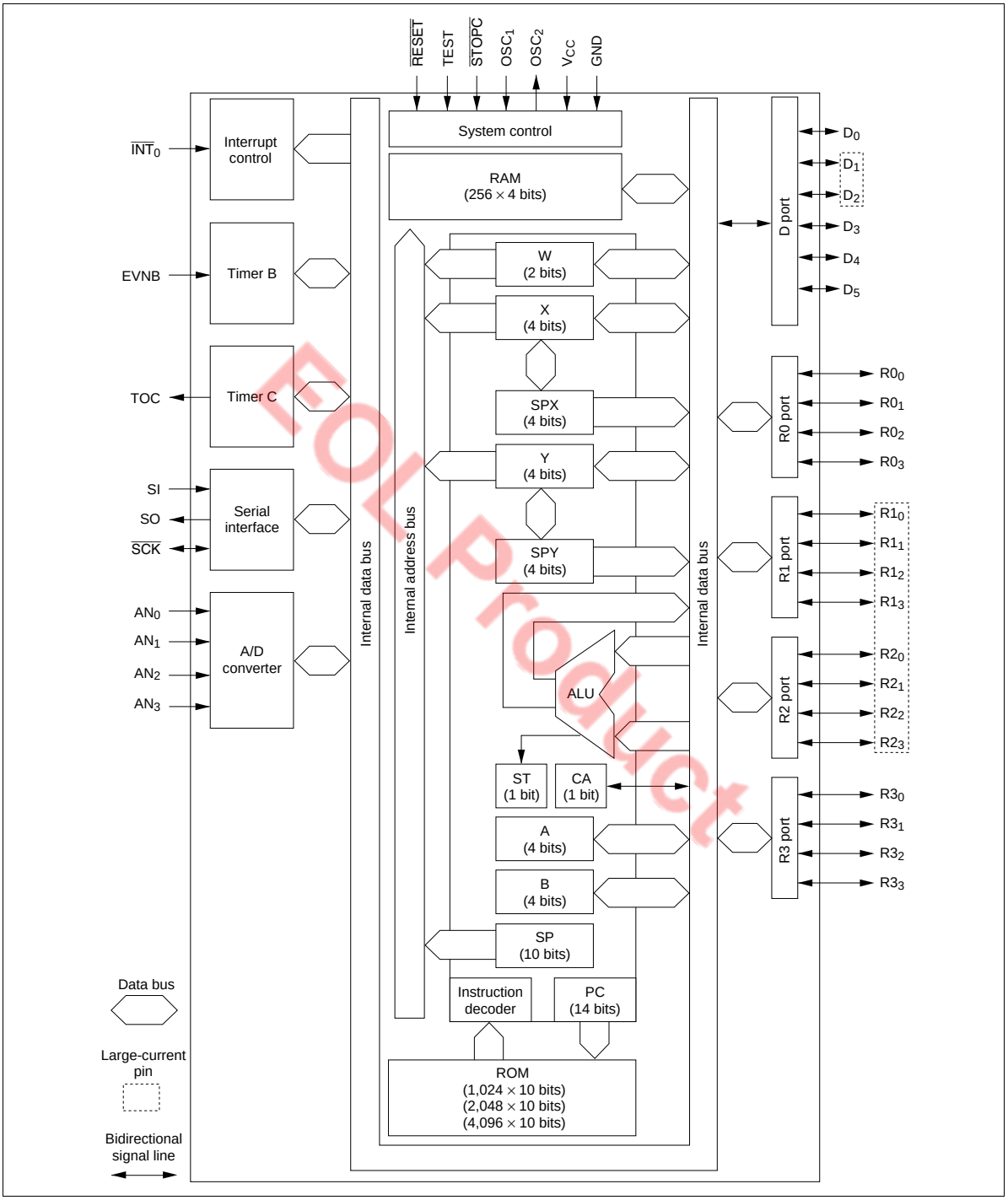
EOL Product

HD404394 Series

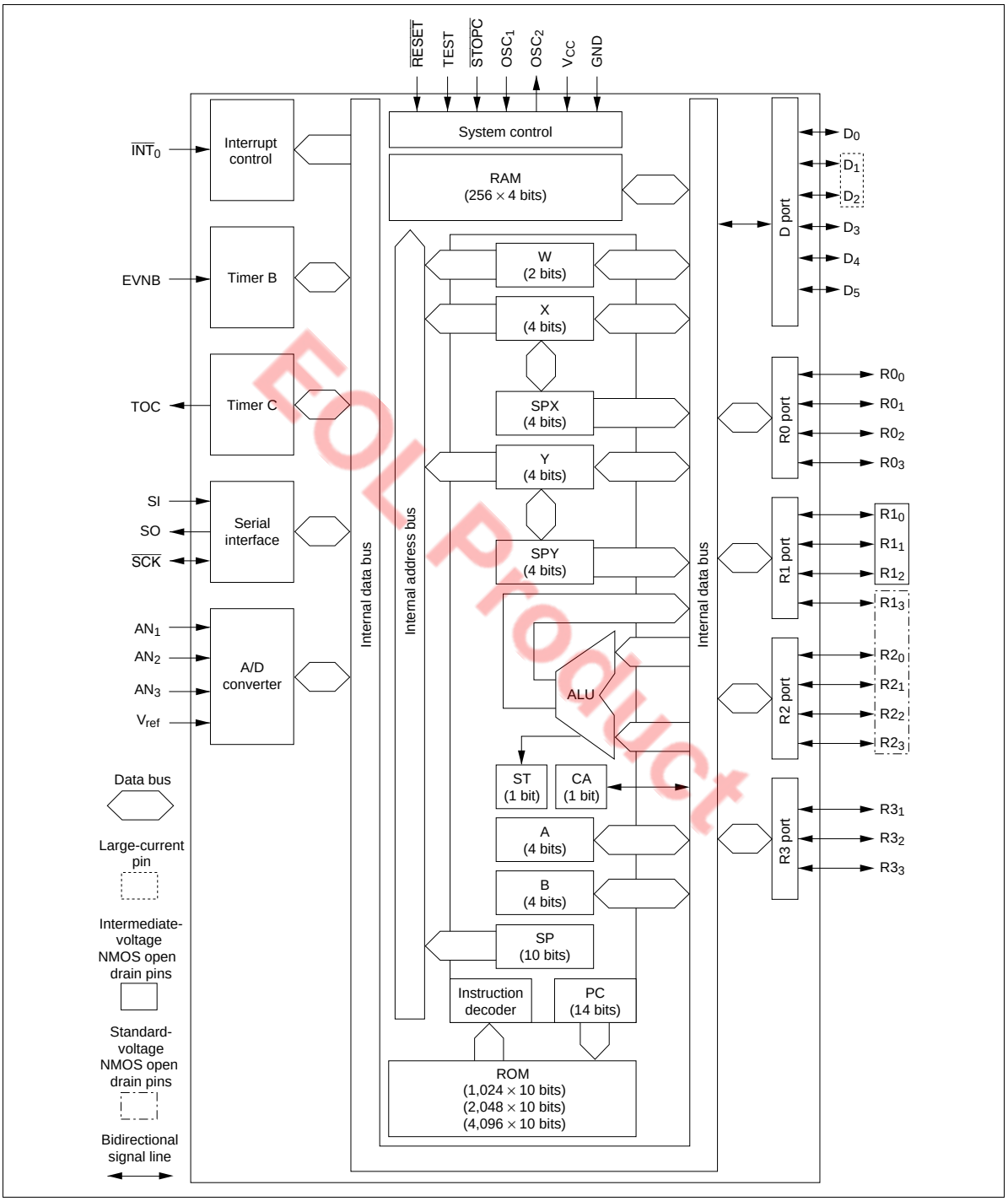
Item	Symbol	Pin Number DP-28S/ FP-28DA	Pin Number FP-30D	I/O	Function
Power supply	V_{CC}	16	18		Applies power voltage
	GND	11	11		Connects to ground
Test	TEST	17	19	I	Cannot be used in user applications. Connect this pin to GND.
Reset	$\overline{RESET}$	18	20	I	Resets the MCU
Oscillator	OSC_1	9	9	I	Input/output pin for the internal oscillator. Connect these pins to the ceramic oscillator, or OSC_1 to an external oscillator circuit
	OSC_2	10	10	O	
Port	D_0–D_5	23–28	25–30	I/O	Input/output pins addressed individually by bits; pins D_1 and D_2 can sink 15 mA max.
	$R0_0$–$R0_3$, $R1_0$–$R1_3$, $R2_0$–$R2_3$, $R3_1$–$R3_3$	1–8, 13–15 19–22	1–8, 14–16, 21–24	I/O	Four-bit input/output pins. Pins $R1_0$–$R1_2$ are NMOS intermediate-voltage open drain pins. Pins $R1_3$–$R2_3$ are NMOS standard-voltage open drain pins which can sink 15 mA max.
Interrupt	$\overline{INT}_0$	23	25	I	Input pin for external interrupts
Stop clear	$\overline{STOPC}$	27	29	I	Input pin for transition from stop mode to active mode
Serial interface	$\overline{SCK}$	19	21	I/O	Serial interface clock input/output pin
	SI	20	22	I	Serial interface receive data input pin
	SO	21	23	O	Serial interface transmit data output pin
Timer	TOC	22	24	O	Timer output pin
	EVNB	23	25	I	Event count input pin
A/D converter	V_{ref}	12	13		Power supply for the internal ladder resistor in the A/D converter
	AN_1–AN_3	13–15	14–16	I	Analog input pins for the A/D converter

EOL Product

HD404344R Series, HD4074344 Block Diagram



HD404394 Series Block Diagram



EOL Product

Memory Map

ROM Memory Map

The ROM memory map for the MCU is shown in figure 1 and explained as follows.

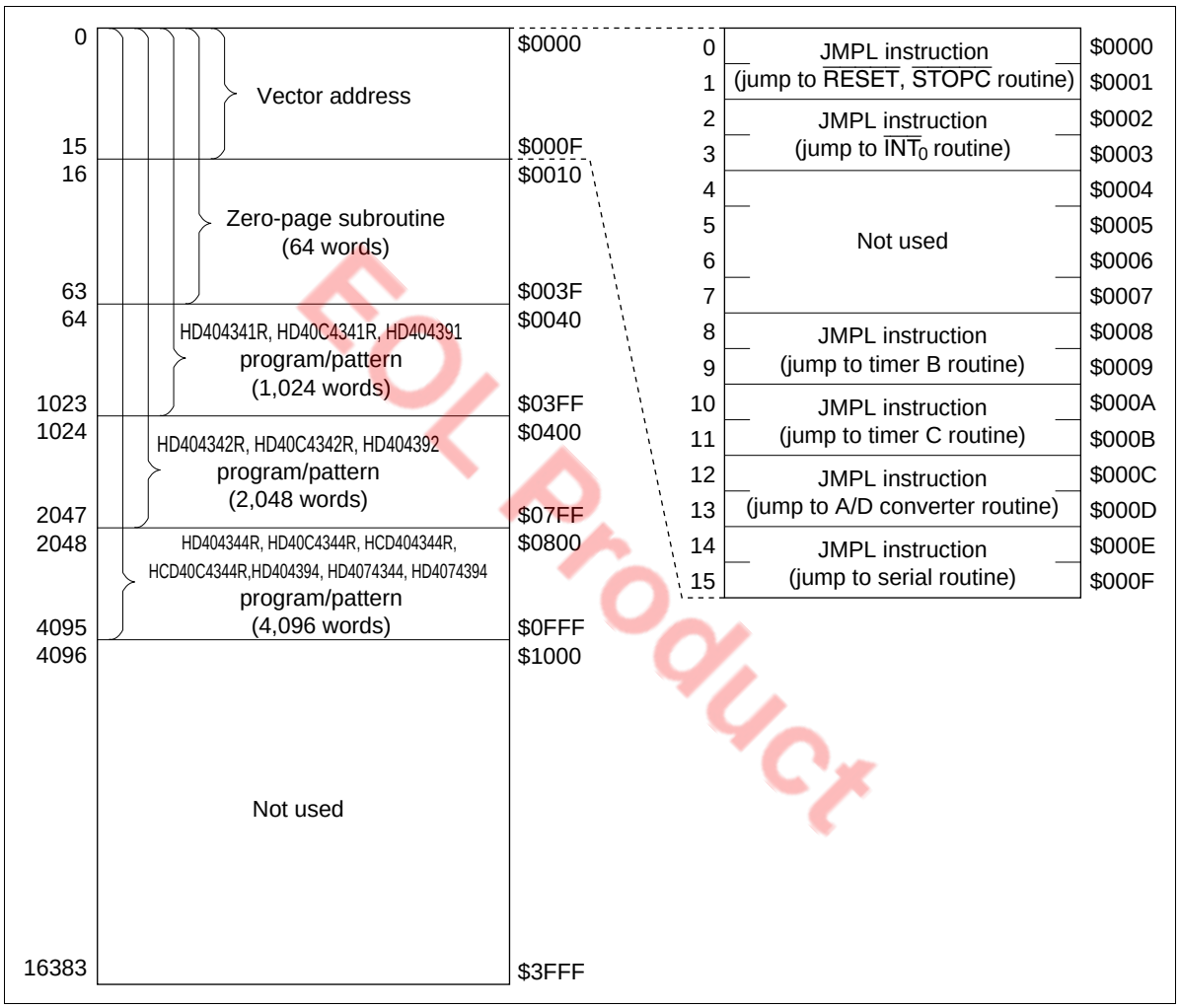


Figure 1 ROM Memory Map

Vector Address Area ($0000 to $000F): When an MCU reset or an interrupt process is executed, the program will begin executing from a vector address. The JMPL instructions which branch to the reset routine and interrupt routine should be programmed at these top addresses.

Zero-Page Subroutine Area ($0000–$003F): This area is reserved for subroutines. The program branches to a subroutine in this area in response to a CAL instruction.

Pattern Area:

HD404341R, HD40C4341R, HD404391—$0000 to $03FF

HD404342R, HD40C4342R, HD404392—$0000 to $07FF

HD404344R, HD40C4344R, HCD404344R, HCD40C4344R, HD404394, HD4074344, HD4074394—$0000 to $0FFF

This area contains ROM data which can be referenced with the P instruction.

Program Area:

HD404341R, HD40C4341R, HD404391—$0000 to $03FF

HD404342R, HD40C4342R, HD404392—$0000 to $07FF

HD404344R, HD40C4344R, HCD404344R, HCD40C4344R, HD404394, HD4074344, HD4074394—$0000 to $0FFF

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RAM Memory Map

The MCU RAM contains 256 digits × 4 bits which is used for the memory registers, and the data and stack areas. The interrupt control bits area, special register area, and the register flag area are mapped into the RAM memory. The RAM memory area is shown in figure 2 and explained as follows.

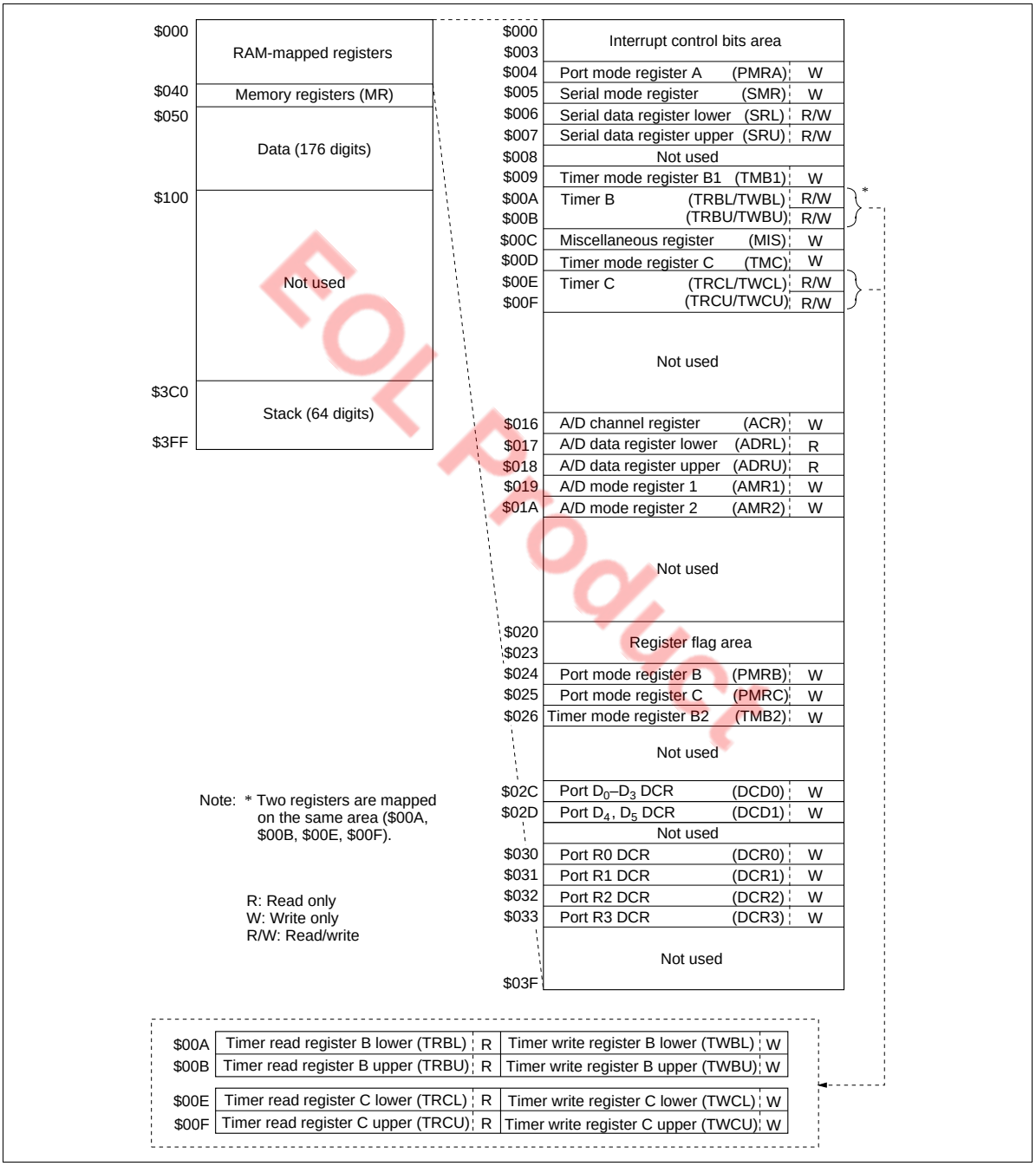

Figure 2 RAM Memory Map

RAM Map Register Area ($000 to $03F):

- Interrupt control bits area: $000 to $003
  This area is made up of bits used for interrupt control as shown in figure 3. Each bit can be accessed only by RAM bit manipulation instructions (SEM/SEMD, REM/REMD, and TM/TMD). Some bits however, have limitations along with certain instructions as shown in figure 4.

- Special register area: $004 to $01F, $024 to $03F
  This area is made up of mode registers and data registers, such as for external interrupt, serial interface, timers, A/D converter, and data control for the I/O ports. Its configurations are shown in figures 2 and 5. These registers are categorized as write-only, read-only, and write/read. They can not be accessed by RAM bit manipulation instructions.

- Register flag area: $020 to $023
  This area is used for the WDON flag and other interrupt control flags. Its configuration is shown in figure 3. Each bit can be accessed only by the SEM/SEMD, REM/REMD, and TM/TMD instructions. Some bits however, have limitations along with certain instructions as shown in figure 4.

Data Area ($040 to $0FF): Sixteen of the 176 digits in this area, from $040 to $04F, are memory registers. These registers can be accessed by the LAMR and XMRA instructions. Its configuration is shown in figure 6.

Stack Area ($3C0 to $3FF): This area is used to hold the program counter (PC), the status flag (ST), and the carry flag (CA) for subroutine calls (CAL and CALL instructions) and interrupts. Since four digits are used for each level, this area can be used for stacking up to 16 subroutines. The stacking order of saved data and the storing of bits are shown in figure 6. The program counter is recovered by the RTN and RTNI instructions. The status and carry flags are recovered only by the RTNI instruction.

Any area not used in the stack area is available for data storage.

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RAM Address	Bit 3	Bit 2	Bit 1	Bit 0
$0000	IM0 (IM of $\overline{INT_0}$)	IF0 (IF of $\overline{INT_0}$)	RSP (Reset SP bit)	IE (Interrupt enable flag)
$0001				
$0002	IMTC (IM of timer C)	IFTC (IF of timer C)	IMTB (IM of timer B)	IFTB (IF of timer B)
$0003	IMS (IM of serial)	IFS (IF of serial)	IMAD (IM of A/D)	IFAD (IF of A/D)

Interrupt control bits area

	Bit 3	Bit 2	Bit 1	Bit 0
$020		ADSF (A/D start flag)	WDON (Watchdog on flag)	
$021	RAME (RAM enable flag)	IAOF (I_{AD} off flag)		
$022				
$023				

Register flag area

: Not used

IF: Interrupt request flag
IE: Interrupt mask
IM: Interrupt enable flag
SP: Stack pointer

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Figure 3 Configuration of Interrupt Control Bits and Register Flag Areas

	SEM/SEMD	REM/REMD	TM/TMD
IE	Can be used	Can be used	Can be used
IM			
IAOF			
IF	Not processed	Can be used	Can be used
RAME			
RSP	Not processed	Can be used	Inhibited to access
WDON	Can be used	Not processed	Inhibited to access
ADSF	Can be used	Inhibited to access	Can be used
Not used	Not processed	Not processed	Inhibited to access

- The WDON bit can be reset by an MCU reset or by stop mode release with $\overline{STOPC}$.
- Do not use REM/REMD for the ADSF bit during A/D conversion.
- If the TM or TMD instruction is excuted for the inhibited or non-existing bits, the value in ST becomes invaild.

Figure 4 Limitations for RAM Bit Manipulation Instructions

Register name		Bit 3	Bit 2	Bit 1	Bit 0
	$000	IM0	IF0	RSP	IE
	$001				
	$002	IMTC	IFTC	IMTB	IFTB
	$003	IMS	IFS	IMAD	IFAD
PMRA	$004		$R0_3$/TOC	$R0_1$/SI	$R0_2$/SO
SMR	$005	$R0_0$/$\overline{SCK}$	Serial data transfer speed		
SRL	$006	Serial data register (lower)			
SRU	$007	Serial data register (upper)			
	$008				
TMB1	$009	Reload control	Timer B clock source		
TRBL/TWBL	$00A	Timer B register (lower)			
TRBU/TWBU	$00B	Timer B register (upper)			
MIS	$00C	Pull-up control	SO PMOS control		
TMC	$00D	Reload control	Timer C clock source		
TRCL/TWCL	$00E	Timer C register (lower)			
TRCU/TWCU	$00F	Timer C register (upper)			
	$010				
	$011				
	$012				
	$013				
	$014				
	$015				
ACR	$016	A/D channel selection			
ADRL	$017	A/D data register (lower)			
ADRU	$018	A/D data register (upper)			
AMR1	$019	$R3_3$/AN_3	$R3_2$/AN_2	$R3_1$/AN_1	$R3_0$/AN_0*
AMR2	$01A				A/D conversion speed
	$01B				
	$01C				
	$01D				
	$01E				
	$01F				
	$020		ADSF	WDON	
	$021	RAME	IAOF		
	$022				
	$023				
PMRB	$024	D_4/$\overline{STOPC}$			D_0/$\overline{INT_0}$/EVNB
PMRC	$025			SO idle level	Transmit clock
TMB2	$026		EVNB edge detection		
	$027				
	$028				
	$029				
	$02A				
	$02B				
DCD0	$02C	D_3 DCR	D_2 DCR	D_1 DCR	D_0 DCR
DCD1	$02D			D_5 DCR	D_4 DCR
	$02E				
	$02F				
DCR0	$030	$R0_3$ DCR	$R0_2$ DCR	$R0_1$ DCR	$R0_0$ DCR
DCR1	$031	$R1_3$ DCR	$R1_2$ DCR	$R1_1$ DCR	$R1_0$ DCR
DCR2	$032	$R2_3$ DCR	$R2_2$ DCR	$R2_1$ DCR	$R2_0$ DCR
DCR3	$033	$R3_3$ DCR	$R3_2$ DCR	$R3_1$ DCR	$R3_0$ DCR*
	$034				
	$035				
	$036				
	$037				
	$038				
	$039				
	$03A				
	$03B				
	$03C				
	$03D				
	$03E				
	$03F				

: Not used

Note: * Applies to the HD404344R series and HD4074344. Does not apply to the HD404394 series.

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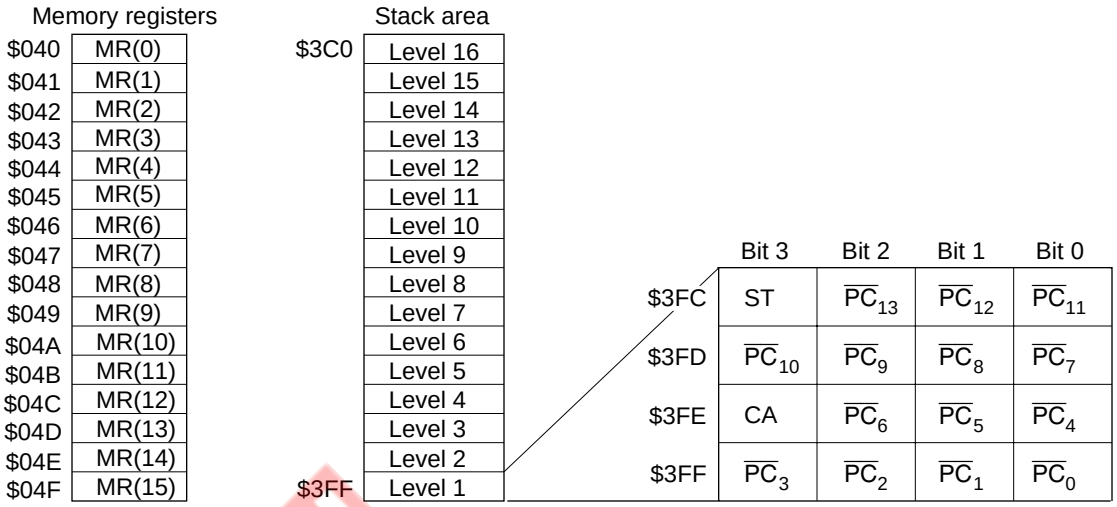
Figure 5 Special Register Area



PC_{13}–PC_0 : Program counter
ST: Status flag
CA: Carry flag

Note: Since HD404344R series, HD4074344 and HD404394 series have a 4-kword ROM, $\overline{PC}_{12}$ and $\overline{PC}_{13}$ are ignored.

Figure 6 Configuration of Memory Registers, Stack Area, and Stack Position

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Functional Description

Registers and Flags

The CPU has nine registers and two flags. Their configurations are shown in figure 7 and explained as follows.

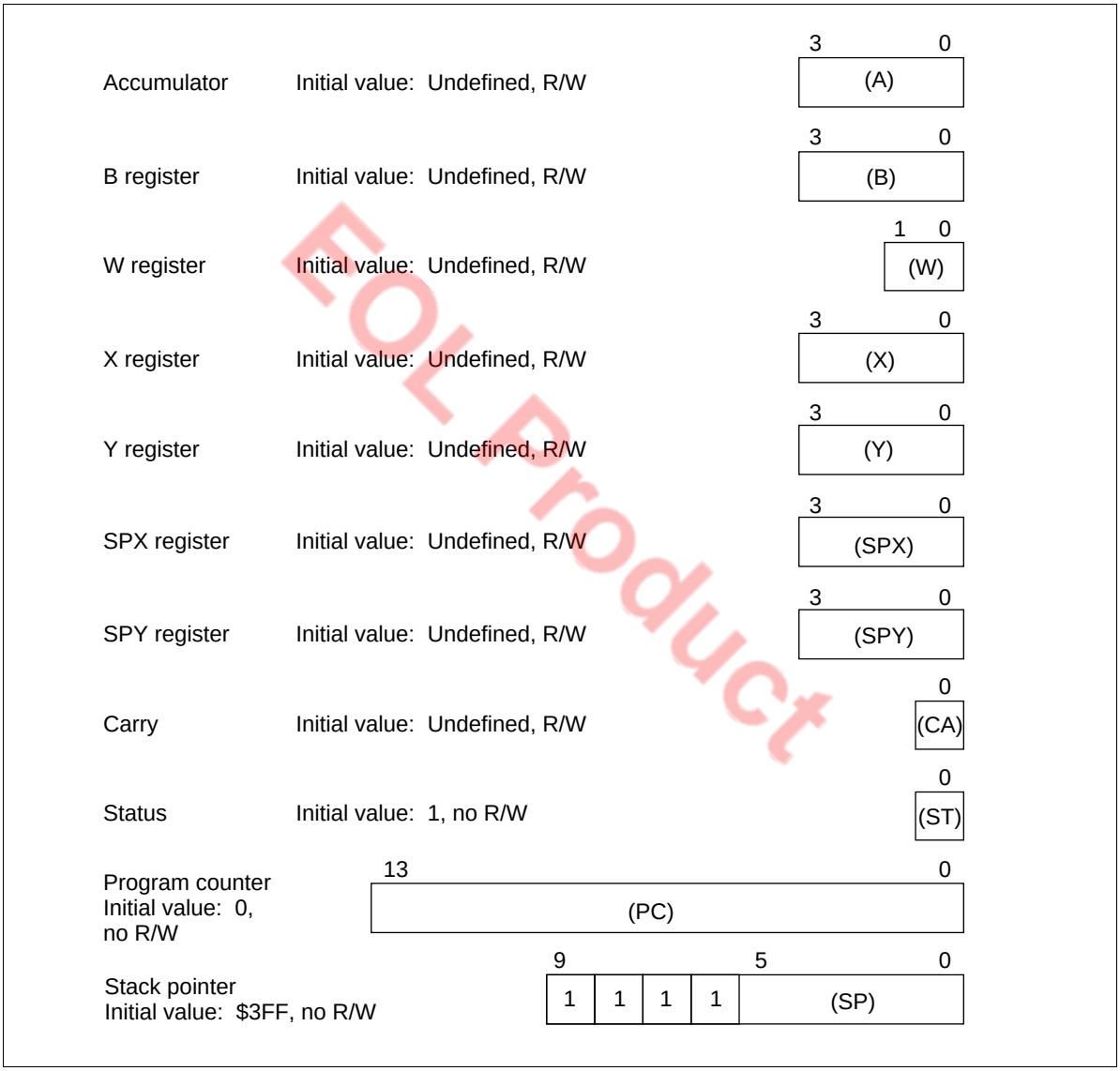

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Figure 7 Registers and Flags

Accumulator (A), B Register (B): The accumulator and B register are 4-bit registers used for storing ALU operation results and data that is transferred between memory and I/O ports or between other registers.

W Register (W), X Register (X), Y Register (Y): The W register is a 2-bit register and the X and Y registers are 4-bit registers.

These are used for indirect addressing to RAM. The Y register is also used for addressing the D port.

SPX Register (SPX), SPY Register (SPY): The SPX and SPY registers are 4-bit registers that supplement the X and Y registers, respectively.

Carry Flag (CA): The carry flag latches the ALU overflow during an arithmetic instruction execution. It is controlled by the SEC, REC, ROTL, and ROTR instructions. The carry flag is stored during interrupt processing, then recovered from the stack by a RTNI instruction. (It is not affected by the RTN instruction.)

Status Flag (ST): The status flag latches the overflow of ALU arithmetic instructions and compara tive instructions, and also the results of ALU non-zero and bit test instructions. It is then used for branch conditions of the BR, BRL, CAL, and CALL instructions. The status flag remains unchanged until the next arithmetic instruction, comparative instruction, or bit test is executed. After a BR, BRL, CAL, or CALL instruction is executed, the status flag will be set to 1 regardless if the instruction is executed or skipped. The contents of the status flag is stored on the stack during interrupt processing, then recovered from the stack by a RTNI instruction.

Program Counter (PC): This 14-bit binary counter maintains ROM address information.

Stack Pointer (SP): The stack pointer is a 10-bit register which contains the address of the next stack space to be used. It is initialized as $3FF by an MCU reset. When data is stored onto the stack, the SP is decremented by 4, and when data is pulled from the stack, it is incremented by 4. The top four bits of the stack pointer are fixed at 1111, so it can be used for a maximum of 16 levels. There are two ways of initializing the stack pointer to $3FF. One is by MCU reset and the other is by resetting the RSP bit with a REM or a REMD instruction.

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Reset

An MCU reset is executed by setting $\overline{\text{RESET}}$ low. The $\overline{\text{RESET}}$ input must be more than t_{RC} so as to keep the oscillator steady during power on or when stop mode is cancelled. For other cases, the MCU can be reset by a $\overline{\text{RESET}}$ input for a minimum of two instruction cycle times.

Initialized values by MCU reset are listed in table 1.

Certain bits in the interrupt control bits area and the register flag area can be set or reset by the SEM/SEMD or REM/REMD instructions. Also these can be tested by the TM/TMD instruction. The following specifies the limitations for each bit.

Table 1 Initial Values After MCU Reset

Item		Abbr.	Initial Value	Contents
Program counter		(PC)	$0000	Indicates program execution point from start address of ROM area
Status flag		(ST)	1	Enables conditional branching
Stack pointer		(SP)	$3FF	Stack level 0
Interrupt flags/mask	Interrupt enable flag	(IE)	0	Inhibits all interrupts
	Interrupt request flag	(IF)	0	Indicates there is no interrupt request
	Interrupt mask	(IM)	1	Prevents (masks) interrupt requests
I/O	Port data register	(PDR)	All bits 1	Enables output at level 1
	Data control register	(DCD0, DCD1)	All bits 0	Turns output buffer off (to high impedance)
		(DCR0,- DCR3)	All bits 0	
	Port mode register A	(PMRA)	- 000	Refer to description of port mode register A
	Port mode register B	(PMRB)	0 - - 0	Refer to description of port mode register B
	Port mode register C	(PMRC)	- - - 0	Refer to description of port mode register C
Timer/ counters, serial interface	Timer mode register B1	(TMB1)	0000	Refer to description of timer mode register B1
	Timer mode register B2	(TMB2)	- - 00	Refer to description of timer mode register B2
	Timer mode register C	(TMC)	0000	Refer to description of timer mode register C
	Serial mode register	(SMR)	0000	Refer to description of serial mode register
	Prescaler S	(PSS)	$000	—
	Timer counter B	(TCB)	$00	—
	Timer counter C	(TCC)	$00	—
	Timer write register B	(TWBU, TWBL)	$X0	—
	Timer write register C	(TWCU, TWCL)	$X0	—
	Octal counter		000	—

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Table 1 Initial Values After MCU Reset (cont)

Item		Abbr.	Initial Value	Contents
A/D	A/D mode register 1	(AMR1)	0000	Refer to description of A/D mode register
	A/D mode register 2	(AMR2)	- - - 0	Refer to description of A/D mode register
Bit register	Watchdog timer on flag	(WDON)	0	Refer to description of timer C
	A/D start flag	(ADSF)	0	Refer to description of A/D converter
	I_{AD} off flag	(IAOF)	0	Refer to description of A/D converter
Others	Miscellaneous register	(MIS)	00 - -	Refer to description of I/O, and serial interface

Notes: 1. The statuses of other registers and flags after MCU reset are shown in the following table.
2. X indicates invalid value. – indicates that the bit does not exist.

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Table 1 Initial Values After MCU Reset (cont)

		After Stop Mode Release by $\overline{\text{STOPC}}$ Input	After Stop Mode Release by $\overline{\text{RESET}}$ Input	After Other Types of MCU Reset
Carry	(CA)	Program needs to initialize these registers.		Program needs to initialize these registers.
Accumulator	(A)			
B register	(B)			
W register	(W)			
X/SPX register	(X/SPX)			
Y/SPY register	(Y/SPY)			
Serial data register	(SRU, SRL)			
A/D data register	(ADRU, ADRL)			
RAM		Data before entering stop mode are kept.		
RAM enable flag	(RAME)	1	0	0
Port mode register B bit 3	(PMRB3)	Data before entering stop mode are kept.	0	0

Interrupts

There are five kinds of interrupts: external $\overline{INT_0}$, timer B, timer C, serial interface, and A/D converter.

An interrupt request flag or an interrupt mask and vector address are used for each type of interrupt. They are used for storing interrupt requests and interrupt controls. An interrupt enable flag is also used for total interrupt control.

Interrupt Control Bits and Interrupt Processing: The interrupt control bits are mapped from $000 to $003 of RAM and can be accessed by RAM bit manipulation instructions. However, the interrupt request flag (IF) cannot be set by software. An MCU reset initializes the interrupt enable flag (IE) and the interrupt request flag (IF) to 0, and the interrupt mask (IM) to 1.

A block diagram of the interrupt control circuit is shown in figure 8. The interrupt priority order and vector addresses are listed in a table in the figure, along with the conditions for executing the interrupt processing of the five types of interrupt requests (table 2). An interrupt request occurs when the interrupt request flag is set to 1 and the interrupt mask to 0. If the interrupt enable flag is 1, interrupt processing has occurred. The vector address which corresponds to the interrupt source is generated from the priority PLA.

The interrupt processing sequence is shown in figure 9 and the interrupt processing flowchart is shown in figure 10. After receiving an interrupt, the previous instruction is completed in the first cycle. The interrupt enable flag (IE) is reset after two cycles. The contents of the carry flag, status flag, and program counter are stored onto the stack at the second and third cycles. Instruction execution is restarted by jumping to the vector address during the third cycle. The JMPL instructions, which branch to the start addresses of the interrupt routines, should be programmed at each vector address area. The interrupt request which initiated the interrupt processing should be reset by software instructions in the interrupt routine.

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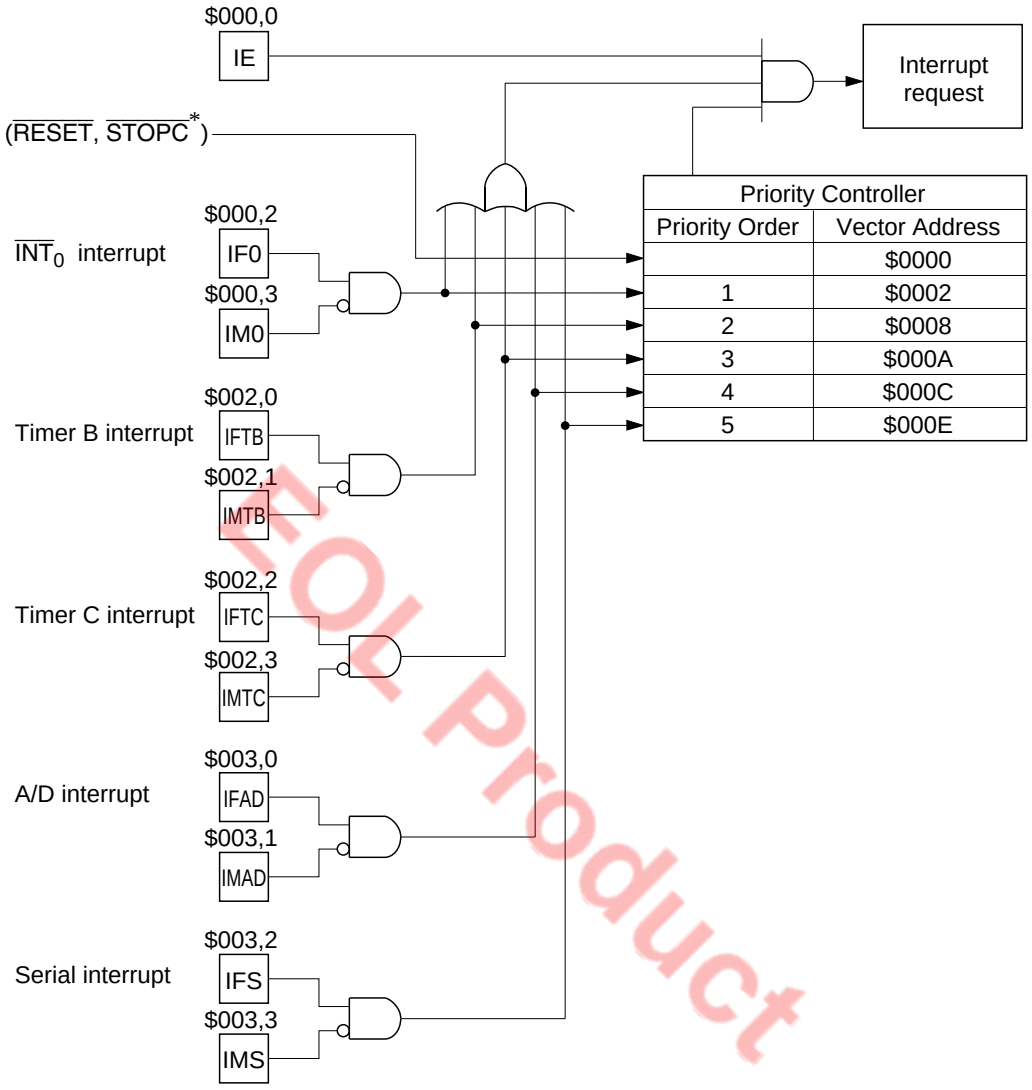

Note: * $\overline{\text{STOPC}}$ interrupt request is enabled only when the MCU is in stop mode.

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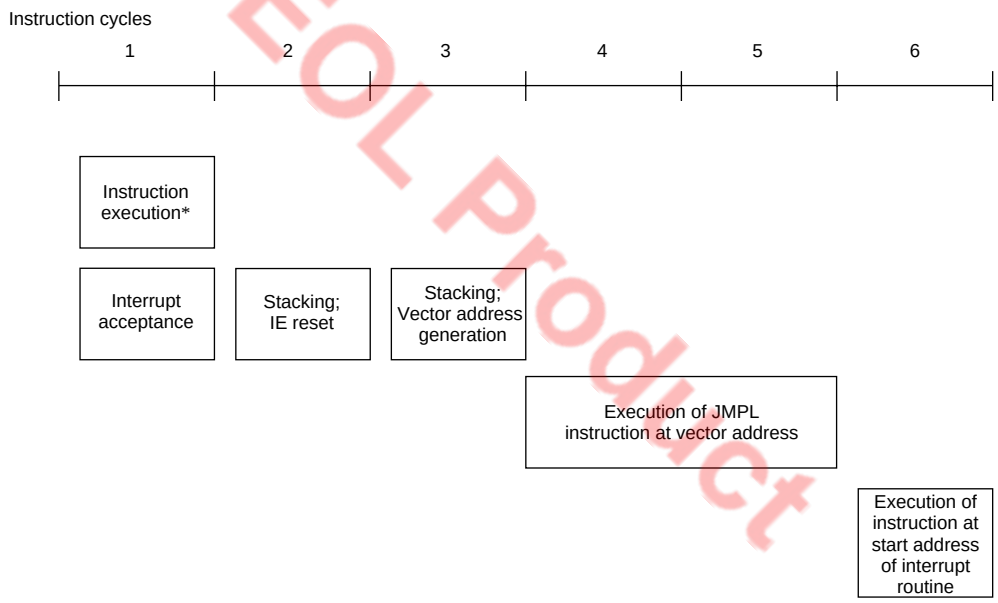
Figure 8 Interrupt Control Circuit, Vector Addresses, and Interrupt Priorities

Table 2 Interrupt Processing and Activation Conditions

	Interrupt Source				
Interrupt Control Bit	**$\overline{INT}_0$**	**Timer B**	**Timer C**	**A/D**	**Serial**
IE	1	1	1	1	1
IF0 · $\overline{IM0}$	1	0	0	0	0
IFTB · $\overline{IMTB}$	*	1	0	0	0
IFTC · $\overline{IMTC}$	*	*	1	0	0
IFAD · $\overline{IMAD}$	*	*	*	1	0
IFS · $\overline{IMS}$	*	*	*	*	1

Note: * Can be either 0 or 1. Their values have no effect on operation.



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Note: * The stack is accessed and the interrupt enable flag is reset after the instruction is executed, even if it is a two-cycle instruction.

Figure 9 Interrupt Processing Sequence

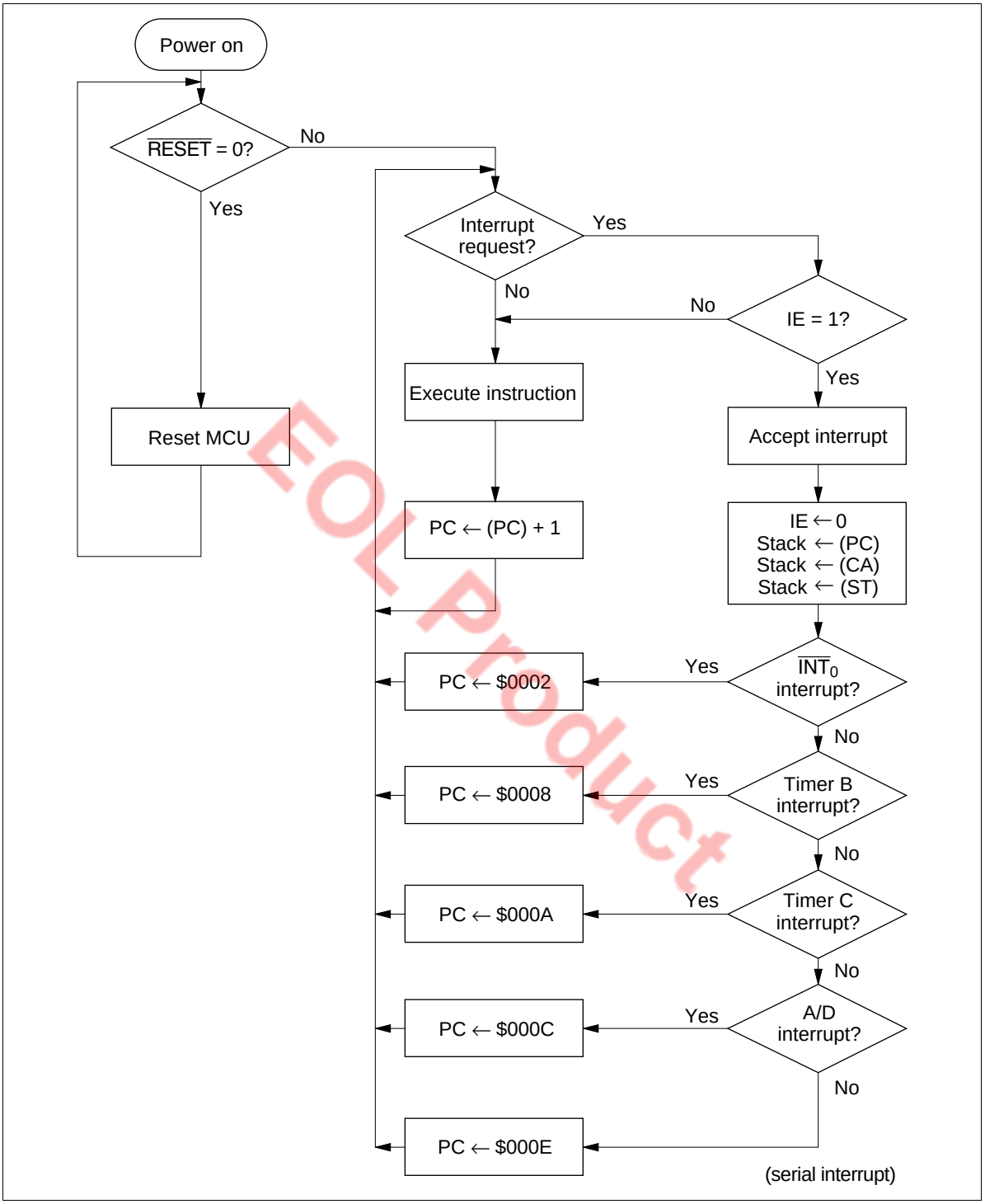

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Figure 10 Interrupt Processing Flowchart

Interrupt Enable Flag (IE: $000, Bit 0): The interrupt enable flag executes interrupt enable/disable for all interrupt requests as listed in table 3. It is reset by interrupt processing and set by the RTNI instruction.

Table 3 Interrupt Enable Flag (IE: $000, Bit 0)

IE	Interrupt Enabled/Disabled
0	Disabled
1	Enabled

External Interrupt ($\overline{INT}_0$): $\overline{INT}_0$ input should be selected by using port mode register B (PMRB: $024), so that the external interrupt request flag (IF0) is set at the falling edge of the $\overline{INT}_0$ input.

External Interrupt Request Flag (IF0: $000, Bit 2): The external interrupt request flag is set by the $\overline{INT}_0$ input edge, as listed in table 4.

Table 4 External Interrupt Request Flag (IF0: $000, Bit 2)

IF0	Interrupt Request
0	No
1	Yes

External Interrupt Mask (IM0: $000, Bit 3): IM0 is a bit which masks the interrupt request caused by an external interrupt request flag, as listed in table 5.

Table 5 External Interrupt Mask (IM0: $000, Bit 3)

IM0	Interrupt Request
0	Enabled
1	Disabled (masked)

Timer B Interrupt Request Flag (IFTB: $002, Bit 0): The timer B interrupt request flag is set by the overflow output of timer B, as listed in table 6.

Table 6 Timer B Interrupt Request Flag (IFTB: $002, Bit 0)

IFTB	Interrupt Request
0	No
1	Yes

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Timer B Interrupt Mask (IMTB: $002, Bit 1): IMTB is a bit which masks the interrupt request caused by the timer B interrupt request flag, as listed in table 7.

Table 7 Timer B Interrupt Mask (IMTB: $002, Bit 1)

IMTB	Interrupt Request
0	Enabled
1	Disabled (masked)

Timer C Interrupt Request Flag (IFTC: $002, Bit 2): The timer C interrupt request flag is set by the overflow output of timer C, as listed in table 8.

Table 8 Timer C Interrupt Request Flag (IFTC: $002, Bit 2)

IFTC	Interrupt Request
0	No
1	Yes

Timer C Interrupt Mask (IMTC: $002, Bit 3): IMTC is a bit which masks the interrupt request caused by the timer C interrupt request flag, as listed in table 9.

Table 9 Timer C Interrupt Mask (IMTC: $002, Bit 3)

IMTC	Interrupt Request
0	Enabled
1	Disabled (masked)

Serial Interrupt Request Flag (IFS: $003, Bit 2): A serial interrupt request flag is set when the serial data transfer is completed or when the data transfer is suspended, as listed in table 10.

Table 10 Serial Interrupt Request Flag (IFS: $003 Bit 2)

IFS	Interrupt Request
0	No
1	Yes

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Serial Interrupt Mask (IMS1: $003, Bit 3): IMS1 is a bit which masks the interrupt request caused by the serial interrupt request flag, as listed in table 11.

Table 11 Serial Interrupt Mask (IMS: $003, Bit 3)

IMS	Interrupt Request
0	Enabled
1	Disabled (masked)

A/D Interrupt Request Flag (IFAD: $003, Bit 0): The A/D interrupt request flag is set after the A/D conversion is completed, as listed in table 12.

Table 12 A/D Interrupt Request Flag (IFAD: $003, Bit 0)

IFAD	Interrupt Request
0	No
1	Yes

A/D Interrupt Mask (IMAD: $003, Bit 1): IMAD is a bit which masks the interrupt request caused by the A/D interrupt request flag, as listed in table 13.

Table 13 A/D Interrupt Mask (IMAD: $003, Bit 1)

IMAD	Interrupt Request
0	Enabled
1	Disabled (masked)

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Operating Modes

The MCU has three operating modes as shown in table 14. The transitions between the operating modes are shown in figure 11.

Table 14 Operations in Each Operating Mode

Function	Active Mode	Standby Mode	Stop Mode
System oscillator	OP	OP	Stopped
CPU	OP	Retained	Reset
RAM	OP	Retained	Retained
Timers B, C	OP	OP	Reset
Serial	OP	OP	Reset
A/D	OP	OP	Reset
I/O	OP	Retained*	Reset

Notes: OP implies in operation.

* Since input/output circuits are in operation, the current will flow in/out depending on the pin status in standby mode. Note that this current is in addition to the standby mode dissipation current.

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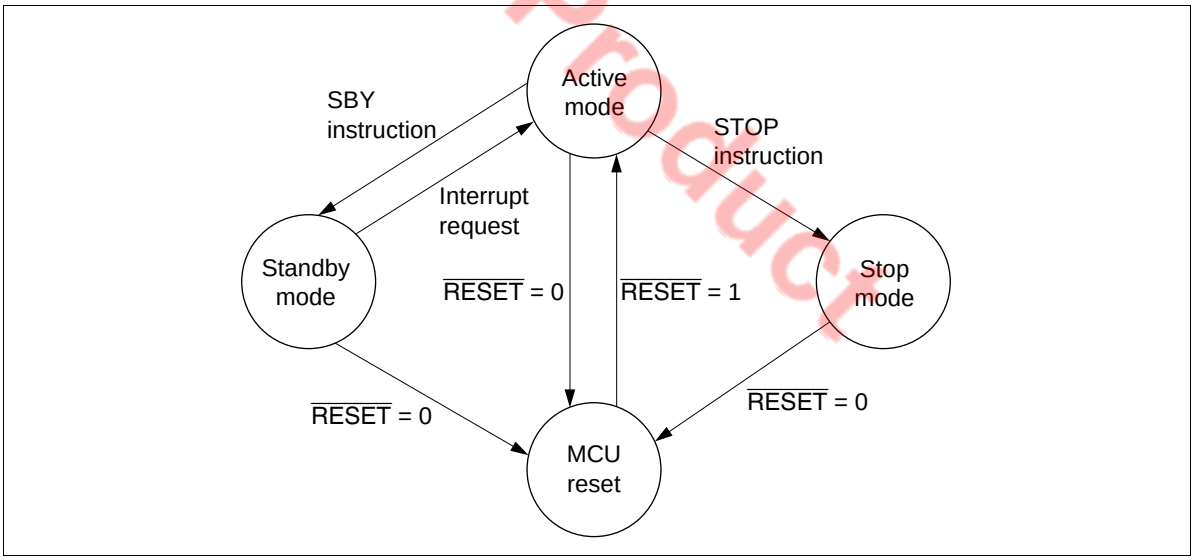

Figure 11 MCU Status Transition

Active Mode: All functions operate in active mode. In active mode, the MCU is controlled by the oscillating circuit of OSC_1 and OSC_2.

Standby Mode: The MCU switches to standby mode when an SBY instruction is executed.

In standby mode, the oscillator continues operating, but the clocks related to instruction execution stops running. This causes the CPU to stop operating. However, the contents of RAM are retained. Also, the D and R ports, which are set as output, maintain their status before entering standby mode. The peripheral functions, such as interrupt, timers, serial interface, and A/D converter, continue operating.

Power dissipation in standby mode is less than in active mode because of the CPU not operating.

The MCU enters standby mode when the SBY instruction is executed in active mode.

To terminate standby mode, provide a $\overline{\text{RESET}}$ input or an interrupt request. If a reset input is given, the MCU will be reset. If an interrupt request is given, the MCU will change to active mode and the next instruction will be executed. After the instruction execution, if the interrupt enable flag is 1, the interrupt operation is executed. If the interrupt enable flag is 0, normal instruction execution continues and the interrupt request is left pending.

The standby mode flowchart is shown in figure 13.

Stop Mode: The MCU enters stop mode when a STOP instruction is received.

In stop mode, all MCU functions stop, except for maintaining RAM data. Power dissipation in this mode is therefore the lowest of all operating modes.

In stop mode, the OSC_1 and OSC_2 oscillator is stopped.

To terminate stop mode provide either a $\overline{\text{RESET}}$ or $\overline{\text{STOPC}}$ input as shown in figure 12.

When terminating stop mode, it is important to ensure a proper oscillation stabilization period of at least t_{RC} for the $\overline{\text{RESET}}$ or $\overline{\text{STOPC}}$ input. (Refer to the AC characteristics tables.)

After clearing stop mode, the RAM maintains its data kept before entering stop mode. However, the contents of the accumulator, B register, W register, X/SPX register, Y/SPY register, carry flag, and the serial data register are not maintained.

Clearing Stop Mode Using $\overline{\text{STOPC}}$: The MCU is transition from stop mode to active mode by either a $\overline{\text{RESET}}$ or $\overline{\text{STOPC}}$ input. The MCU starts instruction execution from the start of the program at address 0. Then the RAM enable flag (RAME: $021, 3) is set accordingly, RAME = 0 for $\overline{\text{RESET}}$ input and RAME = 1 for $\overline{\text{STOPC}}$ input. A $\overline{\text{RESET}}$ input is effective when the MCU is in any mode. A $\overline{\text{STOPC}}$ input however, is effective only in stop mode and is ignored in other modes.

So, when clearing stop mode with a $\overline{\text{STOPC}}$ input the program needs to identify the RAME status. (For example, when the RAM contents before entering stop mode is used after transition to active mode.) A TEST instruction for the RAM enable flag (RAME) should be executed at the beginning of the program.

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Table 15 Operating Modes and Transition Conditions

Mode	Conditions to Enter Mode	Conditions to Exit Mode
Active mode	• $\overline{\text{RESET}}$ release • Interrupt request • $\overline{\text{STOPC}}$ release in stop mode	• $\overline{\text{RESET}}$ input • STOP/SBY instruction
Standby mode	• SBY instruction	• $\overline{\text{RESET}}$ input • Interrupt request
Stop mode	• STOP instruction	• $\overline{\text{RESET}}$ input • $\overline{\text{STOPC}}$ input in stop mode

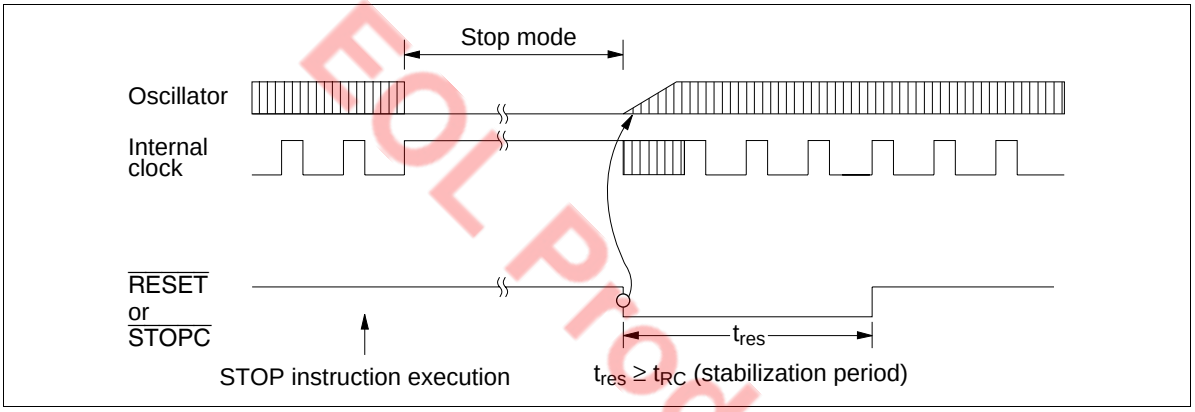

Figure 12 Timing of Stop Mode Cancellation

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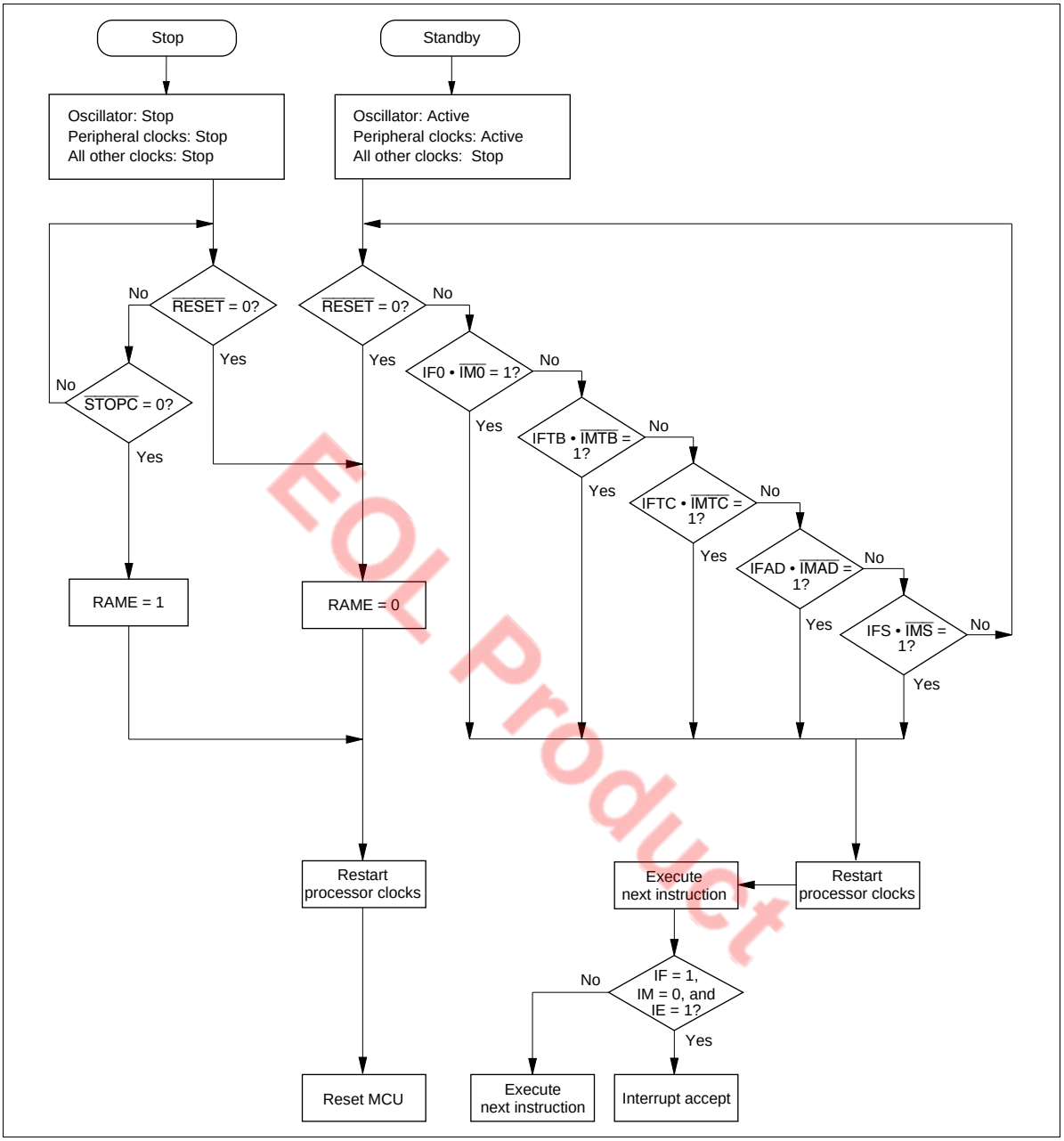

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Figure 13 MCU Process Flowchart

MCU Operation Sequence: The MCU operates according to the flowcharts shown in figures 14 to 16. Since $\overline{\text{RESET}}$ is asynchronous input, the MCU will be reset in any mode that the MCU is operating in.

The low-power mode operation sequence is shown in figure 16. With the IE flag cleared and an interrupt flag set together with its interrupt mask cleared, if a STOP/SBY instruction is executed, the instruction is cancelled (regarded as an NOP) and the following instruction is executed. Before executing a STOP/SBY instruction, make sure all interrupt flags are cleared or all interrupts are masked.

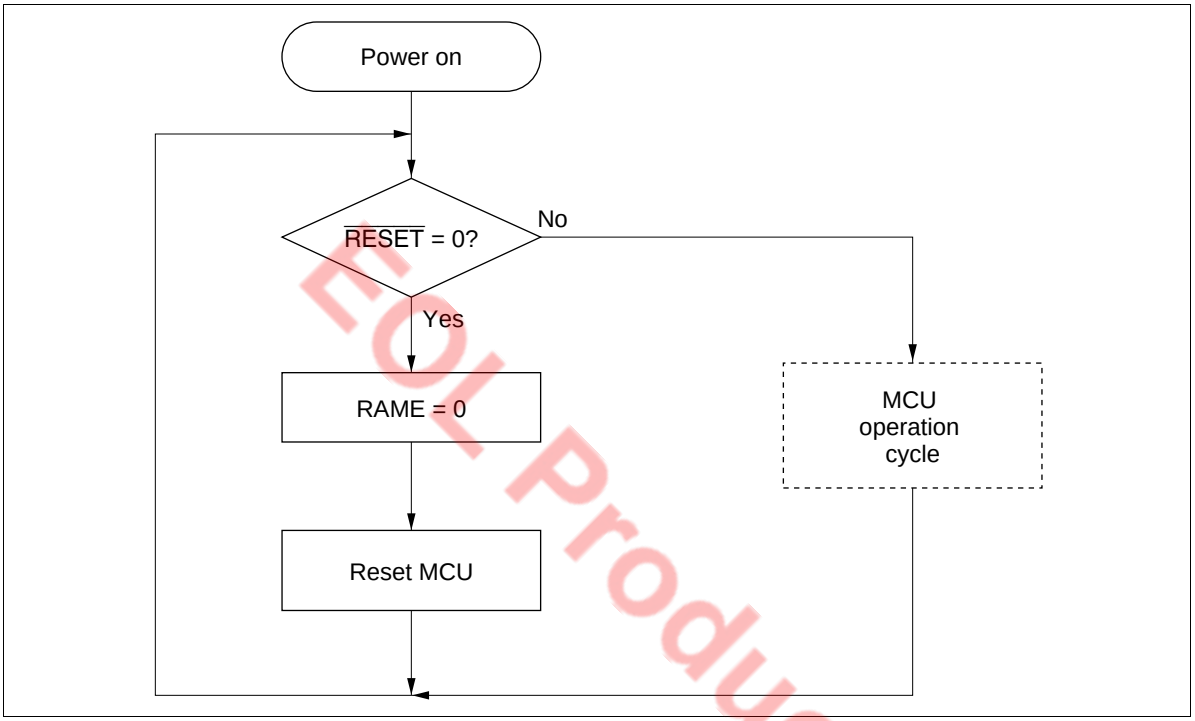

Figure 14 MCU Operation Sequence (Power On)

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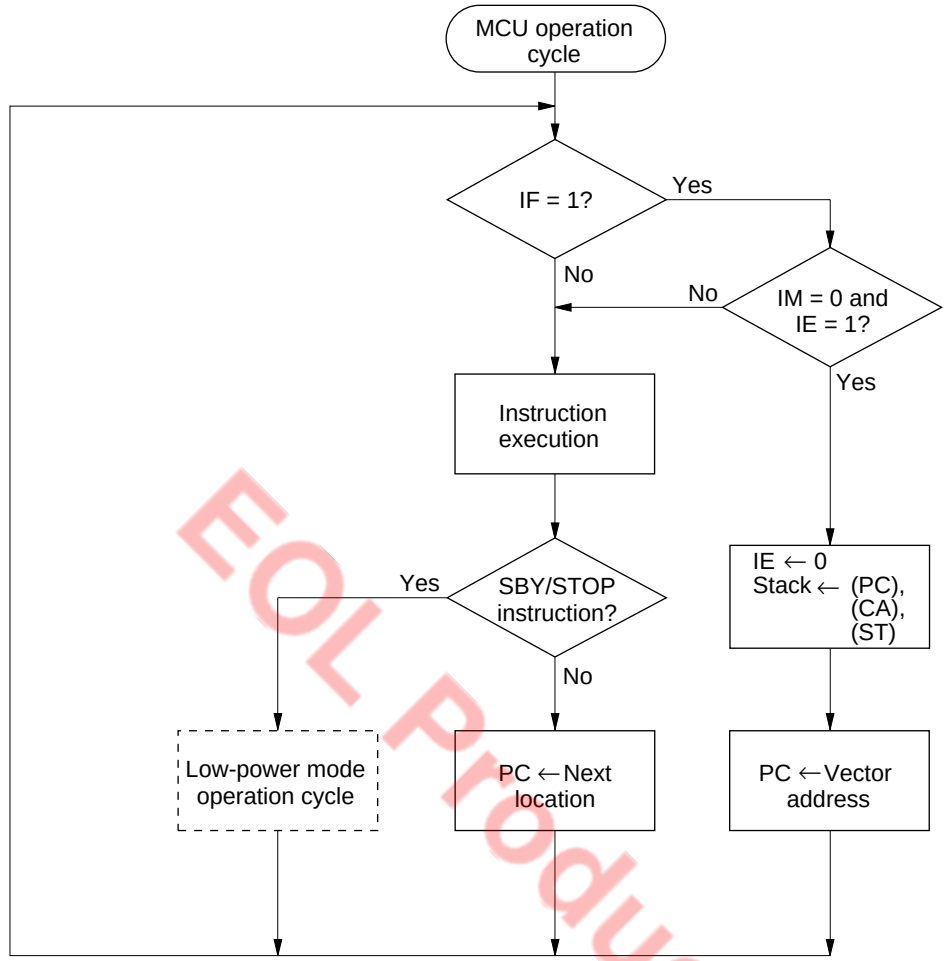

IF: Interrupt request flag
IM: Interrupt mask
IE: Interrupt enable flag
PC: Program counter
CA: Carry flag
ST: Status flag

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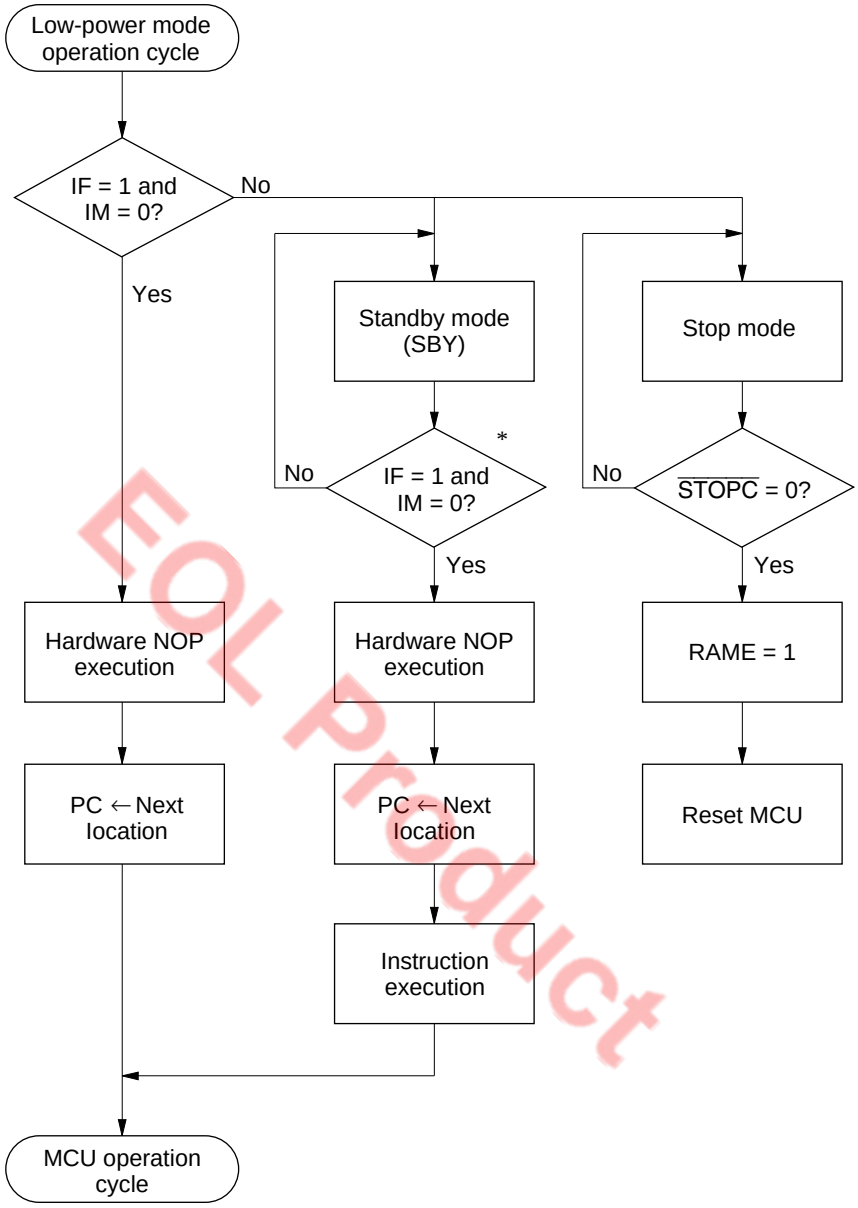
Figure 15 MCU Operation Sequence (MCU Operation Cycle)



Note: * For IF and IM operation, refer to figure 13.

Figure 16 MCU Operation Sequence (Low Power Mode Operation)

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Oscillator Circuit

Figure 17 shows a block diagram of the clock generation circuit. Ceramic oscillator can be connected to OSC_1 and OSC_2 as listed in table 16. An external clock can also be connected. In addition, the system oscillator of the HD404344R Series is capable of CR oscillation.

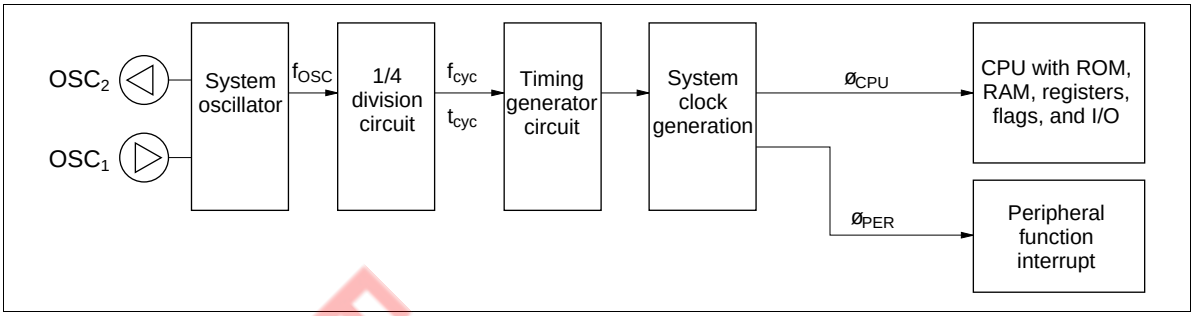

Figure 17 Clock Generation Circuit

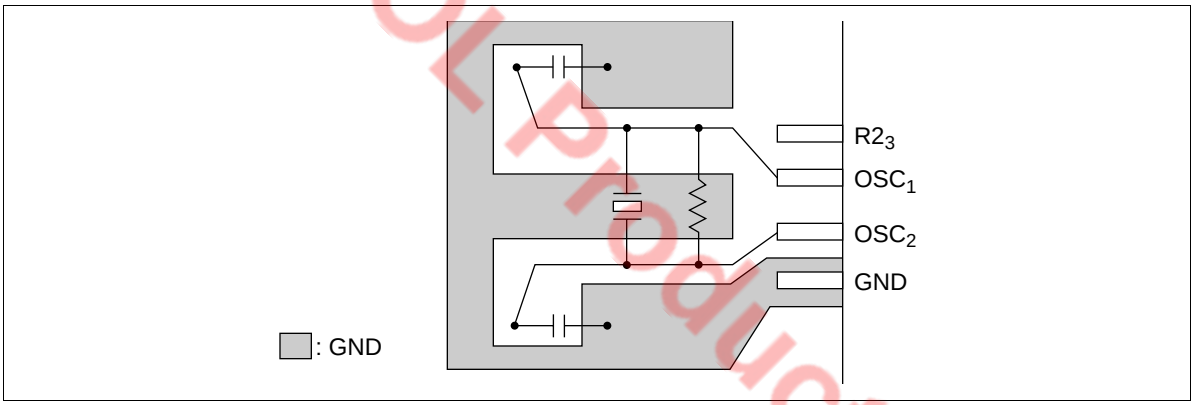

Figure 18 Typical Layout of Ceramic Oscillator

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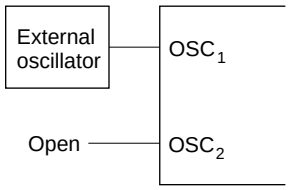
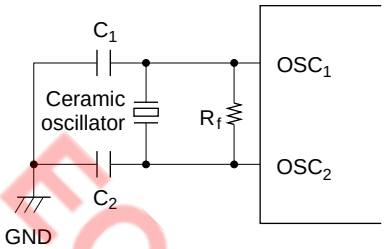
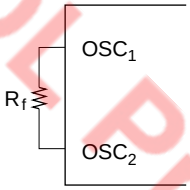
Table 16 Oscillator Circuit Examples

	Circuit Configuration	Circuit Constants
External clock operation		
Ceramic oscillator (OSC_1, OSC_2)		Ceramic oscillator : CSA4.00MG (Murata) R_f = 1 MΩ ±20% C_1 = C_2 = 30 pF ±20% Ceramic oscillator: KBR-4.0MSA (Kyocera) R_f = 1 MΩ ±20% C_1 = C_2 = 33 pF ±20%
CR oscillation (OSC_1, OSC_2) HD404344R series		R_f = 20 kΩ ±1%

Notes: 1. Since the circuit constants change depending on the ceramic oscillator and stray capacitance of the board, the user should consult with the ceramic oscillator manufacturer to determine the circuit parameters.

2. Wiring among OSC_1, OSC_2, and elements should be as short as possible, and must not cross other wiring (see figure 18).

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Input/Output

The HD404344R series and HD4074344 MCU has 22 input/output pins (D_0–D_5, $R0_0$–$R3_3$) and the HD404394 MCU has 21 input/output pins (D_0–D_5, $R0_0$–$R2_3$, $R3_1$–$R3_3$). These input/output pins have the following features:

- All 22 pins for the HD404344R series and HD4074344 have a CMOS output circuit. Ten pins D_1, D_2, and $R1_0$–$R2_3$ are large current input/output pins.
- Three input/output pins of the 21 pins on the HD404394 series, $R1_0$–$R1_2$, have intermediate-voltage NMOS open drain output circuits. Five other input/output pins, $R1_3$ and $R2_0$–$R2_3$, have standard-voltage NMOS open drain output circuits. The remaining 13 input/output pins, D_0–D_5, $R0_0$–$R0_3$ and $R3_1$–$R3_3$, have CMOS output circuits.
  Ten pins D_1, D_2, and $R1_0$–$R2_3$ are high-current input/output pins.
- Some input/output pins are multiplexed with peripheral functions, such as for the timers and serial interface. For these pins, the settings for peripheral functions are done prior to the D or R ports settings. If these pins are set as peripheral functions, the pin functions and input/output selections automatically switch according to the settings.
- Program control of input/output port selection, as well as peripheral function selection.
- All peripheral function output pins are CMOS output pins. However, the $R0_2$/SO pin can be programmed to be NMOS open drain output.
- In stop mode, all peripheral function selections are cleared because of the MCU being reset. Also, the input/output pins go into a high-impedance state.
- All input/output pins for both the HD404344R series, HD4074344 and the HD404394 series except for pins $R1_0$–$R2_3$, have built-in pull-up MOS. Therefore they can be individually turned on or off by software.
- When pin functions are set as peripheral functions after selecting the pins as pull-up MOS, the pins are maintained as pull-up MOS from the time of selection. Also, pull-up MOS can be selected by software after setting the pin functions as peripheral functions. The control of the input/output pins are shown in table 17 and the circuit configuration of each input/output pin is shown in table 18.

Table 17 Programmable Control of Standard I/O Pins

MIS3 (bit 3 of MIS)		**0**				**1**			
DCD, DCR		**0**		**1**		**0**		**1**	
PDR		**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**
CMOS buffer	PMOS	—	—	—	On	—	—	—	On
	NMOS	—	—	On	—	—	—	On	—
Pull-up MOS		—	—	—	—	—	On	—	On

Note: — indicates off.

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Table 18 Circuit Configurations of I/O Pins

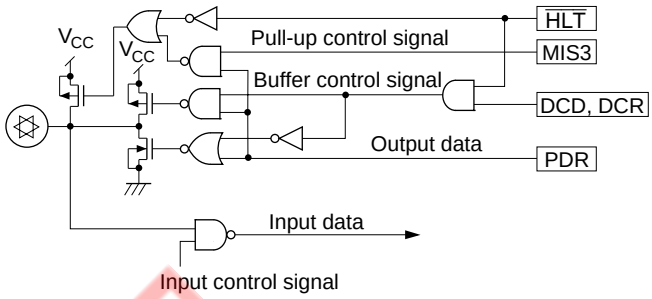
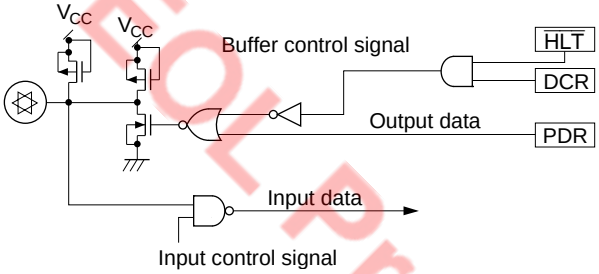
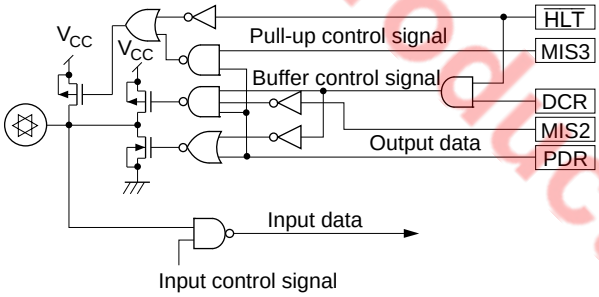
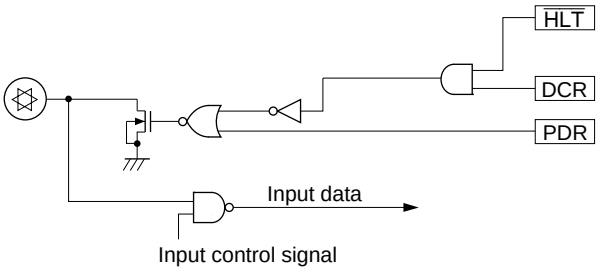
I/O Pin Type	Circuit	Pins: HD404344R Series, HD4074344	Pins: HD404394 Series
Input/output pins		D_0–D_5, $R0_0$, $R0_1$ $R0_3$, $R1_0$–$R3_3$	D_0–D_5, $R0_0$, $R0_1$ $R0_3$, $R3_1$–$R3_3$
		None	$R1_3$, $R2_0$–$R2_3$ (standard voltage pins)
		$R0_2$	$R0_2$
		None	$R1_0$–$R1_2$ (middle voltage pins)

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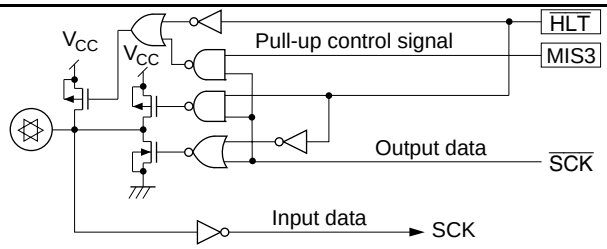
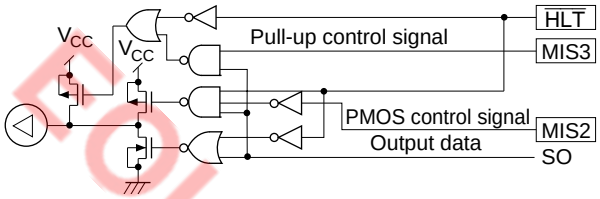
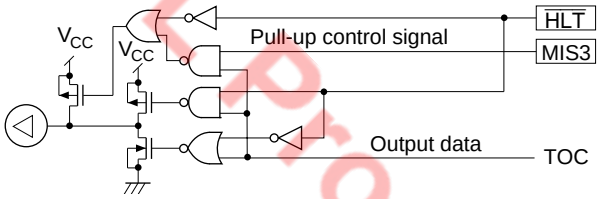
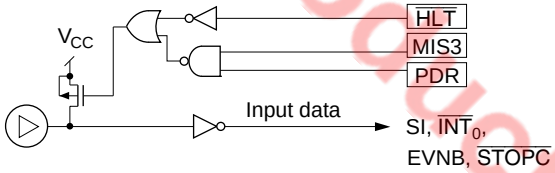
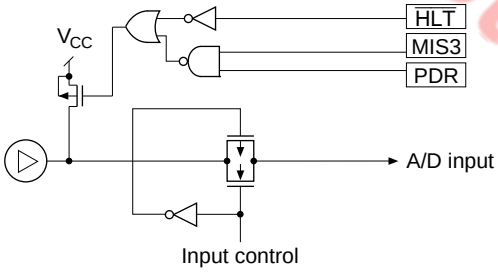
Table 18 Circuit Configurations of I/O Pins (cont)

I/O Pin Type		Circuit	Pins: HD404344R Series, HD4074344	Pins: HD404394 Series
Peripheral function pins	Input/ output pins		$\overline{SCK}$	$\overline{SCK}$
	Output pins		SO	SO
			TOC	TOC
	Input pins		SI, $\overline{INT_0}$, EVNB, $\overline{STOPC}$	SI, $\overline{INT_0}$, EVNB, $\overline{STOPC}$
			AN_0–AN_3	AN_1–AN_3

Note: In stop mode, the MCU is reset and the peripheral function selection is cancelled. Also, the $\overline{HLT}$ signal goes low, and input/output pins enter a high-impedance state.

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D Port

The D port consists of six input/output pins each addressed by one bit.

The D ports can be set and reset by SED/RED and SEDD/REDD instructions. Output data is stored in the port data register (PDR) for each pin. Also, all D ports can tested by the TD/TDD instructions.

The on/off status of the output buffers is controlled by the D-port data control registers (DCD0, DCD1: $02C and $02D), which are mapped to memory addresses (figure 19).

Pins D_0 and D_4 are multiplexed with peripheral function pins $\overline{INT_0}$/EVNB, and $\overline{STOPC}$. Setting of the peripheral functions for these pins is executed by bits 3 and 0 (PMRB3, PMRB0) of port mode register B (PMRB: $024) (figure 20).

Data control register

DCD0, DCD1 **(DCD0, DCD1: $02C, $02D)**
DCR0 to DCR3 **(DCR0 to DCR3: $030 to $033)**

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	DCD03	DCD02	DCD01 to DCD11	DCD00 to DCD10
	DCR03 to DCR33	DCR02 to DCR32	DCR01 to DCR31	DCR00 to DCR30

Bits 0 to 3	CMOS Buffer Control
0	CMOS buffer off (high impedance)
1	CMOS buffer on

Correspondence between ports and DCR bits

Register	Bit 3	Bit 2	Bit 1	Bit 0
DCD0	D_3	D_2	D_1	D_0
DCD1	—	—	D_5	D_4
DCR0	$R0_3$	$R0_2$	$R0_1$	$R0_0$
DCR1	$R1_3$	$R1_2$	$R1_1$	$R1_0$
DCR2	$R2_3$	$R2_2$	$R2_1$	$R2_0$
DCR3	$R3_3$	$R3_2$	$R3_1$	$R3_0$*

Note: * Available for the HD404344R series and HD4074344, but not available for the HD404394 series.

Figure 19 Data Control Register (DCR)

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Port mode register B (PMRB: $024)

Bit	3	2	1	0
Initial value	0	—	—	0
Read/Write	W	—	—	W
Bit name	PMRB3	Not used	Not used	PMRB0

PMRB3	D_4/$\overline{STOPC}$ Mode Selection
0	D_4
1	$\overline{STOPC}$

PMRB0	D_0/$\overline{INT_0}$ /EVNB Mode Selection
0	D_0
1	$\overline{INT_0}$ /EVNB

Figure 20 Port Mode Register B (PMRB)

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R Port

The R port consists of input/output pins each addressed by 4 bits. Input/output is controlled by the LAR and LBR instructions and the LRA and LRB instructions. The output data is stored in the port data register (PDR) of each pin. The on/off status of the output buffers is controlled by the R-port data control registers (DCR0–DCR3: $030–$033), which are mapped to memory addresses (figure 19).

The $R1_0$–$R1_2$ ports of the HD404394 series are n-channel middle-voltage open drain input/output pins.

The $R0_0$–$R0_3$ pins are also used as peripheral function pins: $\overline{SCK}$, SI, SO, and TOC. Setting of the peripheral functions for these pins is executed by bit 3 (SMR3) of the serial mode register (SMR:$005) and by bits 2 to 0 (PMRA2–PMRA0) of port mode register A (PMRA: $004), as shown in figures 21 and 22.

The $R3_0$–$R3_3$ pins of the HD404344R series and HD4074344 are also used as AN_0–AN_3 peripheral function pins. Pins $R3_1$–$R3_3$ of the HD404394 series are also used as AN_1–AN_3 peripheral function pins. The setting of peripheral functions for these pins is executed by bits 3 to 0 (AMR13–AMR10) of A/D mode register 1 (AMR1: $019). For the HD404394 series, the use of AMR10 is prohibited (figure 23).

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Port mode register A (PMRA: $004)

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	W	W	W
Bit name	Not used	PMRA2	PMRA1	PMRA0

PMRA2	$R0_3$/TOC Mode Selection
0	$R0_3$
1	TOC

PMRA0	$R0_2$/SO Mode Selection
0	$R0_2$
1	SO

PMRA1	$R0_1$/SI Mode Selection
0	$R0_1$
1	SI

Figure 21 Port Mode Register A (PMRA)

Serial mode register (SMR: $005)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	SMR3	SMR2	SMR1	SMR0

SMR3	$R0_0/\overline{SCK}$ Mode Selection
0	$R0_0$
1	$\overline{SCK}$

SMR2	SMR1	SMR0	$\overline{SCK}$	Clock Source	Prescaler Division Ratio
0	0	0	Output	Prescaler	See table 22.
		1			
	1	0			
		1			
1	0	0			
		1			
	1	0	Output	System clock	—
		1	Input	External clock	—

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Figure 22 Serial Mode Register (SMR)

A/D mode register 1 (AMR1: $019)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	AMR13	AMR12	AMR11	AMR10

AMR12	$R3_2/AN_2$ Mode Selection
0	$R3_2$
1	AN_2

AMR13	$R3_3/AN_3$ Mode Selection
0	$R3_3$
1	AN_3

AMR10*	$R3_0/AN_0$ Mode Selection
0	$R3_0$
1	AN_0

AMR11	$R3_1/AN_1$ Mode Selection
0	$R3_1$
1	AN_1

Note: * Available for the HD404344R series and HD4074344, but not available for the HD404394 series.

Figure 23 A/D Mode Register 1 (AMR1)

Pull-Up MOS Transistor Control

Pull-up MOS, which can be controlled by software, is built into all input/output pins except $R1_0$–$R2_3$ of the HD404394 series.

The on/off status of all pull-up MOS pins is controlled by bit 3 (MIS3) of the miscellaneous register (MIS: $00C) and the port data registers (PDR) of each pin. Each pin can therefore independently switch between with or without pull-up MOS (table 17 and figure 24).

The on/off status of each transistor and the peripheral function mode of each pin can be set independently.

Miscellaneous register (MIS: $00C)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	MIS3	MIS2	MIS1	MIS0

MIS3	Pull-Up MOS On/Off Selection
0	Pull-up MOS off
1	Pull-up MOS on

MIS2	PMOS On/Off Selection for Pin $R0_2$/SO
0	On
1	Off

Programming MIS1 and MIS0 to 1 is prohibited.

Figure 24 Miscellaneous Register

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How to Deal with Unused I/O Pins

When input/output pins are not being used and are left floating, it is necessary to set these pins to V_{CC} to reduce the possibility of LSI malfunctions due to noise. This can be done by selecting pull-up MOS for the pins or by connecting an external pull-up resistor of about 100 kΩ at each unused pin.

Prescaler

The MCU has one built-in prescaler, S (PSS). This divides the system clock and outputs the divided clock to the peripheral function modules as shown in figure 25.

Clocks for timers B and C except for external events, and clocks for serial interface except for the external clock are all selected from the prescaler output by programming each mode register.

Prescaler S is an 11-bit counter which inputs the system clock. After an MCU reset clears the prescaler to $000, it begins dividing the system clock. Prescaler S stops operating due to either an MCU reset or stop mode. It cannot be stopped by any other mode.

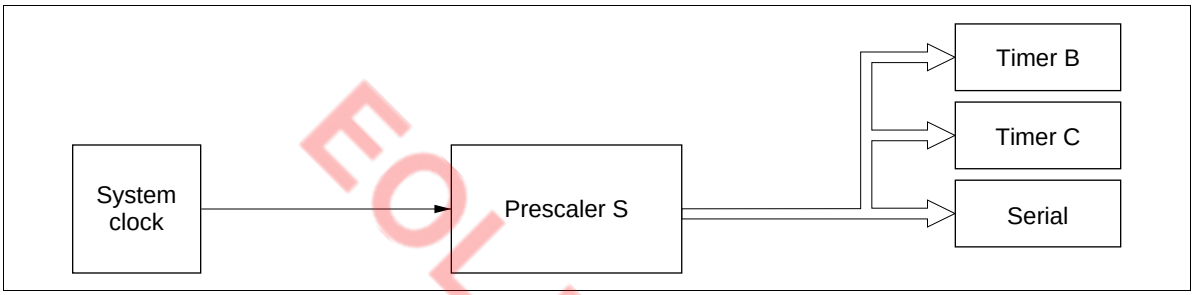

Figure 25 Prescaler Output Supply

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Timers

The MCU has two built-in timers, B and C. The functions of each timer are listed in table 19.

Table 19 Timer Functions

Functions		Timer B	Timer C
Clock source	Prescaler S	Available	Available
	External event	Available	—
Timer functions	Free-running	Available	Available
	Event counter	Available	—
	Reload	Available	Available
	Watchdog	—	Available
Timer output	PWM	—	Available

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Timer B

Timer B is an 8-bit multifunction timer that includes free-running, reload, and event counter features. These are described as follows.

- By setting timer mode register B1 (TMB1: $009), one of seven internal clocks supplied from prescaler S can be selected, or timer B can be used as an external event counter.
- By setting timer mode register B2 (TMB2: $026), timer B can be incremented by each edge detector of input signals at pin EVNB.
- By setting timer write register BL, BU (TWBL, TWBU: $00A, $00B), timer counter B (TCB) can be written to during reload timer operation.
- By setting timer read register BL, BU (TRBL, TRBU: $00A, $00B), the contents of timer counter B can be read out.

Timer B Operation

- Free-running/reload timer operation: The selection of the free-running/reload timer, input clock source, and prescaler division ratio is done by timer mode register B1 (TMB1: $009).

  Timer B is initialized to the data which is written to timer write register B (TWBL: $00A, TWBU: $00B) by software. The data is then incremented in steps of 1 by using the input clock. If the clock input is continued after timer B is set to $FF, an overflow occurs. Timer B then begins counting again, setting the timer to the value in timer write register B (TWBL: $00A, TWBU: $00B) when the reload timer is selected, or reset to $00 when the free-running timer is selected.

The timer B interrupt request flag is set by an overflow. Resetting the timer B interrupt request flag (IFTB: $002, bit 0) is executed by either software or by an MCU reset.

- External event counter operation: By setting the external event input as an input clock source, timer B can operate as an external event counter. The $D_0/\overline{INT}_0$/EVNB pins are set to be $\overline{INT}_0$/EVNB pins by port mode register B (PMRB: $024).

  The detection edge of the external event counter for timer B is selected as rising edge, falling edge, or rising/falling edge by timer mode register B2 (TMB2: $026). When the rising/falling edge is selected, the period must be set to more than $2t_{cyc}$ between the falling edge and the rising edge.

  Timer B is incremented by 1 using the edge selection in timer mode register B2 (TMB2: $026). Other functions are based on the free-running/reload timer.

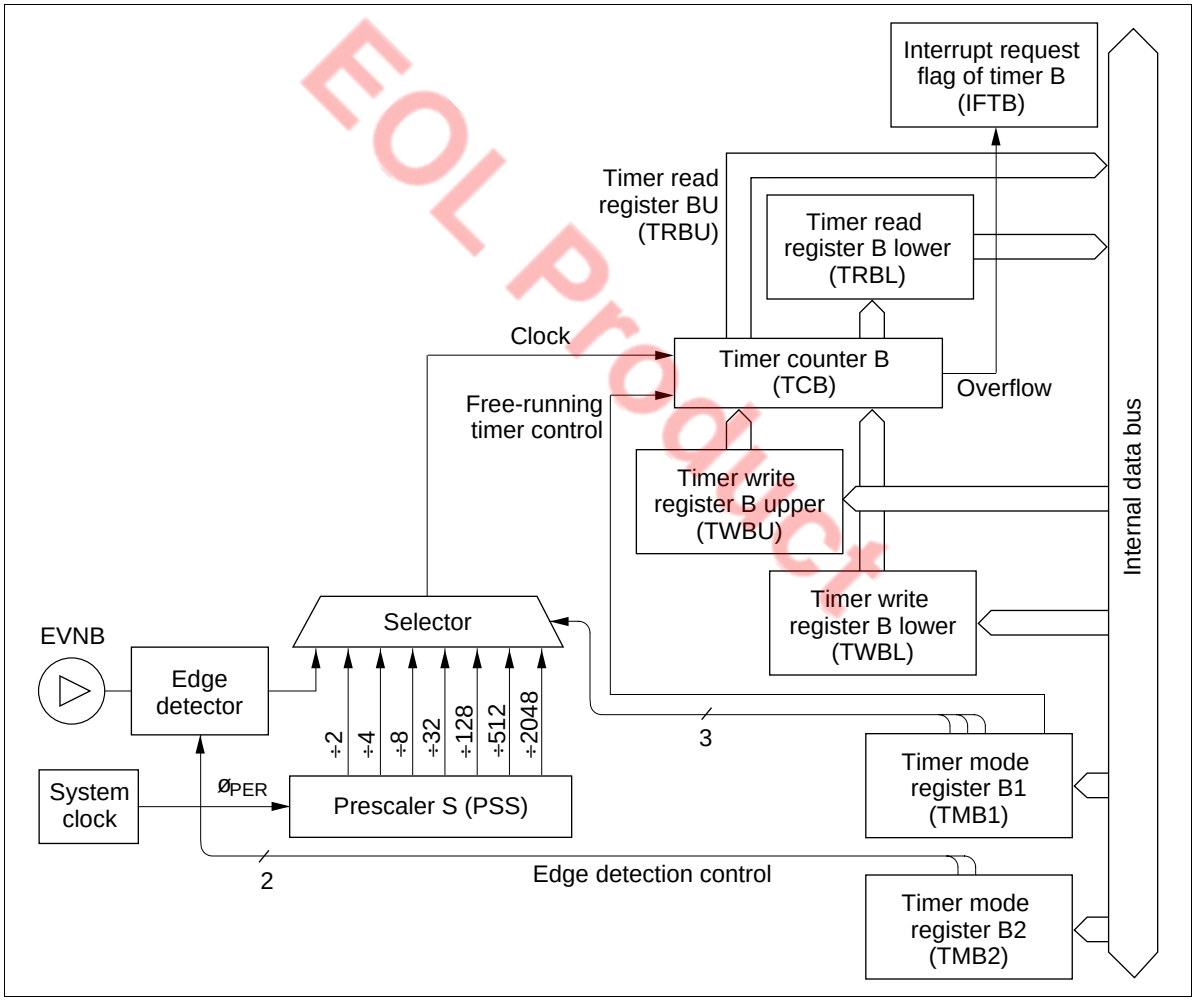

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Figure 26 Timer B Free-Running and Reload Operation Block Diagram

Using Timer B Registers

Timer B sets the operation and the read/write data according to the following registers.

- Timer mode register B1 (TMB1: $009)
- Timer mode register B2 (TMB2: $026)
- Timer write register B
- (TWBL: $00A, TWBU: $00B)
- Timer read register B
- (TRBL: $00A, TRBU: $00B)
- Port mode register B (PMRB: $024)

- Timer mode register B1 (TMB1: $009): Four-bit write-only register that selects the free-running/reload timer, input clock, and prescaler division ratio, as shown in figure 27. It is reset to $0 by an MCU reset. Data written to timer mode register B1 is valid after two instruction cycles. The initial setting of timer B, which is set by writing to timer write register B (TWBL: $00A, TWBU: $00B), should be programmed only after a mode change has been effective.

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Timer mode register B1 (TMB1: $009)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TMB13	TMB12	TMB11	TMB10

TMB13	Free-Running/Reload Timer Selection
0	Free-running timer
1	Reload timer

TMB12	TMB11	TMB10	Input Clock Period and Input Clock Source
0	0	0	$2048t_{cyc}$
		1	$512t_{cyc}$
	1	0	$128t_{cyc}$
		1	$32t_{cyc}$
1	0	0	$8t_{cyc}$
		1	$4t_{cyc}$
	1	0	$2t_{cyc}$
		1	$D_0/\overline{INT}_0$/EVNB (external event input)

Figure 27 Timer Mode Register B1 (TMB1)

- Timer mode register B2 (TMB2: $026): Two-bit write-only register that sets the input edge detection of pin EVNB, as shown in figure 28. It is reset to $0 by an MCU reset.

Timer mode register B2 (TMB2: $026)

Bit	3	2	1	0
Initial value	—	—	0	0
Read/Write	—	—	W	W
Bit name	Not used	Not used	TMB21	TMB20

TMB21	TMB20	EVNB Edge Detection Selection
0	0	No detection
	1	Falling-edge detection
1	0	Rising-edge detection
	1	Rising- and falling-edge detection

Figure 28 Timer Mode Register B2 (TMB2)

- Timer write register B (TWBL: $00A, TWBU: $00B): Write-only register consisting of the lower digit (TWBL) and the upper digit (TWBU). The lower digit is reset to $0 by MCU reset, but the upper digit value cannot be guaranteed. See figures 29 and 30.
  Timer B is initialized by writing to timer write register B (TWBL: $00A, TWBU: $00B). In this case, the lower digit (TWBL) must be written to first, but writing only to the lower digit does not change the timer B value. Timer B is initialized to the value in timer write register B at the same time the upper digit (TWBU) is written to. When timer write register B is written to again and if the lower digit value needs no change, writing only to the upper digit initializes timer B.

Timer write register B (lower) (TWBL: $00A)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TWBL3	TWBL2	TWBL1	TWBL0

Figure 29 Timer Write Register B (lower) (TWBL)

Timer write register B (upper) (TWBU: $00B)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	W	W	W	W
Bit name	TWBU3	TWBU2	TWBU1	TWBU0

Figure 30 Timer Write Register B (upper) (TWBU)

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- Timer read register B (TRBL: $00A, TRBU: $00B): Read-only register consisting of the lower digit (TRBL) and the upper digit (TRBU) that holds the count of the timer B upper digit. See figures 31 and 32.

  The upper digit (TRBU) must be read first. At this time, the count of the timer B upper digit is obtained, and the count of the timer B lower digit is latched to the lower digit (TRBL). After this, by reading TRBL, the count of timer B when TRBU is read can be obtained.

Timer read register B (lower) (TRBL: $00A)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRBL3	TRBL2	TRBL1	TRBL0

Figure 31 Timer Read Register B (lower) (TRBL)

Timer read register B (upper) (TRBU: $00B)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRBU3	TRBU2	TRBU1	TRBU0

Figure 32 Timer Read Register B (upper) (TRBU)

- Port mode register B (PMRB: $024): Write-only register that selects the $D_0/\overline{INT}_0$/EVNB pin as shown in figure 20. It is reset to $0 by an MCU reset.

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Timer C

Timer C is an 8-bit multifunction timer that includes free-running, reload, and watchdog timer features, which are selected and described as follows.

- By setting timer mode register C (TMC: $00D), one of eight internal clocks supplied from prescaler S can be selected.
- By selecting pin TOC with bit 2 (PMRA2) of port mode register A (PMRA: $004), timer C output (PWM output) is enabled.
- By setting timer write register CL, CU (TWCL, TWCU: $00E, $00F), timer counter C (TCC) can be written to.
- By setting timer read register CL, CU (TRCL, TRCU: $00E, $00F), the contents of timer counter C can be read out.
- An interrupt can be requested when timer counter C overflows.
- Timer counter C can be used as a watchdog timer for detecting runaway programs.

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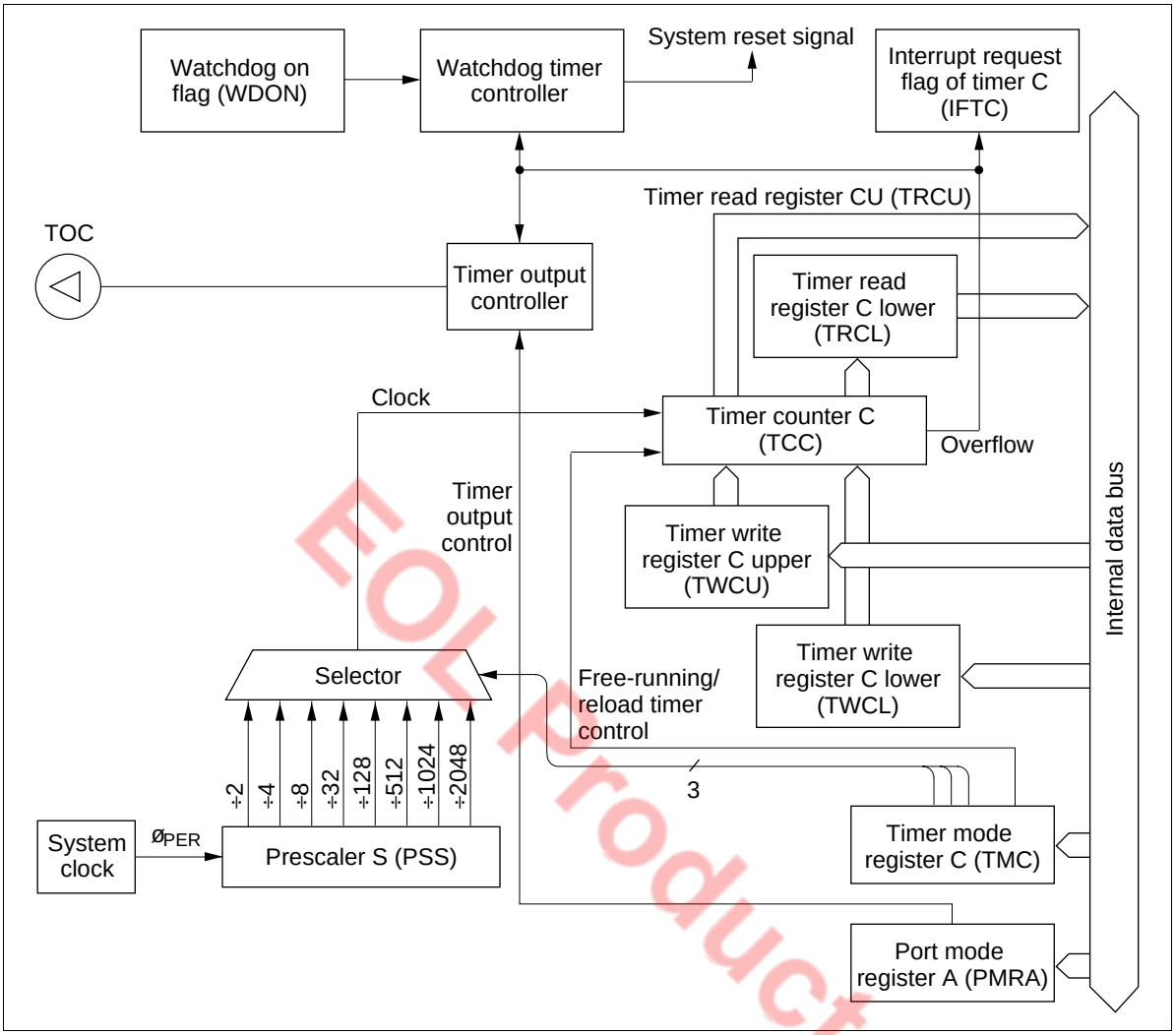

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Figure 33 Timer C Block Diagram

Timer C Operation

- Free-running/reload timer operation: The selection of the free-running/reload timer, input clock source, and prescaler division ratio is done by timer mode register C (TMC: $00D).

  Timer C is initialized to the data, which is written to timer write register C (TWCL: $00E, TWCU: $00F) by software. The data is then incremented in steps of 1 by using the input clock. If the clock input is continued after timer C is set to $FF, an overflow occurs. Timer C then begins counting again, setting the timer to the value in timer write register C (TWCL: $00E, TWCU: $00F) when the reload timer is selected, or reset to $00 when the free-running timer is selected.

  The timer C interrupt request flag is set by an overflow. Resetting the timer C interrupt request flag (IFTC: $002, bit 2) is executed by either software or by an MCU reset.

- Watchdog timer operation: Timer C can be used as a watchdog timer for programs that may run out of control. A watchdog timer is enabled when the setting on the watchdog on flag (WDON: $020, bit 1) is 1. When timer C overflows, an MCU reset occurs. This usually controls programs running out of control by initializing timer C through software before timer C counts up to $FF (figure 34).

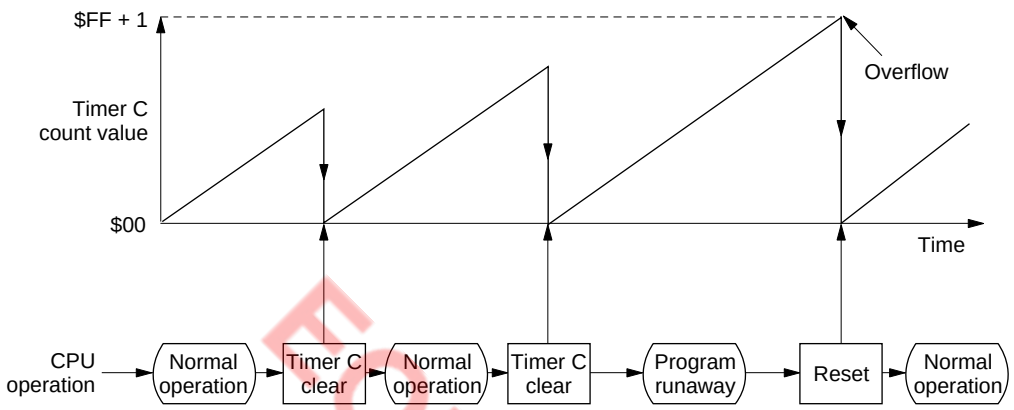
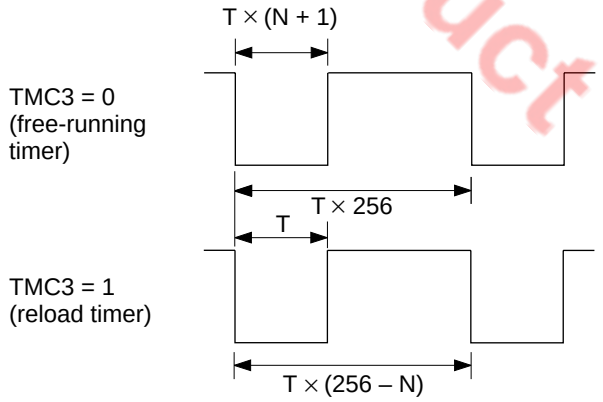


Figure 34 Watchdog Timer Operation Flowchart

- Timer output operation: Timer C can select the timer output mode by selecting the TOC pin after setting bit 2 (PMRA2) of port mode register A (PMRA: $004) to 1. The output of the TOC pin is initialized to 0 by an MCU reset. PWM output is a pulse output function of variable duty. The output wave differs by the contents of timer mode register C and timer write register C, as shown in figure 35.



Notes: T: Input clock period supplied to counter. (The clock input source and system clock division ratio are determined by timer mode register C.)
N: Value in timer write register C. (When N = 255 ($FF), PWM output is fixed low.)

Figure 35 PWM Output Waveform

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Using Timer C Registers

Timer C sets the operation and the read/write data according to the following registers.

— Timer mode register C (TMC: $00D)
— Timer write register C (TWCL: $00E, TWCU: $00F)
— Timer read register C (TRCL: $00E, TRCU: $00F)

- Timer mode register C (TMC: $00D): Four-bit write-only register that selects the free-running/reload timer, input clock, and prescaler division ratio, as shown in figure 36. It is reset to $0 by an MCU reset. The data written to timer mode register C is valid after two instructions cycles. The initial setting of timer C, which is set by writing to timer write register C (TWCL: $00E, TWCU: $00F), should be programmed to execute only after a mode change has been effective.

Timer mode register C (TMC: $00D)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TMC3	TMC2	TMC1	TMC0

TMC3	Free-Running/Reload Timer Selection
0	Free-running timer
1	Reload timer

TMC2	TMC1	TMC0	Input Clock Period
0	0	0	$2048t_{cyc}$
		1	$1024t_{cyc}$
	1	0	$512t_{cyc}$
		1	$128t_{cyc}$
1	0	0	$32t_{cyc}$
		1	$8t_{cyc}$
	1	0	$4t_{cyc}$
		1	$2t_{cyc}$

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Figure 36 Timer Mode Register C (TMC)

- Timer write register C (TWCL: $00E, TWCU: $00F): Write-only register consisting of a lower digit (TWCL: $00E) and an upper digit (TWCU: $00F), as shown in figures 37 and 38.

  The operation of this register is the same as that of timer write register B.

Timer write register C (lower) (TWCL: $00E)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	TWCL3	TWCL2	TWCL1	TWCL0

Figure 37 Timer Write Register C (lower) (TWCL)

Timer write register C (upper) (TWCU: $00F)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	W	W	W	W
Bit name	TWCU3	TWCU2	TWCU1	TWCU0

Figure 38 Timer Write Register C (upper) (TWCU)

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- Timer read register C (TRCL: $00E, TRCU: $00F): Read-only register consisting of a lower digit (TRCL: $00E) and upper digit (TRCU: $00F), which allows the upper digit of timer C to be read directly (figures 39 and 40).

  The operation of this register is the same as that of timer read register B.

Timer read register C (lower) (TRCL: $00E)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRCL3	TRCL2	TRCL1	TRCL0

Figure 39 Timer Read Register C (lower) (TRCL)

Timer read register C (upper) (TRCU: $00F)

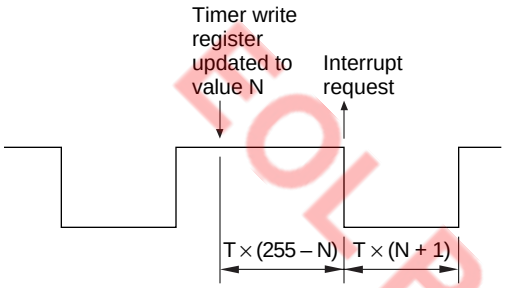
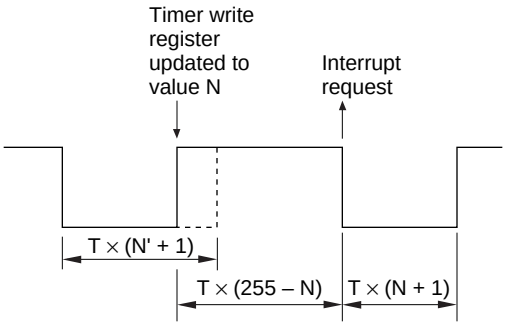
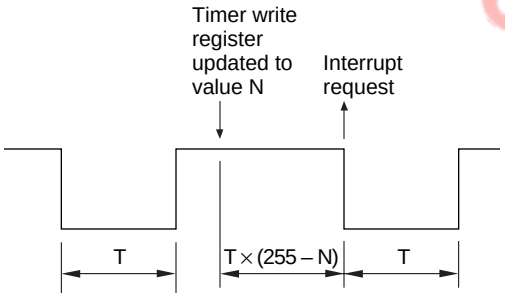
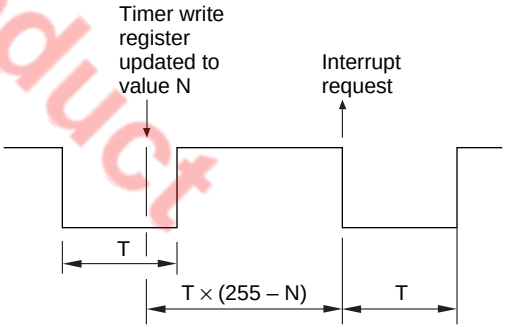
Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R	R	R	R
Bit name	TRCU3	TRCU2	TRCU1	TRCU0

Figure 40 Timer Read Register C (upper) (TRCU)

Notes on Use

When using the timer output as PWM output, note the following point. From the update of the timer write register until the occurrence of the overflow interrupt, the PWM output differs from the period and duty settings, as shown in table 20. The PWM output should therefore not be used until after the overflow interrupt following the update of the timer write register. After the overflow, the PWM output will have the set period and duty cycle.

Table 20 PWM Output Following Update of Timer Write Register

Mode	PWM Output: Timer Write Register is Updated during High PWM Output	PWM Output: Timer Write Register is Updated during Low PWM Output
Free running		
Reload		

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Serial Interface

The MCU has a one-channel 8-bit serial interface built in with the following features.

- One of 12 different internal clocks or an external clock can be selected as the transmit clock. The internal clocks include the six prescaler outputs divided by two and by four, and the system clock.
- During idle states, the serial output pin can be controlled as high or low output.
- Transmit clock errors can be detected.
- An interrupt request can be generated when any errors occurred or data transfer has completed.

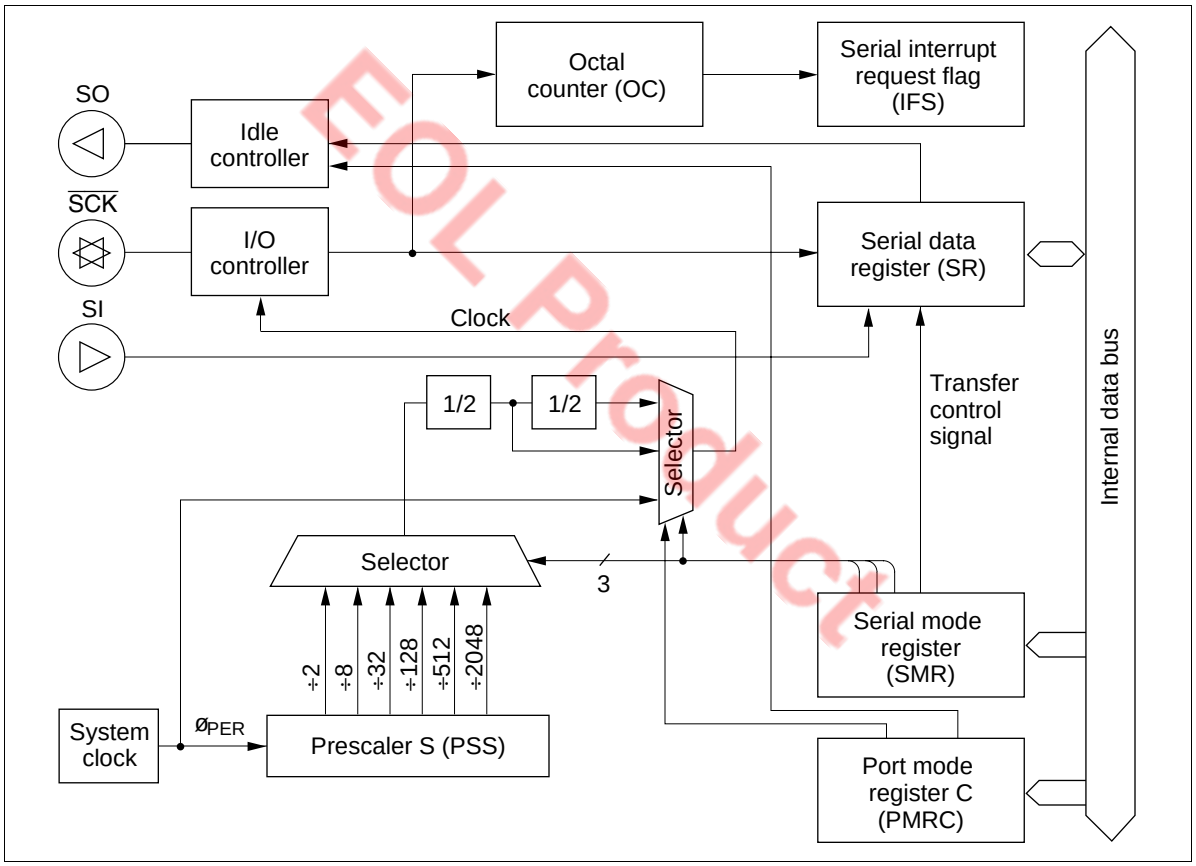

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Figure 41 Serial Interface Block Diagram

Serial Interface Operation

Selection and Changing of Serial Interface Operation Mode: The available settings for port mode register A (PMRA: $004) and the serial mode register (SMR: $005) are shown in table 21. To change the operating mode or to initialize the serial interface, write to the serial mode register.

The $R0_0/\overline{SCK}$ pin is controlled by writing data to serial mode register (SMR: $005). The $R0_1$/SI and $R0_2$/SO pins are controlled by writing data to port mode register A (PMRA: $004).

Table 21 Serial Interface Operating Modes

SMR	PMRA		
Bit 3	Bit 1	Bit 0	Operating Mode
1	0	0	Continuous clock output mode
		1	Transmit mode
	1	0	Receive mode
		1	Transmit/receive mode

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Setting Serial Clock Source: The transmit clock is set by writing to the serial mode register (SMR: $005) and port mode register C (PMRC: $025).

Serial Data Setting: Serial data is sent by writing to the serial data register (SRL: $006 and SRU: $007). Serial data can then be obtained by reading the serial data register. Serial data is shifted by the transmit clock.

The output of the SO pin is undefined until the first serial data is output after an MCU reset, or until the output level control is performed during an idle state.

Transfer Control: Serial interface operation is initiated by an STS instruction. The octal counter is reset by the STS instruction to 000 and then incremented by one by the rising edge of the transmit clock. If eight rising edges from the transmit clock is input or the serial data transfer is cut-off, the counter is reset to 000, the serial interrupt request flag (IFS: $003, bit 2) is set, and the serial data transfer stops.

As for using the built-in prescaler output for the transmit clock, selection for the transmit clock frequency can be from $4t_{cyc}$ to $8192t_{cyc}$ by setting bits 2 to 0 (SMR2–SMR0) of the serial mode register (SMR: $005) and bit 0 (PMRC0) of port mode register C (PMRC: $025). Writing to these registers for the setting of the transmit clock is shown in table 22.

Table 22 Transmit Clock Selection (Prescaler Output)

PMRC	SMR				
Bit 0	**Bit 2**	**Bit 1**	**Bit 0**	**Prescaler Division Ratio**	**Transmit Clock Frequency**
0	0	0	0	÷ 2048	$4096t_{cyc}$
			1	÷ 512	$1024t_{cyc}$
		1	0	÷ 128	$256t_{cyc}$
			1	÷ 32	$64t_{cyc}$
	1	0	0	÷ 8	$16t_{cyc}$
			1	÷ 2	$4t_{cyc}$
1	0	0	0	÷ 4096	$8192t_{cyc}$
			1	÷ 1024	$2048t_{cyc}$
		1	0	÷ 256	$512t_{cyc}$
			1	÷ 64	$128t_{cyc}$
	1	0	0	÷ 16	$32t_{cyc}$
			1	÷ 4	$8t_{cyc}$

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Serial Interface Operating States: The serial interface has the following operating states shown in figure 42, both in external clock mode and internal clock mode.

— STS wait state
— Transmit clock wait state
— Transfer state
— Continuous clock output (internal clock mode only)

- STS wait state: The serial interface is put into the STS wait state by an MCU reset (00, 10 in figure 42). While in this state, the serial interface is initialized and does not operate, even if a transmit clock is provided. If an STS instruction is executed while in this state (01, 11), the serial interface transfers to the transmit clock wait state.

- Transmit clock wait state: Transmit clock wait state period starts from when an STS instruction is executed until the first transmit clock falling edge. While in the transmit clock wait state, if the transmit clock is input (02, 12), the octal counter is incremented by the transmit clock, the data in the serial data register shifts, and the serial interface enters the transfer state. However, note that if continuous clock output mode is selected in internal clock mode, the serial interface does not enter transfer state but enters continuous clock output state (17).

  By writing to the serial mode register (SMR: $005) (04, 14) while in the transmit clock wait state, the serial interface changes to the STS wait state.

- Transfer state: The transfer state period starts from the first falling edge of the transmit clock to the eighth rising edge of the transmit clock. While in the transfer state, if an STS instruction is executed or eight pulses of the transmit clock is applied, the octal counter will reset to 000 and the state will change. If an STS instruction is executed (05, 15), the state changes to the transmit clock wait state. After the

eight pulses of the transmit clock, the state changes to the transmit clock wait state for the external clock mode (03). Also, the state changes to the STS wait state for the internal clock mode (13). In the internal clock mode, the transmit clock stops after eight pulses of the transmit clock are output.

While in the transfer state, if the serial mode register (SMR: $005) (06, 16) is written to, the serial interface is initialized and the state changes to the STS wait state.

After the transfer state has changed to another state, the octal counter is reset to 000 and the serial interrupt request flag (IFS: $003, 2) is set.

- Continuous clock output state (internal clock mode only): Continuous clock output state is the state in which only the transmit clock from the $\overline{\text{SCK}}$ pin is output without data transfer. This can be done only while in internal clock mode.

  When the status of the 1 and 0 bits (PMRA1, PMRA0) of port mode register A (PMRA: $004) is 00 while in transmit clock wait state, the state can be changed to continuous clock output state by enabling the transmit clock (17). By writing to the serial mode register (SMR: $005) while in continuous clock output state (18), the state will change to the STS wait state.

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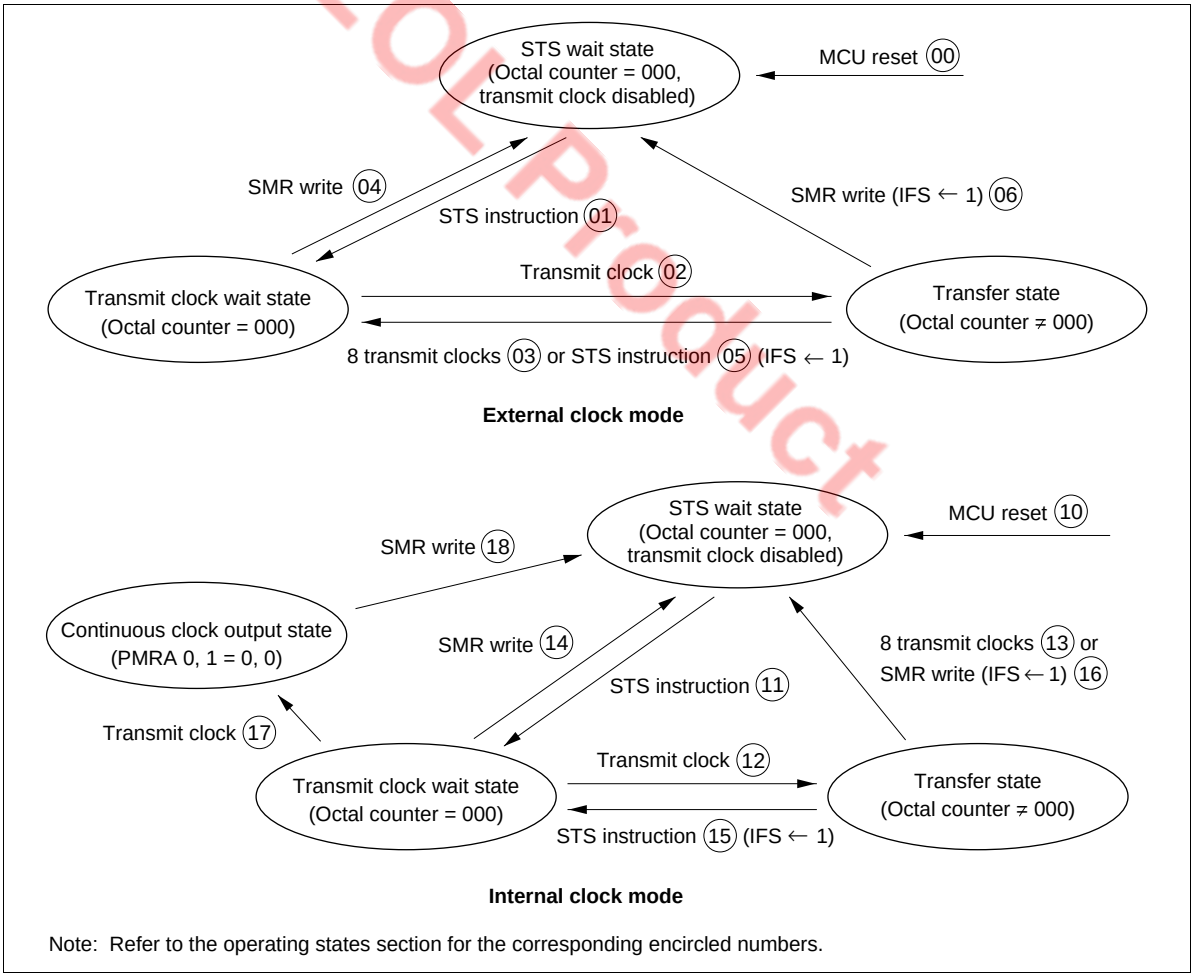

Note: Refer to the operating states section for the corresponding encircled numbers.

Figure 42 Serial Interface State Transitions

Output Level Control During Idle States: The output level of the SO pin can be set during either STS wait state or transmit clock wait state by software. During idle states, the output level is controlled by writing to bit 1 (PMRC1) of port mode register C (PMRC: $025). An example of output level control during idle states is shown in figure 43. During transfer state, output level control cannot be executed.

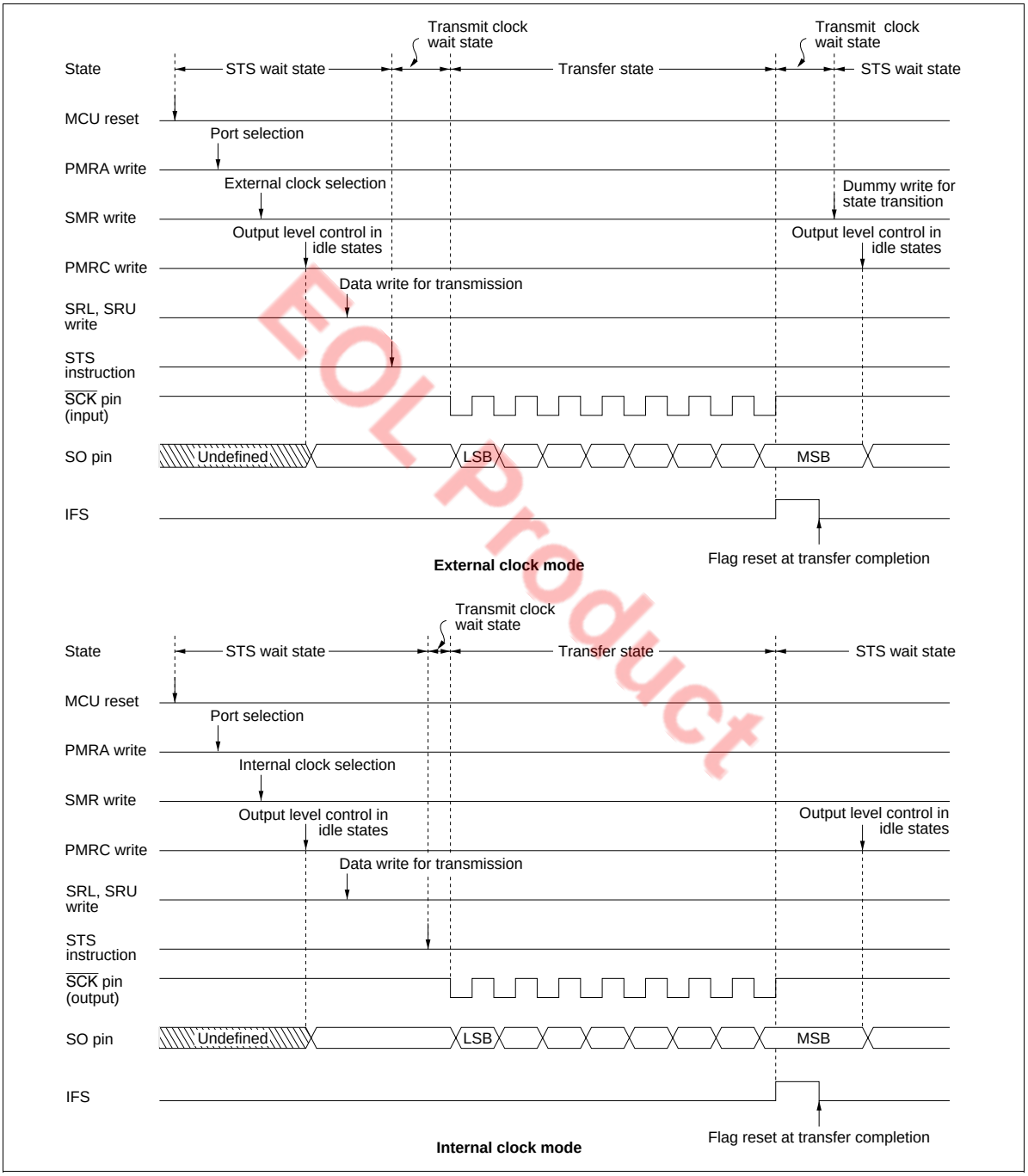

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Figure 43 Example of Serial Interface Operation Sequence

Transmit Clock Error Detection (External Clock Mode): Serial interface will malfunction if a spurious pulse caused by external noise conflicts with a normal transmit clock during data transfer. A transmit clock error of this type can be detected as shown in figure 44.

If more than eight transmit clocks are input in transfer state, at the eighth clock including a spurious pulse by noise, the octal counter reaches 000, the serial interrupt request flag (IFS: $003, bit 2) is set, and transmit clock wait state is entered. At the falling edge of the next normal clock signal, the transfer state is entered. After the transfer is completed and IFS is reset, writing to the serial mode register (SMR: $005) changes the state from transfer to STS wait. At this time the serial interface is in the transfer state, and the serial interrupt request flag (IFS: $003, bit 2) is set again, and therefore the error can be detected.

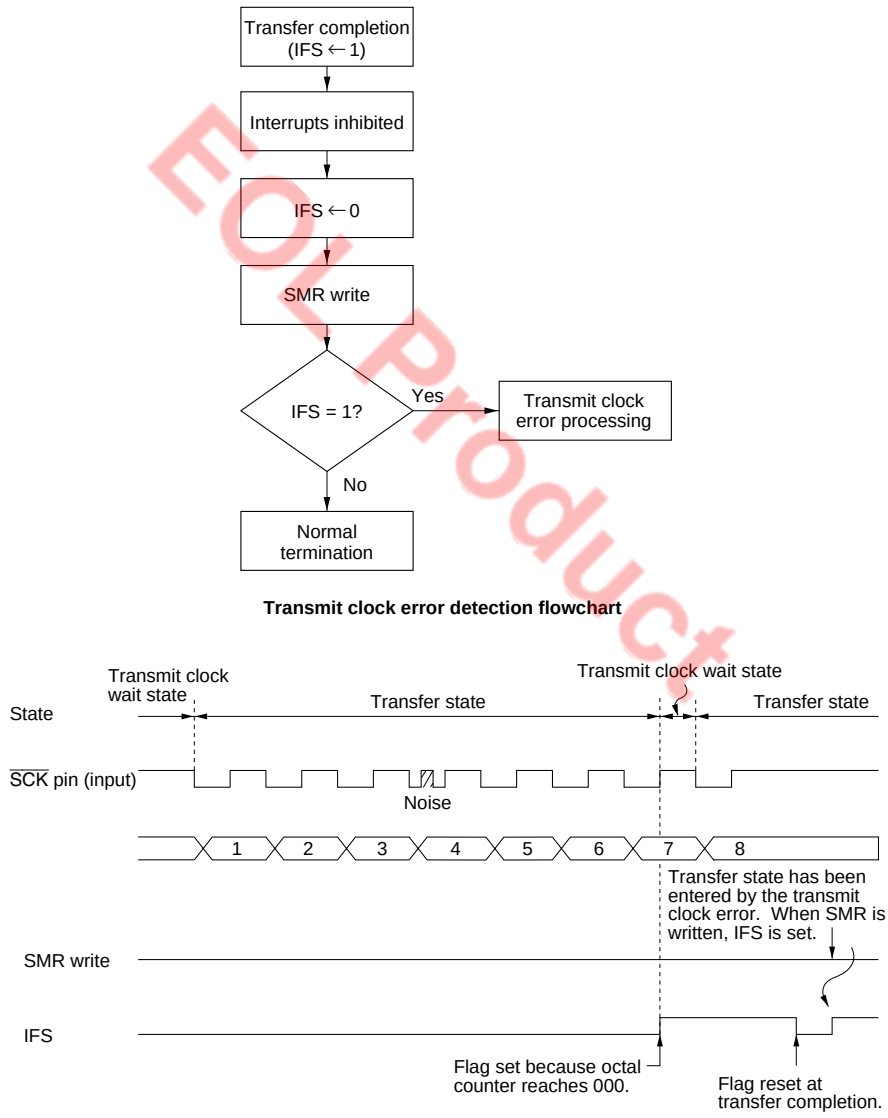

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Figure 44 Transmit Clock Error Detection

Notes On Use:

- Initializing after writing to registers: If port mode register A (PMRA: $004) is written to in the transmit clock wait state or transfer state, the serial interface should be reinitialized by writing to the serial mode register (SMR: $005).

- Serial interrupt request flag (IFS: $003, bit 2) set: For the serial interface, if the state is changed from transfer state to another by writing to serial mode register (SMR:$005) or executing the STS instruction during the first low pulse of the transmit clock, the serial interrupt request flag (IFS: $003, bit 2) is not set. To set the serial interrupt request flag (IFS: $003, bit 2), a serial mode register (SMR: $005) write or STS instruction execution must be programmed to be executed after confirming that the $\overline{SCK}$ pin is at 1, that is, after executing the input instruction to port R0.

Registers for Serial Interface

The serial interface operation is selected, and serial data is read and written using the following registers:

- Serial mode register (SMR: $005)
- Port mode register C (PMRC: $025)
- Serial data registers (SRL: $006 and SRU: $007)
- Port mode register A (PMRA: $004)
- Miscellaneous register (MIS: $00C)

Serial Mode Register (SMRA: $005): This register has the following functions (figure 45):

- $R0_0/\overline{SCK}$ pin function selection
- Selection of transmit clock
- Selection of prescaler division ratio
- Serial interface initialization

The write-only serial mode register is reset to $0 by an MCU reset. Writing to the serial mode register discontinues the transmit clock input to the serial data registers (SRL: $006 and SRU: $007) and the octal counter. The octal counter is then reset to 000. If the serial mode register is written to during serial interface operation, data transfer will be cut off and the serial interrupt request flag (IFS: $003, bit 2) will be set.

Data in the serial mode register becomes effective after two instruction execution cycles from the time the serial mode register is written to. It is therefore necessary to program the STS instruction to be executed two cycles after the serial mode register is written to.

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Serial mode register (SMR: $005)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	SMR3	SMR2	SMR1	SMR0

SMR3	$R0_0/\overline{SCK}$ Mode Selection
0	$R0_0$
1	$\overline{SCK}$

SMR2	SMR1	SMR0	$\overline{SCK}$	Clock Source	Prescaler Division Ratio
0	0	0	Output	Prescaler	See table 22.
		1			
	1	0			
		1			
1	0	0			
		1			
	1	0	Output	System clock	—
		1	Input	External clock	—

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Figure 45 Serial Mode Register (SMR)

Port Mode Register C (PMRC: $025): This register has the following functions:

- Prescaler division ratio selection
- Output level control during idle states

Port mode register C is a two-bit write-only register, which cannot be changed during data transfer.

Bit 0 (PMRC0) selects the prescaler division ratio. Only this bit is reset to 0 by an MCU reset.

Bit 1 enables the output level control of the SO pin during an idle state. The output levels at the pins are therefore changed when writing to bit 1 (PMRC1).

Port mode register C (PMRC: $025)

Bit	3	2	1	0
Initial value	—	—	Undefined	0
Read/Write	—	—	W	W
Bit name	Not used	Not used	PMRC1	PMRC0

PMRC0	Transmit Clock Division Ratio
0	Prescaler output divided by 2
1	Prescaler output divided by 4

PMRC1	Output Level Control in Idle States
0	Low level
1	High level

Figure 46 Port Mode Register C (PMRC)

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Serial Data Register (SRL: $006, and SRU: $007): This register has the following functions (figures 47 and 48):

- Transmission data write and shift
- Receive data shift and read

Data written to the serial data registers is output from the SO pin, LSB first, synchronously with the falling edge of the transmit clock.

Also, data from the SI pin (from the LSB) is input synchronously with the rising edge of the transmit clock.

Reading or writing to the serial data register should be performed after data transfer. Read/write operation to this register during data transfer does not guarantee valid data. The input/output timing chart for the transmit clock and the data are shown in figure 49.

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Serial data register (lower) (SRL: $006)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W
Bit name	SR3	SR2	SR1	SR0

Figure 47 Serial Data Register (SRL)

Serial data register (upper) (SRU: $007)

Bit	3	2	1	0
Initial value	Undefined	Undefined	Undefined	Undefined
Read/Write	R/W	R/W	R/W	R/W
Bit name	SR7	SR6	SR5	SR4

Figure 48 Serial Data Register (SRU)

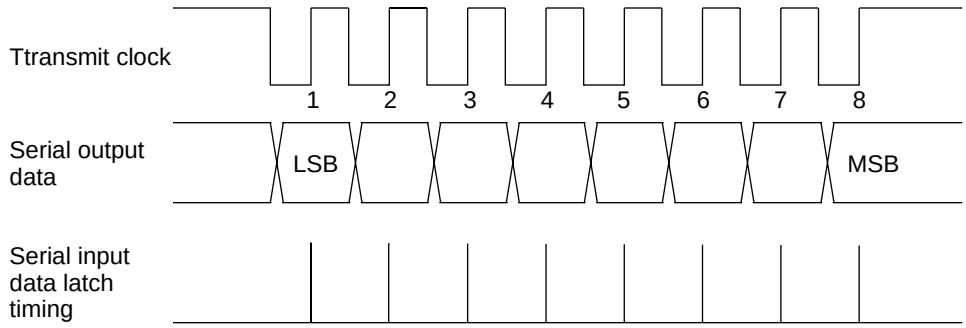


Figure 49 Serial Interface Timing

Port Mode Register A (PMRA: 004): This register A has the following functions:

- $R0_1$/SI pin function selection
- $R0_2$/SO pin function selection

Port mode register A is a three-bit write-only register and reset to 0 by an MCU reset, as listed in figure 50.

Port mode register A (PMRA: $004)

Bit	3	2	1	0
Initial value	—	0	0	0
Read/Write	—	W	W	W
Bit name	Not used	PMRA2	PMRA1	PMRA0

PMRA2	$R0_3$/TOC Mode Selection
0	$R0_3$
1	TOC

PMRA0	$R0_2$/SO Mode Selection
0	$R0_2$
1	SO

PMRA1	$R0_1$/SI Mode Selection
0	$R0_1$
1	SI

Figure 50 Port Mode Register A (PMRA)

EOL Product

Miscellaneous Register

The miscellaneous register (MIS: $00C) has the following functions:

- Control of $R0_2$/SO pin PMOS
- Pull-up MOS on/off selection

It is a two-bit write-only register and is reset to $0 by an MCU reset, as listed in figure 51.

Miscellaneous register (MIS: $00C)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	MIS3	MIS2	MIS1	MIS0

MIS3	Pull-Up MOS On/Off Selection
0	Pull-up MOS off
1	Pull-up MOS on

MIS2	PMOS On/Off Selection for Pin $R0_2$/SO
0	On
1	Off

Programming MIS1 and MIS0 to 1 is prohibited.

Figure 51 Miscellaneous Register

EOL Product

A/D Converter

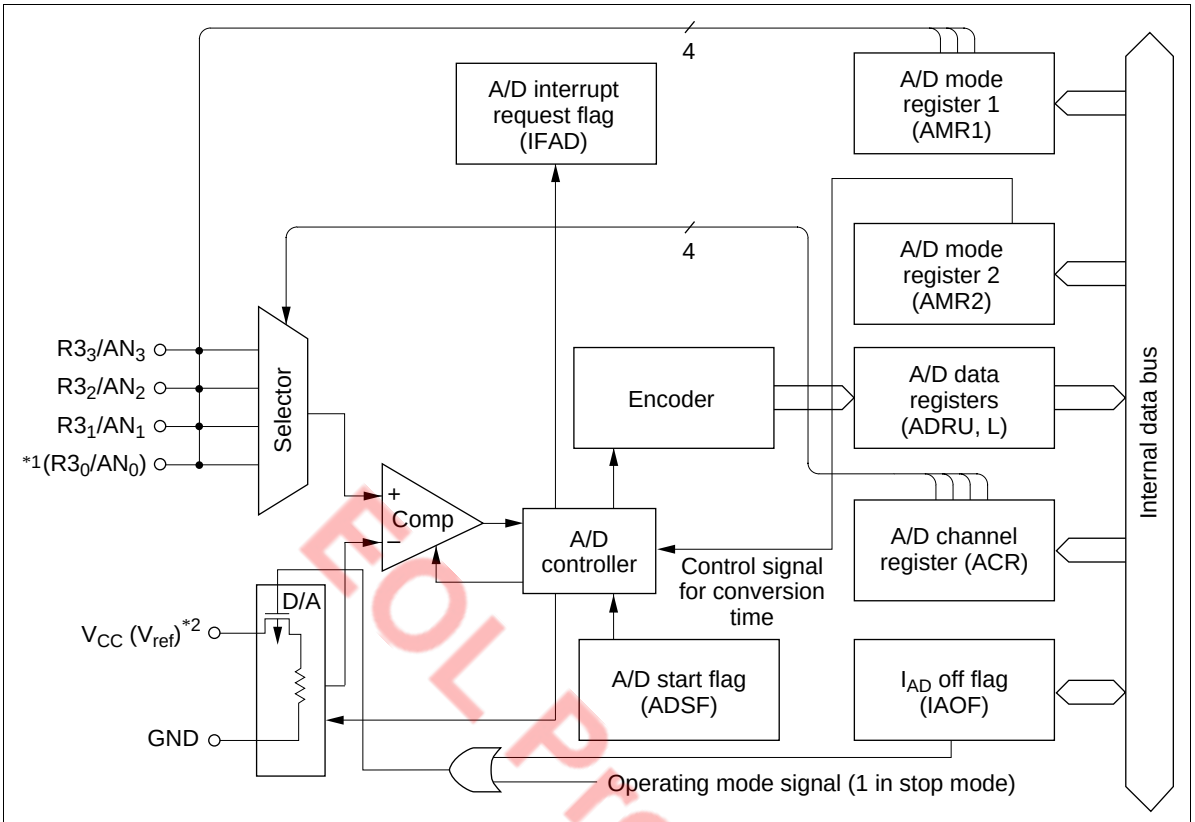
The MCU has a built-in A/D converter that uses a sequential comparison method with a register ladder. It can perform a digital conversion with 3 or 4 analog inputs at 8-bit resolution. The following describes the features of the A/D converter.

- A/D mode register 1 (AMR1: $019) is used to select digital or analog ports (figure 53).
- A/D mode register 2 (AMR2: $01A) is used to set the A/D conversion speed (figure 54).
- The A/D channel register (ACR: $016) is used to select an analog input channel (figure 55).
- A/D conversion is started by setting the A/D start flag (ADSF: $020, bit 2) to 1. After the conversion is completed, converted data is stored in the A/D data register, and at the same time, the A/D start flag is cleared to 0 (figure 56).
- By setting the I_{AD} off flag (IAOF: $021, bit 2) to 1, the current flowing through the resistance ladder can be cut off even in standby or active mode (figure 57).
- A/D data registers (ADRL: $017, ADRU: $018) are read-only registers used to store the conversion result. (ADRL: lower 4 bits, ADRU: upper 4 bits.) These registers cannot be cleared by a reset input. Also, data in these registers are not guaranteed during the conversion period. After the conversion is completed, an 8-bit result is set to these registers and kept until the next conversion starts (figures 58, 59, and 60).

Notes On Use:

- Use the SEM or SEMD instruction for writing to the A/D start flag (ADSF).
- Do not write to the A/D start flag during A/D conversion.
- Data in the A/D data register during A/D conversion is undefined.
- Since the operation of the A/D converter is based on the clock from the system oscillator, the A/D converter does not operate in stop mode. In addition, to save power dissipation while in a stop mode, all current flowing through the converter's resistance ladder is cut off.
- Output signal level from other ports should be fixed during A/D conversion.
- The port data register (PDR) is initialized to 1 by an MCU reset. At this time, if pull-up MOS is selected as active by bit 3 of the miscellaneous register (MIS3), the port will be pulled up to V_{CC}. When using a shared R port/analog input pin as an input pin, clear PDR to 0. Otherwise, if pull-up MOS is selected by MIS3 and PDR is set to 1, a pin selected by bit 1 of the A/D mode register as an analog pin will remain pulled up.

EOL product



Notes: 1. Available for the HD404344R series and HD4074344. Not available for the HD404394 series.
2. Connected to V_{CC} for the HD404344R series and HD4074344. Connected to V_{ref} for the HD404394 series.

Figure 52 A/D Converter Block Diagram

EOL Product

A/D mode register 1 (AMR1: $019)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	AMR13	AMR12	AMR11	AMR10

AMR10*	$R3_0/AN_0$ Mode Selection
0	$R3_0$
1	AN_0

AMR12	$R3_2/AN_2$ Mode Selection
0	$R3_2$
1	AN_2

AMR11	$R3_1/AN_1$ Mode Selection
0	$R3_1$
1	AN_1

AMR13	$R3_3/AN_3$ Mode Selection
0	$R3_3$
1	AN_3

Note: * Available for the HD404344R series and HD4074344, but not available for the HD404394 series.

Figure 53 A/D Mode Register 1 (AMR1)

A/D mode register 2 (AMR2: $01A)

Bit	3	2	1	0
Initial value	—	—	—	0
Read/Write	—	—	—	W
Bit name	Not used	Not used	Not used	AMR20

AMR20	Conversion Time
0	$34t_{cyc}$
1	$67t_{cyc}$

Figure 54 A/D Mode Register 2 (AMR2)

EOL Product

A/D channel register (ACR: $016)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	W	W	W	W
Bit name	ACR3	ACR2	ACR1	ACR0

ACR3	ACR2	ACR1	ACR0	Analog Input Selection
0	0	0	0	AN_0*
			1	AN_1
		1	0	AN_2
			1	AN_3

Note: * Available for the HD404344R series and HD4074344, but not available for the HD404394 series.

Figure 55 A/D Channel Register (ACR)

A/D start flag (ADSF: $020, bit 2)

Bit	3	2	1	0
Initial value	—	0	0	—
Read/Write	—	R/W	W	—
Bit name	Not used	ADSF	WDON	Not used

A/D Start Flag (ADSF)	
0	A/D conversion completed
1	A/D conversion started

WDON
Refer to the description of timers

Figure 56 A/D Start Flag (ADSF)

EOL Product

I_{AD} off flag (IAOF: $021, bit 2)

Bit	3	2	1	0
Initial value	0	0	—	—
Read/Write	R/W	R/W	—	—
Bit name	RAME	IAOF	Not used	Not used

I_{AD} Off Flag (IAOF)	
0	I_{AD} current flows
1	I_{AD} current is cut off

RAME
Refer to the description of operating modes

Figure 57 I_{AD} Off Flag (IAOF)

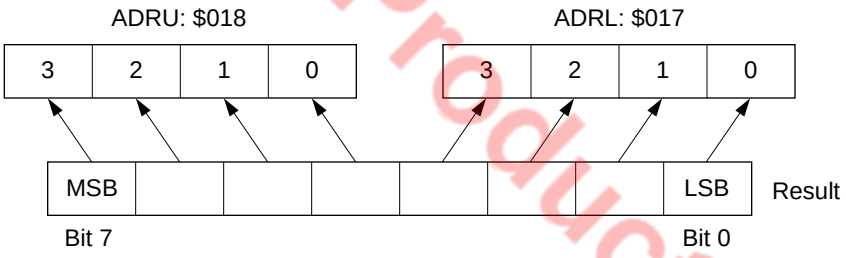


Figure 58 A/D Data Register

A/D data register lower (ADRL: $017)

Bit	3	2	1	0
Initial value	0	0	0	0
Read/Write	R	R	R	R
Bit name	ADRL3	ADRL2	ADRL1	ADRL0

Figure 59 A/D Data Register Lower (ADRL)

EOL Product

A/D data register upper (ADRU: $018)

Bit	3	2	1	0
Initial value	1	0	0	0
Read/Write	R	R	R	R
Bit name	ADRU3	ADRU2	ADRU1	ADRU0

Figure 60 A/D Data Register Upper (ADRU)

EOL Product

Pin Description in PROM Mode

The HD4074344 and the HD4074394 are PROM versions of a ZTAT™ microcomputer. In PROM mode, the MCU stops operating, thus allowing the user to program the on-chip PROM.

Pin Number		MCU Mode		PROM Mode		
DP-28S/FP-28DA	FP-30D	Pin	I/O	Pin	I/O	Remarks
1	1	$R1_0$	I/O	A_5	I	
2	2	$R1_1$	I/O	A_6	I	
3	3	$R1_2$	I/O	A_7	I	
4	4	$R1_3$	I/O	A_8	I	
5	5	$R2_0$	I/O	A_9	I	
6	6	$R2_1$	I/O	A_{10}	I	
7	7	$R2_2$	I/O	A_{11}	I	
8	8	$R2_3$	I/O	A_{12}	I	
9	9	OSC_1	I	$\overline{OE}$	I	
10	10	OSC_2	O			
11	11	GND		GND		
	12	NC				
12	13	$R3_0/AN_0$ or V_{ref}	I/O or V_{ref}			2
13	14	$R3_1/AN_1$	I/O	$\overline{M}_0$	I	
14	15	$R3_2/AN_2$	I/O	$\overline{X}_{ON}$	I	
15	16	$R3_3/AN_3$	I/O	O_0	I/O	
	17	NC				
16	18	V_{CC}		V_{CC}		
17	19	TEST	I	V_{PP}	I	
18	20	$\overline{RESET}$	I	$\overline{RESET}$	I	
19	21	$R0_0/\overline{SCK}$	I/O	O_1	I/O	
20	22	$R0_1$/SI	I/O	O_2	I/O	
21	23	$R0_2$/SO	I/O	O_3	I/O	
22	24	$R0_3$/TOC	I/O	O_4	I/O	
23	25	$D_0/\overline{INT}_0$/EVNB	I/O	A_0	I	
24	26	D_1	I/O	A_1	I	
25	27	D_2	I/O	A_2	I	
26	28	D_3	I/O	A_3	I	
27	29	$D_4/\overline{STOPC}$	I/O	$\overline{CE}$	I	
28	30	D_5	I/O	A_4	I	

Notes: 1. I/O: Input/output pin, I: Input pin, O: Output pin
2. $R3_0/AN_0$ is for the HD404344R series and V_{ref} for the HD404394 series in MCU mode.

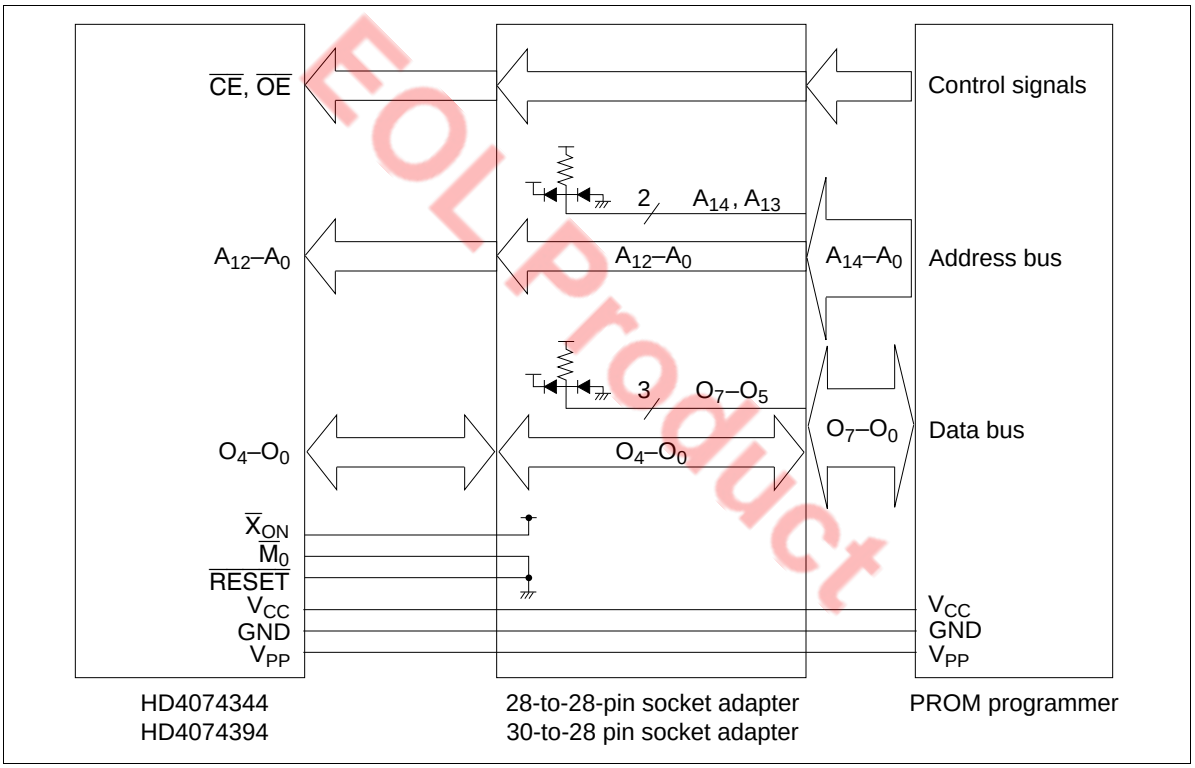
EOL Product

Programmable ROM Operation

The HD4074344 and HD4074394 on-chip PROMs are programmed in PROM mode.

In PROM mode, the MCU does not operate. It can be programmed like a standard 27256 EPROM using a standard PROM programmer and a socket adapter as shown in figure 61. Table 23 lists the recommended PROM programmers and socket adapters.

Since instructions of the HMCS400 series consists of 10 bits, the HMCS400 series microcomputers incorporate a conversion circuit to enable the use of a general-purpose PROM programmer. By this circuit, an instruction is read or written to using two addresses, lower five bits and upper five bits. For example, if 4 kwords of on-chip PROM are programmed by a general-purpose PROM programmer, 8 kbytes of addresses ($0000–$1FFF) should be specified.



EOL Product

Figure 61 PROM Mode Connections

Table 23 PROM Programmer and Socket Adapter

PROM Programmer

Maker	Type Name
DATA I/O	UNISITE
AVAL Corp.	PKW-3100

Socket Adapter

Package	Maker	Type Name
DP-28S	Hitachi	HS4344ESS01H
FP-28DA		HS4344ESP01H
FP-30D		HS4344ESF01H

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Programming and Verification

The HD4074344 and HD4074394 can be high-speed programmed without causing voltage stress or affecting data reliability.

Table 24 shows how programming and verification modes are selected.

Table 24 PROM Mode Selection

	Pin			
Mode	**$\overline{CE}$**	**$\overline{OE}$**	**V_{PP}**	**O_0–O_4**
Programming	Low	High	V_{PP}	Data input
Verification	High	Low	V_{PP}	Data output
Programming inhibited	High	High	V_{PP}	High impedance

Precautions

1. Addresses $0000 to $1FFF should be specified if the PROM is programmed by a PROM programmer. If address $2000 or higher is accessed, the PROM may not be programmed or verified correctly. Note that the plastic package type devices cannot be erased and reprogrammed. Set all data in unused addresses to $FF.
2. Be careful of not using the wrong PROM programmer or socket adapter, which may cause an overvoltage and damage the LSI. Make sure that the LSI is firmly fixed onto the socket adapter, and that the socket adapter is firmly fixed to the programmer.
3. The PROM should be programmed with V_{PP} = 12.5 V. Other PROMs use 21 V. If 21 V is applied to the HD4074344 or HD4074394, the LSI may become permanently damaged. 12.5 V is Intel's 27256 V_{PP}.

Addressing Modes

RAM Addressing Modes

Register Indirect Addressing Mode: The contents of the W, X, and Y registers (10 bits total) are used as a RAM address.

Direct Addressing Mode: A direct addressing instruction consists of two words. The first word contains the opcode, and the contents of the second word (10 bits) are used as a RAM address.

Memory Register Addressing Mode: The memory registers (MR), which are located in 16 digits from $040 to $04F, are accessed with the LAMR and XMRA instructions.

ROM Addressing Modes

Direct Addressing Mode: A program can branch to any address in ROM memory space by executing the JMPL, BRL, or CALL instruction.

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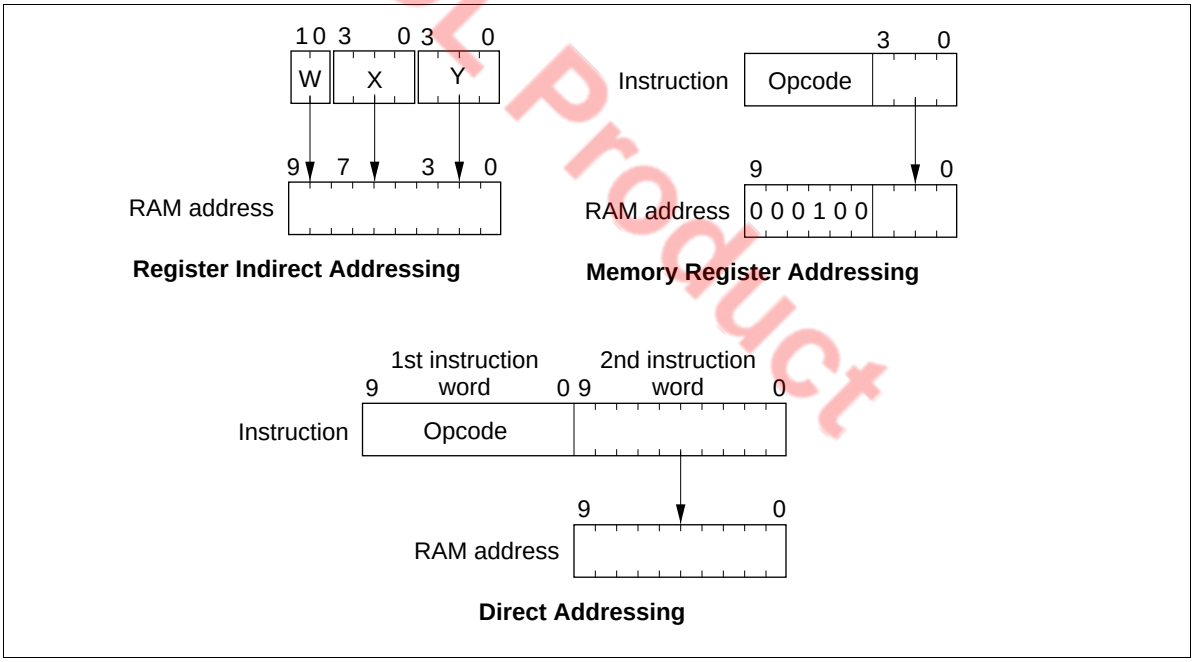

Figure 62 RAM Addressing Modes

Current Page Addressing Mode: A program can branch to any address in the current page (256 words per page) by executing the BR instruction.

Zero-Page Addressing Mode: A program can branch to any subroutine located in the zero-page subroutine area ($0000–$003F) by executing the CAL instruction.

Table Data Addressing Mode: A program can branch to an address determined by the contents of 4-bit immediate data, the accumulator, and the B register by executing the TBR instruction.

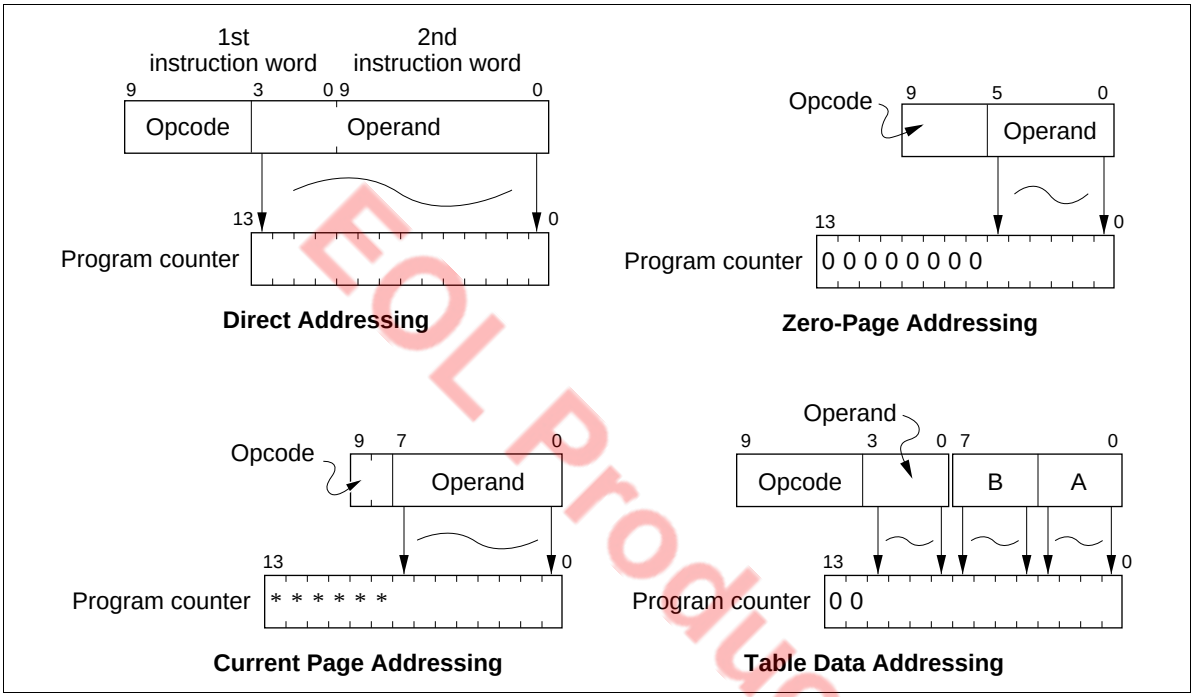

Figure 63 ROM Addressing Modes

EOL Product

Addressing Mode for P Instruction: By using the P instruction, the ROM data determined by table data addressing can be referenced. The lower-order 8 bits of ROM data are written in the accumulator and the B register when bit 8 of the ROM data is 1, and are written in the R1 and R2 port output registers when bit 9 is 1. If bit 8 and bit 9 are both 1, the ROM data is simultaneously written into the accumulator, the B register, and the R1 and R2 port output registers. (See figure 64.)

The program counter is not affected by the P instruction.

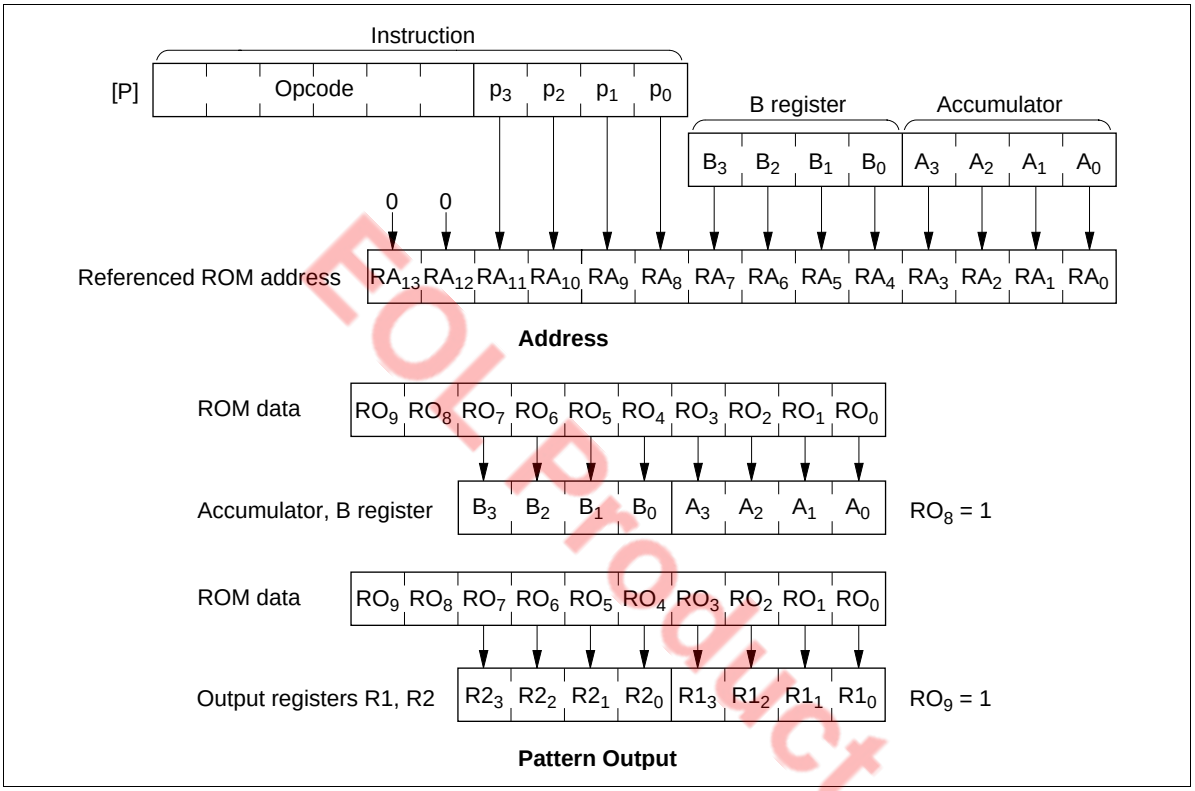

Figure 64 P Instruction

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BR Branching Instruction at Page Boundary: When the BR instruction is at a page boundary (256n + 255), the address in the program counter is transferred over to point to the next page as done by the internal hardware. Therefore, executing the BR instruction at a page boundary will cause the program to branch to the next page. (See figure 65.)

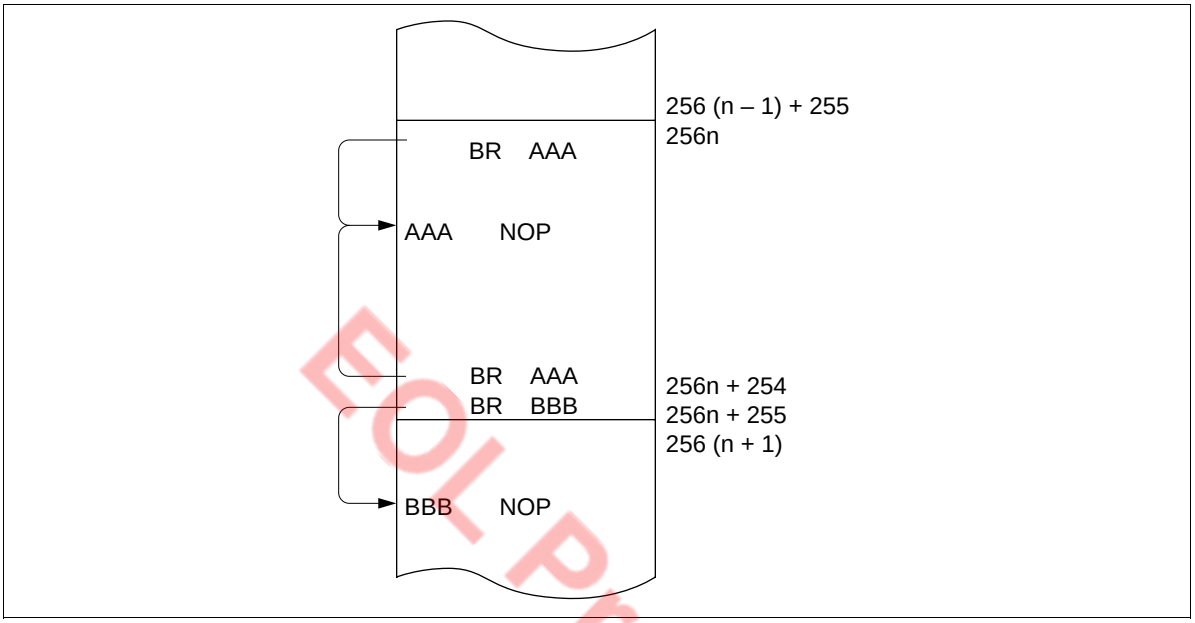

Figure 65 BR Instruction at Page Boundary

EOL Product

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +7.0	V	
Programming voltage	V_{PP}	–0.3 to +14.0	V	1
Pin voltage	V_T	–0.3 to V_{CC} + 0.3	V	2
		–0.3 to +15.0	V	3
Total permissible input current	ΣI_O	100	mA	4
Total permissible output current	$-\Sigma I_O$	30	mA	5
Maximum input current	I_O	30	mA	6, 7
		4	mA	6, 8
Maximum output current	$-I_O$	4	mA	9
Operating temperature	T_{opr}	–20 to +75	°C	10
Storage temperature	T_{stg}	–55 to +125	°C	11

Notes: Permanent damage may occur if these absolute maximum ratings are exceeded. Normal operation must be under the conditions stated in the electrical characteristics tables. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.

1. Applies to pin TEST (V_{PP}) of the HD4074344 and HD4074394.
2. Applies to the following pins.
   HD404344R series and HD4074344: D_0–D_5, R0, R1, R2, R3
   HD404394 series: D_0–D_5, R0, $R1_3$, R2, $R3_1$–$R3_3$
3. Applies to the following pins.
   HD404394 series: $R1_0$–$R1_2$
4. The total permissible input current is the total of input currents simultaneously flowing in from all the I/O pins to GND.
5. The total permissible output current is the total of output currents simultaneously flowing out from V_{CC} to all I/O pins.
6. The maximum input current is the maximum current flowing from each I/O pin to GND.
7. Applies to D_1, D_2, R1, and R2.
8. Applies to the following pins.
   HD404344R series and HD4074344: D_0, D_3–D_5, R0, R3
   HD404394 series: D_0, D_3–D_5, R0, $R3_1$–$R3_3$
9. The maximum output current is the maximum current flowing out from V_{CC} to each I/O pin.
10. The operating temperature indicates the temperature range in which power can be supplied to the LSI (voltage Vcc shown in the electrical characteristics tables can be applied).
11. In the case of chips, the storage specification differs from that of the package products. Please consult your Hitachi sales representative for details.

EOL Product

Electrical Characteristics

DC Characteristics (HD404344R, HD404342R, HD404341R, HD40C4344R, HD40C4342R, HD40C4341R: V_{CC} = 2.5 to 5.5 V, GND = 0 V, T_a = –20 to +75°C, HCD404344R, HCD40C4344R: V_{CC} = 2.5 to 5.5 V, GND = 0 V, T_a = +75°C, HD404394, HD404392, HD404391, HD4074344, HD4074394: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	$\overline{RESET}$, $\overline{SCK}$, $\overline{INT_0}$, $\overline{STOPC}$, EVNB	$0.8V_{CC}$	—	V_{CC} + 0.3	V		
		SI	$0.7V_{CC}$	—	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	$\overline{RESET}$, $\overline{SCK}$, $\overline{INT_0}$, $\overline{STOPC}$, EVNB	–0.3	—	$0.2V_{CC}$	V		
		SI	–0.3	—	$0.3V_{CC}$	V		
		OSC_1	–0.3	—	0.5	V		
Output high voltage	V_{OH}	$\overline{SCK}$, SO, TOC	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	$\overline{SCK}$, SO, TOC	—	—	0.4	V	I_{OL} = 0.5 mA	
I/O leakage current	$\|I_{IL}\|$	$\overline{RESET}$, $\overline{SCK}$, SI, SO, TOC, OSC_1, $\overline{INT_0}$, $\overline{STOPC}$, EVNB	—	—	1	μA	V_{in} = 0 V to V_{CC}	1
Current dissipation in active mode	I_{CC1}	V_{CC}	—	—	3.5	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	2
	I_{CC2}		—	—	0.4	mA	V_{CC} = 3 V,	2, 4
					0.5	mA	f_{OSC} = 400 kHz	5
Current dissipation in standby mode	I_{SBY1}	V_{CC}	—	—	1.5	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	3
	I_{SBY2}		—	—	0.2	mA	V_{CC} = 3 V,	3, 4
			—	—	0.4	mA	f_{OSC} = 400 kHz	3, 5
	I_{SBY3}		—	—	0.6	mA	V_{CC} = 5 V, f_{OSC} = 800 kHz	3, 5, 6

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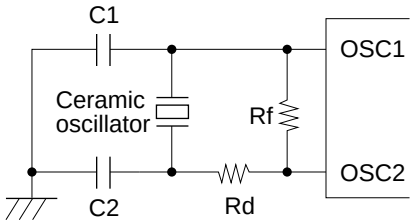
DC Characteristics (HD404344R, HD404342R, HD404341R, HD40C4344R, HD40C4342R, HD40C4341R: V_{CC} = 2.5 to 5.5 V, GND = 0 V, T_a = –20 to +75°C, HCD404344R, HCD40C4344R: V_{CC} = 2.5 to 5.5 V, GND = 0 V, T_a = +75°C, HD404394, HD404392, HD404391, HD4074344, HD4074394: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified) (cont)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	—	10	µA	V_{in} ($\overline{RESET}$) = V_{CC} – 0.3 V to V_{CC}, V_{in} (TEST) = 0 to 0.3 V	
Stop mode retaining voltage	V_{STOP}	V_{CC}	2	—	—	V		

Notes:
1. Excludes current flowing through pull-up MOS and output buffers.
2. I_{CC} is the source current when no I/O current is flowing while the MCU is in reset state.
   Test conditions: MCU: Reset
   Pins: $\overline{RESET}$, TEST at GND
   D_0–D_5, R0–R3 at V_{CC}
3. I_{SBY} is the source current when no I/O current is flowing while the MCU timer is operating.
   Test conditions: MCU: I/O reset
   Standby mode
   Pins: $\overline{RESET}$ at V_{CC}
   TEST at GND
   D_0–D_5, R0–R3 at V_{CC}
4. Applies to the HD404394 series and HD4074344.
5. Applies to the HD404344R series.
6. The current in case of excluding the current through A/D converters ladder resistance (flag I_{AOF} is set to “1”). Circuit structure and circuit constants of oscillator circuit is the following condition.

Circuit Structure



Circuit Constants

Ceramic oscillator: KBR-800FTR (KYOSERA)
C1 = C2 = 100 pF
R_f = 1 MΩ
R_d = 2.2 kΩ

EOL Product

I/O Characteristics for Standard Pins (HD404344R, HD404342R, HD404341R, HD40C4344R, HD40C4342R, HD40C4341R: V_{CC} = 2.5 to 5.5 V, GND = 0 V, T_a = –20 to +75°C, HCD404344R, HCD40C4344R: V_{CC} = 2.5 to 5.5 V, GND = 0 V, T_a = +75°C, HD404394, HD404392, HD404391, HD4074344, HD4074394: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins: HD404344R Series, HD4074344	Pins: HD404394 Series	Min	Typ	Max	Unit	Test Condition	Note
Input high voltage	V_{IH}	D_0–D_5, R0–R3	D_0–D_5, R0, $R1_3$, R2, $R3_1$–$R3_3$	$0.7V_{CC}$	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0–D_5, R0–R3	D_0–D_5, R0, $R1_3$, R2, $R3_1$–$R3_3$	–0.3	—	$0.3V_{CC}$	V		
Output high voltage	V_{OH}	D_0–D_5, R0–R3	D_0–D_5, R0, $R3_1$–$R3_3$	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 0.5 mA	
		—	$R1_3$, R2	V_{CC} – 0.5	—	—	V	500 kΩ at V_{CC}	2
Output low voltage	V_{OL}	D_0–D_5, R0–R3	D_0–D_5, R0, $R1_3$, R2, $R3_1$–$R3_3$	—	—	0.4	V	I_{OL} = 0.5 mA	
		D_1, D_2, R1, R2	D_1, D_2, $R1_3$, R2	—	—	2.0	V	I_{OL} = 15 mA, V_{CC} = 4.5–5.5 V	
Input leakage current	$\|I_{IL}\|$	D_0–D_5, R0–R3	D_0–D_5, R0, $R1_3$, R2, $R3_1$–$R3_3$	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Pull-up MOS current	$-I_{PU}$	D_0–D_5, R0–R3	D_0–D_5, R0, $R3_1$–$R3_3$	30	150	300	µA	V_{CC} = 5 V, V_{in} = 0 V	

Notes: 1. Output buffer current and pull-up MOS current are excluded.
2. Applies to the HD404394 series.

EOL Product

I/O Characteristics for NMOS Intermediate-Voltage Pins for HD404394 Series (V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	$R1_0$–$R1_2$	$0.7V_{CC}$	—	12.0	V		1
Input low voltage	V_{IL}	$R1_0$–$R1_2$	–0.3	—	$0.3V_{CC}$	V		1
Output high voltage	V_{OH}	$R1_0$–$R1_2$	11.5	—	—	V	500 kΩ at 12 V	1
Output low voltage	V_{OL}	$R1_0$–$R1_2$	—	—	0.4	V	I_{OH} = 0.5 mA	1
		$R1_0$–$R1_2$	—	—	2.0	V	I_{OL} = 15 mA, V_{CC} = 4.5 to 5.5 V	1
I/O leakage current	$\|I_{IL}\|$	$R1_0$–$R1_2$	—	—	20	µA	V_{in} = 0 V to 12 V	1, 2

Notes: 1. Applies to the HD404394 series.
2. Excludes output buffer current.

EOL Product

A/D Converter Characteristics (HD404344R, HD404342R, HD404341R, HD40C4344R, HD40C4342R, HD40C4341R: V_{CC} = 2.5 to 5.5 V, GND = 0 V, T_a = –20 to +75°C, HCD404344R, HCD40C4344R: V_{CC} = 2.5 to 5.5 V, GND = 0 V, T_a = +75°C, HD404394, HD404392, HD404391, HD4074344, HD4074394: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Analog reference voltage	V_{ref}	V_{ref}	$0.5V_{CC}$	—	V_{CC}	V		2
Analog input voltage	AV_{in}	AN_0–AN_3	GND	—	V_{CC}	V		1
		AN_1–AN_3	GND	—	V_{ref}	V		2
Current flowing between V_{ref} and GND	I_{AD}		—	—	200	µA	V_{ref} = V_{CC} = 5.0 V	2
Analog input capacitance	CA_{in}	AN_0–AN_3	—	15	—	pF		
Resolution			—	8	—	Bit		
Number of input channels			0	—	4	Channel		1
			0	—	3	Channel		2
Absolute accuracy		AN_0–AN_3	–2.0	—	2.0	LSB		1
		AN_0–AN_3	–2.5	—	2.5	LSB	T_a = 25°C,	2
		AN_1–AN_3	–3.0	—	3.0	LSB	V_{ref} = V_{CC} = 5.0 V	3
Conversion time			34	—	67	t_{cyc}		
Input impedance		AN_0–AN_3	1	—	—	MΩ	f_{OSC} = 1 MHz, V_{in} = 0 V	

Notes: 1. Applies to the HD404344R series.
2. Applies to the HD4074344.
3. Applies to the HD404394 series.

AC Characteristics (HD404344R, HD404342R, HD404341R, HD40C4344R, HD40C4342R, HD40C4341R: V_{CC} = 2.5 to 5.5 V, GND = 0 V, T_a = –20 to +75°C, HCD404344R, HCD40C4344R: V_{CC} = 2.5 to 5.5 V, GND = 0 V, T_a = +75°C, HD404394, HD404392, HD404391, HD4074344, HD4074394: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Clock oscillation frequency (ceramic oscillator)	f_{OSC}	OSC_1, OSC_2	0.4	—	4.5	MHz	Division by 4	
Clock oscillation frequency (resistor oscillator)	f_{OSC}	OSC_1, OSC_2	1.0	2.0	3.5	MHz	Division by 4 R_f = 20 kΩ	
Instruction cycle time (external clock, ceramic oscillator)	t_{cyc}		0.89	—	10	µs	Division by 4	
Instruction cycle time (resistor oscillator)	t_{cyc}		1.14	—	4.0	µs	Division by 4 R_f = 20 kΩ	
Oscillation setting time (external clock)	t_{RC}	OSC_1, OSC_2	—	—	2	ms		1
Oscillation setting time (ceramic oscillator)	t_{RC}	OSC_1, OSC_2	—	—	2	ms		1
Oscillation setting time (resistor oscillator)	t_{RC}	OSC_1, OSC_2	—	—	0.5	ms	R_f = 20 kΩ	1, 11
External clock high-level width	t_{CPH}	OSC_1	92	—	—	ns		2
External clock low-level width	t_{CPL}	OSC_1	92	—	—	ns		2
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns		2
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns		2
$\overline{INT}_0$, EVNB high-level width	t_{IH}	$\overline{INT}_0$, EVNB	2	—	—	t_{cyc}		3
$\overline{INT}_0$, EVNB low-level width	t_{IL}	$\overline{INT}_0$, EVNB	2	—	—	t_{cyc}		3
$\overline{RESET}$ low-level width	t_{RSTL}	$\overline{RESET}$	2	—	—	t_{cyc}		4
$\overline{STOPC}$ low-level width	t_{STPL}	$\overline{STOPC}$	1	—	—	t_{RC}		5
$\overline{RESET}$ rise time	t_{RSTr}	$\overline{RESET}$	—	—	20	ms		4
$\overline{STOPC}$ rise time	t_{STPr}	$\overline{STOPC}$	—	—	20	ms		5

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AC Characteristics (HD404344R, HD404342R, HD404341R, HD40C4344R, HD40C4342R, HD40C4341R: V_{CC} = 2.5 to 5.5 V, GND = 0 V, T_a = –20 to +75°C, HCD404344R, HCD40C4344R: V_{CC} = 2.5 to 5.5 V, GND = 0 V, T_a = +75°C, HD404394, HD404392, HD404391, HD4074344, HD4074394: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified) (cont)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Note
Input capacitance	C_{in}	All input pins except TEST, V_{ref} and $R1_0$–$R1_2$	—	—	15	pF	f = 1 MHz, V_{in} = 0 V	
		TEST	—	—	15	pF	f = 1 MHz, V_{in} = 0 V	6
			—	—	40	pF		7
		V_{ref}	—	—	30	pF		8
		$R1_0$–$R1_2$	—	—	15	pF		9
			—	—	30	pF		10

Notes: 1. The oscillation stabilization time is the period required for the oscillator to stabilize in the following situations:

a. After V_{CC} reaches the minimum specification value at power-on.

b. After $\overline{RESET}$ input goes low when stop mode is cancelled.

c. After $\overline{STOPC}$ input goes low when stop mode is cancelled.

To ensure the oscillation stabilization time at power-on or when stop mode is cancelled, $\overline{RESET}$ or $\overline{STOPC}$ must be input for at least a duration of t_{RC}.

When using a ceramic oscillator, consult with the manufacturer to determine what stabilization time is required, since it will depend on the circuit constants and stray capacitance.

2. Refer to figure 66.
3. Refer to figure 67.
4. Refer to figure 68.
5. Refer to figure 69.
6. Applies to the HD404341R, HD404342R, HD404344R, HD404391, HD404392, and HD404394.
7. Applies to the HD4074344 and HD4074394.
8. Applies to the HD404394 series.
9. Applies to the HD404344R series.
10. Applies to the HD404394 series and HD4074344.
11. Applies to the HD40C4344R, HD40C4342R, HD404341R

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Serial Interface Timing Characteristics (HD404344R, HD404342R, HD404341R, HD40C4344R, HD40C4342R, HD40C4341R: V_{CC} = 2.5 to 5.5 V, GND = 0 V, T_a = –20 to +75°C, HCD404344R, HCD40C4344R: V_{CC} = 2.5 to 5.5 V, GND = 0 V, T_a = +75°C, HD404394, HD404392, HD404391, HD4074344, HD4074394: V_{CC} = 2.7 to 5.5 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

During Transmit Clock Output

Item	Symbol	Pins	Test Condition	Min	Typ	Max	Unit	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	Load shown in figure 71	1	—	—	t_{cyc}	1
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	Load shown in figure 71	0.4	—	—	t_{Scyc}	1
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	Load shown in figure 71	0.4	—	—	t_{Scyc}	1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	Load shown in figure 71	—	—	80	ns	1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	Load shown in figure 71	—	—	80	ns	1
Serial output data delay time	t_{DSO}	SO	Load shown in figure 71	—	—	300	ns	1
Serial input data setup time	t_{SSI}	SI		100	—	—	ns	1
Serial input data hold time	t_{HSI}	SI		200	—	—	ns	1

During Transmit Clock Input

Item	Symbol	Pins	Test Condition	Min	Typ	Max	Unit	Note
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$		1	—	—	t_{cyc}	1
Transmit clock high width	t_{SCKH}	$\overline{SCK}$		0.4	—	—	t_{Scyc}	1
Transmit clock low width	t_{SCKL}	$\overline{SCK}$		0.4	—	—	t_{Scyc}	1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$		—	—	80	ns	1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$		—	—	80	ns	1
Serial output data delay time	t_{DSO}	SO	Load shown in figure 71	—	—	300	ns	1
Serial input data setup time	t_{SSI}	SI		100	—	—	ns	1
Serial input data hold time	t_{HSI}	SI		200	—	—	ns	1

Note: 1. Refer to figure 70.

EOL Product

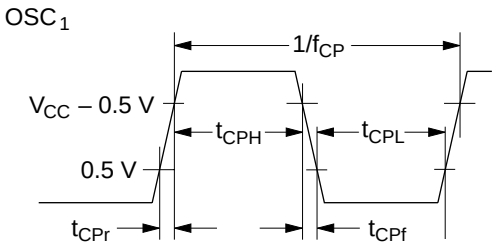


Figure 66 External Clock Timing

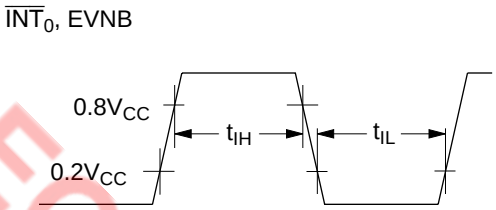


Figure 67 Interrupt Timing

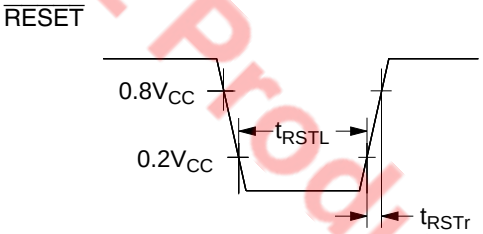


Figure 68 RESET Timing

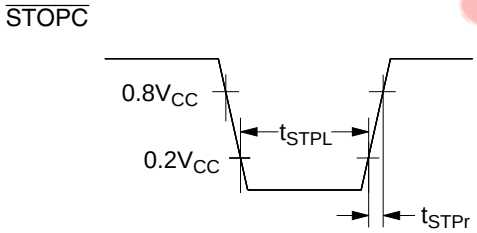
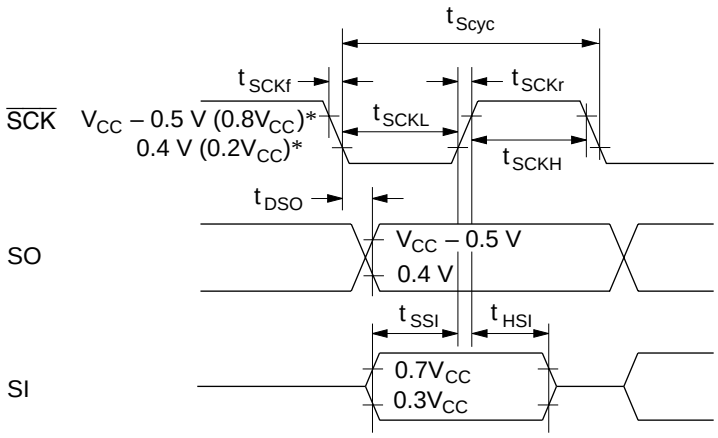


Figure 69 STOPC Timing

EOL Product



Note: * V_{CC} – 0.5 V and 0.4 V are the threshold voltages for transmit clock output, and 0.8V_{CC} and 0.2V_{CC} are the threshold voltages for transmit clock input.

Figure 70 Serial Interface Timing

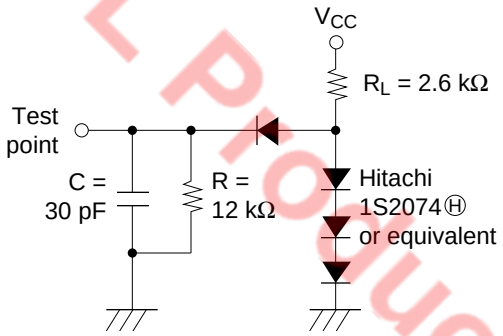


Figure 71 Timing Load Circuit

EOL Product

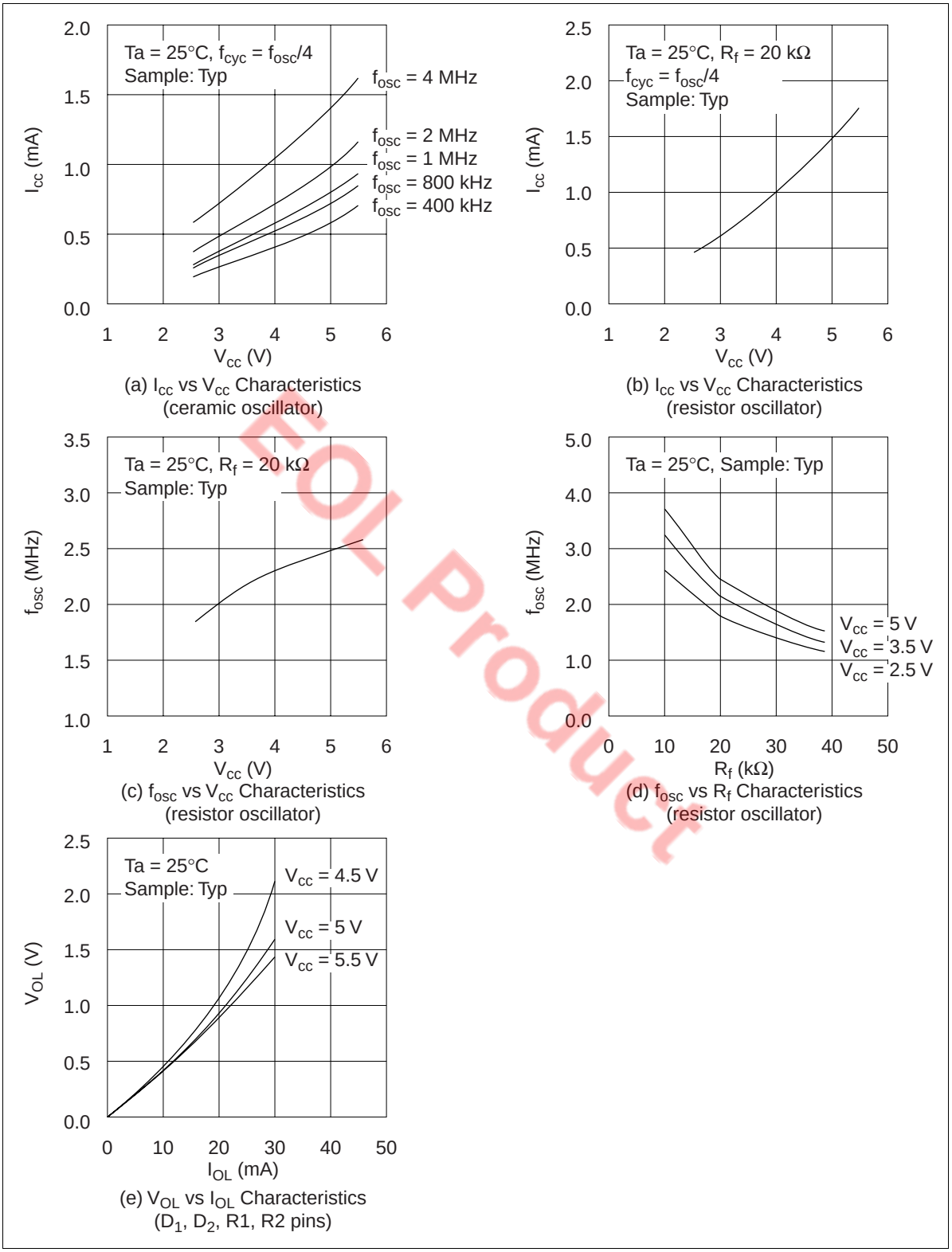


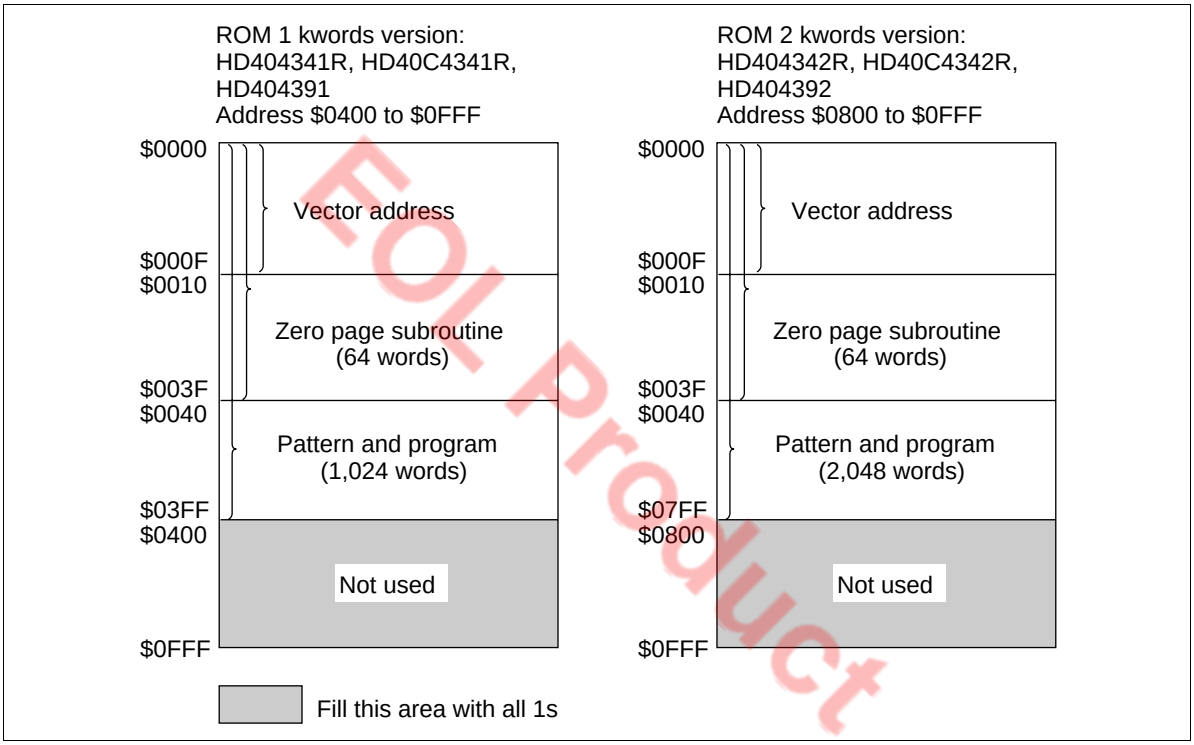
Figure 72 Characteristics curve HD404344R series (consultation value)

Notes On ROM Out

Please pay attention to the following items regarding ROM out.

On ROM out, fill the ROM area indicated below with 1s to create the same data size as 4-kword versions (HD404344R and HD404394). A 4-kword data size is required to change ROM data to mask manufacturing data since the program used is for a 4-kword version.

This limitation apply to the case of using EPROM and the case of using data base.



EOL Product

HD404341R/HD404342R/HD404344R/HCD404344R/HD40C4341R/HD40C4342R/ HD40C4344R/HCD40C4344R Option List

Please check off the appropriate applications and enter the necessary information.

Date of order	
Customer	
Department	
Name	
ROM code name	
LSI number	

1. ROM size

☐ HD404341R	1-kword	Ceramic oscillator External clock	☐ HD404341R	1-kword	RC oscillator
☐ HD404342R	2-kword		☐ HD404342R	2-kword	
☐ HD404344R	4-kword		☐ HD404344R	4-kword	
☐ HCD404344R	4-kword		☐ HCD40C4344R	4-kword	

2. ROM code media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐	EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐	EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

3. System oscillator (OSC1–OSC2) (Shaded areas indicate selections that are not available.)

HD404341R/HD404342R/HD404344R/HCD404344R		HD40C4341R/HD40C4342R/HD40C4344R/HCD40C4344R
☐ Ceramic oscillator	f = MHz	
☐ External clock	f = MHz	
☐ RC oscillator		

4. Stop mode

☐	Used
☐	Not used

5. Package type

☐	DP-28S
☐	FP-28DA
☐	FP-30D
☐	Chip

Note: The specifications of shipped chips differ from of the package product. Please contact our sales staff for details.

EOL Product

HD404391/HD404392/HD404394 Option List

Please check off the appropriate applications and enter the necessary information.

Date of order	
Customer	
Department	
Name	
ROM code name	
LSI number	

1. ROM size

☐ HD404391	1-kword
☐ HD404392	2-kword
☐ HD404394	4-kword

2. ROM code media
   Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐ EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐ EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

3. System oscillator (OSC1–OSC2)

☐ Ceramic oscillator	f =	MHz
☐ External clock	f =	MHz

4. Stop mode

☐ Used
☐ Not used

5. Package type

☐ DP-28S
☐ FP-28DA
☐ FP-30D

EOL Product

Cautions

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