KMM5362205BW/BWG Fast Page Mode with Extended Data Out

2Mx36 DRAM SIMM, 5V, 1K Refresh using 4M Quad CAS EDO DRAM

GENERAL DESCRIPTION

The Samsung KMM5362205BW is a 2M bit x 36 Dynamic RAM high density memory module. The Samsung KMM5362205BW consists of four CMOS 1Mx16 bit EDO DRAMs in 42-pin SOJ packages and two CMOS 1Mx4 bit Quad CAS with EDO DRAMs in 24-pin SOJ packages mounted on a 72-pin glass-epoxy substrate. A 0.1uF or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM5362205BW is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

FEATURES

- Part Identification
  - KMM5362205BW (1024 cycles/16ms Ref, SOJ, Solder)
  - KMM5362205BWG (1024 cycles/16ms Ref, SOJ, Gold)
- Fast Page Mode with Extended data out
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDPin & pinout
- **PCB : Height (750mil), double sided component**

PERFORMANCE RANGE

Speed	tRAC	tCAC	tRC	tHPC
- 6	60ns	17ns	110ns	30ns
- 7	70ns	20ns	130ns	33ns

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	DQ17
2	DQ0	38	DQ35
3	DQ18	39	Vss
4	DQ1	40	$\overline{CAS0}$
5	DQ19	41	$\overline{CAS2}$
6	DQ2	42	$\overline{CAS3}$
7	DQ20	43	$\overline{CAS1}$
8	DQ3	44	$\overline{RAS0}$
9	DQ21	45	$\overline{RAS1}$
10	Vcc	46	NC
11	NC	47	$\overline{W}$
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	Res(A10)	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	Vcc
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	Res(A11)	65	DQ16
30	Vcc	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	$\overline{RAS3}$	69	PD3
34	$\overline{RAS2}$	70	PD4
35	DQ26	71	NC
36	DQ8	72	Vss

PIN NAMES

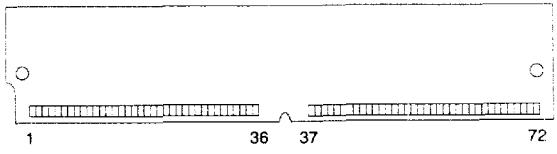
Pin Name	Function
A0 - A9	Address Inputs
DQ0 - DQ35	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS0}$, $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ ~ $\overline{CAS3}$	Column Address Strobe
PD1 - PD4	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection

PRESENCE DETECT PINS (Optional)

Pin	60NS	70NS
PD1	NC	NC
PD2	NC	NC
PD3	NC	Vss
PD4	NC	NC

*Pin Connection Changing Available

PIN CONNECTIONS (Front View)



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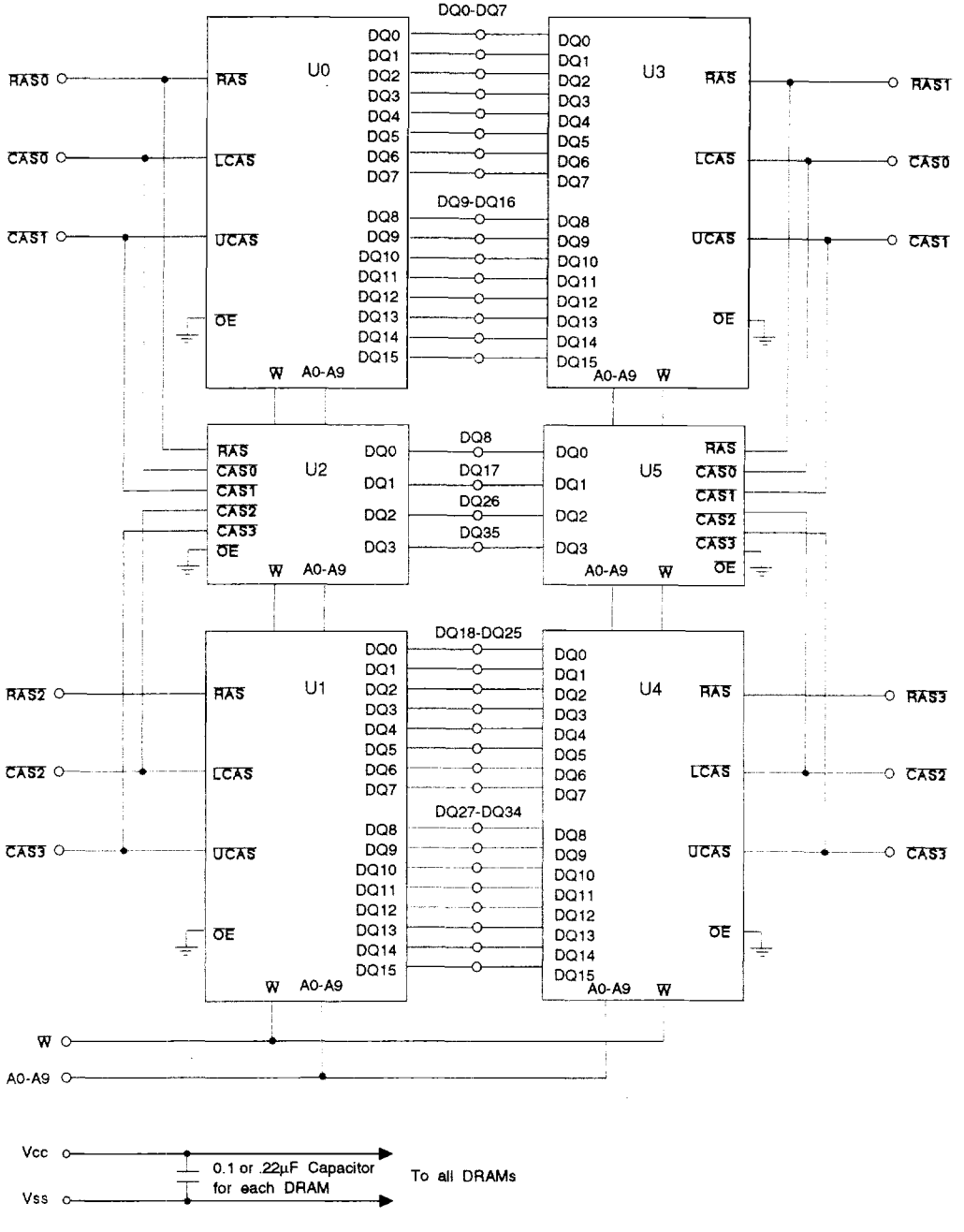
FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	VIN,VOUT	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	Vcc	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	Pd	6	W
Short Circuit Output Current	IOS	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, Ta = 0 to 70 °C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	VIH	2.4	-	Vcc+1*1	V
Input Low Voltage	VIL	-1.0*2	-	0.8	V

*1 : Vcc+2.0V/20ns, Pulse width is measured at Vcc.
*2 : -2.0V/20ns, Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Symbol	Speed	KMM5362205BW/BWG		Unit
		Min	Max	
ICC1	- 6	-	381	mA
	- 7	-	351	mA
ICC2		-	12	mA
ICC3	- 6	-	381	mA
	- 7	-	351	mA
ICC4	- 6	-	281	mA
	- 7	-	251	mA
ICC5		-	6	mA
ICC6	- 6	-	381	mA
	- 7	-	351	mA
II(L)		-30	30	μA
IO(L)		-10	10	μA
VOH		2.4	-	V
VOL		-	0.4	V

ICC1 : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @tRC=min.)
ICC2 : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=VIH)
ICC3 : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$= VIH, $\overline{RAS}$ cycling @tRC=min.)
ICC4 : EDO Mode Current * ($\overline{RAS}$=VIL, $\overline{CAS}$, Address cycling : tHPC=min.)
ICC5 : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)
ICC6 : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)
II(L) : Input Leakage Current (Any input 0 ≤ VIN ≤ Vcc+0.5V, all other pins not under test=0V)
IO(L) : Output Leakage Current (Data out is disabled, 0V ≤ Vout ≤ Vcc)
VOH : Output High Voltage Level (IOH = - 5mA)
VOL : Output Low Voltage Level (IOL = 4.2mA)

* NOTE : ICC1, ICC3, ICC4 and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as an average current. In ICC1 and ICC3, address can be changed maximum once while $\overline{RAS}$=VIL. In ICC4, address can be changed maximum once within one EDO mode cycle, tHPC.

CAPACITANCE (Ta=25°C, Vcc=5V, f=1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance [A0-A9]	C_{IN1}	-	50	pF
Input capacitance [$\overline{W}$]	C_{IN2}	-	60	pF
Input capacitance [$\overline{RAS0}$,$\overline{RAS3}$]	C_{IN3}	-	30	pF
Input capacitance [$\overline{CAS0}$ - $\overline{CAS3}$]	C_{IN4}	-	40	pF
Input/Output capacitance [DQ0-35]	C_{DQ1}	-	30	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, Vcc=5.0V±10%. See notes 1, 2.)

Test condition : Vih/Vil=2.4V/0.8V, Voh/Vol=2.0V/0.8V, Output loading CL=100pF

STANDARD OPERATION	Symbol	-6		-7		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	tRC	110		130		ns	
Access time from $\overline{RAS}$	tRAC		60		70	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		17		20	ns	3,4,5
Access time from column address	tAA		30		35	ns	3,10
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	15	3	20	ns	6,11,12
Transition time (rise and fall)	tT	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	40		50		ns	
$\overline{RAS}$ pulse width	tRAS	60	10K	70	10K	ns	
$\overline{RAS}$ hold time	tRSH	17		20		ns	
$\overline{CAS}$ hold time	tCSH	50		60		ns	
$\overline{CAS}$ pulse width	tCAS	10	10K	15	10K	ns	13
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	45	20	50	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	35	ns	10
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		ns	
Row address set-up time	tASR	0		0		ns	
Row address hold time	tRAH	10		10		ns	
Column address set-up time	tASC	0		0		ns	
Column address hold time	tCAH	10		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		ns	
Read command set-up time	tRCS	0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		ns	8
Write command hold time	tWCH	10		15		ns	
Write command pulse width	tWP	10		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		15		ns	
Write command to $\overline{CAS}$ lead time	tCWL	10		15		ns	
Data set-up time	tDS	0		0		ns	9
Data hold time	tDH	10		15		ns	9
Refresh period	tREF		16		16	ms	
Write command set-up time	tWCS	0		0		ns	7
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		ns	
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		25		ns	

AC CHARACTERISTICS (0°C≤Ta≤70°C, Vcc=5.0V±10%. See notes 1, 2.)

Test condition : Vih/Vil=2.4V/0.8V, Voh/Vol=2.0V/0.8V, Output loading CL=100pF

STANDARD OPERATION	Symbol	-6		-7		Unit	Notes
		Min	Max	Min	Max		
Access time from $\overline{CAS}$ precharge	tCPA		35		40	ns	3
Hyper Page cycle time	tHPC	30		33		ns	13
$\overline{CAS}$ precharge time (Hyper Page cycle)	tCP	10		10		ns	
$\overline{RAS}$ pulse width (Hyper Page cycle)	tRASP	60	200K	70	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	35		40		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	10		10		ns	
Output data hold time	tDOH	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	15	3	20	ns	6,11,12
Output buffer turn off delay from $\overline{W}$	tWEZ	3	15	3	20	ns	6,11
$\overline{W}$ to data delay	tWED	15		20		ns	
$\overline{W}$ pulse width (Hyper Page Cycle)	tWPE	5		5		ns	
Hold time $\overline{CAS}$ low to $\overline{CAS}$ high	tCLCH	5		5		ns	14

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. VIH(min) and VIL(max) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min) and VIL(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2TTL loads and 100pF.

4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.

5. Assumes that tRCD ≥ tRCD(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.

7. tWCS is non restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If tWCS≥tWCS(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.

8. Either tRCH or tRRH must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.

10. Operation within the tRAD(max) limit insures that tRAC (max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.

11. tCEZ(max), tREZ(max), tWEZ(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.

12. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.

13. tASC ≥ tCPmin

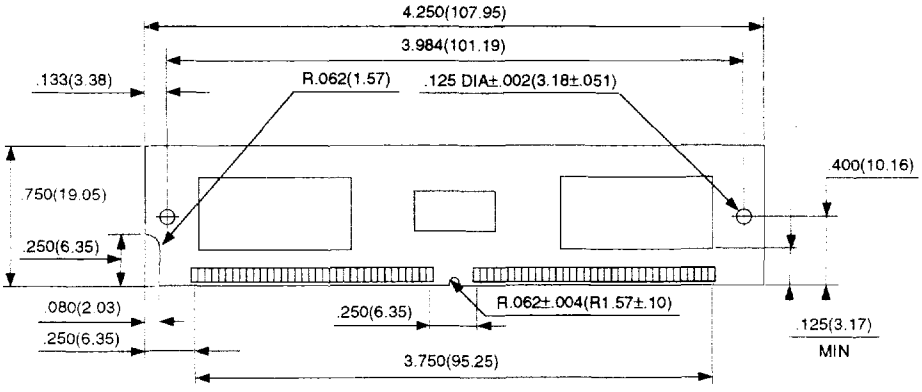
14. In order to hold the address latched by the first $\overline{CAS}$ going low, the parameter tCLCH must be met.

TIMING DIAGRAM

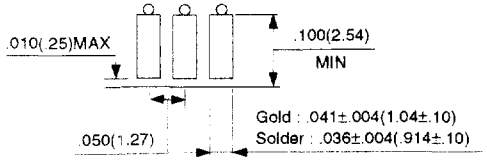
Please refer to attached timing chart (IV) !!!

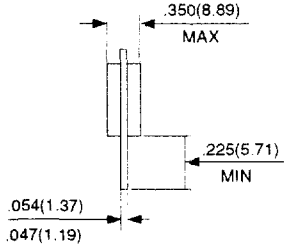
PACKAGE DIMENSIONS (Front View)

Units : Inches (millimeters)



Gold & Solder Plating Lead





Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device are 1Mx16 EDO DRAM and 1M x4 Quad CAS with EDO DRAM.
DRAM Part No. : KM416C1204BJ (400 mil)
KM44C1005CJ (300 mil)

Revision History
Rev. 0.0 : 10 Sep. '95