# 16 Mbps Filter/Equalizer for Tape Drives

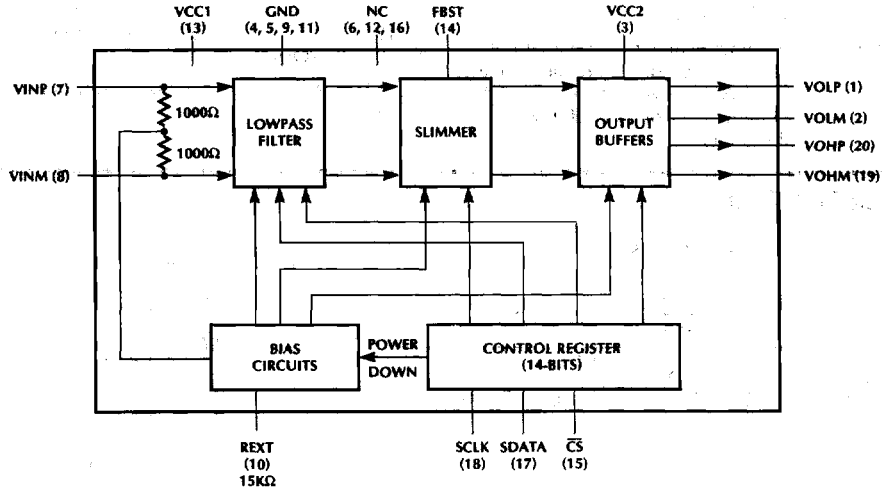
## GENERAL DESCRIPTION

The ML6024 is a monolithic analog filter/equalizer intended for tape drive read channel applications, capable of handling disk data rates up to 16 Mbps, with an operating power dissipation less than 300mW. Its architecture consists of a continuous type filter based on a transconductor and a high speed parasitic free active integrator, allowing complete independence of the filter response from interconnect parasitics, thus realizing a family of frequency response curves optimized for tape drive read channel equalization, especially to handle the different format and media types, for ensuring backward compatibility. It consists of a programmable 6-pole 2-zero lowpass filter stage, two pairs high-speed drivers, and a serial microprocessor interface. The poles of the transfer function approximate a maximally flat group delay (modified bessel type) response, whereas the symmetric zeros provide the high-frequency boost necessary for equalization. The user can independently program the corner frequency, as well as the slimming level and individual bits for power-down, read/write control, and auto-zero control.

## FEATURES

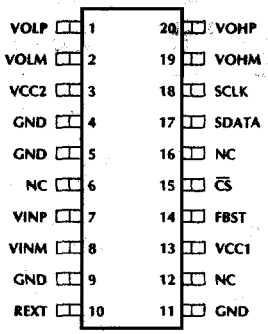
- 6-pole, 2-zero continuous time filter with < –45dB harmonic distortion
- Data transfer rates up to 16 Mbps
- Programmable filter cutoff frequency
  (4.3:1 range in 64 steps)
  ($f_C$ = 2 to 9MHz)
- 32 step programmable pulse slimming equalization, 0 to 10dB boost at $f_C$.
- Power-down, auto-zero, R/W modes programmable through the control register
- Lowpass output and differentiated lowpass (bandpass) output provided.
- High speed (up to 20MHz clock) three wire serial microprocessor interface
- Double buffered data latch for synchronous or asynchronous data loading.
- External pin to disable the slimmer
- Available in 20-pin SSOP package.
- Power Dissipation — $P_{OPR}$ = 300mW, $P_{DN}$ = 7.5mW

## BLOCK DIAGRAM



## PIN CONNECTION

20-Pin SSOP




TOP VIEW

## PIN DESCRIPTION

| PIN# | NAME | FUNCTION |
|---|---|---|
| 1<br>2 | VOLP<br>VOLM | Normal Lowpass outputs |
| 3 | VCC2 | Positive supply for the output drivers |
| 4, 5,<br>9, 11 | GND | Ground |
| 7<br>8 | VINP<br>VINM | Signal Inputs |
| 10 | REXT | A 15K resistor between this pin and ground sets corner frequency |
| 13 | VCC1 | Positive supply |
| 14 | FBST | Slimmer Enable pin. A high input level allows normal operation of the filter. A low level input disables the slimmer, resulting in 0dB boost. A TTL input. |
| 15 | $\overline{CS}$ | Control Register Enable. A logical low level allows the SCLK input to clock data into the control register via the SDATA input line. A logical high level latches the control register contents and issues the information to the appropriate circuitry. A TTL input. |
| 17 | SDATA | Control Register Data. A TTL input. |
| 18 | SCLK | Control Register Clock. Negative edge triggered control register clock input. A TTL input. |
| 19<br>20 | VOHM<br>VOHP | Differentiated lowpass outputs |
| 6, 12,<br>16 | NC | No Connects, reserved for future use. |

## TRANSFER FUNCTION

The transfer function is: (modified Bessel)

$$\frac{\left(1-\frac{k_{SL}\times s^2}{Q_2^2\times\omega_{02}^2}\right)}{\left(\frac{s^2}{\omega_{01}^2}+\frac{s}{Q_1\times\omega_{01}}+1\right)\left(\frac{s^2}{\omega_{02}^2}+\frac{s}{Q_2\times\omega_{02}}+1\right)\left(\frac{s^2}{\omega_{03}^2}+\frac{s}{Q_3\times\omega_{03}}+1\right)}$$

Where: $s = j\omega$
$k_{SL} = 0$ to 7.75
$f_{01} = 1.607$
$Q_1 = 0.51$
$f_{02} = 1.908$
$Q_2 = 1.02$
$f_{03} = 1.692$
$Q_3 = 0.611$
$\omega_{01} = (2\pi f_C)\, f_{01}$
$\omega_{02} = (2\pi f_C)\, f_{02}$
$\omega_{03} = (2\pi f_C)\, f_{03}$
$f_C$ = corner frequency

## ABSOLUTE MAXIMUM RATINGS

VCC1, VCC2 ..... 6.5 volts
VINP, VINM, REXT, $\overline{CS}$, SCLK,
SDATA, R/$\overline{W}$ ..... GND – 0.3V to VCC1 + 0.3V
VOLP, VOLM,
VOHP, VOHM ..... GND – 0.3V to VCC2 + 0.3V
Input Current per pin ..... ± 25 mA
Package Dissipation
at Ta = 25°C (Surface Mount) ..... 1.5 Watts
Junction Temperature ..... 150°C
Storage Temperature ..... –65°C to 150°C

## OPERATING CONDITIONS

VCC1 = VCC2 ..... 5 volts ± 10%
VIN = (VINP-VINM) ..... 1 Vp-p
Rext ..... 10 Kohms
Serial Clock Frequency (SCLK) ..... < 25 MHz
AC Coupling Capacitors ..... > 0.0001 µF

## ELECTRICAL CHARACHTERISTICS

The following specifications apply over the recommended operating conditions, unless otherwise stated. Please refer to the application/test setup digram: (Note 1)

VCC1 = VCC2 = 5V ± 10%, $T_A$ = 0°C to 70°C, Rext = 15kΩ
VIN = (VINP – VINM) = 1 $V_{P-P}$ sinewave input
VOL = (VOLP – VOLM) and VOH = (VOHP – VOHM)
Input and Output coupling capacitors = 0.47µF
RB1 = 750Ω (pins 1 & 2), RB2 = 750Ω (pins 19 & 20)
RL = 1000Ω (1000) and CL = 50 (50) pF on pins 1 (19) and 2 (20)
Serial Clock Frequency = 20 MHz, Power Down, Read/Write bits = 0, Auto Zero = 1
Digital timing measured at 1.4V midpoint
Input control signals from 10% - 90% of VCC1 with ($t_r$ = $t_f$) < 5 ns.

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | | |
| $I_{CC}$ | VCC Supply Current | RB1 = RB2 = INF | | 60 | 77 | mA |
| Ipd | Standby Current | VIN = 0 | | 1.5 | 1.75 | mA |
| **DIGITAL INPUT CHARACTERISTICS (SCLK, SDATA, $\overline{CS}$)** | | | | | | |
| VIL | Low Voltage | | | | 0.8 | V |
| VIH | High Voltage | | 2.2 | | | V |
| IIH | High Current | | | | 1.0 | µA |
| IIL | Low Current | | | | –1.0 | µA |
| CIN | Input Capacitance | | | 5 | | pF |
| **DIGITAL TIMING CHARACTERISTICS (SCLK, SDATA, $\overline{CS}$)** | | | | | | |
| $t_{PW}$-$\overline{CS}$ | Width of $\overline{CS}$, High/Low | | 25 | | | ns |
| $t_{SU}$-SDATA | SDATA Setup time to SCLK | | 15 | | | ns |
| $t_H$-SDATA | SDATA Hold Time | | 5 | | | ns |
| $t_{SU}$-$\overline{CS}$ | $\overline{CS}$ Setup Time to SCLK | | 15 | | | ns |
| $t_H$-$\overline{CS}$ | $\overline{CS}$ Hold Time to SCLK | | 0 | | | ns |
| $t_{PH}$-SCLK | SCLK Pulse Width | | 20 | | | ns |
| $t_H$-SCLK | $\overline{CS}$ Inactive to SCLK Active | | 125 | | | ns |

## ELECTRICAL CHARACHTERISTICS

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP. | MAX | UNITS |
|---|---|---|---|---|---|---|
| **EQUALIZER (NORMAL AND LOWPASS OUTPUT)** | | | | | | |
| AG | Absolute Gain | S0-S4 = 0, F0-F5 = 0 at 0.5MHz | –1.5 | –0.5 | 0.5 | dB |
| CF | Cutoff Frequency, –3dB ±1.5 ($f_{ref}$ = 0.5MHz) | S0-S4 = 0, (no slimming)<br>F5 F4 F3 F2 F1 F0 ($f_C$) | | | | |
| | | 0 0 0 0 0 0 | 8.1 | 9.0 | 9.9 | MHz |
| | | 0 0 0 0 0 1 | 7.69 | 8.55 | 9.4 | MHz |
| | | 0 0 0 0 1 0 | 7.36 | 8.18 | 9.0 | MHz |
| | | 0 0 0 1 0 0 | 6.75 | 7.5 | 8.25 | MHz |
| | | 0 0 1 0 0 0 | 5.79 | 6.43 | 7.07 | MHz |
| | | 0 1 0 0 0 0 | 4.50 | 5.0 | 5.50 | MHz |
| | | 1 0 0 0 0 0 | 3.11 | 3.46 | 3.80 | MHz |
| | | 1 1 1 1 1 1 | 1.88 | 2.09 | 2.30 | MHz |
| SL | Slimming Level (Gain at CF Referred to AG, Vout = 1Vp-p | F0-F5 = 0; at CF<br>S4 S3 S2 S1 S0 | | | | |
| | | 0 0 0 0 1 | –0.4 | 0.6 | 1.6 | dB |
| | | 0 0 0 1 0 | 0.1 | 1.1 | 2.1 | dB |
| | | 0 0 1 0 0 | 1.1 | 2.1 | 3.1 | dB |
| | | 0 1 0 0 0 | 2.8 | 3.8 | 4.8 | dB |
| | | 1 0 0 0 0 | 5.4 | 6.4 | 7.4 | dB |
| | | 1 1 1 1 1 | 8.9 | 9.9 | 10.9 | dB |
| GD | Diff Group Delay | $0.3f \le f \le f_C$, F0-F5 = 0, Note 2 | | | ±5 | % |
| HD | Harmonic Distortion Second and Third related to Fundamental | F0-F5 = 0,<br>Vout = 1.5Vp-p, Fin = 6.0MHz<br>S0-S4 = 0 (no slimming)<br>S0-S4 = 1 (full slimming) | | | <br>–45<br>–40 | <br>dB<br>dB |
| ICN | Idle Channel Noise (VIN = 0, DC – 78MHz) | F0-F5 = 0, VOLP<br>S0-S4 = 0 (no slimming)<br>S0-S4 = 1 (full slimming) | | | <br>2<br>6 | <br>mVrms<br>mVrms |
| DR | Dynamic Range (Signal/(Noise + Distor)) Signal = 1Vp-p | F0-F5 = 0, Fin = 6.0MHz<br>S0-S4 = 0 (no slimming)<br>S0-S4 = 1 (full slimming) | | | <br>–41<br>–35 | <br>dB<br>dB |
| PSRR | Power Supply Rejection | 100mVp-p sinewave on Vcc<br>F0-F5 = 0, S0-S4 = 0, Vin = 0<br>Fin = 1.0MHz<br>Fin = 40MHz | | <br><br>40<br>30 | | <br><br>dB<br>dB |
| DELP HI | Phase Shift between LP and HP Output | All F's and S's = 0<br>Vin = 1Vp-p, Fin = 6.0MHz | 87.5 | 90 | 92.5 | Degree |
| **ANALOG** | | | | | | |
| VIP | Input Signal Monotonicity | All F's and S's = 0, (VINP - VINM)<br>Fin = 6.0MHz | | <br>1 | <br>2 | <br>Vp-p |
| RID | Differential Input Resistance | VIN = 100mVp-p at 4.5MHz | 1.6 | 2 | 2.5 | Kohms |
| CID | Differential Input Capacitance | VIN = 100mVp-p at 4.5MHz | | 5 | | pF |
| ZIC | Common-mode Input Impedence | | | 1 | | Kohms |
| VOS | Output Offset Voltage | Differential VOLP or VOHP<br>Auto Zero ON (S0-S4 = 0 or 1)<br>Auto Zero OFF (S0-S4 = 0)<br>Auto Zero OFF (S0-S4 = 1) | | | <br>±10<br>±400<br>±400 | <br>mV<br>mV<br>mV |

## ELECTRICAL CHARACHTERISTICS

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP. | MAX | UNITS |
|---|---|---|---|---|---|---|
| **ANALOG (Continued)** | | | | | | |
| ROD | Output Resistance | Differential VIN = 0; at 4.5MHz | | 5 | | Ω |
| COD | Output Capacitance | Differential VIN = 0; at 4.5MHz | | 8 | | pF |
| ROC | Output Resistance<br>Common Mode | Common mode<br>VIN = 0; at 4.5MHz | | 5 | | Ω |
| COC | Output Capacitance<br>Common Mode | Common mode<br>VIN = 0; at 4.5MHz | | 15 | | pF |
| CLSE | Load Capacitance | VOLP; RB1 = 750Ω<br>VOHP; RB2 = 750Ω | | | 50<br>50 | pF<br>pF |
| RLSE | Load Resistance | VOLP<br>VOHP | 400<br>400 | | | Ω<br>Ω |
| RLOZ | Input Resistance | Diff; PD and/or RW bit = 1 | | | 350 | Ω |
| $I_{OB}$ | Output Buffer Bias Current | VOLP or VOHP, VOLM or VOHM | 1 | 1.4 | | mA |
| $I_{OSC}$ | Short Circuit Output Current | VOLP or VOHP, VOLM or VOHM | | 44 | 60 | mA |

**Note 1:** Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.
**Note 2:** Tested only at max $f_C$ setting, however this parameter is guaranteed by characterization over entire range.

## FUNCTIONAL DESCRIPTION

### INTRODUCTION

Many of the high-frequency continuous-time filters have principally utilized a basic integrator consisting of a transconductance stage driving a passive integrating capacitor. These approaches are susceptible to frequency response variations due to the parasitic capacitances associated with the parasitic-sensitive output nodes of the integrator. This type of transconductance stage also often has low open-circuit voltage gain, resulting in limited practical Q range in the filter. The use of an active parasitic-insensitive integrator, has generally been avoided in these filters because of the additional excess phase that the amplifier contributes.

The ML6024 is a continuous-time filter based on a transconductor and a high-speed parasitic free active integrator, allowing complete independence of the filter response from interconnect parasitics and a very wide range of realizable filter Q. A unique approach to cancelling the excess phase contributed by the hi-speed amplifier allows this filter to achieve reproducible responses at 9.0MHz filter bandwidth. This active integrator incorporates a novel technique for setting the transconductance Gm value as a function of an external precision resistor, independent of temperature and supply, in conjunction with a trim technique to adjust capacitor process tolerances, thus eliminating the need for an on-chip PLL for tuning.

The ML6024 filter consists of a 6th order Bessel low-pass and a 2nd order cosine equalizer stage. It is made up of three biquads with lowpass and bandpass outputs. Both outputs of the last stage are available with matched group-delay characteristics. The corner frequency is digitally programmable to 64 values over a 4 to 1 range, through the serial microprocessor interface. This is accomplished internally by changing the integrating capacitor value. Slimming equalization is done by digitally programming two real-symmetric zeroes, through the serial microprocessor interface. This boosts the high frequency response in 32 steps from 0 to 10 dB. The slimmer can also be disabled through an external pin.

In a typical application, the ML6024 is used together with a pulse detector such as the ML541, ML4041 or the ML8464 , making up a section of the AGC loop. Thus, the output of the AGC amplifier is AC coupled to the ML6024 input and the output of the ML6024 is AC coupled not only to the rectifier input thus closing the AGC loop, but also to the pulse detector input. The ML6024 provides two sets of fully balanced outputs. The lowpass outputs and the differentiated lowpass outputs. The ML6024 input and output common mode voltage biases are generated on-chip. The ML6024 consists of an input common bias circuit, a programmable continuous type equalizer filter with normal and differentiated lowpass outputs, followed by output buffers, and a high speed serial microprocessor interface. The ML6024 processes only differential input signals, common mode inputs are rejected. The output should also be taken differentially in order to obtain the best performance.

### INPUT COMMON MODE

The input common mode bias consists of two resistors as shown in the block diagram, and a buffer which biases the center point with a well defined voltage required by the internal circuitry. These resistors are 1000 Ohms each and together with the external coupling capacitor define the lower corner frequency of the transfer function.

## EQUALIZER FILTER

The filter transfer function is composed of a second order numerator and a sixth order denominator. The low frequency attenuation is set internally to 0dB. The numerator realizes two zeros symmetrical to the imaginary axis, one in the left and the other in the right half plane. The location of the zeros is programmable. This realizes a digitally programmable pulse slimming function in order to overcome intersymbol interference and thus contribute to increasing bit density. The slimming level is controlled by 5 bits in the control register, thus providing 32 different choices between 0 to 10 dB. The denominator approximately realizes a maximally flat group delay (Bessel) function with a digitally programmable corner frequency controlled by 6 bits in the control register, thus providing 64 different cutoff frequencies. (Table 2)

## SLIMMING LEVEL

The slimming levels generated by the slimming bits are shown below. There are 5 bits of control, S0 - S4. The typical gain of the equalizer at the cutoff frequency is shown in the table below. The gain at $f_C$ in dB is also given by the formula :

$$\text{Gain (dB)} = 20 \times \text{Log}\,(0.707 \times (1 + 0.06868 \times K))$$

where K = 0, 1, . . . 31

## CUTOFF FREQUENCY

There are 6 bits in the control register that controls the position of the cutoff frequency, F0 - F5. The typical values of the cutoff (-3dB) frequency are shown in the table below for the case when S0 - S4=0 (no slimming). There are a total of 64 frequencies available from 9.0MHz down to 2.09MHz. Bits F1 - F5 will select one of 32 frequency settings in a monotonic fashion. Bit F0 is used to shift the whole frequency setting range by 5% lower than each of the 32 settings given by F1 - F5. This offers a scheme to increase the effective resolution of the cutoff frequency programmability. This feature is specially useful in the higher frequency range, where the granularity is coarse.

For example :

By setting F0 = 0,

Cutoff frequency = 9.0MHz with F5 - F1 = 00000 and

Cutoff frequency = 8.18MHz with F5 - F1 = 00001, the next consecutive setting.

Frequency delta between consecutive settings = .81MHz or about 9% of 9.0MHz.

By setting F0 = 1, we can shift the consecutive cutoff frequency settings as follows :

Cutoff frequency = 9.0MHz with (F5 - F1, F0) = (00000, 0)

Cutoff frequency = 8.55MHz with (F5 - F1, F0) = (00000, 1) Delta = 0.45MHz

**TABLE 1: TABLE OF SLIMMING LEVEL PROGRAMMING VALUES**

| S4 | S3 | S2 | S1 | S0 | K | GAIN AT $f_C$ (dB) | STEPS (dB) |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | - 3.0 | |
| 0 | 0 | 0 | 0 | 1 | 1 | - 2.4 | 0.6 |
| 0 | 0 | 0 | 1 | 0 | 2 | - 1.9 | 0.5 |
| 0 | 0 | 0 | 1 | 1 | 3 | - 1.4 | 0.5 |
| 0 | 0 | 1 | 0 | 0 | 4 | - 0.9 | 0.5 |
| 0 | 0 | 1 | 0 | 1 | 5 | - 0.4 | 0.5 |
| 0 | 0 | 1 | 1 | 0 | 6 | - 0.0 | 0.4 |
| 0 | 0 | 1 | 1 | 1 | 7 | 0.4 | 0.4 |
| 0 | 1 | 0 | 0 | 0 | 8 | 0.8 | 0.4 |
| 0 | 1 | 0 | 0 | 1 | 9 | 1.2 | 0.4 |
| 0 | 1 | 0 | 1 | 0 | 10 | 1.5 | 0.3 |
| 0 | 1 | 0 | 1 | 1 | 11 | 1.9 | 0.4 |
| 0 | 1 | 1 | 0 | 0 | 12 | 2.2 | 0.3 |
| 0 | 1 | 1 | 0 | 1 | 13 | 2.5 | 0.3 |
| 0 | 1 | 1 | 1 | 0 | 14 | 2.8 | 0.3 |
| 0 | 1 | 1 | 1 | 1 | 15 | 3.1 | 0.3 |
| 1 | 0 | 0 | 0 | 0 | 16 | 3.4 | 0.3 |
| 1 | 0 | 0 | 0 | 1 | 17 | 3.7 | 0.3 |
| 1 | 0 | 0 | 1 | 0 | 18 | 4.0 | 0.3 |
| 1 | 0 | 0 | 1 | 1 | 19 | 4.2 | 0.2 |
| 1 | 0 | 1 | 0 | 0 | 20 | 4.5 | 0.3 |
| 1 | 0 | 1 | 0 | 1 | 21 | 4.7 | 0.2 |
| 1 | 0 | 1 | 1 | 0 | 22 | 5.0 | 0.3 |
| 1 | 0 | 1 | 1 | 1 | 23 | 5.2 | 0.2 |
| 1 | 1 | 0 | 0 | 0 | 24 | 5.4 | 0.2 |
| 1 | 1 | 0 | 0 | 1 | 25 | 5.7 | 0.3 |
| 1 | 1 | 0 | 1 | 0 | 26 | 5.9 | 0.2 |
| 1 | 1 | 0 | 1 | 1 | 27 | 6.1 | 0.2 |
| 1 | 1 | 1 | 0 | 0 | 28 | 6.3 | 0.2 |
| 1 | 1 | 1 | 0 | 1 | 29 | 6.5 | 0.2 |
| 1 | 1 | 1 | 1 | 0 | 30 | 6.7 | 0.2 |
| 1 | 1 | 1 | 1 | 1 | 31 | 6.9 | 0.2 |

Cutoff frequency = 8.18MHz with (F5 - F1, F0) = (00001, 0) Delta = 0.37MHz

Hence the frequency delta between consecutive settings is lower, thus giving higher resolution.

In the table 2 below, the cutoff frequencies are shown as two columns depending on the F0 bit being zero or one. The monotonicity is guaranteed within the individual frequency columns, however because of the limitations of the 5% frequency circuitry, the monotonicity between the two columns cannot be guaranteed. This is especially significant at the lower end of the frequency range, where the difference in frequencies between the two column settings becomes very close (< 1%). Further tuning of the cutoff frequency down to the 1 to 10% range can be achieved by modifying the value of the external resistor

from its ideal 15kΩ value by 1 to 10%, which shifts the whole response. Larger changes are not recommended for proper operation of the filter. The corner frequency is given by the formula outlined below :

$$f_C = \left( \frac{13.5 \times (1 - F0 \times 0.05)}{[1 + 0.1 \times INT(N/2)]} \times \frac{10k\Omega}{Rext} \right) MHz$$

INT = Integer

## OUTPUT BUFFER

The output buffer is the final stage of the ML6024 for both the normal and differentiated outputs. This is a fully differential buffer with unity gain. Only 1.4 mA of sinking current is provided on chip. More drive can be obtained by connecting external resistors to ground. The common mode output voltage is typically 2V.

## SERIAL MICROPROCESSOR INTERFACE

The serial microprocessor interface consists of a simple three-wire serial port. It consists of a fourteen bit serial shift register with a double bufferred latch for synchronous and asynchronous loading. A timing diagram and the control word definition are shown below. The 14-bit data word present on the SDATA line is serially shifted into the register on falling edges of the serial shift clock, SCLK, provided the $\overline{CS}$ pin is active (logical zero). F0 should be shifted in first, and F13 (the auto-zero bit) shifted in last as shown below. When the $\overline{CS}$ pin is inactive (logical one), SDATA and SCLK are ignored, and the previously shifted information is latched at the rising edge of $\overline{CS}$ becoming inactive (logical one). It is reccommended that the SCLK input be kept inactive low till such time when it is in use. The SCLK input can run up to speeds of 25 MHz. The Autozero function, if enabled, minimizes the offsets at the filter outputs to 20mV.

**TABLE 2: TABLE OF CUTOFF FREQUENCY PROGRAMMING VALUES IN MHZ**

| F5 | F4 | F3 | F2 | F1 | N | $f_C$ with F0 = 0 | N | $f_C$ with F0 = 1 |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 9.0 | | |
| 0 | 0 | 0 | 0 | 0 | | | 1 | 8.55 |
| 0 | 0 | 0 | 0 | 1 | 2 | 8.18 | | |
| 0 | 0 | 0 | 0 | 1 | | | 3 | 7.77 |
| 0 | 0 | 0 | 1 | 0 | 4 | 7.50 | | |
| 0 | 0 | 0 | 1 | 0 | | | 5 | 7.13 |
| 0 | 0 | 0 | 1 | 1 | 6 | 6.92 | | |
| 0 | 0 | 0 | 1 | 1 | | | 7 | 6.57 |
| 0 | 0 | 1 | 0 | 0 | 8 | 6.43 | | |
| 0 | 0 | 1 | 0 | 0 | | | 9 | 6.11 |
| 0 | 0 | 1 | 0 | 1 | 10 | 6.0 | | |
| 0 | 0 | 1 | 0 | 1 | | | 11 | 5.70 |
| 0 | 0 | 1 | 1 | 0 | 12 | 5.63 | | |
| 0 | 0 | 1 | 1 | 0 | | | 13 | 5.35 |
| 0 | 0 | 1 | 1 | 1 | 14 | 5.29 | | |
| 0 | 0 | 1 | 1 | 1 | | | 15 | 5.03 |
| 0 | 1 | 0 | 0 | 0 | 16 | 5.0 | | |
| 0 | 1 | 0 | 0 | 0 | | | 17 | 4.75 |
| 0 | 1 | 0 | 0 | 1 | 18 | 4.74 | | |
| 0 | 1 | 0 | 0 | 1 | | | 19 | 4.50 |
| 0 | 1 | 0 | 1 | 0 | 20 | 4.50 | | |
| 0 | 1 | 0 | 1 | 1 | 22 | 4.29 | | |
| 0 | 1 | 0 | 1 | 0 | | | 21 | 4.27 |
| 0 | 1 | 1 | 0 | 0 | 24 | 4.09 | | |
| 0 | 1 | 0 | 1 | 1 | | | 23 | 4.07 |
| 0 | 1 | 1 | 0 | 1 | 26 | 3.91 | | |
| 0 | 1 | 1 | 0 | 0 | | | 25 | 3.89 |
| 0 | 1 | 1 | 1 | 0 | 28 | 3.75 | | |
| 0 | 1 | 1 | 0 | 1 | | | 27 | 3.71 |
| 0 | 1 | 1 | 1 | 1 | 30 | 3.60 | | |
| 0 | 1 | 1 | 1 | 0 | | | 29 | 3.56 |
| 1 | 0 | 0 | 0 | 0 | 32 | 3.46 | | |
| 0 | 1 | 1 | 1 | 1 | | | 31 | 3.42 |
| 1 | 0 | 0 | 0 | 1 | 34 | 3.33 | | |
| 1 | 0 | 0 | 0 | 0 | | | 33 | 3.29 |
| 1 | 0 | 0 | 1 | 0 | 36 | 3.21 | | |
| 1 | 0 | 0 | 0 | 1 | | | 35 | 3.17 |
| 1 | 0 | 0 | 1 | 1 | 38 | 3.11 | | |
| 1 | 0 | 0 | 1 | 0 | | | 37 | 3.05 |
| 1 | 0 | 1 | 0 | 0 | 40 | 3.0 | | |
| 1 | 0 | 0 | 1 | 1 | | | 39 | 2.95 |
| 1 | 0 | 1 | 0 | 1 | 42 | 2.9 | | |
| 1 | 0 | 1 | 0 | 0 | | | 41 | 2.85 |
| 1 | 0 | 1 | 1 | 0 | 44 | 2.81 | | |
| 1 | 0 | 1 | 0 | 1 | | | 43 | 2.76 |
| 1 | 0 | 1 | 1 | 1 | 46 | 2.73 | | |
| 1 | 0 | 1 | 1 | 0 | | | 45 | 2.67 |
| 1 | 1 | 0 | 0 | 0 | 48 | 2.65 | | |
| 1 | 0 | 1 | 1 | 1 | | | 47 | 2.59 |
| 1 | 1 | 0 | 0 | 1 | 50 | 2.57 | | |
| 1 | 1 | 0 | 0 | 0 | | | 49 | 2.51 |
| 1 | 1 | 0 | 1 | 0 | 52 | 2.50 | | |
| 1 | 1 | 0 | 0 | 1 | | | 51 | 2.44 |
| 1 | 1 | 0 | 1 | 1 | 54 | 2.43 | | |
| 1 | 1 | 0 | 1 | 0 | | | 53 | 2.38 |
| 1 | 1 | 1 | 0 | 0 | 56 | 2.37 | | |
| 1 | 1 | 1 | 0 | 0 | | | 55 | 2.31 |
| 1 | 1 | 1 | 0 | 1 | 58 | 2.31 | | |
| 1 | 1 | 1 | 0 | 0 | | | 57 | 2.25 |
| 1 | 1 | 1 | 1 | 0 | 60 | 2.25 | | |
| 1 | 1 | 1 | 0 | 1 | | | 59 | 2.19 |
| 1 | 1 | 1 | 1 | 1 | 62 | 2.19 | | |
| 1 | 1 | 1 | 1 | 0 | | | 61 | 2.14 |
| 1 | 1 | 1 | 1 | 1 | | | 63 | 2.08 |

**Note:** N is the decimal value of the cutoff frequency bits (F5 - F0), in the control register

## TIMING DIAGRAM

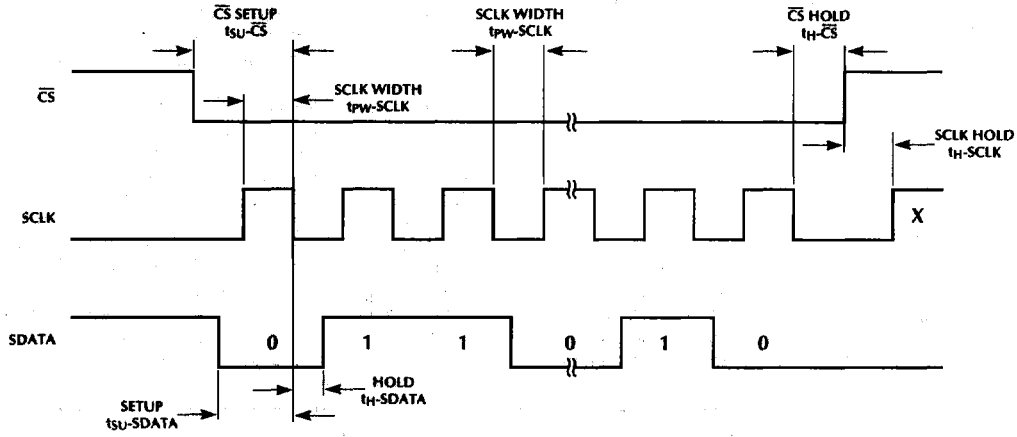


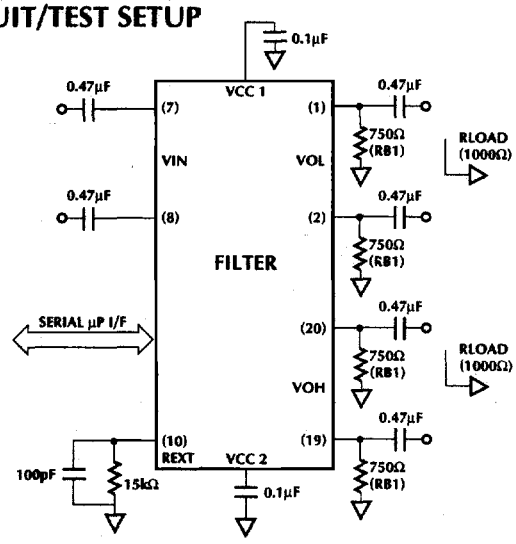

Figure 1.

## CONTROL REGISTER DEFINITION

| END | F13 | F12 | F11 | S4 | S3 | S2 | S1 | S0 | F5 | F4 | F3 | F2 | F1 | F0 | START |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | AZ | PD | R/W | SLIMMING CONTROL | | | | | FREQUENCY CONTROL | | | | | | |

| | | |
|---|---|---|
| AZ | AutoZero | 1 = Autozero circuitry activated<br>0 = Autozero circuitry inactive |
| PD | Power Down | 1 = Chip is in power down mode<br>0 = Chip is fully powered up |
| R/W | Read/Write | 1 = Write data mode<br>0 = Read data mode |

## APPLICATIONS CIRCUIT/TEST SETUP




Note: Decoupling capacitors need to be very close to the chip, to prevent oscillations.

## ORDERING INFORMATION

| PART NUMBER | TEMPERATURE RANGE | PACKAGE |
|---|---|---|
| ML6024CR | 0°C to 70°C | 20-Pin SSOP (R20) |