ULTRA PRECISION 4×4 CML SWITCH WITH INTERNAL I/O TERMINATION

Precision Edge® SY58040U

FEATURES

- **Provides crosspoint switching between any input pair to any output pair**
- **Guaranteed AC performance over temperature and voltage:**
  - **DC to >5Gbps throughput**
  - **<350ps propagation delay**
  - **<60ps t_r/t_f times**
  - **<25ps skew (output-to-output)**
- **Unique, patent-pending, channel-to-channel isolation design provides superior crosstalk performance**
- **Ultra-low jitter design:**
  - **<1ps$_{RMS}$ random jitter**
  - **<10ps$_{PP}$ deterministic jitter**
  - **<10ps$_{PP}$ total jitter (clock)**
  - **<0.7ps$_{RMS}$ crosstalk-induced jitter**
- **Unique, patent-pending, 50Ω input termination extended CMVR, and VT pin accepts DC- and AC-coupled differential inputs**
- **400mV CML output swing**
- **50Ω source terminated outputs minimize round-trip reflections**
- **Power supply 2.5V ±5% or 3.3V ±10%**
- **–40°C to +85°C temperature range**
- **Available in 44-pin (7mm × 7mm) MLF® package**
- **Pb-Free green package**

APPLICATIONS

- **Data communication systems**
- **All SONET/SDH data/clock applications**
- **All Fibre Channel applications**
- **All Gigabit Ethernet applications**

Precision Edge®

DESCRIPTION

The SY58040U is a low jitter, low skew, high-speed 4×4 crosspoint switch optimized for precision telecom and enterprise server/storage distribution applications. The SY58040U distributes clock frequencies from DC to 4GHz, and data rates to 5Gbps guaranteed over temperature and voltage.

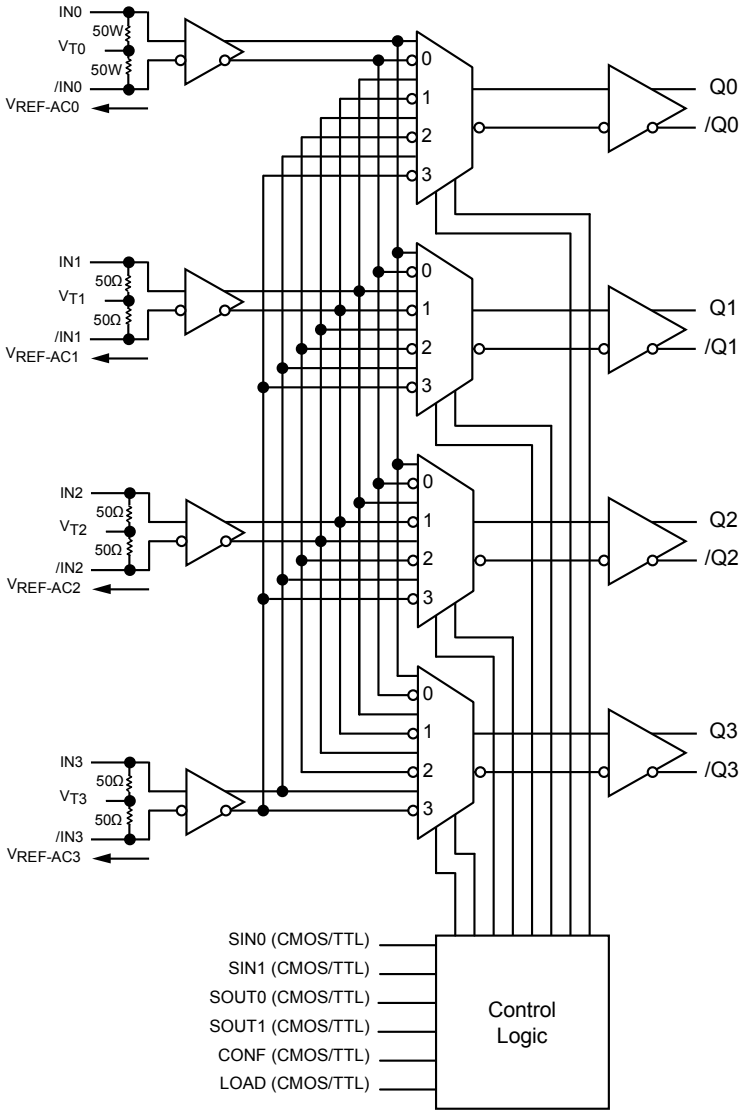
The SY58040U differential input includes Micrel's unique, 3-pin input termination architecture that directly interfaces to any differential signal (AC- or DC-coupled) as small as 100mV (200mV$_{pp}$) without any level shifting or termination resistor networks in the signal path. The outputs are 50Ω source-terminated CML with extremely fast rise/fall times guaranteed to be less than 60ps.

The SY58040U features a patent-pending isolation design that significantly improves on channel-to-channel crosstalk performance.

The SY58040U operates from a 2.5V ±5% or 3.3V ±10% supply and is guaranteed over the full industrial temperature range of –40°C to +85°C. The SY58040U is part of Micrel's high-speed, Precision Edge® product line.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

FUNCTIONAL BLOCK DIAGRAM

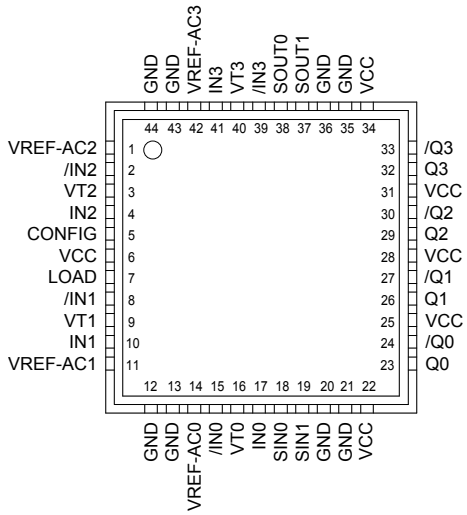


TRUTH TABLES

Input Select Address Table		
SIN1	**SIN0**	**INPUT**
0	0	IN0
0	1	IN1
1	0	IN2
1	1	IN3

Output Select Address Table		
SOUT1	**SOUT0**	**OUTPUT**
0	0	Q0
0	1	Q1
1	0	Q2
1	1	Q3

PACKAGE/ORDERING INFORMATION



44-Pin MLF® (MLF-44)

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY58040UMI	MLF-44	Industrial	SY58040U	Sn-Pb
SY58040UMITR[2]	MLF-44	Industrial	SY58040U	Sn-Pb
SY58040UMY[3]	MLF-44	Industrial	SY58040U Pb-Free bar-line indicator	Pb-Free Matte-Sn
SY58040UMYTR[2, 3]	MLF-44	Industrial	SY58040U Pb-Free bar-line indicator	Pb-Free Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC electricals only.
2. Tape and Reel.
3. Pb-Free package recommended for new designs.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
17, 15, 10, 8, 4, 2, 41, 39	IN0, /IN0 IN1, /IN1 IN2, /IN2 IN3, /IN3	Differential Inputs: These input pairs are the differential signal inputs to the device. Inputs accept AC or DC-coupled signals as small as 100mV. Each pin of a pair internally terminates to a VT pin through 50Ω. Note that these inputs will default to an indeterminate state if left open. Please refer to the “Input Interface Applications” section for more details.
16, 9, 3, 40	VT0, VT1 VT2, VT3	Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. The VT pins provide a center-tap to a termination network for maximum interface flexibility. See “Input Interface Applications” section for more details.
14, 11, 1, 42	VRef_AC0 VRef_AC1 VRef_AC2 VRef_AC3	Reference Voltage: This output biases to V_{CC}–1.2V. It is used when AC coupling the inputs. Connect VRef-AC output pin to the VT input pin. Bypass each VRef-AC pin with a 0.01µF low ESR capacitor to V_{CC}. See “Input Interface Applications” section for more details.
18 19	SIN0 SIN1	These single-ended TTL/CMOS-compatible inputs address the data inputs. Note that these inputs are internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open.
38 37	SOUT0 SOUT1	These single-ended TTL/CMOS-compatible inputs address the data outputs. Note that these inputs are internally connected to a 25kΩ pullup resistor and will default to a logic HIGH state if left open.
5 7	CONF, LOAD	These single-ended TTL/CMOS compatible inputs control the transfer of the addresses to the internal multiplexers. See “Address Tables” and “Timing Diagram” sections for more details. Note that these inputs are internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open. *Configuration Sequence* 1. Load: Loads configuration into buffer, while Configuration Buffer holds existing switch configuration. 2. Configuration: Loads new configuration into the Configuration Buffer and updates switch configuration. *Buffer Mode* The SY58040U defaults to buffer mode (IN-to-Q) if the load and configuration control signals are floating.
23, 24, 26, 27, 29, 30 32, 33	Q0, /Q0, Q1, /Q1, Q2, /Q2, Q3, /Q3,	Differential Outputs: These CML output pairs are the outputs of the device. Please refer to the truth table below for details. Unused output pairs may be left open. Each output is designed to drive 400mV into 100Ω across the pair, or 50Ω to V_{CC}.
6, 22, 25, 28, 31, 34	VCC	Positive power supply. Bypass with 0.1µF//0.01µF low ESR capacitors and place as close to each V_{CC} pin.
12, 13, 20, 21, 35, 36, 43, 44	GND, Exposed pad	Ground. GND and EPad must both be connected to most negative potential of chip ground.

Absolute Maximum Ratings[1]

Power Supply Voltage (V_{CC}) .....–0.5V to +4.0V
Input Voltage (V_{IN}).....–0.5V to V_{CC}
CML Output Voltage (V_{OUT}) .....V_{CC} –0.5V to V_{CC} +5.0V
Termination Current[3]
Source or sink current on VT pin ..... ±100mA
Input Current[3]
Source or sink current on IN, /IN ..... ±50mA
V_{REF-AC} Current[3]
Source or sink current on IN, /IN ..... ±2mA
Lead Temperature (soldering, 20 sec.)..... 260°C
Storage Temperature Range (T_S)..... –65°C to +150°C

Operating Ratings[2]

Power Supply Voltage (V_{CC}) ..... +2.375V to +3.60V
Ambient Temperature Range (T_A) ..... –40°C to +85°C
Package Thermal Resistance[4]
MLF® (θ_{JA})
Still-Air ..... 23°C/W
MLF® (ψ_{JB})
Junction-to-board..... 12°C/W

DC ELECTRICAL CHARACTERISTICS[5]

T_A= –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage	V_{CC} = 2.5V.	2.375	2.5	2.625	V
		V_{CC} = 3.3V.	3.0	3.3	3.6	V
I_{CC}	Power Supply Current	No load, max. V_{CC}. Includes current from internal 50Ω pull-up on each output.		225	300	mA
R_{IN}	Input Resistance (IN-to-V_T, /IN-to-V_T)		45	50	55	Ω
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
V_{IH}	Input HIGH Voltage (IN-to-/IN)	**Note 6**	V_{CC}–1.6		V_{CC}	V
V_{IL}	Input LOW Voltage (IN-to-/IN)		0		V_{IH}–0.1	V
V_{IN}	Input Voltage Swing (IN-to-/IN)	See Figure 1a.	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage Swing |IN – /IN|	See Figure 1b.	0.2			V
V_{T_IN}	IN to V_T (IN-to-/IN)				1.28	V
V_{REF-AC}	Output Reference Voltage		V_{CC}–1.3	V_{CC}–1.2	V_{CC}–1.1	V

Notes:

1. Permanent device damage may occur if ratings in the “Absolute Maximum Ratings” section are exceeded. This is a stress rating only and functional operation is not implied for conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability, use for input of the same package only.
4. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device’s most negative potential on the PCB. θ_{JA} uses 4-layer in still-air number, unless otherwise stated.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. V_{IH} (min) not lower than 1.2V.

CML OUTPUT DC ELECTRICAL CHARACTERISTICS[7]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A= –40°C to +85°C; R_L = 100Ω across each output pair, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage Q, /Q		V_{CC}–0.040	V_{CC}–0.010	V_{CC}	V
V_{OUT}	Output Differential Swing Q, /Q	See Figure 1a.	325	400		mV
V_{DIFF_OUT}	Differential Output Voltage Swing Q, /Q	See Figure 1b.	650	800		mV
R_{OUT}	Output Source Impedance		45	50	55	Ω

LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS[7]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A= –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current		–125		30	µA
I_{IL}	Input LOW Current	V_{IL} = 0V.	–300			µA

Note:

7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS[8]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A= –40°C to +85°C, R_L = 100Ω across each output pair, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	NRZ data	5			Gbps
		V_{OUT} ≥ 200mV Clock		3		GHz
t_{pd}	Differential Propagation Delay	IN-to-Q	150	225	350	ps
		CONFIG-to-Q			500	ps
t_{pw}	Pulse Width of LOAD/CONFIG signal		1500			ps
Δt_{pd} Tempco	Differential Propagation Delay Temperature Coefficient			225		fs/°C
t_S	Set-Up Time SIN-to-LOAD		800			ps
	SOUT-to-LOAD		800			ps
	LOAD-to-CONFIG		800			ps
	CONFIG-to-LOAD		950			ps
t_H	Hold Time LOAD-to-SIN, LOAD-to-SOUT		800			ps
t_{SKEW}	Output-to-Output Skew	**Note 9**			25	ps
	Part-to-Part Skew	**Note 10**			150	ps
t_{JITTER}	Data Random Jitter (RJ)	**Note 11**			1	ps_{RMS}
	Deterministic Jitter (DJ)	**Note 12**			10	ps_{PP}
	Clock Cycle-to-Cycle Jitter	**Note 13**			1	ps_{RMS}
	Total Jitter (TJ)	**Note 14**			10	ps_{PP}
	Crosstalk-induced Jitter	**Note 15**			0.7	ps_{RMS}
t_r, t_f	Output Rise/Fall Time	At full output swing, 20% to 80%.	20	40	60	ps

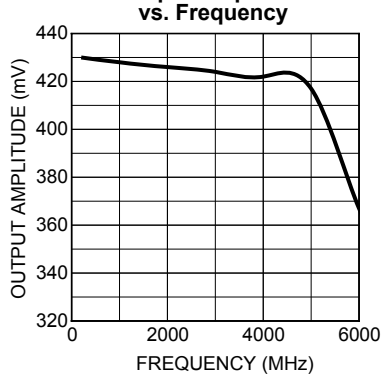
Notes:

8. High-frequency AC-parameters are guaranteed by design and characterization.
9. Output-to-output skew is measured between two different outputs under identical input transitions.
10. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs
11. Random jitter is measured with a K28.7 character pattern, measured at <f_{MAX}.
12. Deterministic jitter is measured at 2.5Gbps/3.2Gbps, with both K28.5 and 2^{23}–1 PRBS pattern.
13. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, $T_n - T_{n-1}$ where T is the time between rising edges of the output signal.
14. Total jitter definition: with an ideal clock input of frequency <f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.
15. Crosstalk induced jitter is defined as the added jitter that results from signals applied to two adjacent channels. It is measured at the output while applying two similar differential clock frequencies that are asynchronous with respect to each other at the inputs.

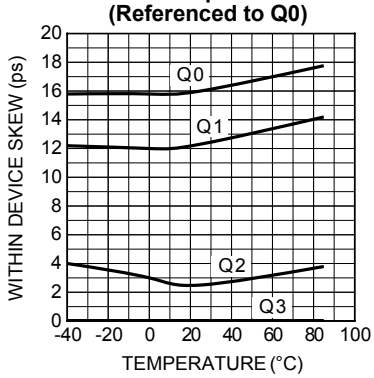
TYPICAL OPERATING CHARACTERISTICS

V_{CC} = 3.3V, GND = 0, V_{IN} = 100mV, T_A = 25°C, unless otherwise stated.

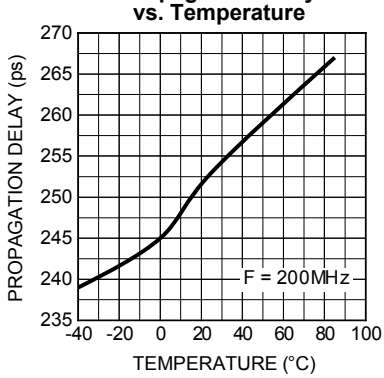
Output Amplitude vs. Frequency



Within-Device Skew vs. Temperature (Referenced to Q0)



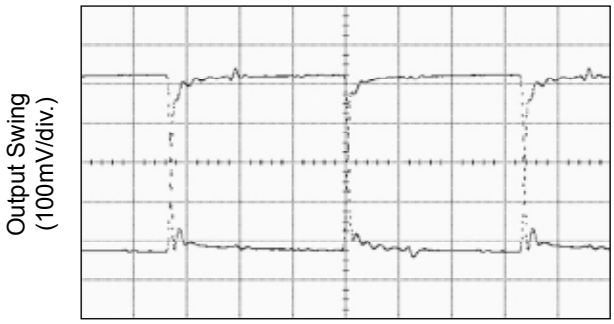
Propagation Delay vs. Temperature



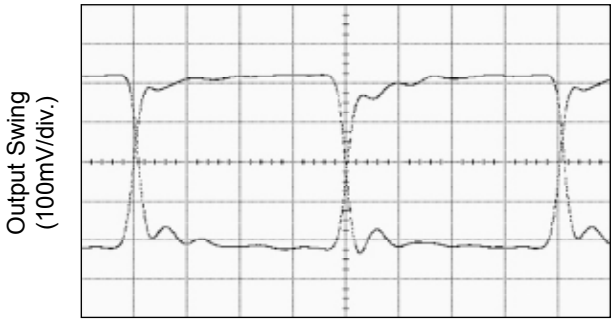
FUNCTIONAL CHARACTERISTICS

V_{CC} = 3.3V, GND = 0, V_{IN} = 100mV, T_A = 25°C, unless otherwise stated.

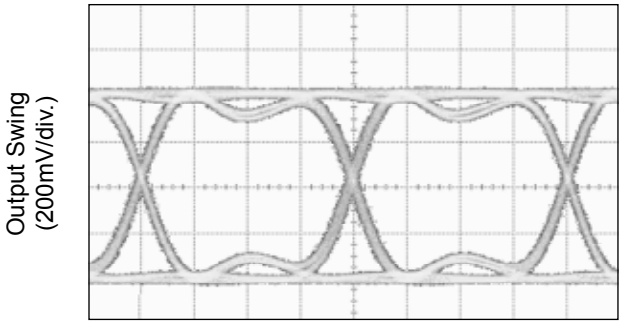
200MHz Output



622MHz Output



5Gbps Output (Q – /Q)



SINGLE-ENDED AND DIFFERENTIAL SWINGS

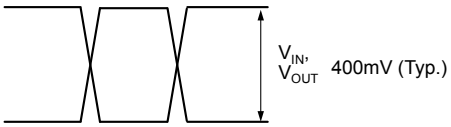


Figure 1a. Single-Ended Voltage Swing

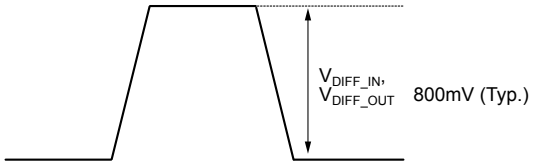
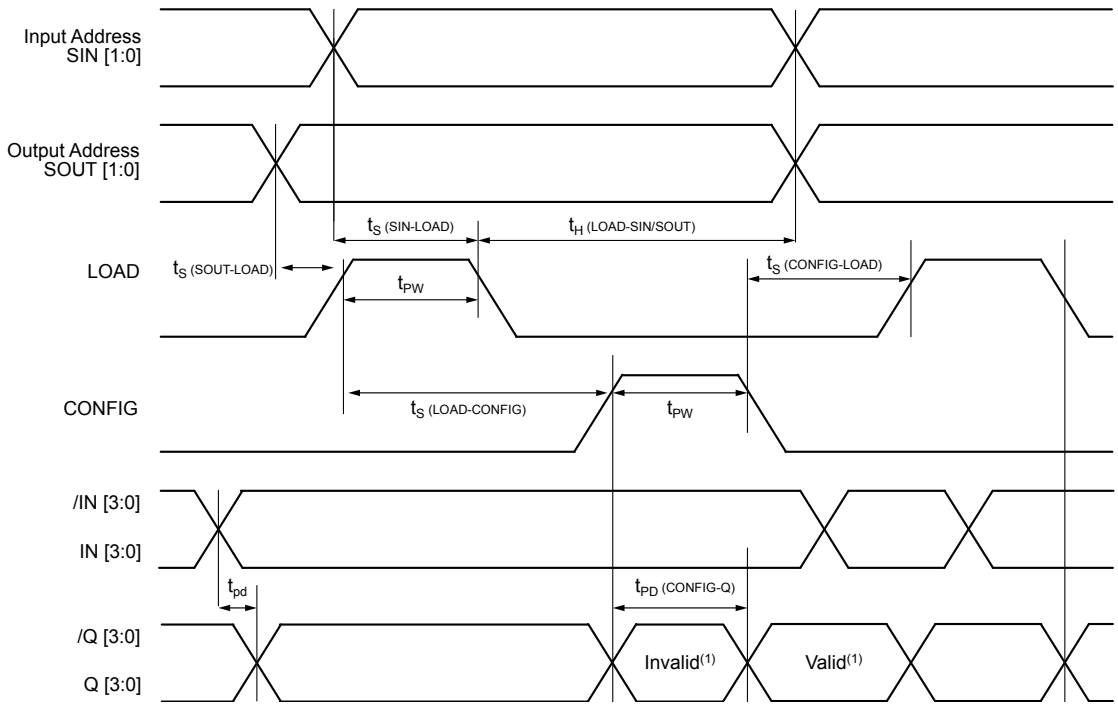


Figure 1b. Differential Voltage Swing

TIMING DIAGRAM



Note:
1. Invalid and Valid refers to onfiguation being changed. All outputs with unchanged configuration remain valid.

INPUT AND OUTPUT STAGES

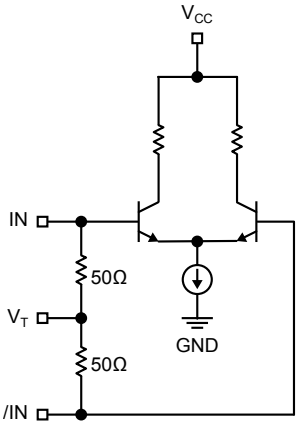


Figure 2a. Simplified Differential Input Stage

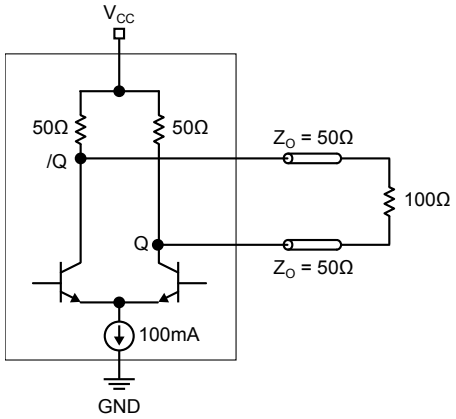


Figure 2b. CML DC-Coupled (100Ω Termination)

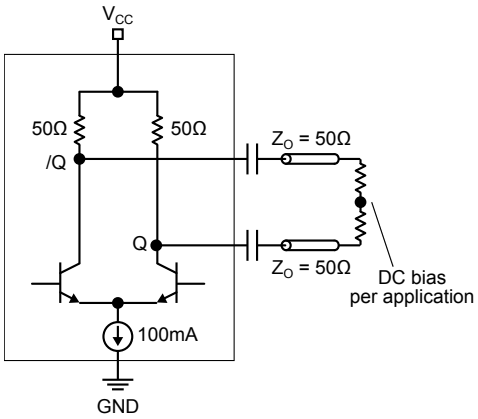
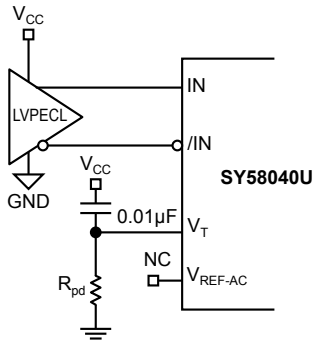


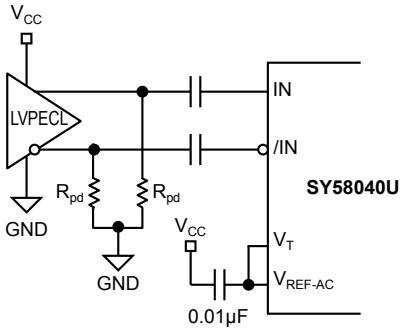
Figure 2c. CML AC-Coupled (50Ω Termination)

INPUT INTERFACE APPLICATIONS



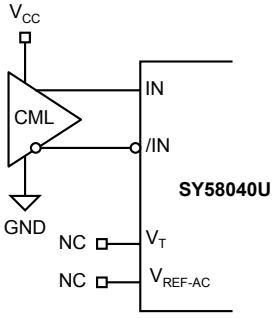
For V_{CC} = 3.3V, R_{pd} = 50Ω.
For V_{CC} = 2.5V, R_{pd} = 19Ω.

Figure 3a. LVPECL Interface (DC-Coupled)



For 3.3V, R_{pd} = 100Ω.
For 2.5V, R_{pd} = 50Ω.

Figure 3b. LVPECL Interface (AC-Coupled)



Option: May connect V_T to V_{CC}.

Figure 3c. CML Interface (DC-Coupled)

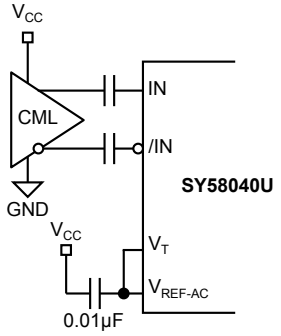


Figure 3d. CML Interface (AC-Coupled)

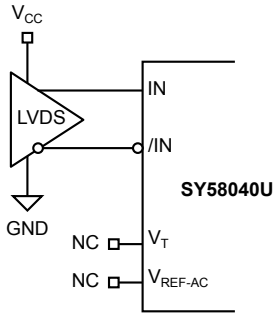
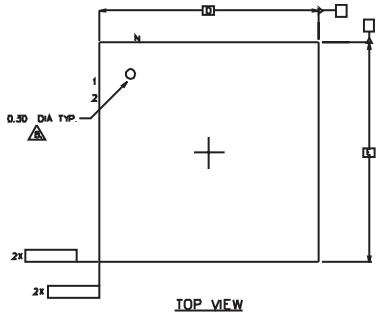


Figure 3e. LVDS Interface

RELATED MICREL PRODUCTS AND SUPPORT DOCUMENTATION

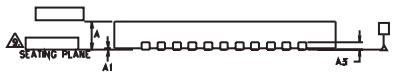
Part Number	Function	Data Sheet Link
SY58040U	Ultra Precision 4×4 CML Crosspoint Switch with Internal Input/Output Termination	http://www.micrel.com/product-info/products/sy58040u.shtml
	MLF® Application Note	www.amkor.com/products/notes_paper/MLF_AppNote.pdf
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

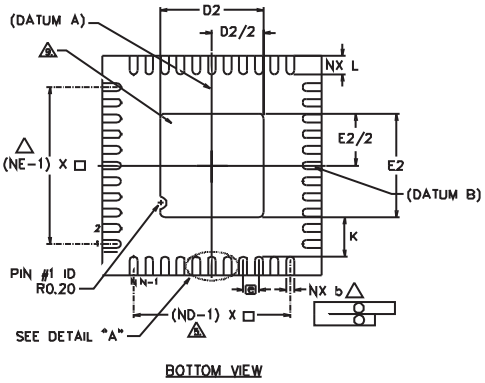
44-PIN *Micro*LeadFrame® (MLF-44)

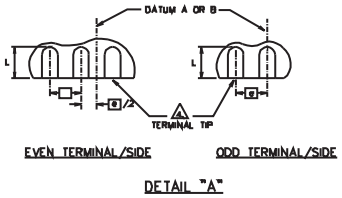


NOTES :

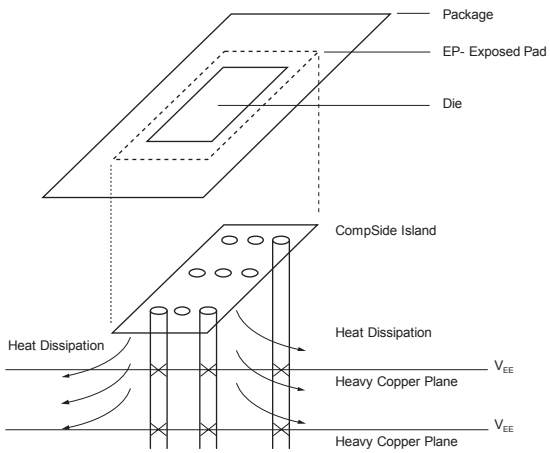
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M, – 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS, θ IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP, IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
6. MAX. PACKAGE WARPAGE IS 0.05 mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LASER MARKED.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. THIS DRAWING CONFORMES TO JEDEC REGISTERED OUTLINE MO-220







SYMBOL	DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		44		3
ND		11		5
NE		11		
L	0.55	0.60	0.65	
b	0.18	0.25	0.30	4
D2	3.20	3.30	3.40	
E2	3.20	3.30	3.40	
D		7.00 BSC		
E		7.00 BSC		
A	0.80	0.85	1.00	
A1	0.00	0.02	0.05	
K		0.20 MIN.		
θ	0	——	12	2



PCB Thermal Consideration for 44-Pin MLF® Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

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