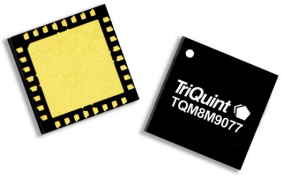
# TQM8M9077

## *0.05-4 GHz Digital Variable Gain Amplifier*

## Applications

- 2G / 3G / 4G Wireless Infrastructure
- LTE / WCDMA / CDMA / EDGE
- IF and RF Applications
- General Purpose Wireless

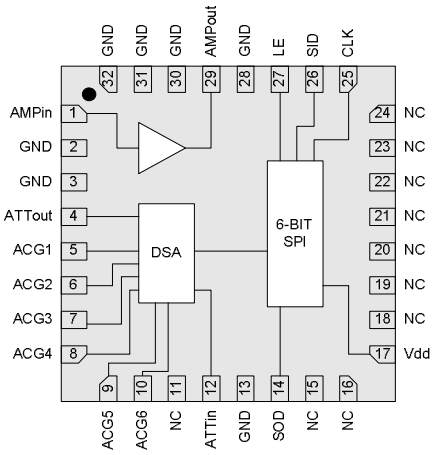



32-pin 5x5mm leadless SMT package

## Product Features

- Integrates DSA + Amp Functionality
- 50-4000 MHz Broadband Performance
- 13 dB Gain @ 2.14 GHz
- 3.9 dB Noise Figure @ max gain setting
- +21.5 dBm P1dB
- +38.5 dBm OIP3
- +5 V Supply Voltage
- 88 mA Operating Current
- MTTF > 1000 Years

## Functional Block Diagram




## General Description

The TQM8M9077 is a digitally controlled variable gain amplifier (DVGA) with a broadband frequency range of 50 to 4000 MHz. The DVGA features high linearity and low noise while providing digital variable gain with a 31.5 dB of range in 0.5 dB steps through a 6-bit serial mode control interface. This combination of performance parameters makes the DVGA ideal for receiver applications requiring gain control with high IIP3.

The TQM8M9077 integrates a high performance digital step attenuator and a high linearity, broadband gain block. Both stages are internally matched to 50 Ohms and do not require any external matching components. A serial output port enables cascading with other serial controlled devices.

The TQM8M9077 is packaged in a RoHS-compliant, compact 5x5 mm surface-mount leadless package. Superior thermal design allows the product to have a minimum MTTF rating of 1000 years at a mounting temperature of +85° C.

The TQM8M9077 is targeted for use in wireless infrastructure, point-to-point, or can be used for any general purpose wireless application.

## Pin Configuration

| Pin # | Symbol |
|---|---|
| 1 | Ampin |
| 2, 3, 13, 28, 30, 31, 32 | GND (Ground) |
| 4 | ATTout |
| 5, 6, 7, 8, 9, 10 | ACG1-6 |
| 11, 15, 16, 18-24 | NC (No Connect) |
| 14 | SOD |
| 12 | ATTin |
| 17 | Vdd |
| 25 | CLK |
| 26 | SID |
| 27 | LE |
| 29 | Ampout |
| Backside Paddle | RF/DC Ground |

## Ordering Information

| Part No. | Description |
|---|---|
| TQM8M9077 | Digital Variable Gain Amplifier |
| TQM8M9077-PCB | 0.3-4.0 GHz Evaluation Board |

Standard T/R size = 2500 pieces on a 13” reel.

# Specifications

## Absolute Maximum Ratings

| Parameter | Rating |
|---|---|
| Storage Temperature | -65 to 150 °C |
| RF Input Power, CW, 50Ω,T = 25ºC | +24 dBm |
| Supply Voltage ($V_{dd}$) | +6 V |
| Digital Input Voltage | $V_{dd}$+0.5 V |

Operation of this device outside the parameter ranges given above may cause permanent damage.

## Recommended Operating Conditions

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| $V_{dd}$ | 4.75 | 5 | 5.25 | V |
| $I_{dd}$ | | 87 | | mA |
| Operating Temp. Range | -40 | | +85 | °C |
| $T_{ch}$ (for >$10^6$ hours MTTF) | | | 190 | °C |

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

## Electrical Specifications

Test conditions unless otherwise noted: $T_{LEAD}$=+25°C, $V_{dd}$=+5V (Configured as DSA followed by Amp)

| Parameter | Conditions | Min | Typical | Max | Units |
|---|---|---|---|---|---|
| Operational Frequency Range | | 50 | | 4000 | MHz |
| Test Frequency | | | 2140 | | MHz |
| Gain | | 11 | 13 | | dB |
| Gain Control Range | | | 31.5 | | dB |
| Gain Accuracy | | | ± (0.3 + 4% of Atten. Setting) Max | | dB |
| Attenuation Step | | | 0.5 | | dB |
| Time $_{rise\ /\ fall}$ | 10% / 90% RF | | 90 | | ns |
| Time $_{on,}$ Time $_{off}$ | 50% CTL to 10% / 90% RF | | 100 | | ns |
| Input Return Loss | | | -17 | | dB |
| Output Return Loss | | | -10.5 | | dB |
| Output P1dB | | | +21.5 | | dBm |
| Output IP3 | See Note 1 | +35.5 | +38.5 | | dBm |
| Noise Figure | At max gain level | | 3.9 | | dB |
| Supply Voltage | | | +5 | | V |
| Supply Current | | 70 | 88 | 110 | mA |
| Thermal Resistance (Rth) | Channel to case | | | 41 | °C/W |

Notes:
1. OIP3 measured with two tones at an output power of +3 dBm / tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the OIP3 using a 2:1 rule.

## Serial Control Interface

The TQM8M9077 has a CMOS SPI™ input compatible serial interface. This serial control interface converts the serial data input stream to parallel output word. The input is 3-wire (CLK, LE and SERIN) SPI™ input compatible. At power up, the serial control interface resets the DSA to the minimum gain state. The 6-bit SERIN word is loaded into the register on rising edge of the CLK, MSB first. When LE is high, CLK is disabled.

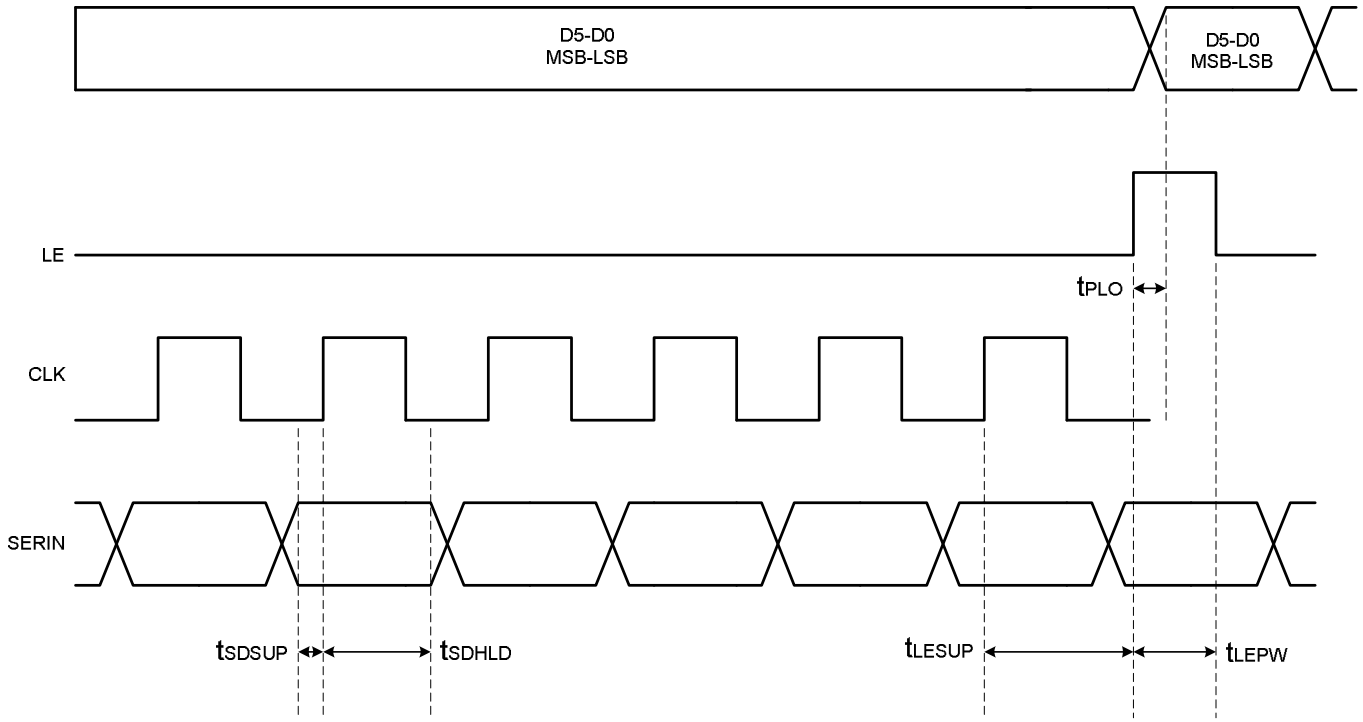
## SERIN (MSB in First 6-Bit Word) Control Logic Truth Table

Test conditions: 25ºC, $V_{dd}$ = +5V

| 6-Bit Control Word to DSA | | | | | | Gain Relative to Maximum Gain |
|---|---|---|---|---|---|---|
| LSB | | | | | MSB | |
| D5 | D4 | D3 | D2 | D1 | D0 | |
| 1 | 1 | 1 | 1 | 1 | 1 | Reference : IL |
| 1 | 1 | 1 | 1 | 1 | 0 | 0.5 dB |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 dB |
| 1 | 1 | 1 | 0 | 1 | 1 | 2 dB |
| 1 | 1 | 0 | 1 | 1 | 1 | 4 dB |
| 1 | 0 | 1 | 1 | 1 | 1 | 8 dB |
| 0 | 1 | 1 | 1 | 1 | 1 | 16 dB |
| 0 | 0 | 0 | 0 | 0 | 0 | 31.5 dB |
| Any combination of the possible 64 states will provide a reduction in gain of approximately the sum of the bits selected. | | | | | | |

## Serial Control Interface Timing Diagram

CLK is disabled when LE is high



## Serial Control Timing Characteristics

Test conditions: 25ºC, $V_{dd}$ = +5V

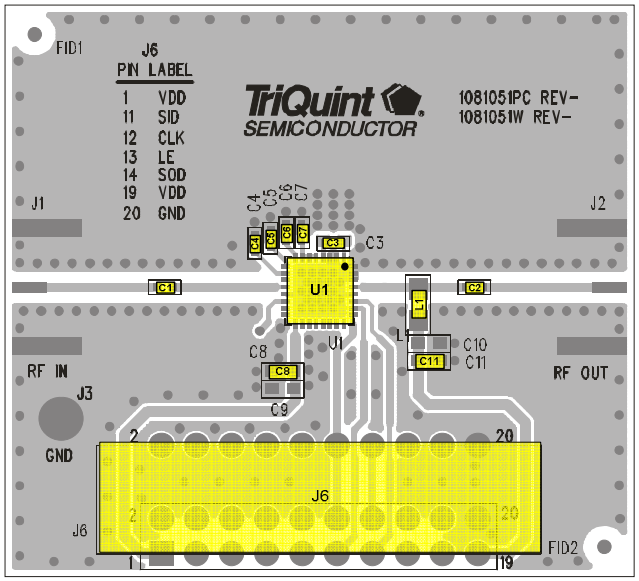
| Parameter | Condition | Min | Max | Units |
|---|---|---|---|---|
| Clock Frequency | 50% Duty Cycle | | 10 | MHz |
| LE Setup Time, $t_{LESUP}$ | after last CLK rising edge | 10 | | ns |
| LE Pulse Width, $t_{LEPW}$ | | 30 | | ns |
| SERIN set-up time, $t_{SDSUP}$ | before CLK rising edge | 10 | | ns |
| SERIN hold-time, $t_{SDHLD}$ | after CLK rising edge | 10 | | ns |
| LE Pulse Spacing $t_{LE}$ | LE to LE pulse spacing | 630 | | ns |
| Propagation Delay $t_{PLO}$ | LE to Parallel output valid | | 30 | ns |

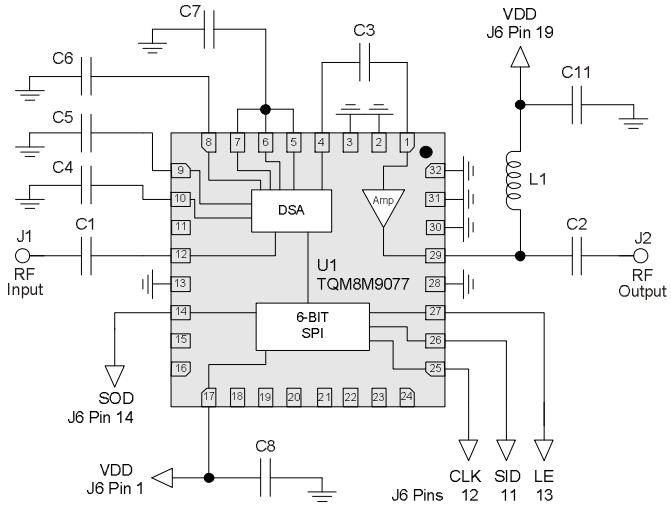
## Serial Control DC Logic Characteristics

Test conditions: 25ºC, $V_{dd}$ = +5V

| Parameter | Condition | Min | Max | Units |
|---|---|---|---|---|
| Low State Input Voltage | | 0 | 0.8 | V |
| High State Input Voltage | | 2.1 | Vdd | V |
| Output High Voltage | On SEROUT | 2.0 | Vdd | V |
| Output Low Voltage | On SEROUT | 0 | 0.8 | V |
| Input Current, $I_{IH}$ / $I_{IL}$ | On SERIN, LE and CLK | -10 | +10 | µA |

## Reference Design 300-4000 MHz




Notes:

1. See PC Board Specifications section for material and stackup.
2. C4, C5, C6 and C7 may be removed for operation above 700 MHz.

## Bill of Material

| Ref Des | Value | Description | Manufacturer | Part Number |
|---|---|---|---|---|
| U1 | n/a | Digital Variable Gain Amp | TriQuint | TQM8M9077 |
| L1 (Note 4) | 47 nH | Inductor, 0603 | Coilcraft | 0603CS-47NXJLW |
| C1, C2, C3 | 68 pF | Capacitor, 0402 | various | |
| C4, C5, C6, C7 | 330 pF | Capacitor, 0402 | various | |
| C8 | 1000 pF | Capacitor, 0603 | various | |
| C11 | 0.01 uF | Capacitor, 0603 | various | |

Note 4: For IF applications (<300 MHz) increase L1 to 330 nH.

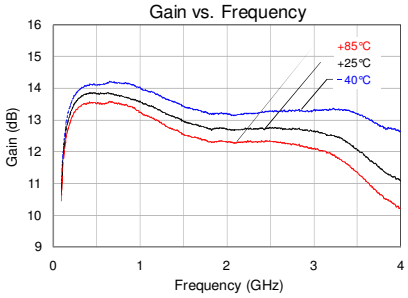
## Typical Performance

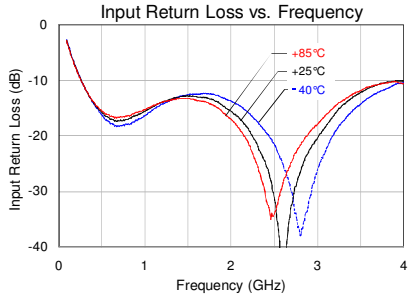
Test Conditions: $V_{dd}$=+5 V, Temp=+25°C

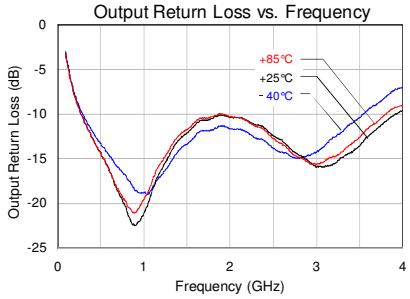
| Frequency | MHz | 500 | 900 | 2140 | 2700 | 3500 | 4000 |
|---|---|---|---|---|---|---|---|
| Gain[1] | dB | 14.1 | 14.0 | 13.0 | 13.0 | 12.4 | 11.4 |
| Input Return Loss | dB | -15.8 | -16.2 | -17.6 | -32.5 | -12.2 | -10.1 |
| Output Return Loss | dB | -14.3 | -22.5 | -10.5 | -13.9 | -13.6 | -9.6 |
| Output P1dB | dBm | +21.5 | +21.7 | +21.5 | +20.5 | +19.6 | +18.3 |
| Output IP3[2] | dBm | +40.7 | +41.2 | +38.5 | +37.8 | +36.3 | +35.6 |
| Noise Figure[3] | dB | 3.0 | 3.1 | 3.9 | 4.3 | 5.5 | 6.2 |
| Amplifier Current | mA | 88 | | | | | |

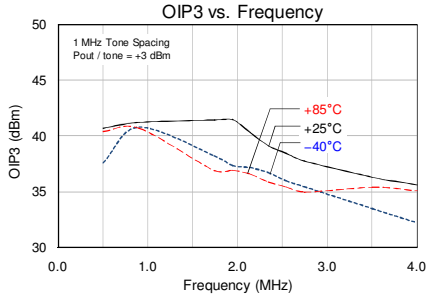
Notes:

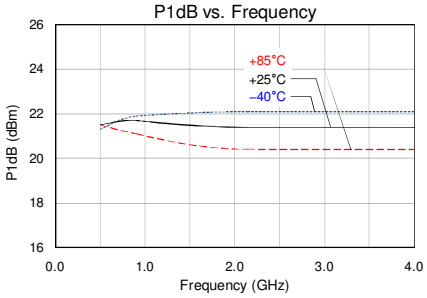
1. Gain values reflect de-embedding of 0.4 dB eval board RF I/O line losses that would not be present in target applications.
2. OIP3 measured with two tones at an output power of +3 dBm / tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the OIP3 using 2:1 rule.
3. NF values reflect de-embedding of eval board RF I/O line losses that would not be present in target applications.
4. Unless otherwise stated, performance plots shown below for DVGA maximum gain state.

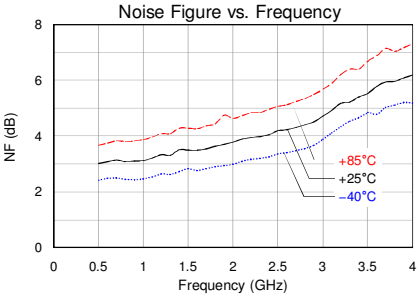


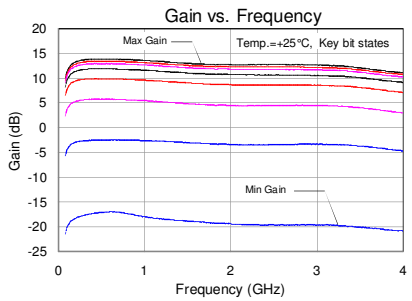



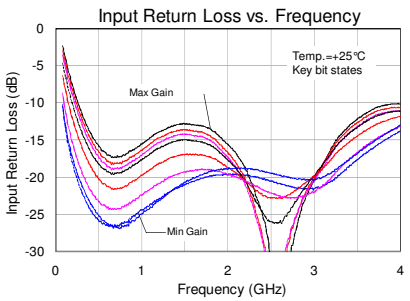



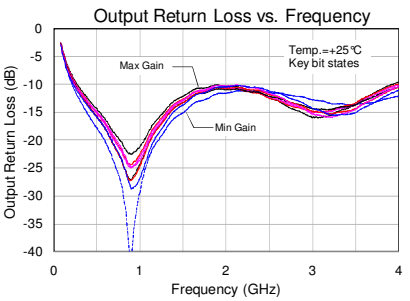



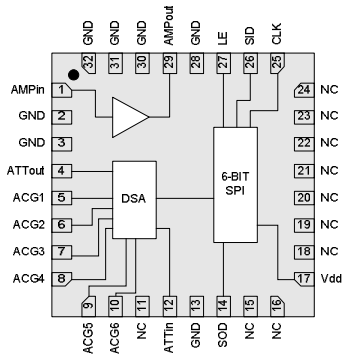



## Pin Description




| Pin # | Symbol | Description |
|---|---|---|
| 1 | Ampin | Amp RF input |
| 2, 3, 13, 28, 30, 31, 32 | GND (Ground) | DC ground |
| 11, 15, 16, 18-24 | NC (No Connect) | No electrical connection. Provide land pads for PCB mounting integrity. |
| 29 | Ampout | Amp RF output / DC supply |
| 12 | ATTin | DSA Input |
| 4 | ATTout | DSA Output |
| 5, 6, 7, 8, 9, 10 | ACG1-6 | Place external capacitor to Ground for applications below 700 MHz. |
| 14 | SOD | Serial Data Out |
| 17 | Vdd | DC supply |
| 25 | CLK | Serial Clock |
| 26 | SID | Serial Data In |
| 27 | LE | Latch Enable |
| Backside Paddle | RF/DC Ground | RF/DC ground. Provide recommended via pattern (see page 8) and ensure good solder attach for best thermal and electrical performance. |

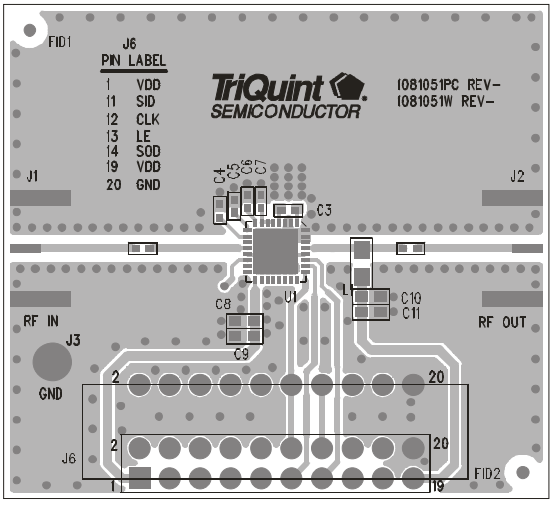
## Applications Information

### PC Board Layout

PCB Material (stackup):

1 oz. Cu top layer
0.014 inch Nelco N-4000-13 ($\varepsilon_r$=3.7 typ.)
1 oz. Cu middle layer 1
Core Nelco N-4000-13
1 oz. Cu middle layer 2
0.014 inch Nelco N-4000-13
1 oz. Cu bottom layer
Finished board thickness is 0.062±.006 inches

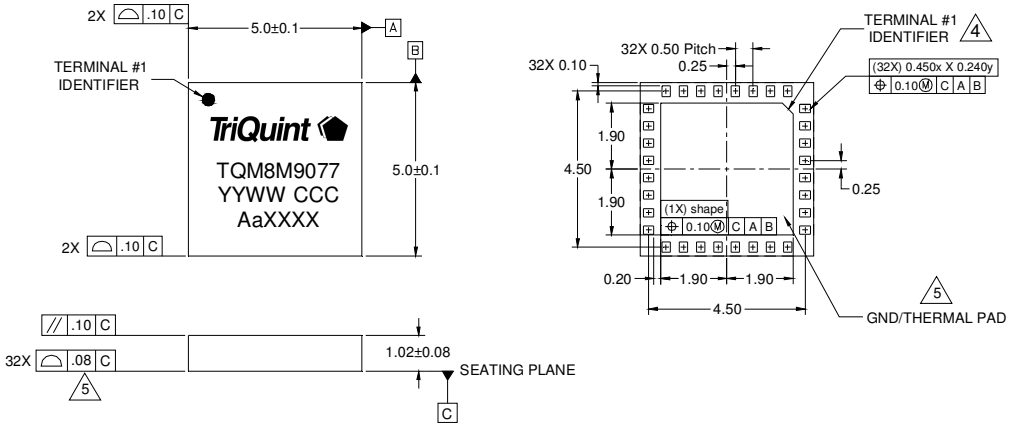
The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.



## Mechanical Information

### Package Information & Dimensions

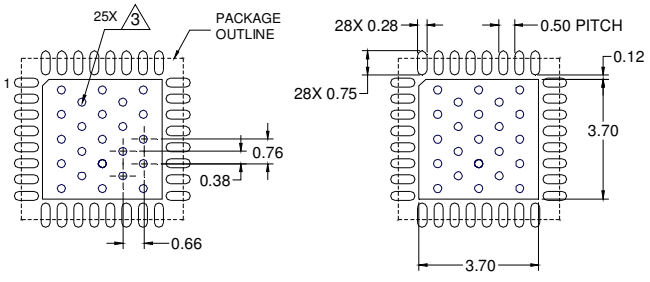
Marking: Part number - TQM8M9077
Year, week, country code - YYWW CCCC
Assembly code – AaXXXX




NOTES:

1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-270, Issue B (Variation DAE) for extra thin profile, fine pitch, internal stacking module (ISM).
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
5. Co-planarity applies to the exposed ground/thermal pad as well as the contact pins.
6. Contact plating: Electrolytic plated Au over Ni

### PCB Mounting Pattern




COMPONENT SIDE

NOTES:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25mm (0.10").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.
5. Place mounting screws near the part to fasten a back side heat sink.
6. Do not apply solder mask to the back side of the PC board in the heat sink contact region.
7. Ensure that the backside via region makes good physical contact with the heat sink.

## Product Compliance Information

### ESD Information

**Caution! ESD-Sensitive Device**

| | |
|---|---|
| ESD Rating: | Class 1A |
| Value: | ≥250V to <500V |
| Test: | Human Body Model (HBM) |
| Standard: | JEDEC Standard JESD22-A114 |

| | |
|---|---|
| ESD Rating: | Class IV |
| Value: | ≤1000V |
| Test: | Charged Device Model (CDM) |
| Standard: | JEDEC Standard JESD22-C101 |

### MSL Rating

Level 3 at +260 °C convection reflow per JEDEC standard IPC/JEDEC J-STD-020.

### Solderability

Compatible with both J-STD-020 lead-free (maximum 260 °C reflow temperature) and lead (maximum 245 °C reflow temperature) soldering processes.

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

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