54F/74F168 • 54F/74F169

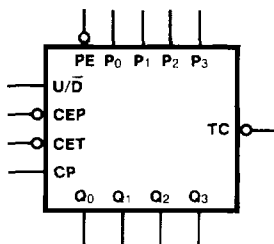## 4-Stage Synchronous Bidirectional Counters

Description

The 'F168 and 'F169 are fully synchronous 4-stage up/down counters. The 'F168 is a BCD decade counter; the 'F169 is a modulo-16 binary counter. Both feature a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the clock.
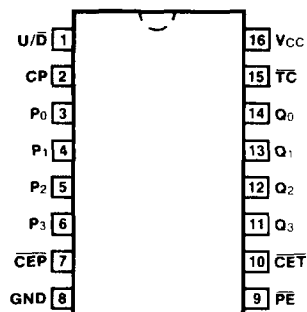
- Asynchronous Counting and Loading
- Built-In Lookahead Carry Capability
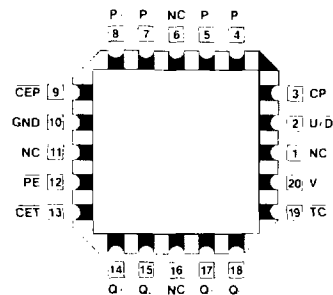- Presettable for Programmable Operation

Ordering Code: See Section 5

Logic Symbol

Pin		Pin
U/$\overline{D}$ 1		16 V$_{CC}$
CP 2		15 $\overline{TC}$
P$_0$ 3		14 Q$_0$
P$_1$ 4		13 Q$_1$
P$_2$ 5		12 Q$_2$
P$_3$ 6		11 Q$_3$
$\overline{CEP}$ 7		10 $\overline{CET}$
GND 8		9 $\overline{PE}$

**Pin Assignment
for DIP and SOIC**

**Pin Assignment
for LCC and PCC**

Input Loading/Fan-Out: See Section 3 for U.L. definitions

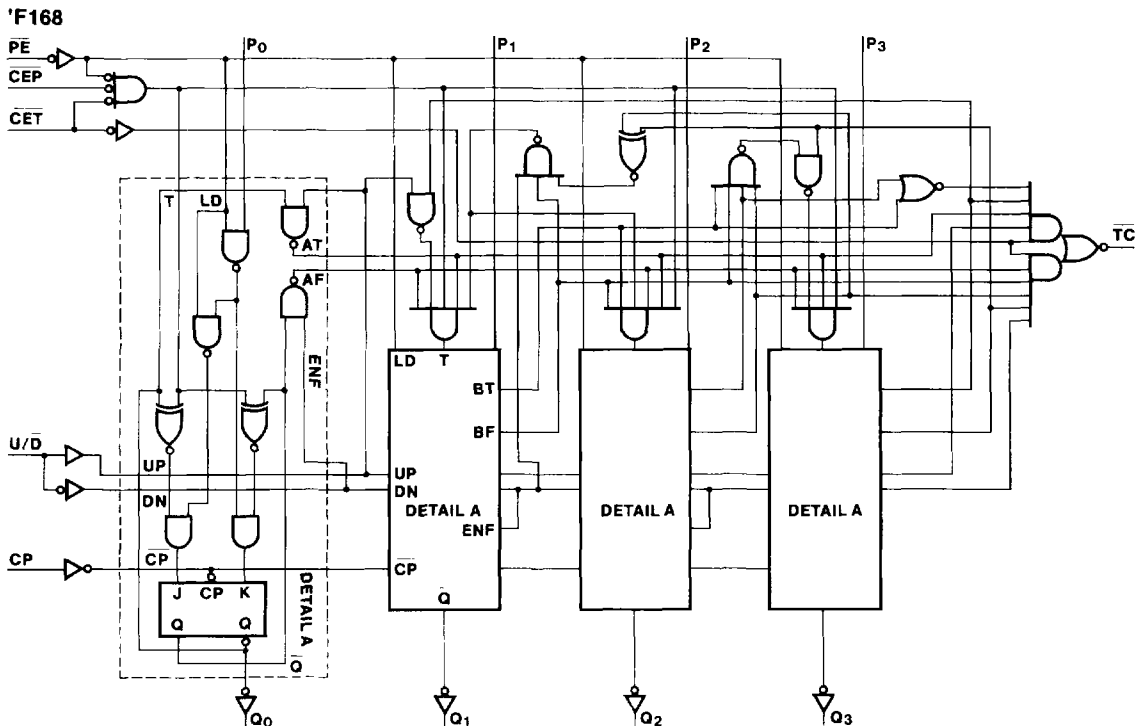| Pin Names	Description	54F/74F(U.L.) HIGH/LOW
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)	0.5/0.375
$\overline{CET}$	Count Enable Trickle Input (Active LOW)	0.5/0.75
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
P$_0$-P$_3$	Parallel Data Inputs	0.5/0.375
$\overline{PE}$	Parallel Enable Input (Active LOW)	0.5/0.375
U/$\overline{D}$	Up-Down Count Control Input	0.5/0.375
Q$_0$-Q$_3$	Flip-Flop Outputs	25/12.5
$\overline{TC}$	Terminal Count Output (Active LOW)	25/12.5

Functional Description

The 'F168 and 'F169 use edge-triggered J-K type flip-flops and have no constraints on changing the control or data input signals in either state of the clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is LOW, the data on the P_0-P_3 inputs enters the flip-flops on the next rising edge of the clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be LOW and $\overline{PE}$ must be HIGH; the U/$\overline{D}$ input then determines the direction of counting. The Terminal Count ($\overline{TC}$) output is normally HIGH and goes LOW, provided that $\overline{CET}$ is LOW, when a counter reaches zero in the Count Down mode or reaches 9 (15 for the 'F169) in the

Count Up mode. The $\overline{TC}$ output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. The $\overline{TC}$ output of the 'F168 decade counter can also be LOW in the illegal states 11, 13, and 15, which can occur when power is turned on or via parallel loading. If an illegal state occurs, the 'F168 will return to the legitimate sequence within two counts. Since the $\overline{TC}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on $\overline{TC}$. For this reason the use of $\overline{TC}$ as a clock signal is not recommended (see logic equations below).
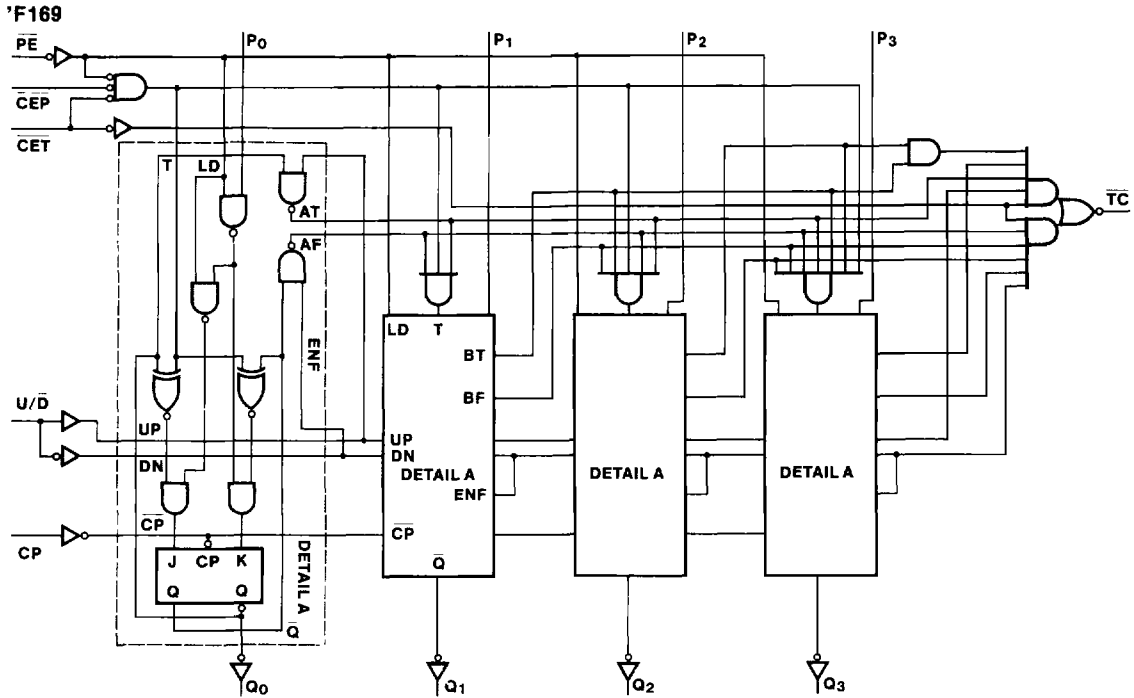
1) Count Enable = $\overline{CEP} \cdot \overline{CET} \cdot \overline{PE}$
2) Up: ('F168): $\overline{TC} = Q_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot Q_3 \cdot (Up) \cdot \overline{CET}$
   ('F169): $\overline{TC} = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (Up) \cdot \overline{CET}$
3) Down: $\overline{TC} = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot (Down) \cdot \overline{CET}$

Logic Diagram

Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.
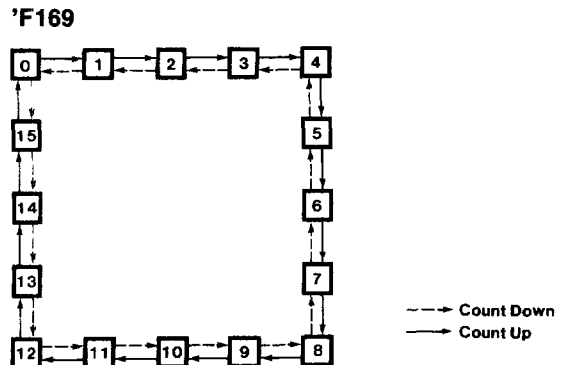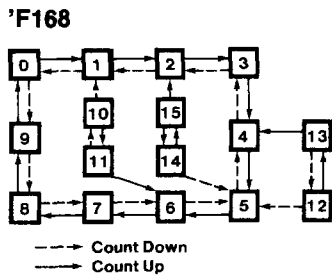
'F169

Mode Select Table

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	$U/\overline{D}$	Action on Rising Clock Edge
L	X	X	X	Load ($P_n \rightarrow Q_n$)
H	L	L	H	Count Up (Increment)
H	L	L	L	Count Down (Decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagrams

'F169

- - - → Count Down
———→ Count Up

'F168

- - - → Count Down
———→ Count Up

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		35	52	mA	$V_{CC} = Max$

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F $T_A = +25°C$ $V_{CC} = +5.0\,V$ $C_L = 50\,pF$			54F $T_A, V_{CC} =$ Mil $C_L = 50\,pF$		74F $T_A, V_{CC} =$ Com $C_L = 50\,pF$		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	115					90	MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ HIGH or LOW)	3.0 4.0	6.5 9.0	8.5 11.5			3.0 4.0	9.5 13.0	ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$	5.5 4.0	12.0 8.5	15.5 11.0			5.5 4.0	17.0 12.5	ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	2.5 2.5	4.5 6.0	6.0 8.0			2.5 2.5	7.0 9.0	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay ('F168) U/$\overline{D}$ to $\overline{TC}$	3.5 4.0	8.5 12.5	11.0 16.0			3.5 4.0	12.5 17.5	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay ('F169) U/$\overline{D}$ to $\overline{TC}$	3.5 4.0	8.5 8.0	11.0 10.5			3.5 4.0	12.5 12.0	ns	3-1 3-10

4

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F $T_A = +25°C$ $V_{CC} = +5.0$ V			54F $T_A, V_{CC} =$ Mil		74F $T_A, V_{CC} =$ Com		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW P_n to CP	4.0 4.0					4.5 4.5		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW P_n to CP	3.0 3.0					3.5 3.5			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CEP}$ or $\overline{CET}$ to CP	5.0 5.0					6.0 6.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CEP}$ or $\overline{CET}$ to CP	0 0					0 0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{PE}$ to CP	8.0 8.0					9.0 9.0		ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{PE}$ to CP	0 0					0 0			
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW U/$\overline{D}$ to CP ('F168)	11.0 16.5					12.5 18.0		ns	3-5
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW U/$\overline{D}$ to CP ('F169)	11.0 7.0					12.5 8.0			
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW U/$\overline{D}$ to CP	0 0					0 0			
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	5.0 5.0					5.5 5.5		ns	3-7