ADVANCE INFORMATION

Am29LV256M

256 Megabit (16 M x 16-Bit/32 M x 8-Bit) MirrorBit™ 3.0 Volt-only Uniform Sector Flash Memory with VersatileI/O™ Control

DISTINCTIVE CHARACTERISTICS

ARCHITECTURAL ADVANTAGES

- **Single power supply operation**
  - 3 volt read, erase, and program operations
- **VersatileI/O™ control**
  - Device generates and tolerates voltages on CE# and DQ I/Os as determined by the voltage on the V_{IO} pin; operates from 1.65 to 3.6 V
- **Manufactured on 0.23 µm MirrorBit process technology**
- **SecSi™ (Secured Silicon) Sector region**
  - 128-word/256-byte sector for permanent, secure identification through an 8-word/16-byte random Electronic Serial Number, accessible through a command sequence
  - May be programmed and locked at the factory or by the customer
- **Flexible sector architecture**
  - Five hundred twelve 32 Kword (64 Kbyte) sectors
- **Compatibility with JEDEC standards**
  - Provides pinout and software compatibility for single-power supply flash, and superior inadvertent write protection
- **Minimum 100,000 erase cycle guarantee per sector**
- **20-year data retention at 125°C**

PERFORMANCE CHARACTERISTICS

- **High performance**
  - 90 ns access time
  - 25 ns page read times
  - 0.4 s typical sector erase time
  - 5.9 µs typical write buffer word programming time: 16-word/32-byte write buffer reduces overall programming time for multiple-word updates
  - 4-word/8-byte page read buffer
  - 16-word/32-byte write buffer
- **Low power consumption (typical values at 3.0 V, 5 MHz)**
  - 30 mA typical active read current
  - 50 mA typical erase/program current
  - 1 µA typical standby mode current
- **Package options**
  - 56-pin TSOP
  - 64-ball Fortified BGA

SOFTWARE & HARDWARE FEATURES

- **Software features**
  - Program Suspend & Resume: read other sectors before programming operation is completed
  - Erase Suspend & Resume: read/program other sectors before an erase operation is completed
  - Data# polling & toggle bits provide status
  - Unlock Bypass Program command reduces overall multiple-word or byte programming time
  - CFI (Common Flash Interface) compliant: allows host system to identify and accommodate multiple flash devices
- **Hardware features**
  - Sector Group Protection: hardware-level method of preventing write operations within a sector group
  - Temporary Sector Unprotect: V_{ID}-level method of changing code in locked sectors
  - WP#/ACC input accelerates programming time (when high voltage is applied) for greater throughput during system production. Protects first or last sector regardless of sector protection settings
  - Hardware reset input (RESET#) resets device
  - Ready/Busy# output (RY/BY#) detects program or erase cycle completion

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GENERAL DESCRIPTION

The Am29LV256M is a 256 Mbit, 3.0 volt single power supply flash memory devices organized as 16,777,216 words or 33,554,432 bytes. The device has a 16-bit wide data bus that can also function as an 8-bit wide data bus by using the BYTE# input. The device can be programmed either in the host system or in standard EPROM programmers.

An access time of 90, 100, 110, or 120 ns is available. Note that each access time has a specific operating voltage range (V_{CC}) and an I/O voltage range (V_{IO}), as specified in the Product Selector Guide and the Ordering Information sections. The device is offered in a 56-pin TSOP or 64-ball Fortified BGA package. Each device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

Each device requires only a **single 3.0 volt power supply** for both read and write functions. In addition to a V_{CC} input, a high-voltage **accelerated program (**WP#/**ACC)** input provides shorter programming times through increased current. This feature is intended to facilitate factory throughput during system production, but may also be used in the field if desired.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the device using standard microprocessor write timing. Write cycles also internally latch addresses and data needed for the programming and erase operations.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Device programming and erasure are initiated through command sequences. Once a program or erase operation has begun, the host system need only poll the DQ7 (Data# Polling) or DQ6 (toggle) **status bits** or monitor the **Ready/Busy# (RY/BY#)** output to determine whether the operation is complete. To facilitate programming, an **Unlock Bypass** mode reduces command sequence overhead by requiring only two write cycles to program data instead of four.

The **VersatileI/O™** (V_{IO}) control allows the host system to set the voltage levels that the device generates and tolerates voltages on the CE# and DQ I/Os to the same voltage level that is asserted on the V_{IO} pin. This allows the device to operate in a 1.8 V or 3 V system environment as required.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The hardware sector protection feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend/Erase Resume** feature allows the host system to pause an erase operation in a given sector to read or program any other sector and then complete the erase operation. The **Program Suspend/Program Resume** feature enables the host system to pause a program operation in a given sector to read any other sector and then complete the program operation.

The **hardware RESET# pin** terminates any operation in progress and resets the device, after which it is then ready for a new operation. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the host system to read boot-up firmware from the Flash memory device.

The device reduces power consumption in the **standby mode** when it detects specific voltage levels on CE# and RESET#, or when addresses have been stable for a specified period of time.

The **SecSi™ (Secured Silicon) Sector** provides a 128-word/256-byte area for code or data that can be permanently protected. Once this sector is protected, no further changes within the sector can occur.

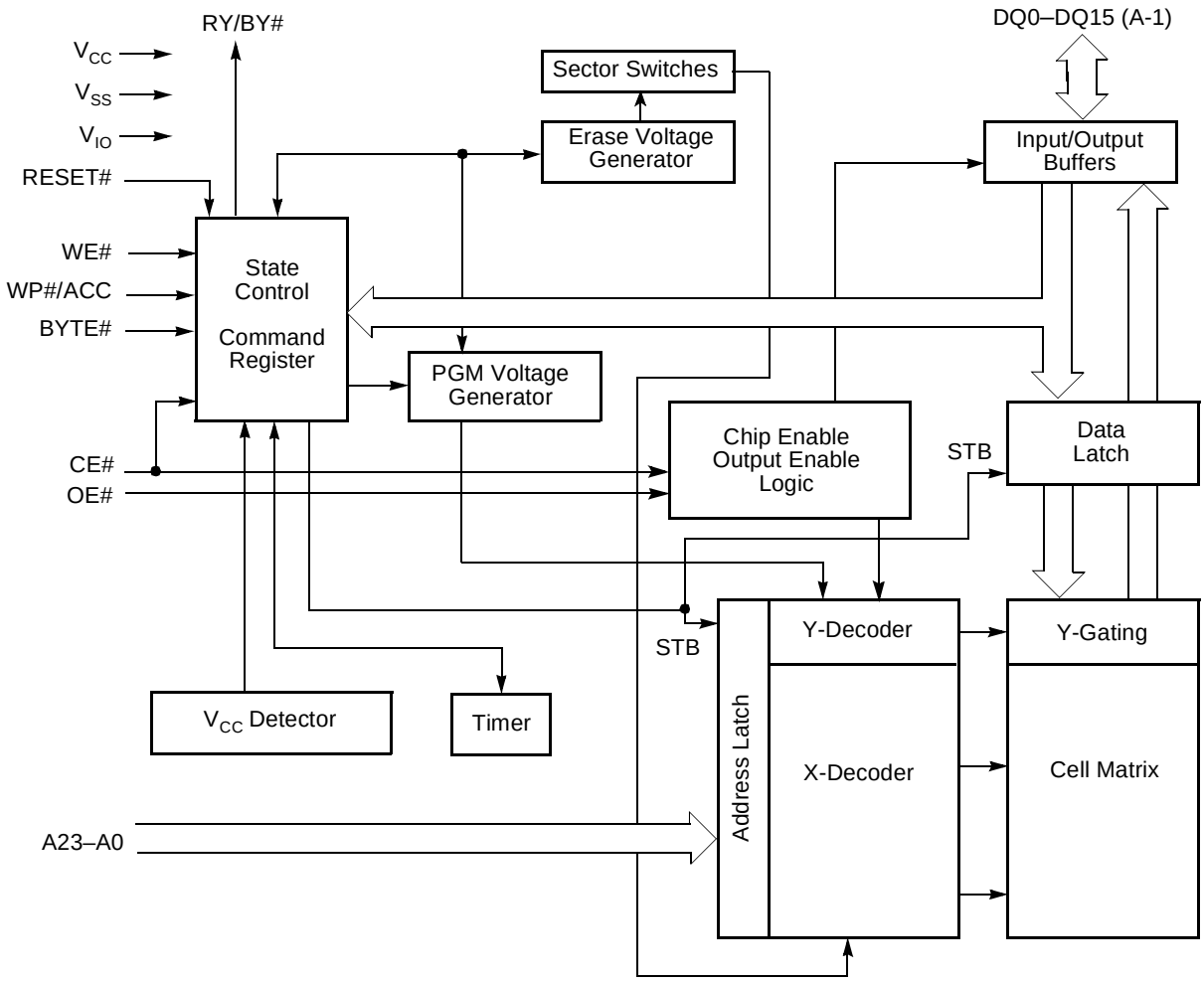
The **Write Protect (WP#**/ACC**)** feature protects the first or last sector by asserting a logic low on the WP# pin.

AMD MirrorBit flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via hot-hole assisted erase. The data is programmed using hot electron injection.

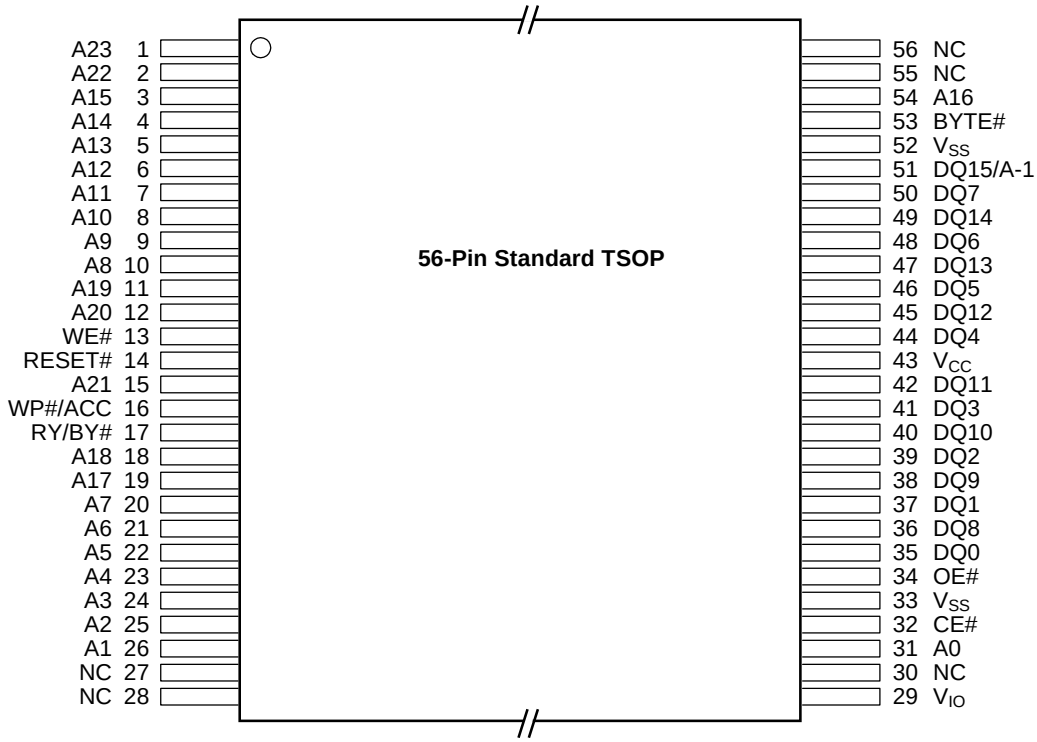
PRODUCT SELECTOR GUIDE

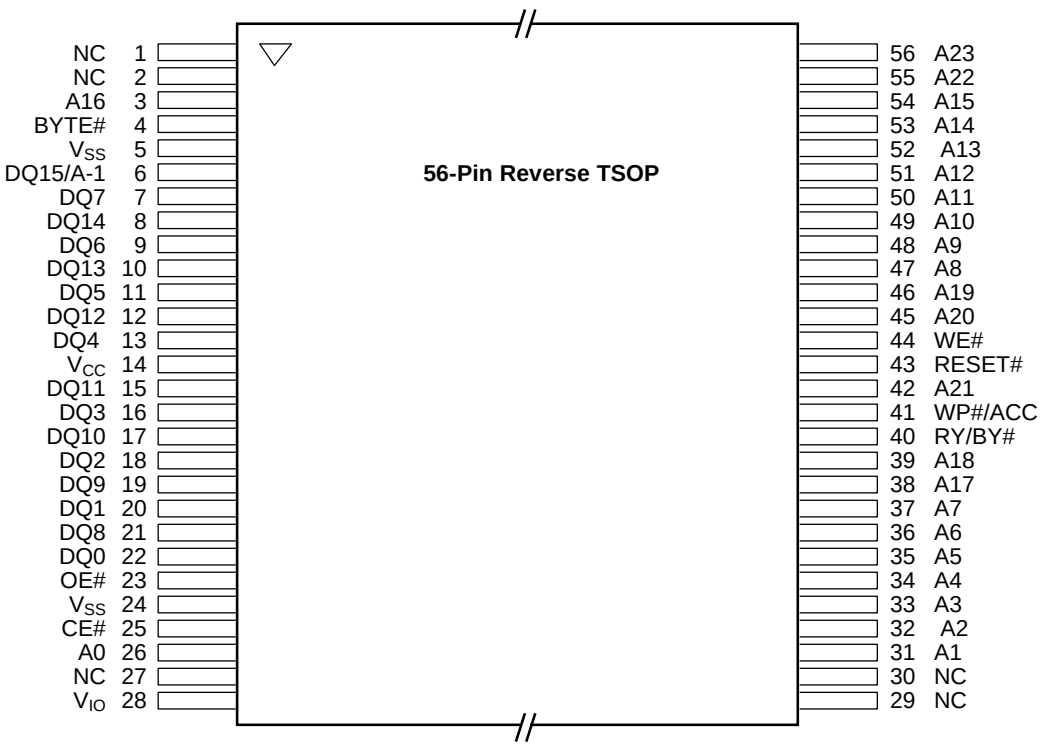
Part Number		Am29LV256M			
Speed Option	V_{CC} = 3.0–3.6 V	**90R** (V_{IO} = 3.0–3.6 V)			
	V_{CC} = 2.7–3.6 V		**101** (V_{IO} = 2.7–3.6 V)	**112** (V_{IO} = 1.65–3.6 V)	**120** (V_{IO} = 1.65–3.6 V)
Max. Access Time (ns)		90	100	110	120
Max. CE# Access Time (ns)		90	100	110	120
Max. Page access time (t_{PACC})		25	30	40	40
Max. OE# Access Time (ns)		25	30	40	40

BLOCK DIAGRAM



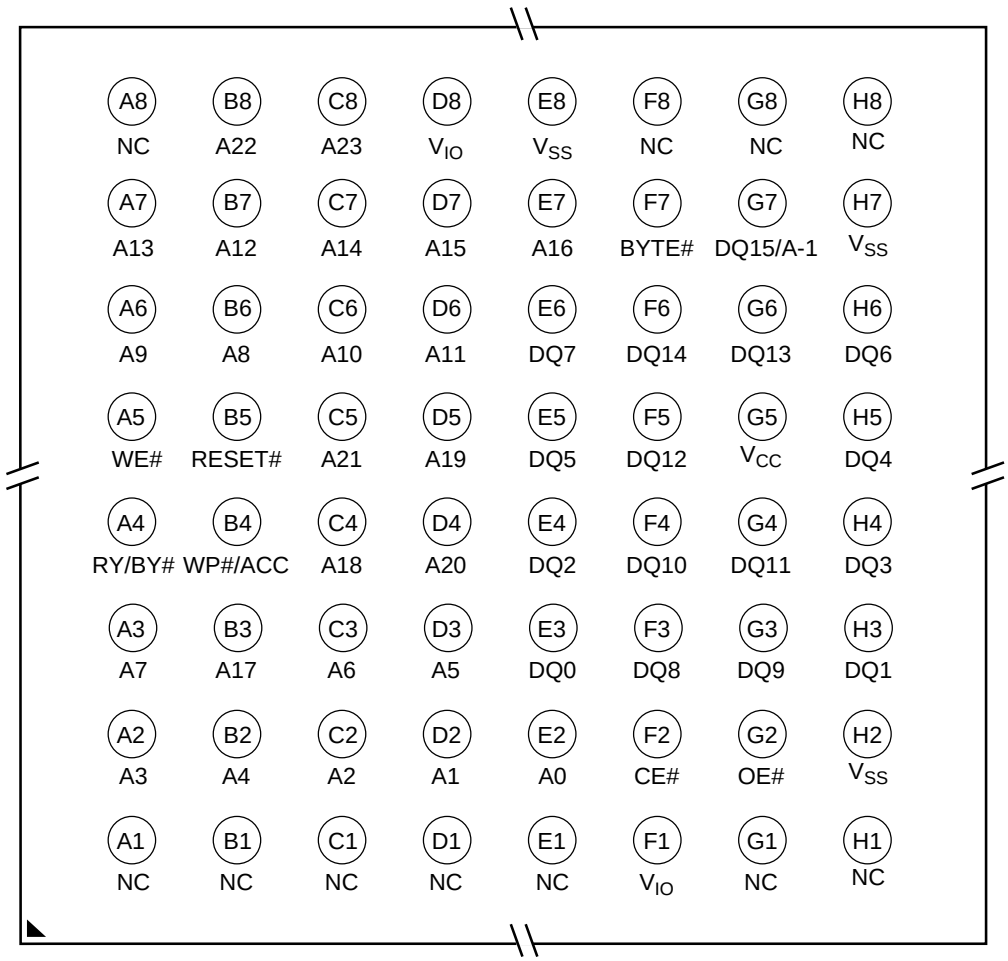
CONNECTION DIAGRAMS





CONNECTION DIAGRAMS

64-ball Fortified BGA
Top View, Balls Facing Down



Note: *The FBGA package pinout configuration shown is preliminary. The ball count and package physical dimensions have not yet been determined. Contact AMD for further information.*

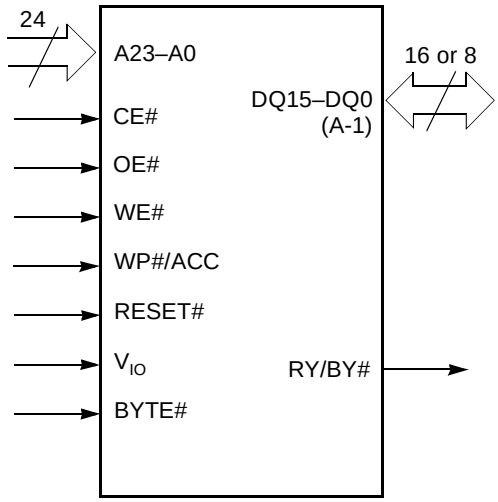
Special Package Handling Instructions

Special handling is required for Flash Memory products in molded packages (TSOP, BGA, PLCC, PDIP, SSOP). The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

PIN DESCRIPTION

A23–A0	=	24 Address inputs
DQ14–DQ0	=	15 Data inputs/outputs
DQ15/A-1	=	DQ15 (Data input/output, word mode), A-1 (LSB Address input, byte mode)
CE#	=	Chip Enable input
OE#	=	Output Enable input
WE#	=	Write Enable input
WP#/ACC	=	Hardware Write Protect input; Acceleration input
RESET#	=	Hardware Reset Pin input
BYTE#	=	Selects 8-bit or 16-bit mode
RY/BY#	=	Ready/Busy output
V_{CC}	=	3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
V_{IO}	=	Output Buffer power
V_{SS}	=	Device Ground
NC	=	Pin Not Connected Internally

LOGIC SYMBOL



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:

Am29LV256M H 90R PC I

TEMPERATURE RANGE
I = Industrial (–40°C to +85°C)

PACKAGE TYPE
E = 56-Pin Thin Small Outline Package (TSOP) Standard Pinout (TS 056)
F = 56-Pin Thin Small Outline Package (TSOP) Reverse Pinout (TSR056)
PC = 64-Ball Fortified Ball Grid Array (**F**BGA), 12 x 18 mm, 1.0 mm pitch *(Package name TBD)*

SPEED OPTION
See Product Selector Guide and Valid Combinations

SECTOR ARCHITECTURE AND SECTOR WRITE PROTECTION (WP# = V_{IL})
H = Uniform sector device, highest address sector protected
L = Uniform sector device, lowest address sector protected

DEVICE NUMBER/DESCRIPTION
Am29LV256MH/L
256 Megabit (16 M x 16-Bit/32 M x 8-Bit) MirrorBit Uniform Sector Flash Memory with VersatileIO™ Control 3.0 Volt-only Read, Program, and Erase

Valid Combinations for TSOP Package		Speed(ns)	V_{IO} Range	V_{CC} Range
Am29LV256MH90R, Am29LV256ML90R	EI, FI	90	3.0–3.6 V	3.0–3.6 V
Am29LV256MH101, Am29LV256ML101		100	2.7–3.6 V	2.7–3.6 V
Am29LV256MH112, Am29LV256ML112		110	1.65–3.6 V	
Am29LV256MH120, Am29LV256ML120		120	1.65–3.6 V	

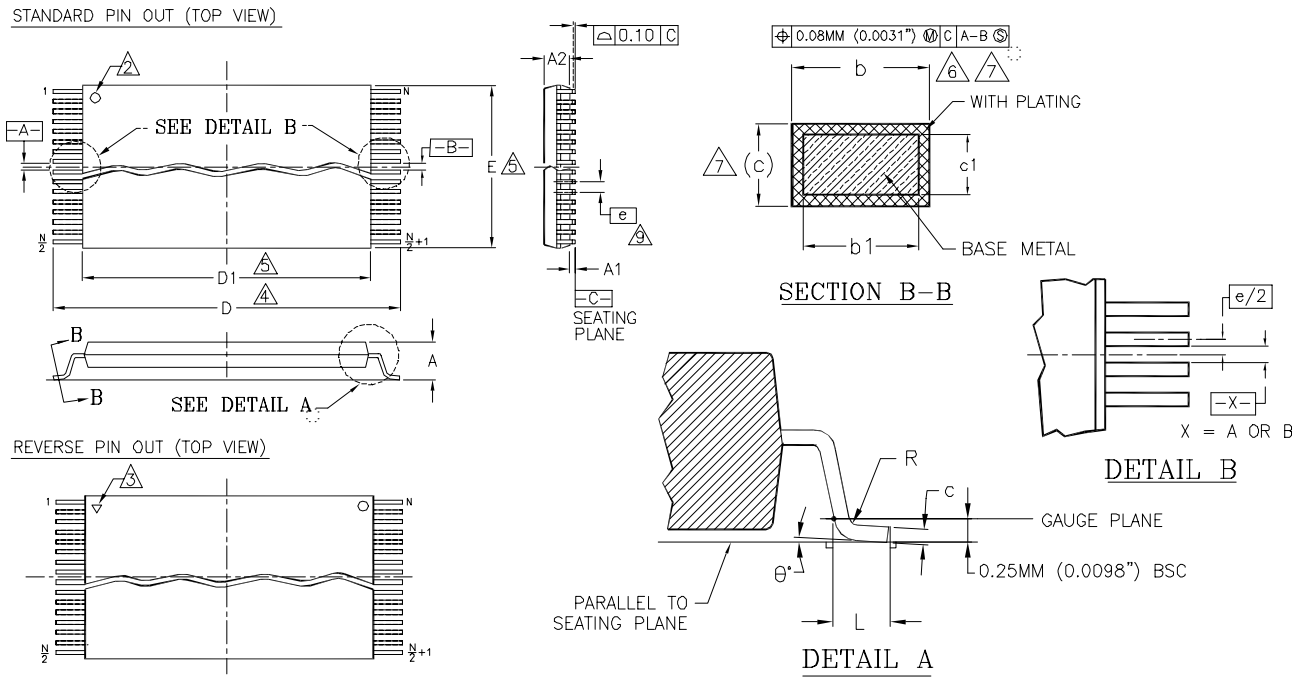
Valid Combinations for Fortified BGA Package				Speed (ns)	V_{IO} Range	V_{CC} Range
Order Number		Package Marking				
Am29LV256MH90R, Am29LV256ML90R	PCI	*Package marking TBD*	I	90	3.0–3.6 V	3.0–3.6 V
Am29LV256MH101, Am29LV256ML101				100	2.7–3.6 V	2.7–3.6 V
Am29LV256MH112, Am29LV256ML112				110	1.65–3.6 V	
Am29LV256MH120, Am29LV256ML120				120	1.65–3.6 V	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PHYSICAL DIMENSIONS

TS056/TSR056—56-Pin Standard/Reverse Thin Small Outline Package (TSOP)



PACKAGE	TS/TSR 56		
JEDEC	MO-142 (B) EC		
SYMBOL	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.05	---	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	---	0.16
c	0.10	---	0.21
D	19.90	20.00	20.20
D1	18.30	18.40	18.50
E	13.90	14.00	14.10
e	0.50 BASIC		
L	0.50	0.60	0.70
ø	0°	3°	5°
R	0.08	---	0.20
N	56		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982.)
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN), INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C-. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTUSION IS 0.15 mm PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08 mm TOTAL IN EXCESS OF b DIMENSION AT MAX MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07 mm.
7. THESE DIMESIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

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PHYSICAL DIMENSIONS

LAA064—64-Ball Fortified Ball Grid Array (FBGA) 12 x 18 mm Package

TBD

REVISION SUMMARY

Revision A (August 3, 2001)

Initial release as abbreviated Advance Information data sheet.

Revision A+1 (September 12, 2001)

Ordering Information

Changed package part number designation from WH to PC.

Physical Dimensions

Added the TS056 and LAA064 packages.

Revision A+2 (October 3, 2001)

Global

Corrected title from 64 Mbit to 256 Mbit. Added 120 ns speed option.

Distinctive Characteristics

SecSi™ (Secured Silicon) Sector region: Corrected 64-byte to 256-byte.

Connection Diagram

Modified fBGA ball grid to an 8 x 8 ball matrix. Changed RFU (reserved for future use) balls to NC (No Connection).

Ordering Information

Changed operating voltage range on 90 ns speed option to 3.0–3.6 V.

Pin Description

Added A-1 description.

Revision A+3 (March 25, 2002)

Distinctive Characteristics

Clarified description of Enhanced VersatileIO control.

Physical Dimensions

Added drawing that shows both TS056 and TSR056 specifications.

Revision A+4 (April 26, 2002)

Global

The LAA064 (13 x 11 mm Fortified BGA) package has been removed. A 12 x 18 Fortified BGA package will be offered in its place.

Distinctive Characteristics

Deleted “Enhanced” from VersatileIO and mofified decscription.