3W Mono Low-Voltage Audio Power Amplifier

Features

- **Operating Voltage : 2.5V-5.5V**
- **Bridge-Tied Load (BTL) Mode Operation**
- **Supply Current – I_{DD}=7mA at V_{DD}=5V**
- **Low Shutdown Current – I_{DD}=0.1μA**
- **Low Distortion**
  - **–2.5W, at V_{DD}=5V, BTL, R_L=3Ω, THD+N=0.1%**
  - **–2.1W, at V_{DD}=5V, BTL, R_L=4Ω, THD+N=0.1%**
- **Output Power**
  at 1% THD+N
  - **–2.6W, at V_{DD}=5V, BTL, R_L=3Ω**
  - **–2.3W, at V_{DD}=5V, BTL, R_L=4Ω**

  at 10% THD+N
  - **–3.3W at V_{DD}=5V, BTL, R_L=3Ω**
  - **–2.7W at V_{DD}=5V, BTL, R_L=4Ω**
- **Depop Circuitry Integrated**
- **Thermal Shutdown Protection and Over-Current Protection Circuitry**
- **High Supply Voltage Ripple Rejection**
- **Surface-Mount Packaging**
  - **–MSOP-8P (with Enhanced Thermal Pad)**
  - **–SOP-8P (with Enhanced Thermal Pad)**
  - **–SOP-8**
- **Lead Free and Green Devices Available (RoHS Compliant)**

General Description

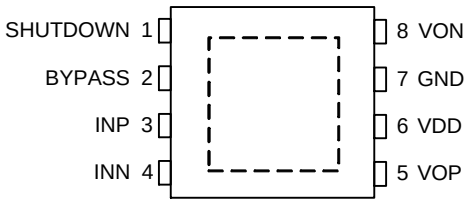
The APA3010/1 is a bridged-tied load (BTL) audio power amplifier developed especially for low-voltage applications where internal speakers. Operating with a 5V supply, the APA3010/1 can deliver 3.3W of continuous power into a BTL 3Ω load at 10% THD+N throughout voice band frequencies. Although this device is characterized out to 20kHz, its operation is optimized for narrow band applications such as wireless communications. The BTL configuration eliminates the need for external coupling capacitors on the output in most applications, which is particularly important for small battery-powered equipment. This device features a shutdown mode for power sensitive applications with special depop circuitry to eliminate speaker noise when exiting shutdown mode. The APA3010/1 are available in a SOP-8, SOP-8P or MSOP-8P.

Applications

- **Mobil Phones**
- **PDAs**
- **Portable Electronic Devices**
- **Desktop Computers**

Pin Configuration

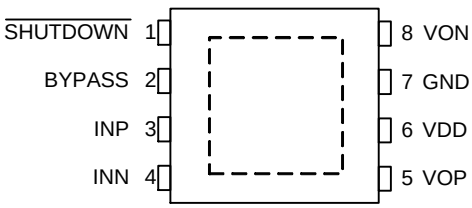
APA3010



MSOP-8P / SOP-8P
TOP VIEW

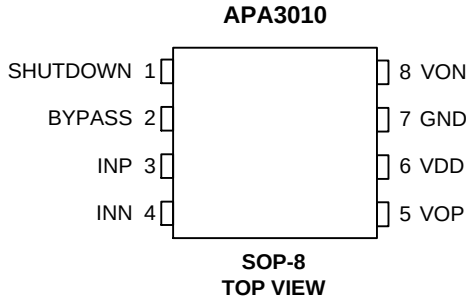
= Thermal Pad (connected to the GND plane for better heat dissipation)

APA3011



MSOP-8P / SOP-8P
TOP VIEW

Pin Configuration (Cont.)



Ordering and Marking Information

APA3010/1 □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code K : SOP-8 KA : SOP-8P XA : MSOP-8P Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APA3010/1 K / KA : APA3010/1 XXXXX	XXXXX - Date Code
APA3010/1 XA : A3010/1 XXX XX	XXXXX - Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings

(Over operating free-air temperature range unless otherwise noted.)

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage	-0.3 to 6	V
V_{IN}, V_O	Input Voltage Range, SHUTDOWN, $\overline{SHUTDOWN}$, BYPASS, V_O	-0.3 to V_{DD}+0.3	V
T_A	Operating Junction Temperature Range	-40 to 85	°C
T_J	Maximum Junction Temperature	Internally Limited	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_S	Soldering Temperature Range	260	°C
P_D	Power Dissipation	Internally Limited	W

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance - Junction to Ambient (Note 1) MSOP-8P SOP-8P SOP-8	 50 56 160	°C/W

Note 1 : Please refer to "Thermal Pad Consideration." 2 layered 5 in^2 printed circuit board with 2oz trace and copper through several thermal vias. The thermal pad is solder on the PCB.

Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Range	Unit
V_{DD}	Supply Voltage		2.5 ~ 5.5	V
V_{IH}	High-Level Voltage	SHUTDOWN, $\overline{SHUTDOWN}$	2.2 ~	V
V_{IL}	Low-Level Voltage	SHUTDOWN, $\overline{SHUTDOWN}$	~ 0.4	V

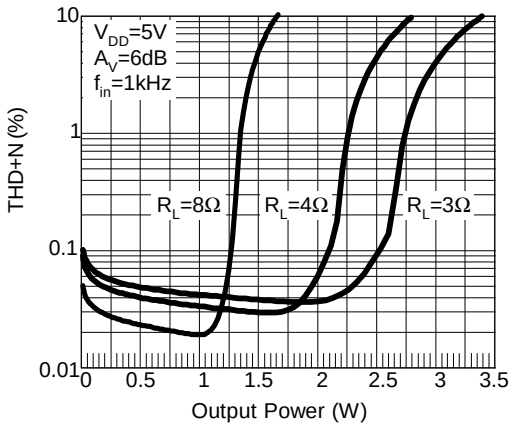
Electrical Characteristics

Unless otherwise noted these specifications apply over full temperature V_{DD}= 5V, T_A= 25°C (unless otherwise noted).

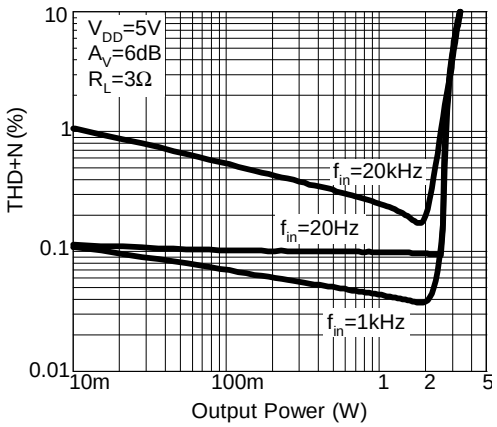
Symbol	Parameter	Test Conditions	APA3010/1			Unit
			Min.	Typ.	Max.	
V_{OS}	Output Offset Voltage	R_L=8Ω, R_i=R_f=20kΩ	-	-	20	mV
I_{DD}	Supply Current	I_O=0mA	-	7	14	mA
$I_{DD(SD)}$	Supply Current	Shutdown Mode	-	0.1	-	μA
$\|I_H\|$		SHUTDOWN, V_i=V_{DD}	-	0.1	-	μA
		$\overline{SHUTDOWN}$, V_i=V_{DD}	-	0.1	-	
$\|I_L\|$		SHUTDOWN, V_i=0V	-	0.1	-	μA
		$\overline{SHUTDOWN}$, V_i=0V	-	0.1	-	
OPERATING CHARACTERISTICS, V_{DD}=5V,T_A=25°C						
P_O	Output Power	THD+N=1%, f_{in}=1kHz, R_L=3Ω R_L=4Ω R_L=8Ω	-	 2.6 2.3 1.3	-	W
		THD+N=10%, f_{in} =1kHz, R_L=3Ω R_L=4Ω R_L=8Ω	-	 3.3 2.7 1.7	-	
THD+N	Total Harmonic Distortion Plus Noise	f_{in} =1kHz, P_O=2W, R_L=3Ω P_O=1.6W, R_L=4Ω P_O=1W, R_L=8Ω	-	 0.06 0.04 0.03	-	%
B1	Unity-Gain Bandwidth	Open Loop	-	2	-	MHz
PSRR	Power Supply Rejection Ratio	C_B=1μF, R_L=8Ω, f_{in} =120kHz	-	60	-	dB
V_n	Noise Output Voltage	A_V=6dB, C_B=1μF, R_L=8Ω	-	28	-	μV(rms)
T_{WU}	Wake-Up Time	C_B=1μF	-	380	-	ms

Typical Operating Characteristics

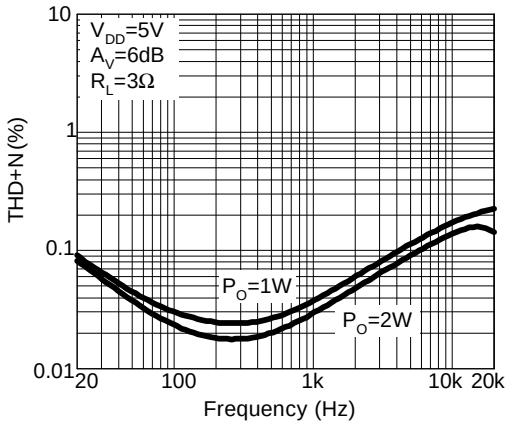
THD+N vs. Output Power



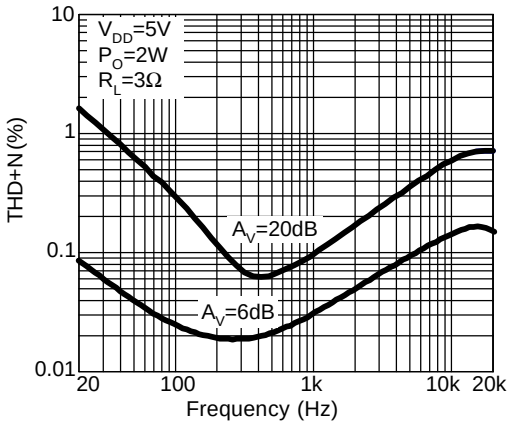
THD+N vs. Output Power



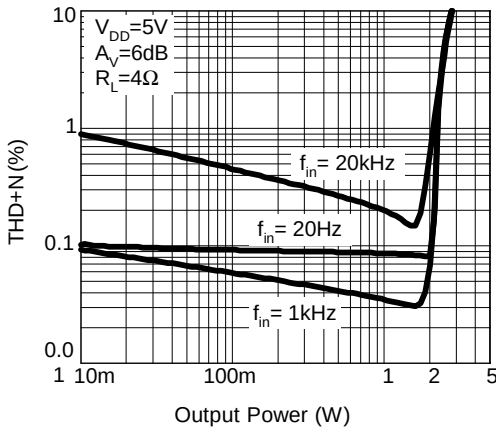
THD+N vs. Frequency



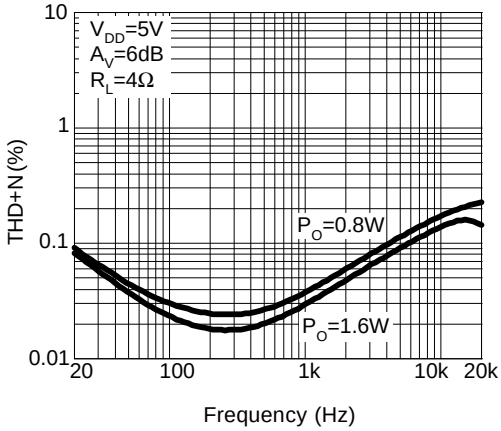
THD+N vs. Frequency



THD+N vs. Output Power

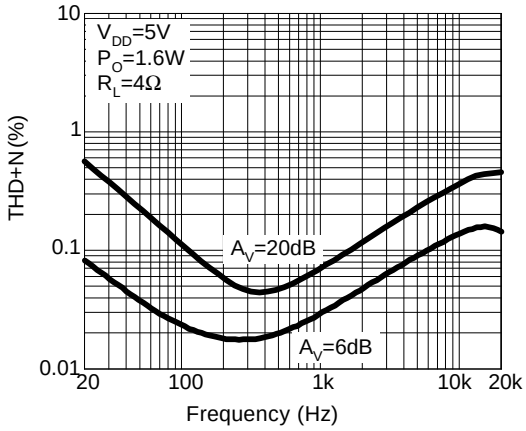


THD+N vs. Frequency

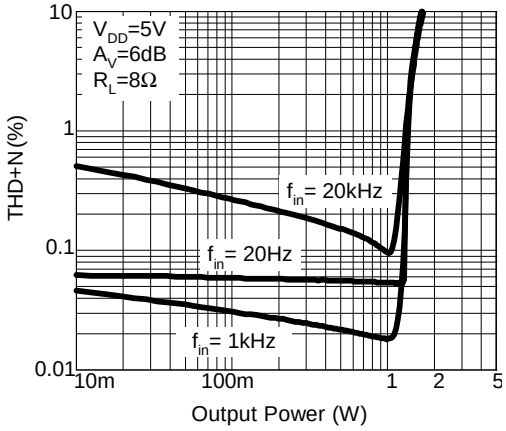


Typical Operating Characteristics (Cont.)

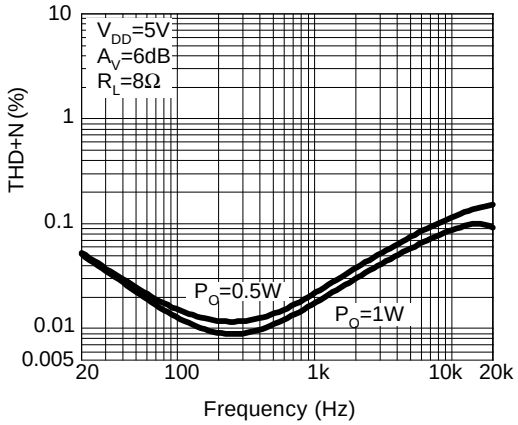
THD+N vs. Frequency



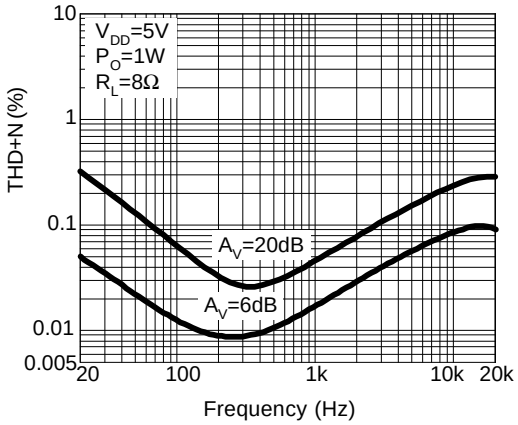
THD+N vs. Output Power



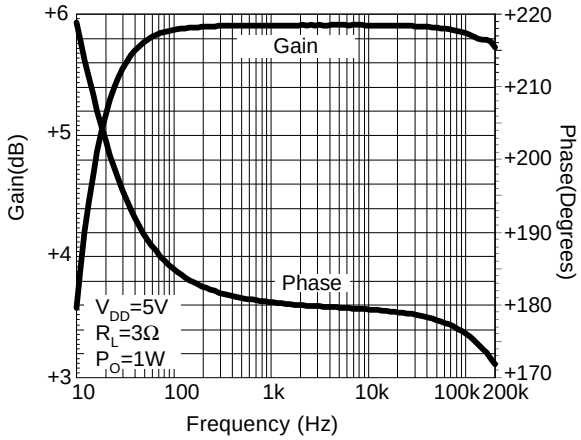
THD+N vs. Frequency



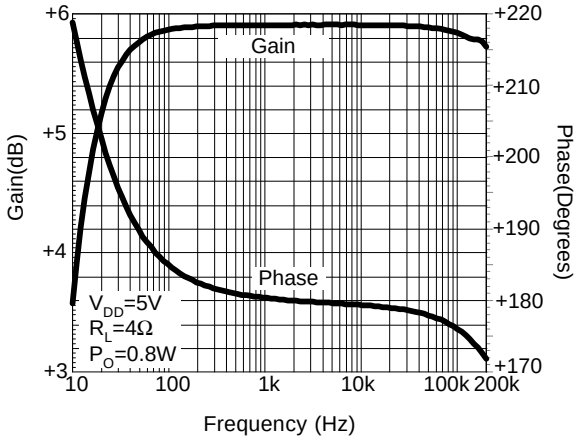
THD+N vs. Frequency



Frequency Response

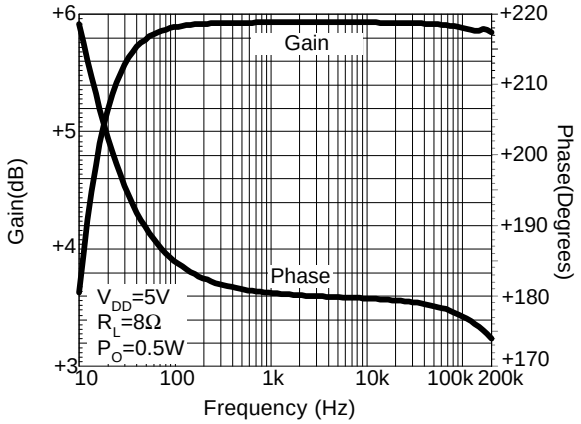


Frequency Response

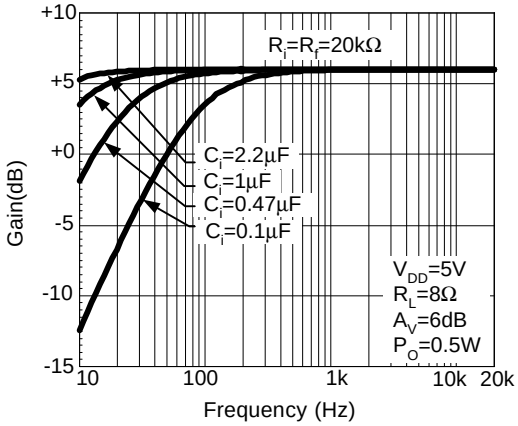


Typical Operating Characteristics (Cont.)

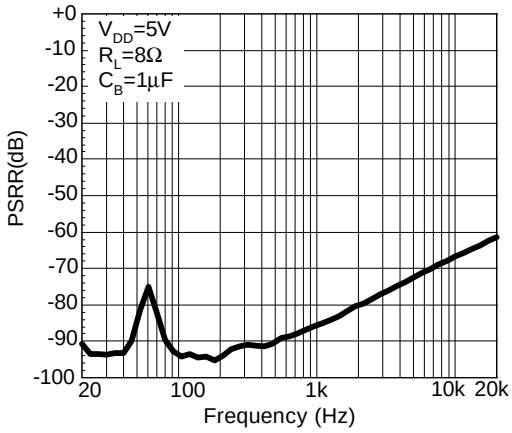
Frequency Response



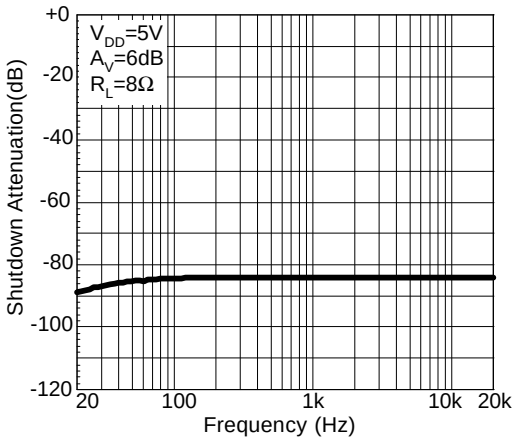
Input Capacitor vs. Frequency Response



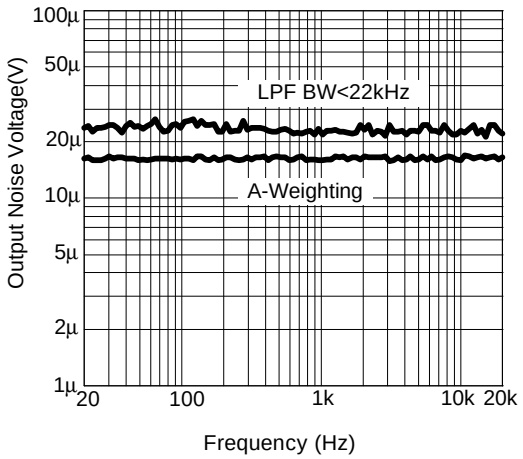
PSRR vs. Frequency



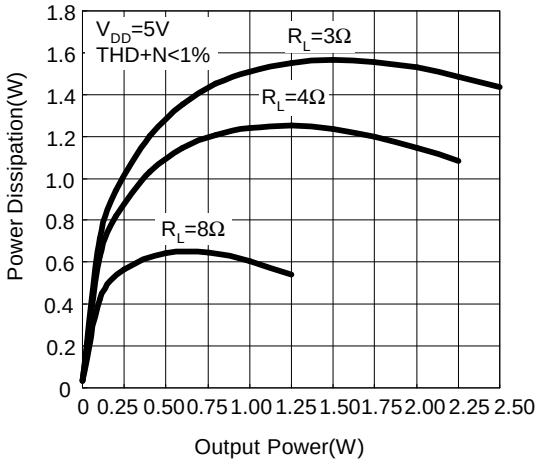
Shutdown Attenuation vs. Frequency



Output Noise Voltage vs.Frequency

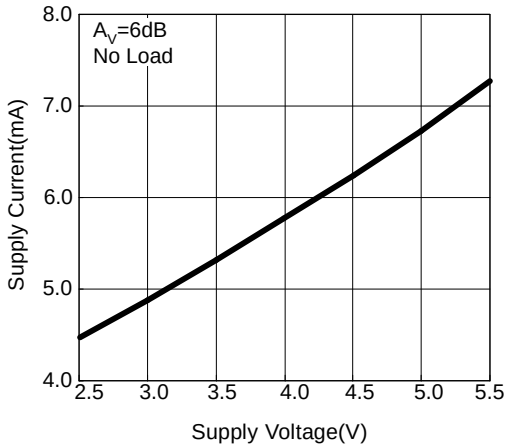


Power Dissipation vs. Output Power

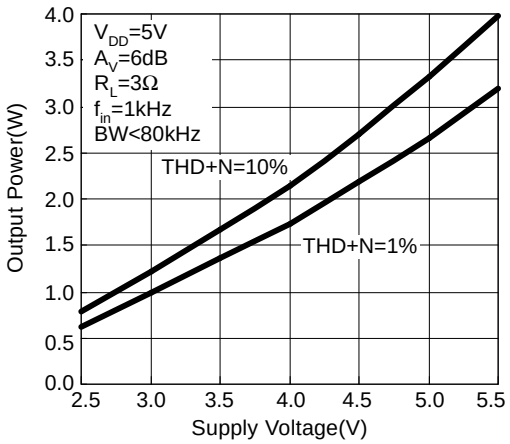


Typical Operating Characteristics (Cont.)

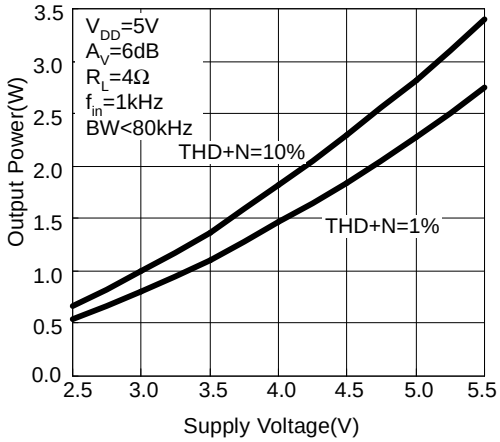
Supply Current vs. Supply Voltage



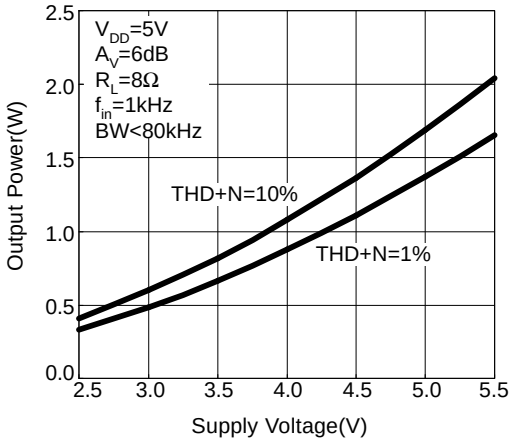
Supply Voltage vs. Output Power



Power Dissipation vs. Output Power



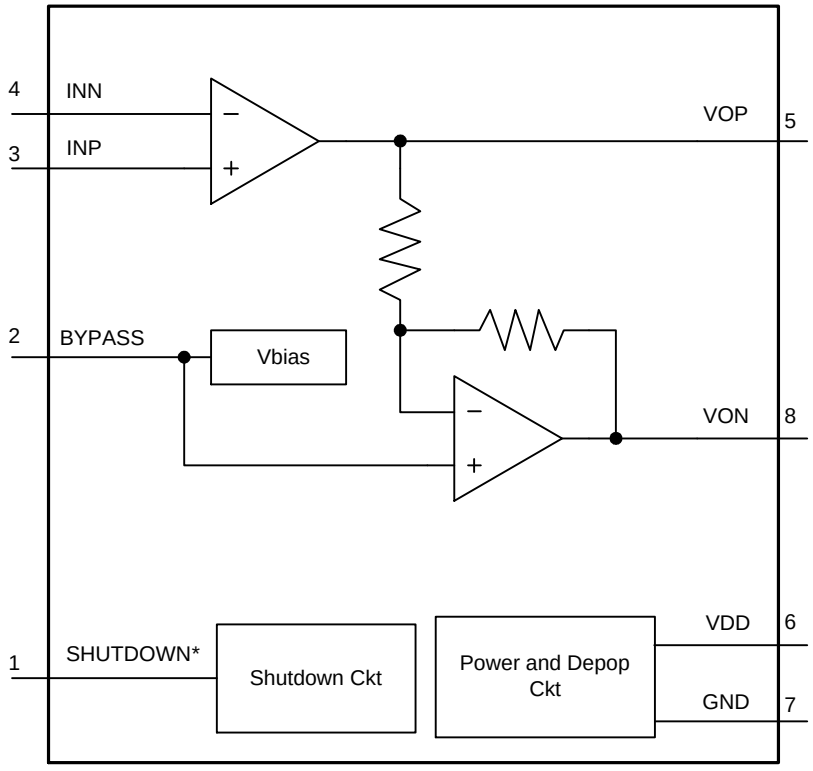
Supply Current vs. Supply Voltage



Pin Description

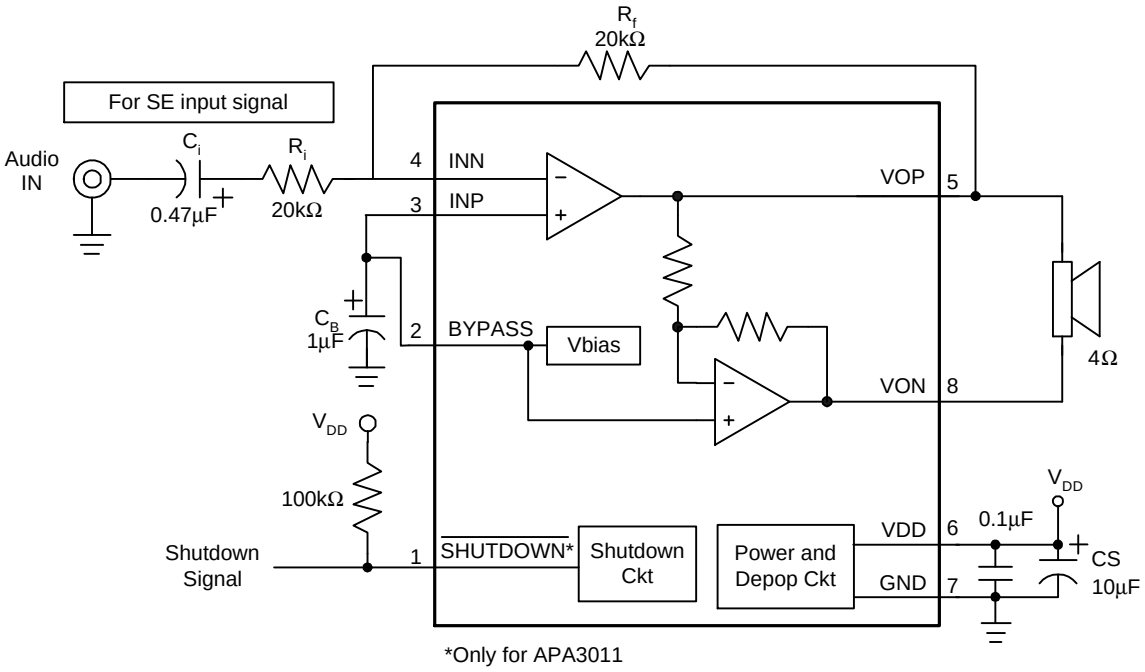
PIN		I/O	FUNCTION
NO.	NAME		
1	SHUTDOWN (APA3010) $\overline{\text{SHUTDOWN}}$ (APA3011)	I	Shutdown mode control signal input, place entire IC in shutdown mode when held high in APA3010 (APA3011 held low).
2	BYPASS	I	Bypass pin.
3	INP	I	INP is the non-inverting input. INP is typically tied to the Bypass terminal.
4	INN	I	INN is the inverting input. INN is typically used as the audio input terminal.
5	VOP	O	VOP is the positive BTL output.
6	VDD	-	Supply voltage input pin.
7	GND	-	Ground connection for circuitry.
8	VON	O	VON is the negative BTL output.

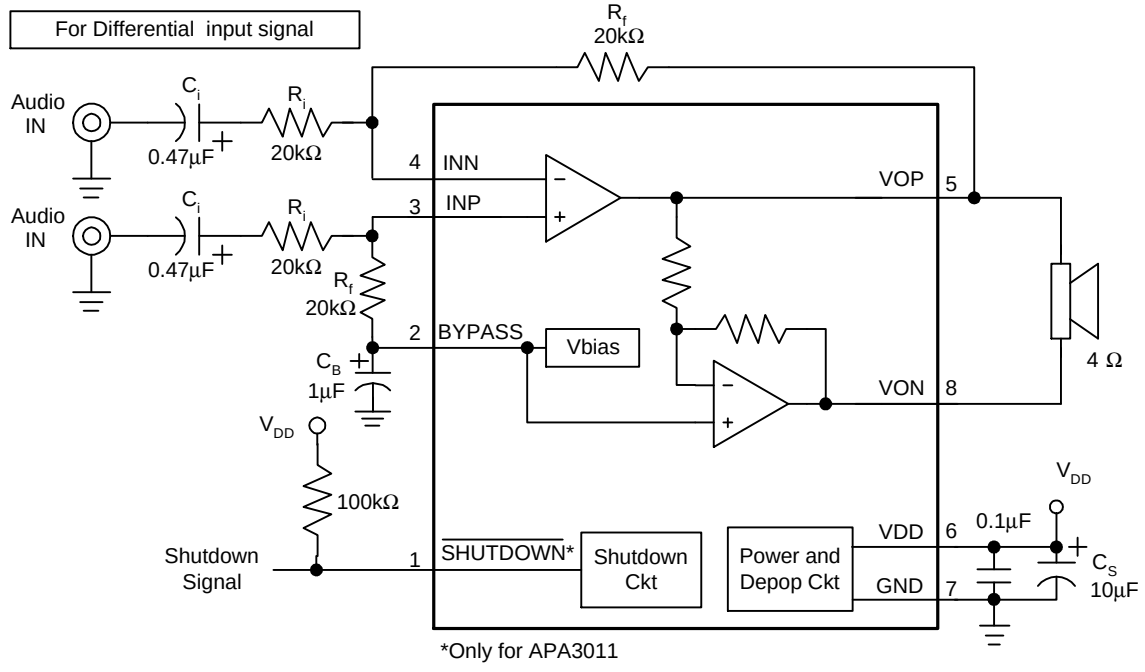
Block Diagram



Note * : APA3011 is $\overline{\text{SHUTDOWN}}$

Typical Application Circuit





Application Information

BTL Operation

The APA3010/1 output stage (power amplifier) has two pairs of operational amplifiers internally, allowed for different amplifier configurations.

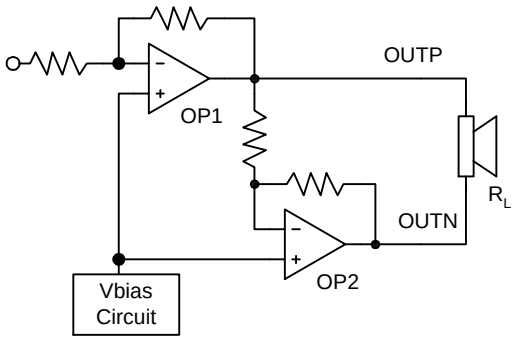


Figure 1. APA3010/1 Internal Configuration

The power amplifier's OP1 gain is setting by Ri and Rf while the second amplifier OP2 is internally fixed in a unity-gain, inverting configuration. Figure 1 shows that the output of OP1 is connected to the input to OP2, which results in the output signals of with both amplifiers with identical in magnitude but out of phase 180°. Consequently, the differential gain for each channel is 2 x (Gain of SE mode).

By driving the load differentially through outputs OUTP and OUTN, an amplifier configuration commonly referred to bridged mode is established. BTL mode operation is different from the classical single-ended SE amplifier configuration where one side of its load is connected to the ground.

A BTL amplifier design has few distinct advantages over the SE configuration, as it provides differential drive to the load, thus, doubling the output swing for a specified supply voltage.

When placed under the same conditions, a BTL amplifier has four times the output power of a SE amplifier. A BTL configuration, such as the one used in APA3010/1, also creates a second advantage over SE amplifiers. Since the differential outputs, OUTP and OUTN, are biased at half-supply, it is not necessary for DC voltage to be across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, SE configuration.

Input Resistance, R_i

The gain for audio input of the APA3010/1 is set by the external resistors (R_i and R_f).

$$\text{BTL Gain} = -2 \times \frac{R_f}{R_i} \qquad (1)$$

BTL mode operation brings the factor of 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. The input resistance will affect the low frequency performance of audio signal.

Input Capacitor, C_i

In the typical application, an input capacitor, C_i, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, C_i and the input impedance R_i (20kΩ) form a high-pass filter with the corner frequency determined in the following equation :

$$f_C(\text{highpass}) = \frac{1}{2\pi \times 20k\Omega \times C_i} \qquad (2)$$

The value of C_i must be considered carefully because it directly affects the low frequency performance of the circuit. Consider the example where R_i is 10kΩ and the specification calls for a flat bass response down to 50Hz. Equation is reconfigured as below :

$$C_i = \frac{1}{2\pi \times 20k\Omega \times f_C} \qquad (3)$$

When input resistance is considered, the C_i is 0.16μF, so a value in the range of 0.22μF to 1.0μF would be chosen. A further consideration for this capacitor is the leakage path from the input source through the input network (R_i+R_f, C_i) to the load.

This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the DC level of the amplifier input is held at $V_{DD}/2$. Please note that it is important to confirm the capacitor polarity in the application.

Application Information (Cont.)

Effective Bypass Capacitor, C_B

As other power amplifiers, proper supply bypassing is critical for low noise performance and high power supply rejection.

The capacitors located on both the bypass and power supply pins should be as close to the device as possible. The effect of a larger bypass capacitor will improve PSRR due to increased supply stability. Typical applications employ a 5V regulator with 1.0µF and a 0.1µF bypass capacitor as supply filtering. This does not eliminate the need for bypassing the supply nodes of the APA3010/1. The selection of bypass capacitors, especially C_B, is thus dependent upon desired PSRR requirements, click and pop performance.

To avoid the start-up pop noise occurred, the bypass voltage should rise slower than the input bias voltage and the relationship shown in equation (4) should be maintained.

$$\frac{1}{C_B \times 125k\Omega} << \frac{1}{40k\Omega \times C_i} \qquad (4)$$

The bypass capacitor is fed thru from a 125kΩ resistor inside the amplifier and the 40kΩ is maximum input resistance of (R_i+ R_f). Bypass capacitor, C_B, values of 3.3µF to 10µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

The bypass capacitance also effects to the start-up time. It is determined in the following equation :

$$Tstart\ up = 5 \times (C_B \times 125k\Omega) \qquad (5)$$

Power Supply Decoupling, C_S

The APA3010/1 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents the oscillations being caused by long lead length between the amplifier and the speaker. The optimum decoupling is achieved by using two different types of capacitors that target on different types of noise on the power supply leads.

For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance(ESR) ceramic capacitor, typically 0.1µF placed as close as possible to the device V_{DD} lead works best. For filtering lower-frequency noise signals, a large aluminum electrolytic capacitor of 10µF or greater placed near the audio power amplifier is recommended.

Optimizing Depop Circuitry

Circuitry has been included in the APA3010/1 to minimize the amount of popping noise at power-up and when coming out of shutdown mode. Popping occurs whenever a voltage step is applied to the speaker. In order to eliminate clicks and pops, all capacitors must be fully discharged before turn-on. Rapid on/off switching of the device or the shutdown function will cause the click and pop circuitry.

The value of C_i will also affect turn-on pops. (Refer to Effective Bypass Capacitance) The bypass voltage ramp up should be slower than input bias voltage. Although the bypass pin current source cannot be modified, the size of C_B can be changed to alter the device turn-on time and the amount of clicks and pops. By increasing the value of C_B, turn-on pop can be reduced. However, the tradeoff for using a larger bypass capacitor is to increase the turn-on time for this device. There is a linear relationship between the size of C_B and the turn-on time.

A high gain amplifier intensifies the problem as the small delta in voltage is multiplied by the gain. Therefore, it is advantageous to use low-gain configurations.

Shutdown Function

In order to reduce power consumption while not in use, the APA3010/1 contain a SHUTDOWN pin to externally turn off the amplifier bias circuitry. This shutdown feature turns the amplifier off when a logic high (APA3011 held low) is placed on the SHUTDOWN pin. The trigger point between a logic high and logic low level is typically 2.0V. It is best to switch between the ground and the supply V_{DD} to provide maximum device performance.

By switching the SHUTDOWN pin to high, the amplifier enters a low-current state, I_{DD}< 0.1µA. APA3010 is in shutdown mode. On normal operating, the SHUTDOWN pin pulls to a low level to keep the IC out of the shutdown mode. The SHUTDOWN pin should be tied to a definite voltage to avoid unwanted state change.

BTL Amplifier Efficiency

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load.

Application Information (Cont.)

BTL Amplifier Efficiency (Cont.)

The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_O}{P_{SUP}} \quad (6)$$

Where :

$$P_O = \frac{V_{Orms} \times V_{Orms}}{R_L} = \frac{V_P \times V_P}{2R_L}$$

$$V_{Orms} = \frac{V_P}{\sqrt{2}} \quad (7)$$

$$P_{SUP} = V_{DD} \times I_{DDAVG} = V_{DD} \times \frac{2V_P}{\pi R_L} \quad (8)$$

Efficiency of a BTL configuration :

$$\frac{P_O}{P_{SUP}} = \left(\frac{V_P \times V_P}{2R_L}\right) / \left(V_{DD} \times \frac{2V_P}{\pi R_L}\right) = \frac{\pi V_P}{4V_{DD}} \quad (9)$$

Table 1 calculates efficiencies for four different output power levels.

Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range.

Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design.

A final point to remember about linear amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to an utmost advantage when possible. Note that in equation, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up. In other words, use the efficiency analysis to choose the correct supply voltage and speaker impedance for the application.

P_O (W)	Efficiency (%)	I_{DD}(A)	V_{PP}(V)	P_D (W)
0.25	31.25	0.16	2.00	0.55
0.50	47.62	0.21	2.83	0.55
1.00	66.67	0.30	4.00	0.5
1.25	78.13	0.32	4.47	0.35

** High peak voltages cause the THD to increase.

Table 1. Efficiency Vs Output Power in 5-V/8Ω BTL Systems.

Power Dissipation

In BTL mode operation, the output voltage swing is doubled as in SE mode. Thus, the maximum power dissipation point for a BTL mode operating at the same given conditions is 4 times as in SE mode.

$$\text{BTL mode : } P_{D,MAX} = \frac{4V_{DD}^2}{2\pi^2 R_L} \quad (10)$$

Even with this substantial increase in power dissipation, the APA3010/1 do not require extra heatsink. The power dissipation from equation11, assuming a 5V-power supply and an 8Ω load, must not be greater than the power dissipation that results from the equation11 :

$$P_{D,MAX} = \frac{T_{J,MAX} - T_A}{\theta_{JA}} \quad (11)$$

For MSOP-8P package with thermal pad, the thermal resistance (θ_{JA}) is equal to 48°C/W.

Since the maximum junction temperature ($T_{J,MAX}$) of APA3010/1 is 150°C and the ambient temperature (T_A) is defined by the power system design, the maximum power dissipation which the IC package is able to handle can be obtained from equation11.

Once the power dissipation is greater than the maximum limit ($P_{D,MAX}$), either the supply voltage (V_{DD}) must be decreased, the load impedance (R_L) must be increased or the ambient temperature should be reduced.

Thermal Pad Consideration

The thermal pad must be connected to the ground. The package with thermal pad of the APA3010/1 requires special attention on thermal design. If the thermal design issues are not properly addressed, the APA3010/1 4Ω will go into thermal shutdown when driving a 4Ω load.

The thermal pad must be connected to the ground. The package with thermal pad of the APA3010/1 requires special attention on thermal design.

The thermal pad on the bottom of the APA3010/1 should be soldered down to a copper pad on the circuit board. Heat can be conducted away from the thermal pad through the copper plane to ambient. If the copper plane is not on the top surface of the circuit board, 8 to 12 vias of 15 mil or smaller in diameter should be used to thermally couple the thermal pad to the bottom plane.

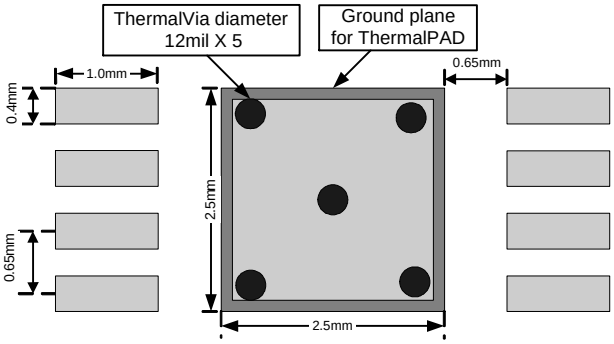
For good thermal conduction, the vias must be plated through and solder filled. The copper plane used to conduct heat away from the thermal pad should be as large as practical.

Application Information (Cont.)

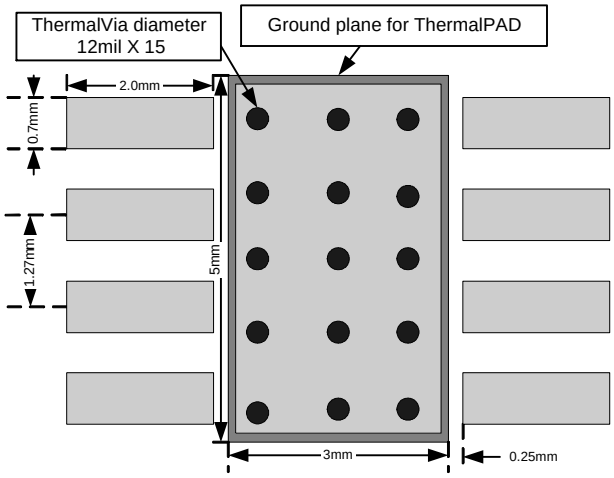
Thermal Pad Consideration (Cont.)

For good thermal conduction, the vias must be plated through and solder filled. The copper plane used to conduct heat away from the thermal pad should be as large as practical.

If the ambient temperature is higher than 25°C, a larger copper plane or forced-air cooling will be required to keep the APA3010/1 junction temperature below the thermal shutdown temperature (150°C). In higher ambient temperature, higher airflow rate and/or larger copper area will be required to keep the IC out of thermal shutdown.



MSOP-8P Land Pattern Recommendation



SOP-8P Land Pattern Recommendation

Thermal Consideration

Linear power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. To calculate maximum ambient temperatures, refer the **"Power Dissipation vs. Output Power"** graphs. Given θ_{JA}, the maximum allowable junction temperature (T_{JMAX}), and the total internal dissipation (P_D), the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the APA3010/1 is 150°C. The internal dissipation figures are taken from the **Power Dissipation vs. Output Power** graphs.

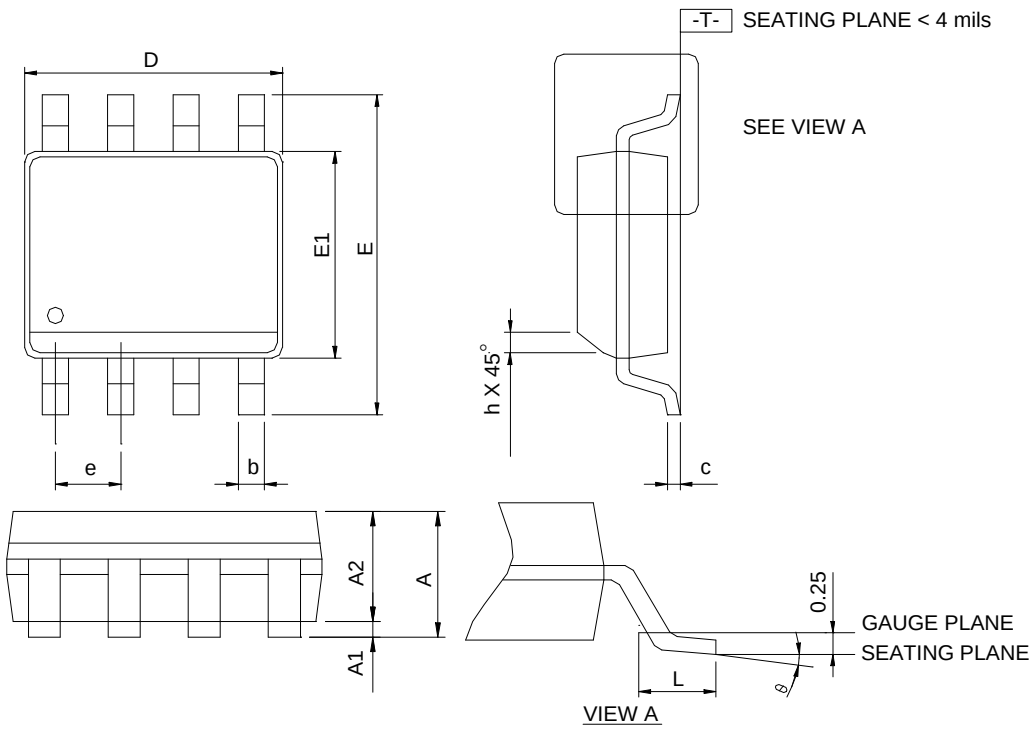
$$T_{AMax} = T_{JMax} - \theta_{JA} P_D \quad (12)$$

$$150 - 50(1.3) = 85°C$$

The APA3010/1 is designed with a thermal shutdown protection that turns the device off when the junction temperature surpasses 150°C to prevent damaging the IC.

Package Information

SOP-8

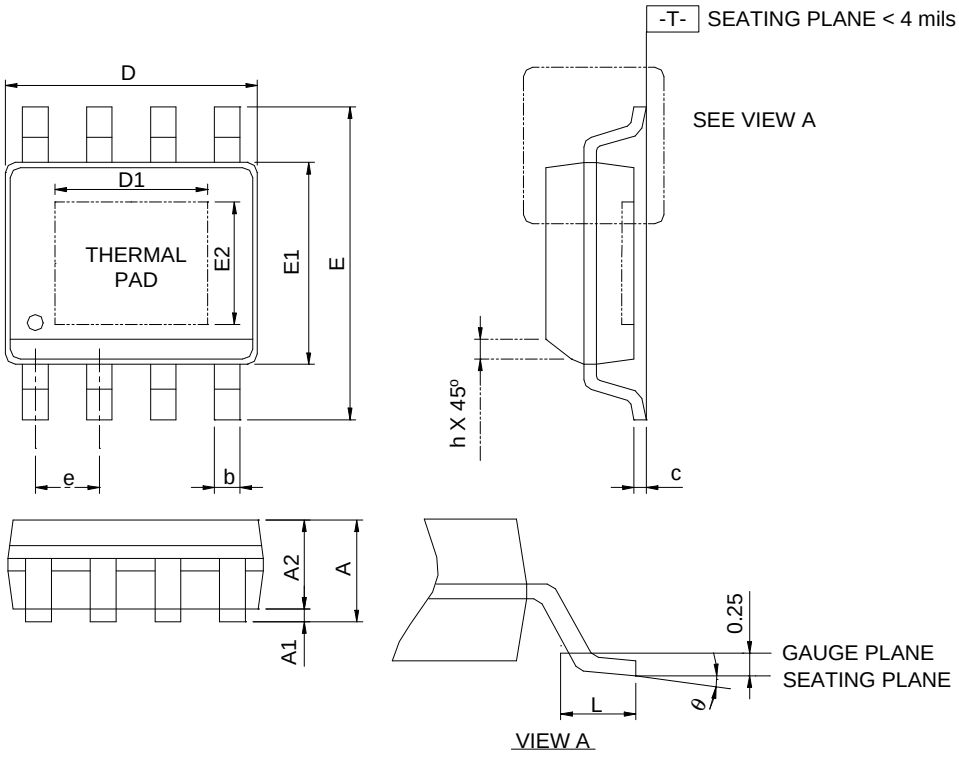


SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AA.
2. Dimension “D” does not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension “E” does not include inter-lead flash or protrusions.
Inter-lead flash and protrusions shall not exceed 10 mil per side.

Package Information

SOP-8P

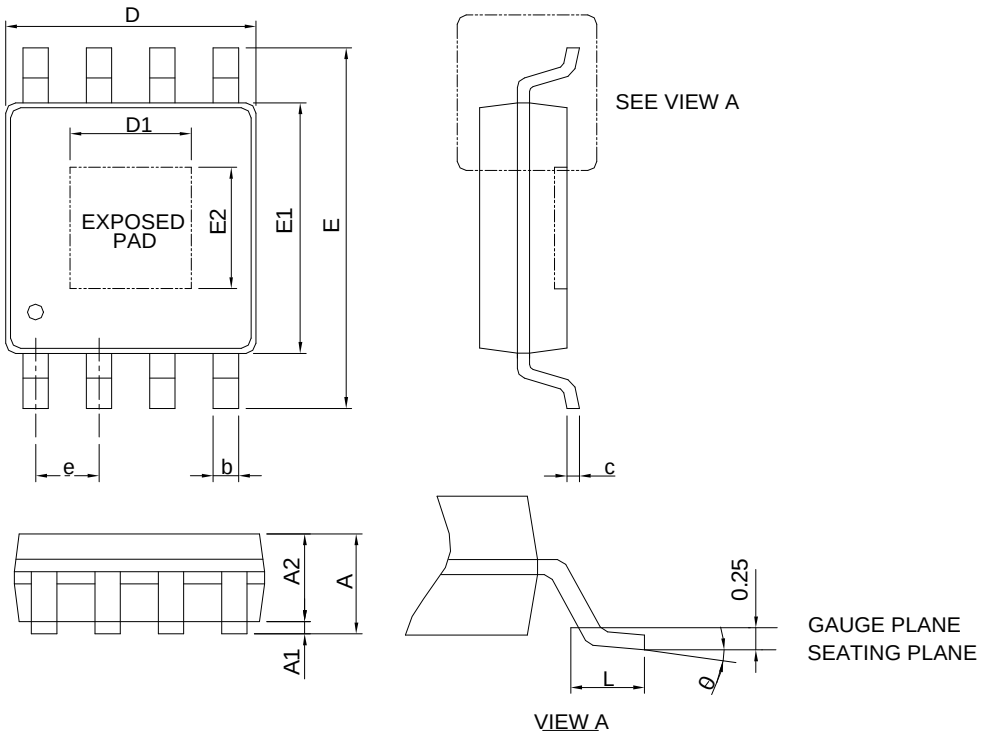


SYMBOL	SOP-8P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.60		0.063
A1	0.00	0.15	0.000	0.006
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
D1	2.50	3.50	0.098	0.138
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
E2	2.00	3.00	0.079	0.118
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°C	8°C	0°C	8°C

Note : 1. Followed from JEDEC MS-012 BA.
2. Dimension "D" does not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "E" does not include inter-lead flash or protrusions.
Inter-lead flash and protrusions shall not exceed 10 mil per side.

Package Information

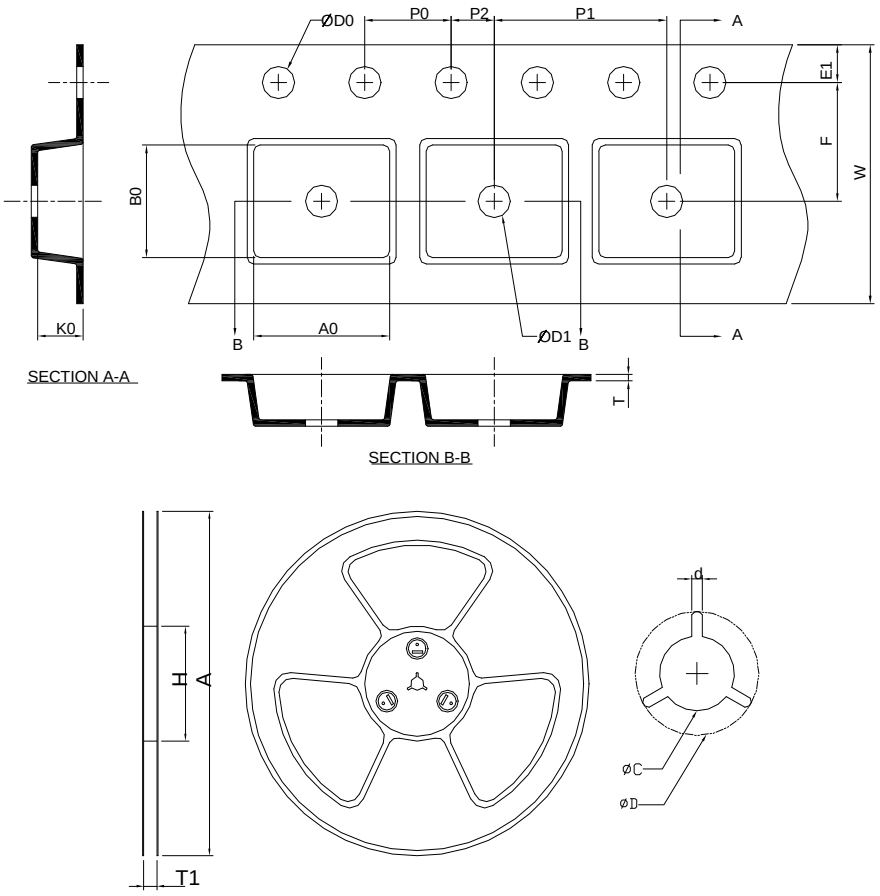
MSOP-8P



SYMBOL	MSOP-8P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.10		0.043
A1	0.00	0.15	0.000	0.006
A2	0.75	0.95	0.030	0.037
b	0.22	0.38	0.009	0.015
c	0.08	0.23	0.003	0.009
D	2.90	3.10	0.114	0.122
D1	1.50	2.50	0.059	0.098
E	4.70	5.10	0.185	0.201
E1	2.90	3.10	0.114	0.122
E2	1.50	2.50	0.059	0.098
e	0.65 BSC		0.026 BSC	
L	0.40	0.80	0.016	0.031
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MO-187 AA-T
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not flash or protrusions.
3. Dimension "E1" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 6 mil per side.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOP-8(P)	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
MSOP-8P	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.00±0.10	8.00±0.10	2.00±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	5.30±0.20	3.30±0.20	1.40±0.20

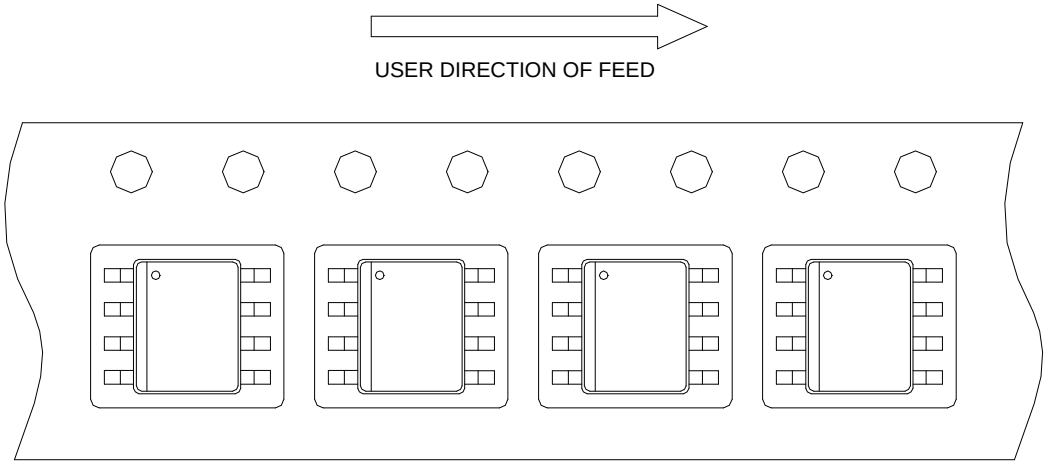
(mm)

Devices Per Unit

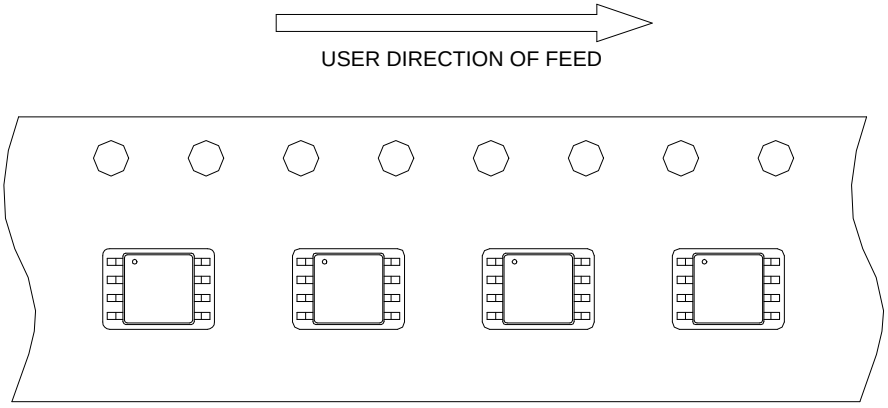
Package Type	Unit	Quantity
SOP-8(P)	Tape & Reel	2500
MSOP-8P	Tape & Reel	3000

Taping Direction Information

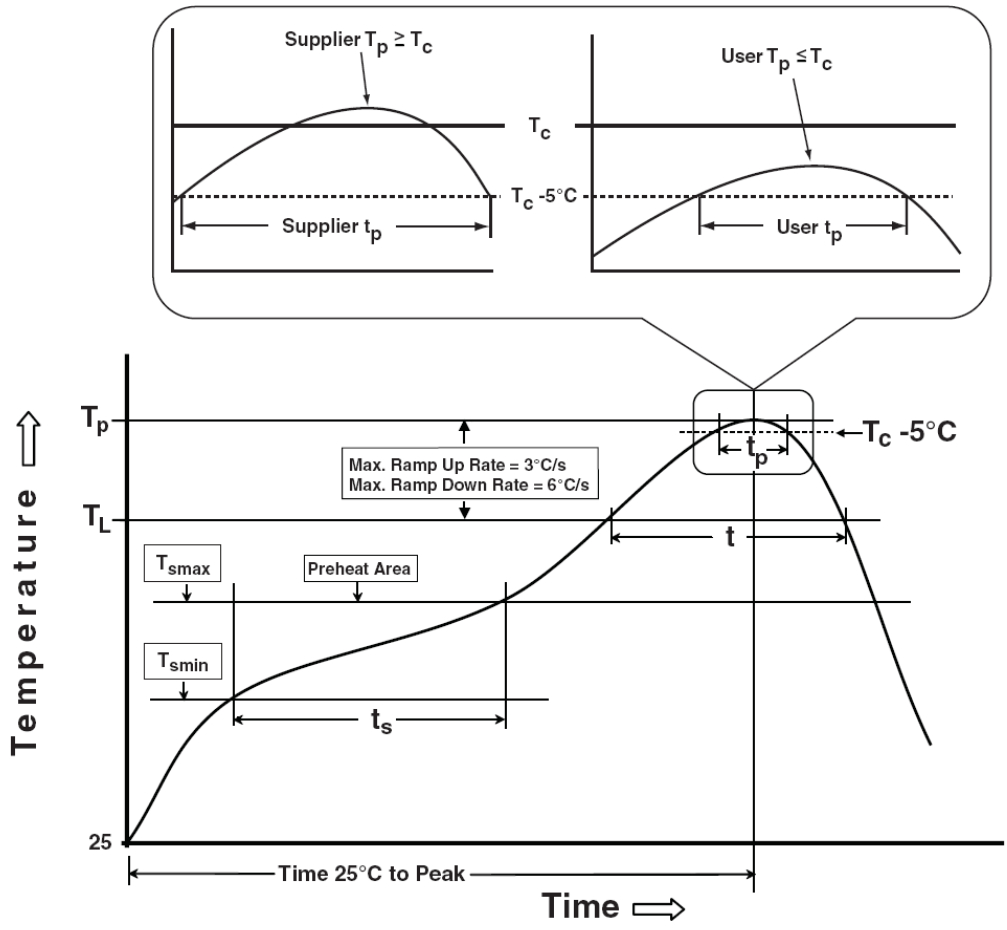
SOP-8(P)



MSOP-8P



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Classification Reflow Profiles

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ Tj=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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