

IECQ-CECC QC 88000-C001

COMPONENT ISSUE 6

SPECIFICATION March 2007

# Component Specification For Ceramic Hermetically Sealed Transistor Optocouplers





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#### **IEC**

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Box 131, rue de Varembé, CH 1211 Geneva 20, Switzerland

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#### **FOREWORD**

The IECQ Quality Assessment System for Electronic Components (IECQ) is composed of those member countries of the International Electrotechnical Commission (IEC) who wish to take part in a harmonized system for electronic components of assessed quality. IECQ is also known in some European member countries as IECQ-CECC.

The object of the System is to facilitate international trade by the harmonization of the specifications and quality assessment procedures for electronic components, and by the grant of an internationally recognised Mark, or Certificate of Conformity. The components produced or services provided under the system are thereby acceptable in all member countries without further testing.

This Component Specification is based upon the requirements of IEC Publication QC 001002-2, and has been prepared by:

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#### **AMENDMENT RECORD**

Issue 1 - Changed Page 10 - Amendments 25/06/10

Issue 2 - Changed Page 4 – Amendments 22/03/10

Issue 3 - Changed Pages 4 & 6 - Updated Drawings 25/06/10

Issue 4 - Changed Pages 3 & 4 - Added devices IS49 & 4N49 05/07/10

Issue 5 - Changed Pages 3, 4, 5, 6, 7 & 10 - RoHS Compliant, Added CSM165-2 & Amendments 13/07/10

#### **REQUIREMENTS**

The requirements for IECQ-CECC Component Specifications as detailed in QC 001002-2 Amendment 1 clause 5.4 are satisfied by the following data sheet.

It should note that IECQ-CECC are not responsible for manufacturers declarations made in data sheets which fall outside the limits of approved detailed in IECQ-CECC certificates.

This Component Specification is intended for use with applicable IECQ-CECC Assessment Specifications. Eg: QC 88000-A0001

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## **Ceramic Hermetically Sealed Transistor Optocouplers**

■ 4N24

■ 4N49

■ CD500/501

■ CH300

■ CS200/201

**■ CS224** 

CSM200

■ CSM1200

■ CSM1224

■ CSM165-2

CSM165-4

CSM2224

■ IS49

#### **Features**

- Release to IECQ-CECC
- Hermetically Sealed
- High Density Packaging
- 1500V DC withstand Test Voltage
- Low Input Requirements
- High Current Transfer Ratio
- RoHS Compliant

## **Applications**

- Military, high reliability system
- Medical instruments
- Mos, Cmos Applications
- Logic Interfacing
- Data Transmission
- Power Supply
- Modems

#### **Description**

These devices are single, dual and quad, hermetically sealed optocouplers. Each channel is composed of an infra-red emitting diode and a silicon phototransistor. Package styles for these devices include 6 pin, 8 pin, 16 pin flat pack, and hybrid 4 pin, with surface mount, butt cut and gull wing options available.

The same electrical die, assembly processes and materials are used for each channel of each device shown below. Therefore absolute maximum ratings, recommended operating conditions, electrical specifications and performance characteristics are identical for all units. Any exceptions, due to packaging variations and limitations, are as noted.

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## **Selection Guide Package Styles and Configuration Options**

Package	4 pin Hybrid	6 pin Metal Can TO-5	6 pin LCC	6 pin DIP	8 pin DIP	16 pin Flat Pack
Lead Style						
Channels	1	1	1	1	2	2/4
Common Channel Wiring						

**Isocom Part Numbers and Options** 

		4N24	CSM200, IS49	CS200/201	CD500	
Commercial	CH300	4N49	CSM1200/1244/2224	CS224	CD501	CSM165
		4N24/L2	CSM200/L2, IS49/L2	CM200/201/L2	CD500/L2	
Defense Screen Level	CH300/L2	4N49/L2	CSM1200/1244/2224/L2	CS224/L2	CD501/L2	CSM165/L2
		4N24/L2S	CSM200/L2S, IS49/L2S	CS200/201/L2S	CD500/L2S	
Space Screen Level	CH300/L2S	4N49/L2S	CSM1200/1244/2224/L2S	CS224/L2S	CD501/L2S	CSM165/L2S
Standard Gold Plate Finish		Gold Plate	Gold Plate	Gold Plate	Gold Plate	Gold Plate
Solder Dipped				Option 20	Option 20	
Butt Cut/Gold Plate				Option 10	Option 10	
Gull Wing/Soldered				Option 30	Option 30	
Crew Cut/Gold Plate				Option 60	Option 60	

## **Functional Diagrams**

CH300	CS200/201	CSM200	CSM1224 IS49	CD500 CD501	CSM165-2
4 pin Hybrid	6 pin DIP	6 pin LCC	6 pin LCC	8 pin DIP	16 pin Flat Pack
1 Channel	1 Channel	1 Channel	1 Channel	2 Channel	*2 Channel
4 3 医之 以 1 2	6 5 4   \2    \1  1 2 3	1 2 5 4	5 4 3 3	8 7 6 5	16 15 14 13 12 11 10 9
4N24 4N49	CS224	CSM1200	CSM2224		CSM165-4
6 pin TO-5	6 pin DIP	** 6 pin LCC	6 pin LCC		16 pin Flat Pack
1 Channel	1 Channel	1 Channel	1 Channel		4 Channel
5 7 1	6 5 4 	6 5 4 1 3	5		16 15 14 13 12 11 10 9

Note 2 channel is only for circuit of 2 middle channels 2 & 3 channel on the circuits.

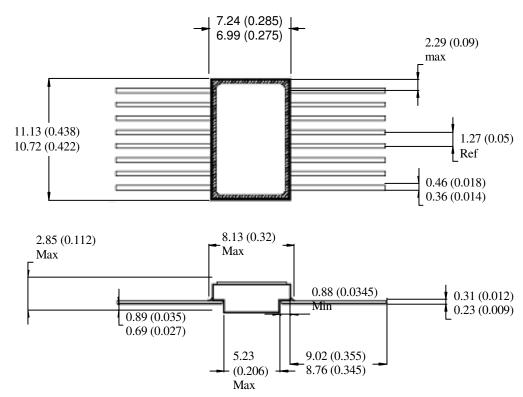
\*\* See Outline Drawings 6 Terminal LCC Surface Mount, 1 Channel

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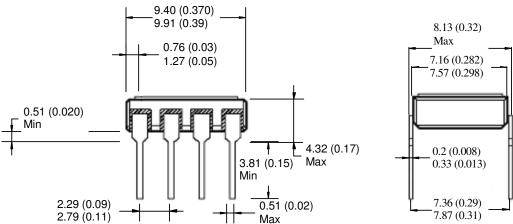
## **Outline Drawings**

16 pin Flat Pack, 2 and 4 Channel



NOTE: DIMENSIONS IN MILLIMETERS

#### 8 pin DIP 2 Channel

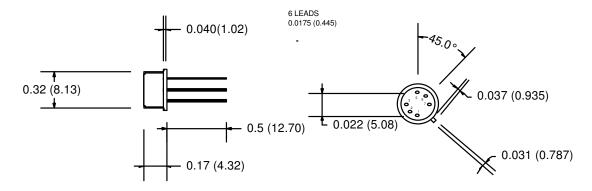


NOTE: DIMENSIONS IN MILLIMETERS

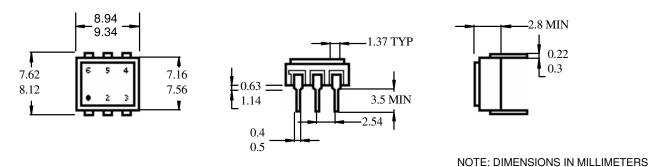
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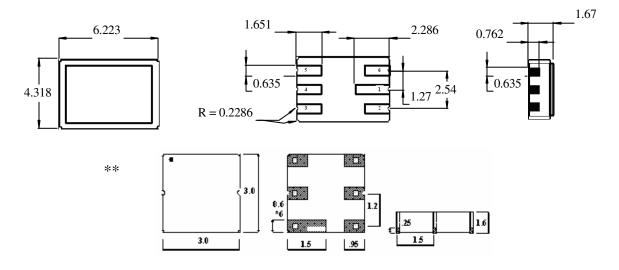
#### 6 pin TO-5, 1 Channel



#### 6 pin DIP 1 channel



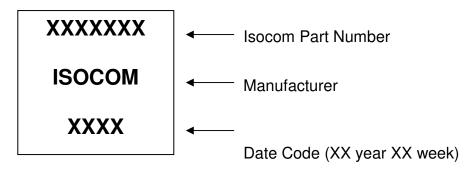
#### 6 Terminal LCC Surface Mount, 1 Channel



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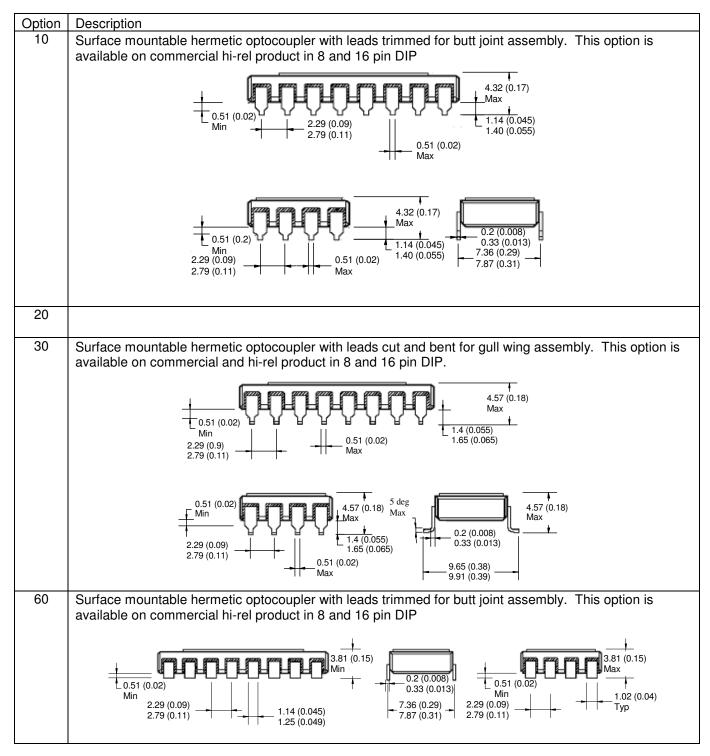
## **Device Marking**



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### **Hermetic Optocoupler Options**



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## **Absolute Maximum Ratings**

Storage Temperature	-65 ℃ to +150 ℃
Operating Temperature	-55 ℃ to +125 ℃
Lead Soldering Temperature	260 °C 1.6mm from case for 10S
Input-to-Output Isolation Voltage	û1500VDC
	û500VDC for CH300

**Input Diode** 

Forward DC Current	50mA	
	15mA	For CH300
Reverse DC Voltage	7V	
	5V	For CH300
	3V	For CSM165
	2V	For CS224
Peak forward Current	1.5mA	≤ 10µS duration
Power Dissipation	100mW	Derate linearly above 100 °C at 1.6W/ °C.
	150mW	For CD500/501 andCSM165. Derate linearly above 100 °C at 1.4W/ °C for CD500/501, and at 1.6 W/ °C for CSM165
	25mW	For CH300

**Output Transistor** 

Collector-Emitter Voltage	50V	BV <sub>CEO</sub>
	30V	For CH300
	35V	For CS224
Emitter-Collector Voltage	7V	BV <sub>ECO</sub>
Collector-Base Voltage	70V	BV <sub>CBO</sub> For CS200/201 and CS224
	35V	For CS224
Collector Current	50mA	
	20mA	For CH300
Collector Current	100mA	t = 1mS
Power Dissipation	100mW	For CH300. Derate linearly above 100 °C at 1.4W/°C
	150mW	For CS200/201, CS224, CD500/501 and CSM165.
		Derate linearly above 100 °C at 1.4W/ °C

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## Electrical Characteristics T<sub>A</sub> = 25 °C U.O.S. (each channel where appropriate).

**Input Diode Electrical Characteristics** 

Parameter	Symbol	Test Conditions	Device	Min	Type	Max	Units
Forward Voltage	V <sub>F</sub>	$I_F = 10mA$		0.7	1.18	1.8	V
_		I <sub>F</sub> = 10mA, T <sub>A</sub> = 125 ℃		0.7	1.10	1.8	(note 4)
		I <sub>F</sub> = 10mA, T <sub>A</sub> = -55 ℃		0.7	1.29	1.8	
Reverse Breakdown	V <sub>R</sub>	$I_R = 0.1 \text{mA}$		5	-	-	V
Voltage							
Reverse Current	I <sub>R</sub>	$V_R = 3V$		-	-	100	μΑ
Capacitance	C <sub>IN</sub>	V = 0, $f = 1MHz$		-	25	-	pF

**Output Detector Electrical Characteristics** 

			1		1	1	
Collector-Emitter	BV <sub>CEO</sub>	$I_C = 1 \text{mA}$		40	-	-	V
Breakdown Voltage			CH300	30			
(See note 1 below)							
Collector-Base Breakdown	$BV_CBO$	$I_B = 0.1 \text{mA}$		70	-	-	V
Voltage							
(See note 1 below)							
Emitter-Collector	BV <sub>ECO</sub>	$I_E = 0.1 \text{mA}$		7	-	-	V
Breakdown Voltage							
Emitter-Base Breakdown	BV <sub>EBO</sub>	$I_B = 0.1 \text{mA}$		5	-	-	V
Voltage							
Collector-Emitter Leakage	I <sub>CEO</sub>	$V_{CE} = 20V, I_F = 0$		-	6	100	μΑ
Current		$V_{CE} = 15v I_F = 0$	CSM165				'
		V <sub>CE</sub> = 20V, I <sub>F</sub> = 0, T <sub>A</sub> = 125 °C		-	8	100	μΑ

**Coupled Electrical Characteristics** 

Odupica Electrical O	iiai aotoi	101100					
DC Current Transfer Ratio	IC/IF	$I_F = 10 \text{mA}, V_{CE} = 5 \text{V}$		50	-	-	%
(See note 3)			CS201	100			
		$I_F = 10 \text{mA}, V_{CE} = 5 \text{V}, T_A = 125 ^{\circ}\text{C}$	CS201	50	-	-	
		$I_F = 10 \text{mA}, V_{CE} = 5 \text{V}, T_A = -55 ^{\circ}\text{C}$	CS201	50	-	-	
		$I_F = 10 \text{mA}, V_{CE} = 5 \text{V}; T_A = -55  \text{C} - 125  \text{C}$		35	-	-	
Optical Crosstalk	I <sub>CEOX</sub>	$V_{CE} = 15v$ , , $I_F 2-4 = 10mA$ .	CSM165			250	μΑ
Collector-Emitter Saturation	$V_{CE}$	$I_F = 10 \text{mA}, I_C = 2.5 \text{mA}$		-	-	0.3	V
Voltage	(Sat)	$I_F = 10 \text{mA}, I_C = 10 \text{mA}$	CSM165		0.4	0.9	
		$I_F = 2mA, I_C = 0.2mA$	CH300			0.25	
Input to Output Capacitance	C <sub>IO</sub>	V <sub>IO</sub> = 0, f = 1mhz (See note 2 below)		-	3	5	pF
Input to Output Resistance	R <sub>IO</sub>	V <sub>IO</sub> = 500V (See note 2 below)		-	10 <sup>11</sup>	-	Ω
Isolation Voltage	V <sub>IO</sub>	(See note 2 below)		1500	-	-	VDC
· ·			CH300	500			
Delay Time	td	$V_{CC} = 5V$ , $I_C = 2mA$		-	4.0		μS
Rise Time	tr	$R_L = 100Ohms$		-	5.0		μS
Storage Time	ts			-	0.7		μS
Fall Time	tf			-	5.0		μS
Turn -on Time	t <sub>on</sub>	$V_{CC} = 5V$ , $I_f = 5mA$		-	9		μS
Turn-off Time	t <sub>off</sub>	$R_L = 1KOhms$		-	25		μS

1.  $BV_{CEO}$  and  $BV_{CBO}$  can be selected to suit customer specifications. Notes:

- 2. Measured between input when leads 1, 2 and 3 are shorted together and output when leads 4, 5 and 6 are shorted together.
- 3. A higher CTR can be selected to suit customer specification as a standard part.
- 4. For Radiation Tolerant  $V_F$  max = 2.0v

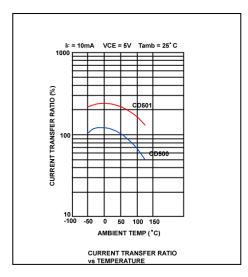
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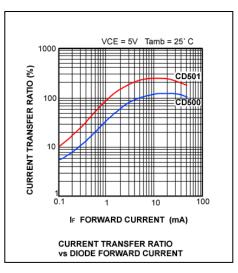
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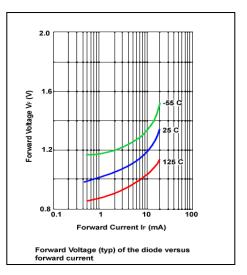
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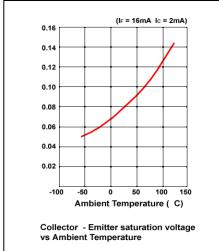


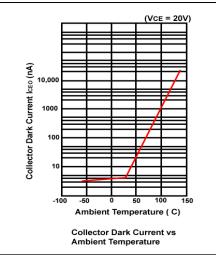
## **Electrical Characteristics**

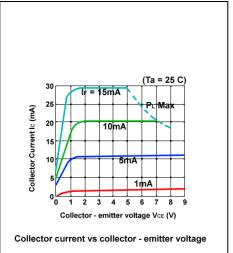






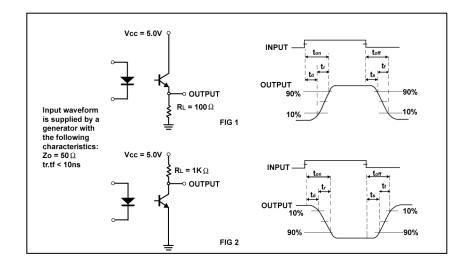






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