GAL 20RA10

High Performance E²CMOS® Generic Array Logic™

FEATURES

- **HIGH PERFORMANCE E²CMOS TECHNOLOGY**
  - **15 ns Maximum Propagation Delay**
  - **Fmax = 50 MHz**
  - **15 ns Maximum from Clock Input to Data Output**
  - **TTL Compatible 8 mA Outputs**
  - **UltraMOS® III Advanced CMOS Technology**
  - **Internal Pull-Up Resistor on all Pins**
- **50% REDUCTION IN POWER**
  - **100 mA MAX I_{cc}**
- **E² CELL TECHNOLOGY**
  - **Reconfigurable Logic**
  - **Reprogrammable Cells**
  - **100% Tested/Guaranteed 100% Yields**
  - **High Speed Electrical Erasure (<50ms)**
  - **20 Year Data Retention**
- **TEN OUTPUT LOGIC MACROCELLS**
  - **Maximum Flexibility for Complex Logic Designs**
    Registered or Combinational with Polarity
  - **Individually Programmable Macrocell Functions:**
    Product Term Clock
    Asynchronous Reset
    Asynchronous Preset
    Output Enable
  - **Common Output Enable & Preload Functions**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **100% Functional Testability**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

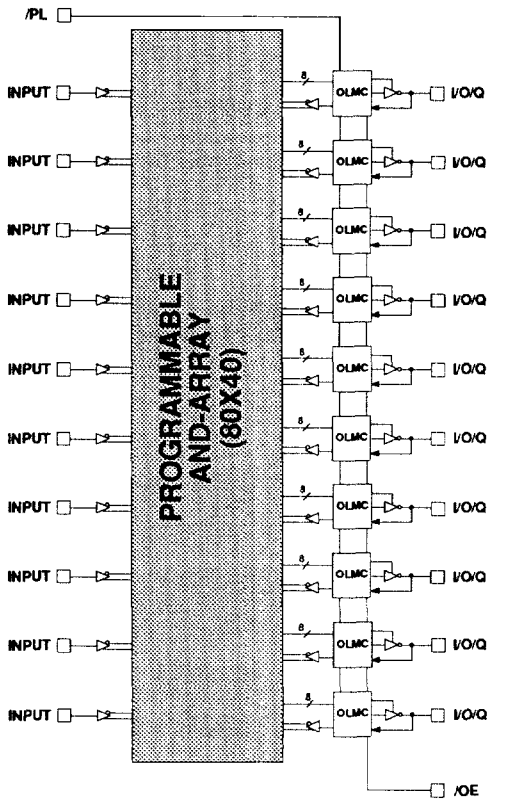
DESCRIPTION

The GAL®20RA10, at 15 ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest performance available of any 20RA10 device on the market. CMOS circuitry allows the GAL20RA10 to consume just 100 mA maximum I_{cc} which represents a 50% savings in power when compared to its bipolar counterparts. The E² technology offers high speed (50ms) erase times providing the ability to reprogram or reconfigure the devices quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL20RA10 is fully function/fuse map/parametric compatible with bipolar and CMOS 20RA10 devices.

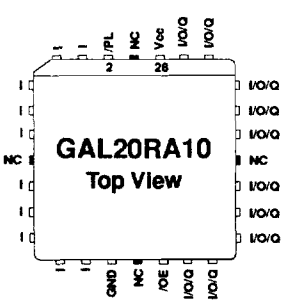
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. Therefore, LATTICE guarantees 100% field programmability and functionality of all GAL products. LATTICE also guarantees 100 erase/rewrite cycles and that data retention exceeds 20 years.

FUNCTIONAL BLOCK DIAGRAM



PIN DIAGRAMS

Chip Carrier



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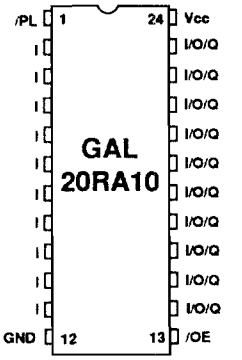


LATTICE SEMICONDUCTOR CORP., 5555 N.E. Moore Ct., Hillsboro, Oregon 97124, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503) 681-3037

ABSOLUTE MAXIMUM RATINGS[1]

Supply voltage V_{CC} ..... –.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

Tri-state levels are measured 0.5V from steady-state active level.

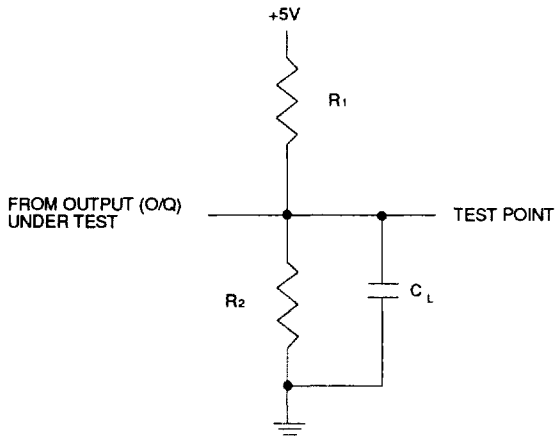
COMMERCIAL		INDUSTRIAL		MILITARY	
R_1	R_2	R_1	R_2	R_1	R_2
470	390	470	390	470	390

AC Test Conditions:

Cond. 1) R_1 per table; C_L = 50pF; R_2 per above table

Cond. 2) Active High R_1 = ∞; Active Low R_1 per table; C_L = 50pF; R_2 per above table

Cond. 3) Active High R_1 = ∞; Active Low R_1 per table; C_L = 5pF; R_2 per above table



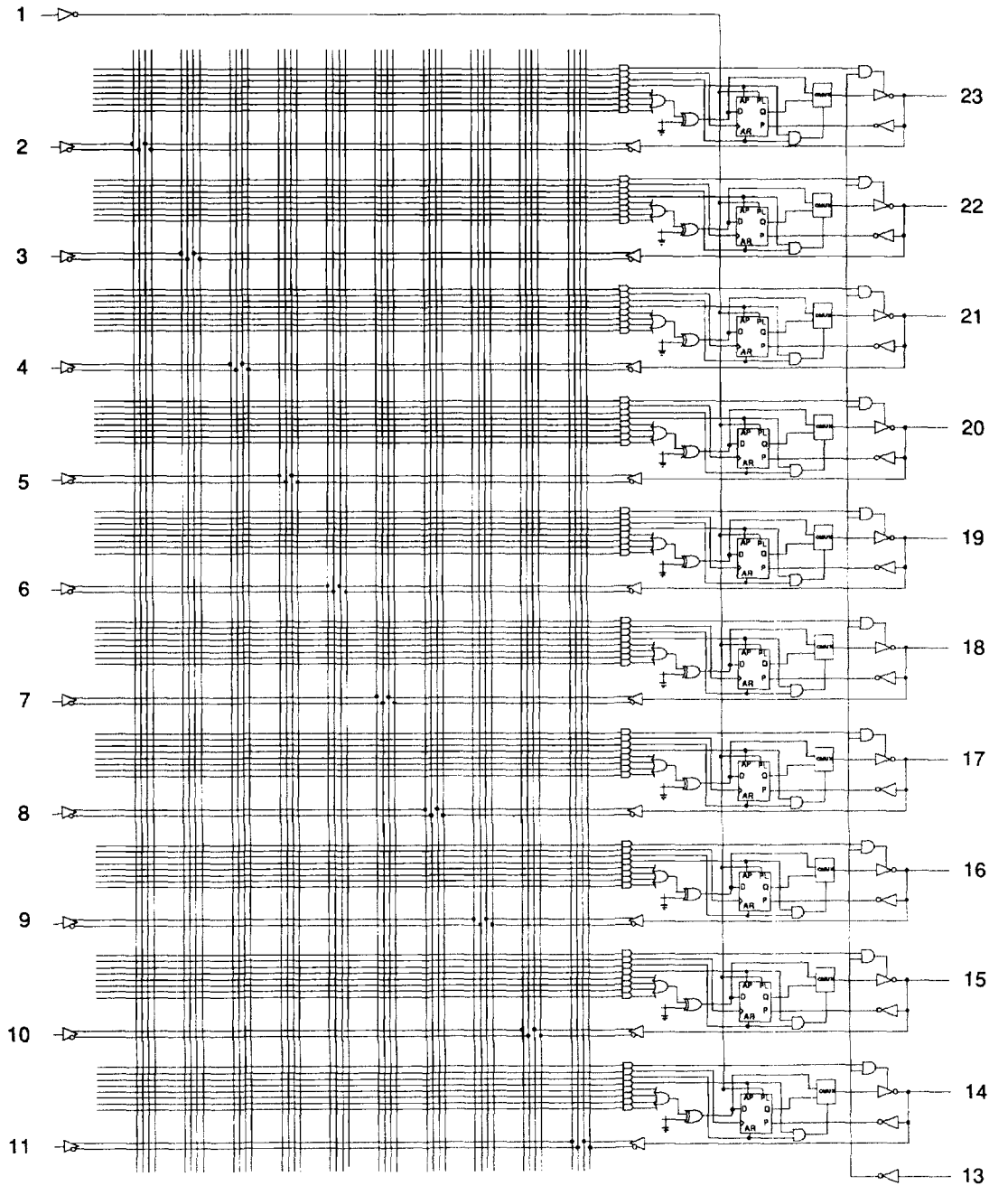
CL INCLUDES JIG AND PROBE TOTAL CAPACITANCE

CAPACITANCE (T_A = 25 C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O/Q}$	I/O/Q Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O/Q}$ = 2.0V

*Guaranteed but not 100% tested.

GAL20RA10 LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS — GAL20RA10-15L Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = Max.	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = Max.	2.4	—	—	V
I_{IL}, $I_{I/O/QL}$[1]	Leakage Current Low	V_{IL} = 0V	—	—	–100	µA
I_{IH}, $I_{I/O/QH}$[1]	Leakage Current High	$V_{IH} \geq 3.5V$	—	—	10	µA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T = 25° C	–50	—	–135	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	75	100	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — GAL20RA10-15L Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	75	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	8	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — GAL20RA10-15L Commercial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Input or Feedback to Combinational Output	1	—	15	ns
t_{co}	2	I, I/O	Q	Input Clock to Registered Output	1	—	15	ns
$t_{en/dis}$	3	I, I/O	O, Q	Input to Output Enable/Disable	2,3	—	15	ns
$t_{en/dis}$	4	I	O, Q	Pin 13 to Output Enable/Disable	2,3	—	12	ns
$t_{ar/ap}$	5	I, I/O	Q	Asynchronous Register Reset/Preset	1	—	15	ns

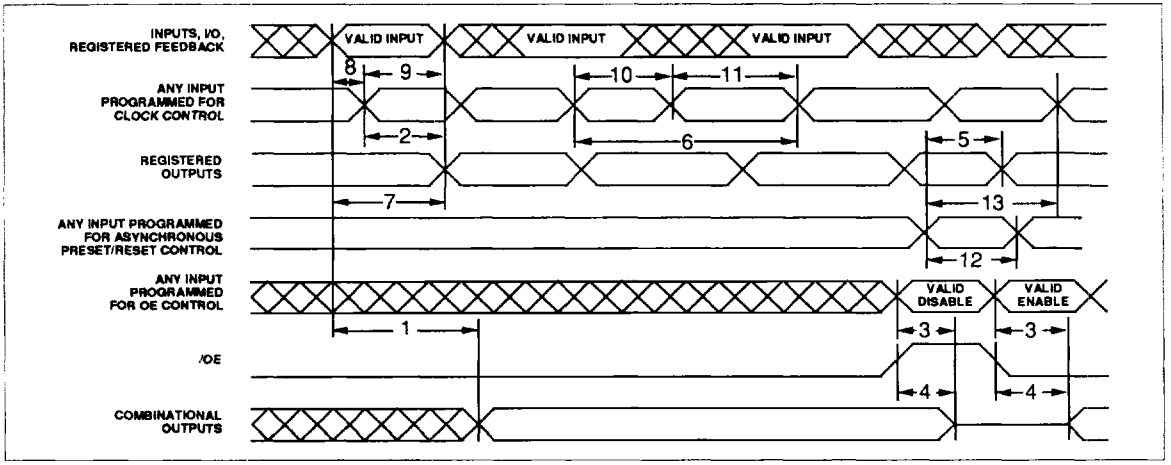
1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL20RA10-15L Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	6	Clock Frequency without Feedback[1] = $1/(t_{wh}+t_{wl})$	—	0	50.0	MHz
	7	Clock Frequency with Feedback[1] = $1/(t_{su}+t_{co})$	—	0	45.0	MHz
t_{su}	8	Setup Time, Input or Feedback, before Clk ↑	—	7	—	ns
t_h	9	Hold Time, Input or Feedback, after Clk ↑	—	0	—	ns
t_w	10	Clock Pulse Duration, High[2]	—	10	—	ns
	11	Clock Pulse Duration, Low[2]	—	10	—	ns
t_{rpw}	12	Asynchronous Reset/Preset Pulse Duration	—	15	—	ns
t_{rec}	13	Asynchronous Reset/Preset to Clk ↑ Recovery Time	—	10	—	ns

1) fclk is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing fclk specifications.
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL20RA10-20L Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = Max.	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = Max.	2.4	—	—	V
I_{IL}, $I_{I/O/QL}$[1]	Leakage Current Low	V_{IL} = 0V	—	—	–100	µA
I_{IH}, $I_{I/O/QH}$[1]	Leakage Current High	$V_{IH} \geq 3.5V$	—	—	10	µA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T = 25° C	–50	—	–135	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	75	100	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — GAL20RA10-20L Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	75	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	8	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — GAL20RA10-20L Commercial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Input or Feedback to Combinational Output	1	—	20	ns
t_{co}	2	I, I/O	Q	Input Clock to Registered Output	1	—	20	ns
$t_{en/dis}$	3	I, I/O	O, Q	Input to Output Enable/Disable	2,3	—	20	ns
$t_{en/dis}$	4	I	O, Q	Pin 13 to Output Enable/Disable	2,3	—	15	ns
$t_{ar/ap}$	5	I, I/O	Q	Asynchronous Register Reset/Preset	1	—	20	ns

1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL20RA10-20L Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	6	Clock Frequency without Feedback[1] = $1/(t_{wh}+t_{wl})$	—	0	41.7	MHz
	7	Clock Frequency with Feedback[1] = $1/(t_{su}+t_{co})$	—	0	33.3	MHz
t_{su}	8	Setup Time, Input or Feedback, before Clk ↑	—	10	—	ns
t_h	9	Hold Time, Input or Feedback, after Clk ↑	—	0	—	ns
t_w	10	Clock Pulse Duration, High[2]	—	12	—	ns
	11	Clock Pulse Duration, Low[2]	—	12	—	ns
t_{rpw}	12	Asynchronous Reset/Preset Pulse Duration	—	20	—	ns
t_{rec}	13	Asynchronous Reset/Preset to Clk ↑ Recovery Time	—	12	—	ns

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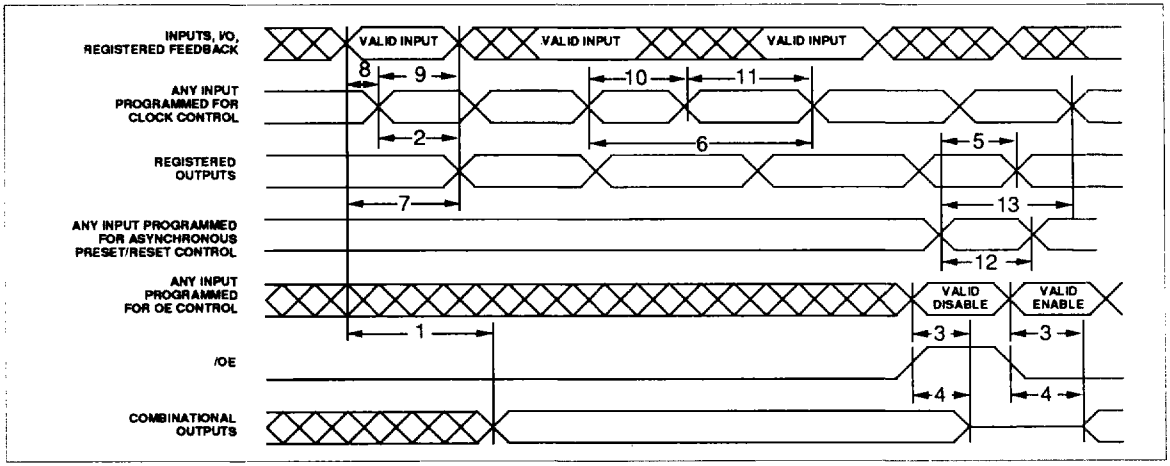
SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL20RA10-20L Industrial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = Max.	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = Max.	2.4	—	—	V
I_{IL}, $I_{I/O/QL}$[1]	Leakage Current Low	V_{IL} = 0V	—	—	-100	µA
I_{IH}, $I_{I/O/QH}$[1]	Leakage Current High	$V_{IH} \geq 3.5V$	—	—	10	µA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T = 25° C	-50	—	-135	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	75	120	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — GAL20RA10-20L Industrial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	-40	85	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	8	mA
I_{OH}	High Level Output Current	—	-3.2	mA

SWITCHING CHARACTERISTICS — GAL20RA10-20L Industrial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Input or Feedback to Combinational Output	1	—	20	ns
t_{co}	2	I, I/O	Q	Input Clock to Registered Output	1	—	20	ns
$t_{en/dis}$	3	I, I/O	O, Q	Input to Output Enable/Disable	2,3	—	20	ns
$t_{en/dis}$	4	I	O, Q	Pin 13 to Output Enable/Disable	2,3	—	15	ns
$t_{ar/ap}$	5	I, I/O	Q	Asynchronous Register Reset/Preset	1	—	20	ns

1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL20RA10-20L Industrial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	6	Clock Frequency without Feedback[1] = $1/(t_{wh}+t_{wl})$	—	0	41.7	MHz
	7	Clock Frequency with Feedback[1] = $1/(t_{su}+t_{co})$	—	0	33.3	MHz
t_{su}	8	Setup Time, Input or Feedback, before Clk ↑	—	10	—	ns
t_h	9	Hold Time, Input or Feedback, after Clk ↑	—	0	—	ns
t_w	10	Clock Pulse Duration, High[2]	—	12	—	ns
	11	Clock Pulse Duration, Low[2]	—	12	—	ns
t_{rpw}	12	Asynchronous Reset/Preset Pulse Duration	—	20	—	ns
t_{rec}	13	Asynchronous Reset/Preset to Clk ↑ Recovery Time	—	12	—	ns

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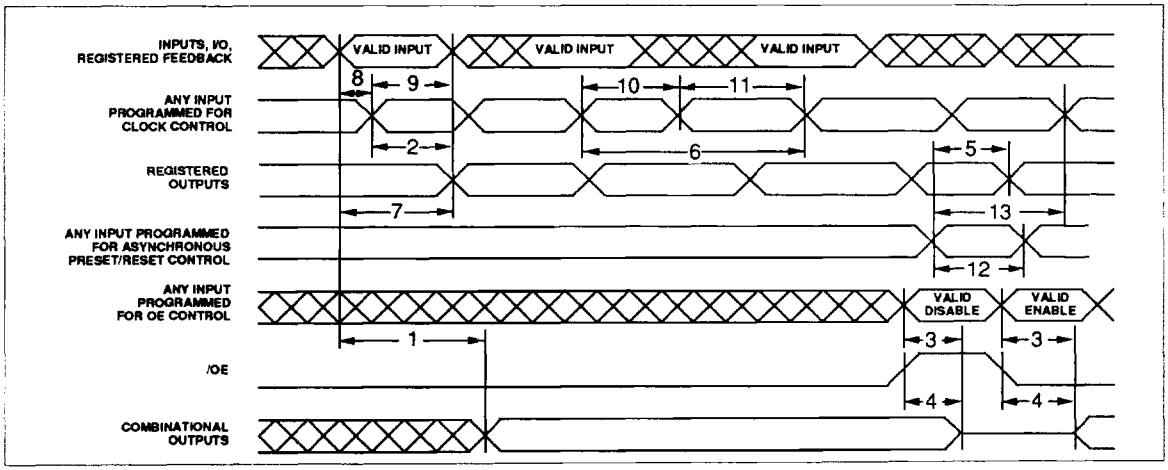
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL20RA10-20L Military

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = Max.	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = Max.	2.4	—	—	V
I_{IL}, $I_{I/O/QL}$[1]	Leakage Current Low	V_{IL} = 0V	—	—	-100	µA
I_{IH}, $I_{I/O/QH}$[1]	Leakage Current High	$V_{IH} \geq$ 3.5V	—	—	10	µA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T = 25° C	-50	—	-135	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	75	120	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — GAL20RA10-20L Military

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_C	Case Temperature	-55	125	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	V_{SS} – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	8	mA
I_{OH}	High Level Output Current	—	-3.2	mA

SWITCHING CHARACTERISTICS — GAL20RA10-20L Military

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Input or Feedback to Combinational Output	1	—	20	ns
t_{co}	2	I, I/O	Q	Input Clock to Registered Output	1	—	20	ns
$t_{en/dis}$	3	I, I/O	O, Q	Input to Output Enable/Disable	2,3	—	20	ns
$t_{en/dis}$	4	I	O, Q	Pin 13 to Output Enable/Disable	2,3	—	15	ns
$t_{ar/ap}$	5	I, I/O	Q	Asynchronous Register Reset/Preset	1	—	20	ns

1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL20RA10-20L Military

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
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	7	Clock Frequency with Feedback[1] = $1/(t_{su}+t_{co})$	—	0	33.3	MHz
t_{su}	8	Setup Time, Input or Feedback, before Clk ↑	—	10	—	ns
t_h	9	Hold Time, Input or Feedback, after Clk ↑	—	0	—	ns
t_w	10	Clock Pulse Duration, High[2]	—	12	—	ns
	11	Clock Pulse Duration, Low[2]	—	12	—	ns
t_{rpw}	12	Asynchronous Reset/Preset Pulse Duration	—	20	—	ns
t_{rec}	13	Asynchronous Reset/Preset to Clk ↑ Recovery Time	—	12	—	ns

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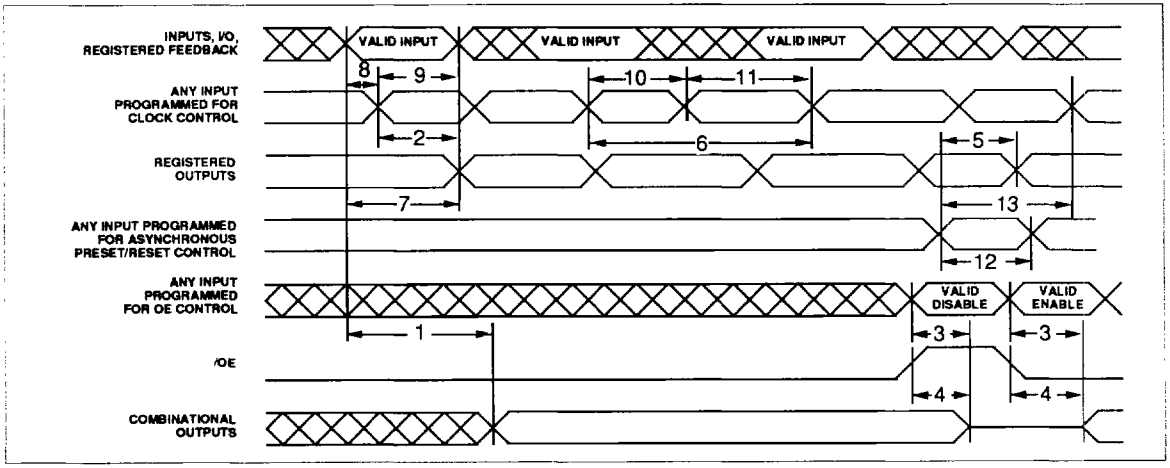
SWITCHING WAVEFORMS



OUTPUT LOGIC MACROCELL ARCHITECTURE

The GAL20RA10 has eight product terms for each of the ten available OLMCs. Four of the product terms are used for generating the logic function. The remaining four product terms control asynchronous reset, asynchronous preset, clock and output enable individually for every OLMC. Each OLMC can also be individually configured as registered or combinational.

All of the 20 input and I/O pins have a unique array input path assigned to them. This allows input functions of up to 19 inputs (assuming at least one output function is used) using any combination of 10 dedicated and 9 of the 10 programmable I/O pins. All macrocells are controlled by the same configuration of data and control pins allowing the design engineer to exchange pin assignments for I/O functions without restriction.

OUTPUT ENABLE

The output enable function of each macrocell is controlled by a dynamic "AND" function of a product term in each macrocell and a common, active low /OE device pin. If product term control is selected then all macrocells must be product term controlled as the /OE device pin must be tied to a logic "0" for product term control to be effective.

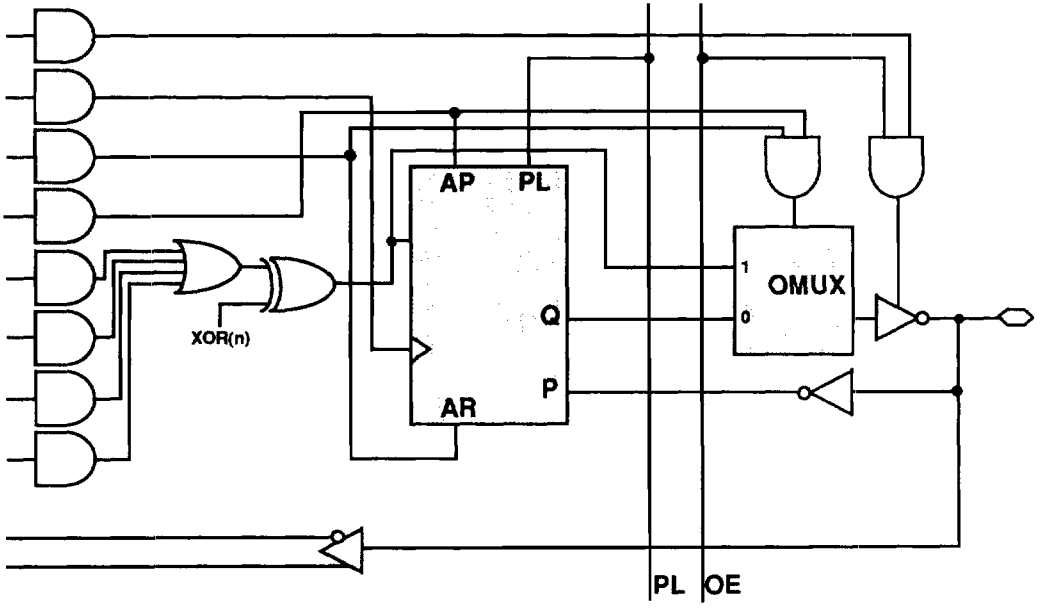
REGISTER / COMBINATIONAL CONTROL

Register control in each macrocell is dynamic through the use of the individual Clock, Reset and Preset product terms. Macrocells with both the Reset and Preset product terms held logic "1" simultaneously will have register-bypass enabled for asynchronous operation. Selection of the registered operating mode is accomplished by not allowing both the Reset & Preset product terms to be logic "1" simultaneously. Preset and Reset affect the register on the rising edge of a logic "1" level of the appropriate product term. Similarly, the data is clocked into the register on the rising edge of the Clock product term. The GAL20RA10 has a common register preload function controlled by the PL pin.

OUTPUT POLARITY

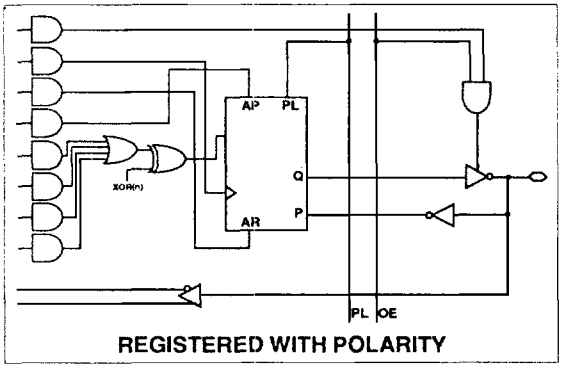
The output polarity can be individually programmed to be true or inverting without any performance degradation, in either combinational or registered mode. This allows the user to reduce the overall number of product terms required in a design and to invert the output signal.

NOTE: Output polarity selection does NOT affect the behavior of the OLMC's integral "D" flip-flop. The AR and AP product terms will force the flip-flop to Reset/Preset regardless of the polarity of the output.

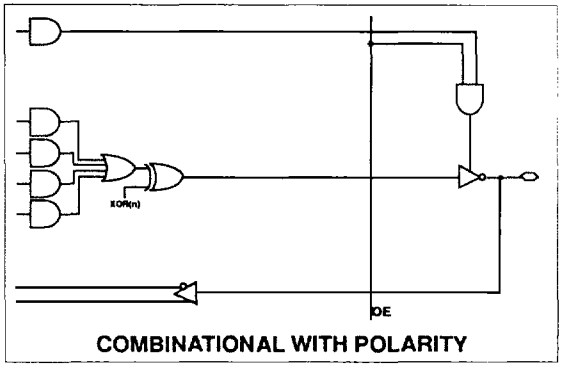


GAL20RA10 OUTPUT LOGIC MACROCELL (OLMC)

OUTPUT LOGIC MACROCELL CONFIGURATIONS



REGISTERED WITH POLARITY



COMBINATIONAL WITH POLARITY

RESET/PRESET FUNCTIONALITY

The AR and AP product terms are sensed on the rising edge. In addition, these pins control the selection of registered or combinational operating mode.

RESET	PRESET	FUNCTION
0	0	Registered function of data product terms
↑	0	Reset register to "0" (device pin = "1")
0	↑	Preset register to "1" (device pin = "0")
0	↑	Register-bypass (combinational output)

ELECTRONIC SIGNATURE

An electronic signature (ES) is provided with every GAL®20RA10 device. It contains 80 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

SECURITY CELL

A security cell is provided with every GAL®20RA10 device as a deterrent to unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the AND array. This cell can be erased only during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

BULK ERASE MODE

Before writing a new pattern into a previously programmed part, the old pattern must first be erased. This erasure is done automatically by the programming hardware as part of the programming cycle and takes only 50 milliseconds.

ASYNCRHONOUS CLOCK

A separate clock control product term is provided for each GAL20RA10 macrocell. The data is clocked into the register on the rising edge of the clock product term. The use of individual clock control product terms allows up to ten seperate clocks or clock pins for a highly asynchrounous system, or through the use of a common AND function driving several clock product terms groups of registers can be clocked together.

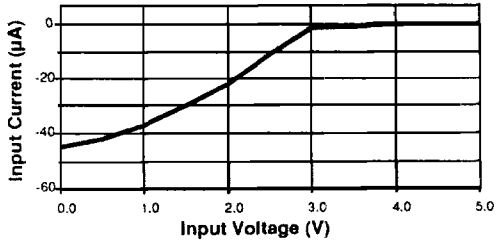
LATCH-UP PROTECTION

GAL®20RA10 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullup instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

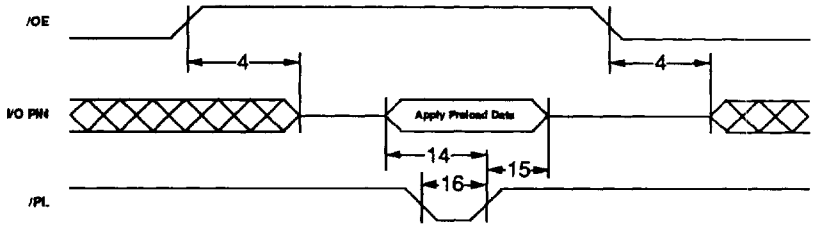
INPUT BUFFERS

GAL®20RA10 devices are designed with TTL level compatible input buffers. These buffers, with their characteristically high impedance, load driving logic much less than traditional bipolar logic.

The buffers also possess active pull-ups within their input structure. As a result, unused inputs and I/O's will float to a TTL "high" (logical "1"), however, Lattice recommends that all unused inputs and tri-stated I/O pins be connected to an adjacent active input, V_{CC}, or GND. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.



REGISTER PRELOAD



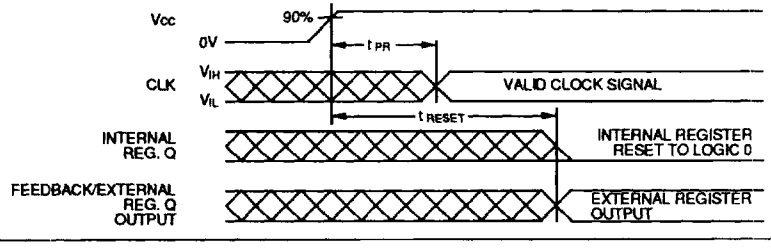
Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	MIN.	MAX.	UNITS
$t_{en/dis}$	4	/OE ↑	O	Pin 13 to Output Enable/Disable	—	*	ns
t_{sup}	14	I/O	/PL ↑	Setup Time, Apply Preload Data before /PL↑	15	—	ns
t_{hp}	15	/PL ↑	no data	Hold Time, after /PL ↑	—	15	ns
t_{wp}	16	/PL ↓	/PL ↑	Preload Pulse Duration	—	15	ns

* Refer to **Switching Characteristics Table**.

The registers of the GAL20RA10 can be preloaded from the I/O pins to facilitate board-level (TTL-level) control for initialization and testing of state machine designs. This capability can be used to force the device into a particular state without lengthy sequencing operations. Non-valid (illegal) states for a given design can also be entered to assure that the state machine recovers properly. This function is used by qualified device programmers to apply test vector sequences during functional testing.

POWER-UP RESET



Circuitry within the GAL20RA10 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{RESET}, 45µs MAX). This feature can greatly simplify state machine design by providing a known state on power-up.

The timing diagram for power-up is shown above. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL20RA10. First, the V_{CC} rise must be monotonic. Second, the clock input must become a proper TTL level within the specified time (t_{PR}, 100ns MAX). The registers will reset within a maximum of t_{RESET} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met.