Datasheet, V1.0, 10 Sep 2001

PFC-CoolSET

ICE1PD265G

IC for High Power Factor
and Low THD

Power Management & Supply

Never stop thinking.

Revision History:	**2001-09-10**	Datasheet
Previous Version:	v1.0	

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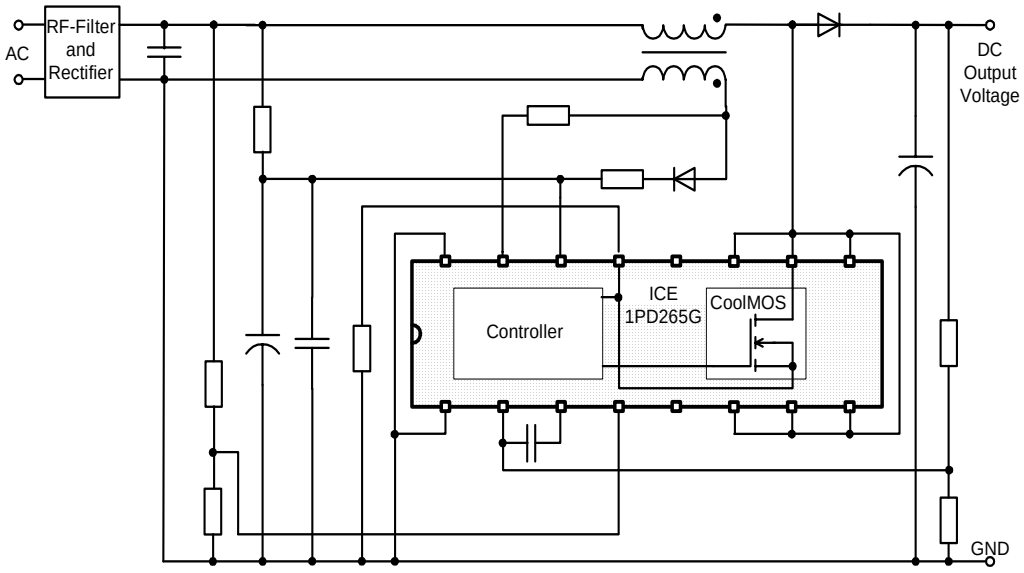
Power Factor Controller + CoolMOS: BoostSET
IC for High Power Factor and low THD

- IC for sinusoidal line-current consumption
- Controller and CoolMOS within one package
- P-DSO-16-10
- Power factor achieves nearly 1
- Controls boost converter as active harmonic filter for low THD
- Start up with very low current consumption
- Zero current detector for discontinuous operation mode
- Output overvoltage protection
- Output undervoltage lockout
- Internal start up timer
- Totem pole output with active shut down
- Internal leading edge blanking LEB
- Very low comparator and multiplier offsets for universal input applications
- High sophisticated amplifier minimizes distortion inteferences caused by MOSFET switching

The ICE1PD265G IC controls a boost converter in a way that sinusoidal current is taken from the single phase line supply and stabilized DC voltage is available at the output. CoolMOS and controller are placed together in one package.

This active harmonic filter limits the harmonic currents resulting from the capacitor pulsed charge currents during rectification. The power factor which descibes the ratio between active and apparent power is almost one. Line voltage fluctuations can be compensated very efficiently

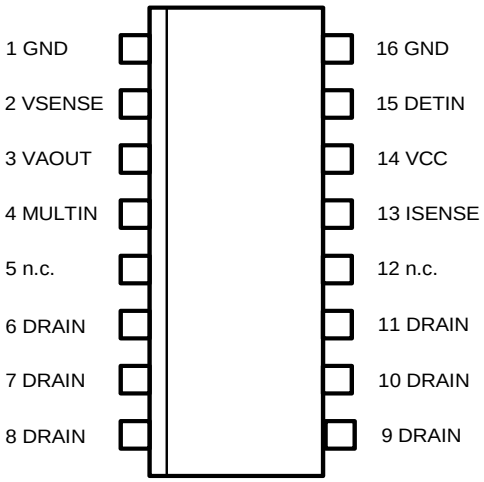


Type	Ordering Code	Package
ICE1PD265G		P-DSO-16-10

Pin Connections

Pin	Symbol	Function
1	GND	Ground
2	VSENSE	Voltage amplifier inverting input
3	VAOUT	Voltage amplifier output
4	MULTIN	Multiplier input
5	n.c.	
6	DRAIN	650V Drain
7	DRAIN	650V Drain
8	DRAIN	650V Drain
9	DRAIN	650V Drain
10	DRAIN	650V Drain
11	DRAIN	650V Drain
12	n.c.	
13	ISENSE	Current sense input + Source
14	VCC	Positive voltage supply
15	DETIN	Zero current detector input
16	GND	Ground

P-DSO-16-10



Do not touch DRAIN pins on application board: 650V

Pin Description

Pin1,16 GND (Ground)
The GND pins are internally connected via the lead frame

Pin 2 VSENSE (voltage amplifier inverting input)
VSENSE is connected via a resistive divider to the boost converter output. With a capacitor connected to VAOUT the internal error amplifier acts as an integrator.

Pin 3 VAOUT (voltage amplifier output)
VAOUT is connected internally to the first multiplier input. To prevent overshoot the input voltage is clamped internally at 5V. Input voltage less then 2.2V shuts the gate driver down. If the current flowing into this pin is exceeding an internal threshold the multiplier output voltage is reduced to prevent the MOSFET from overvoltage damage.

Pin 4 MULTIN (multipier input)
MULTIN is the second multiplier input and is connected via a resistive divider to the rectifier output voltage.

Pin 5, 12
not connected

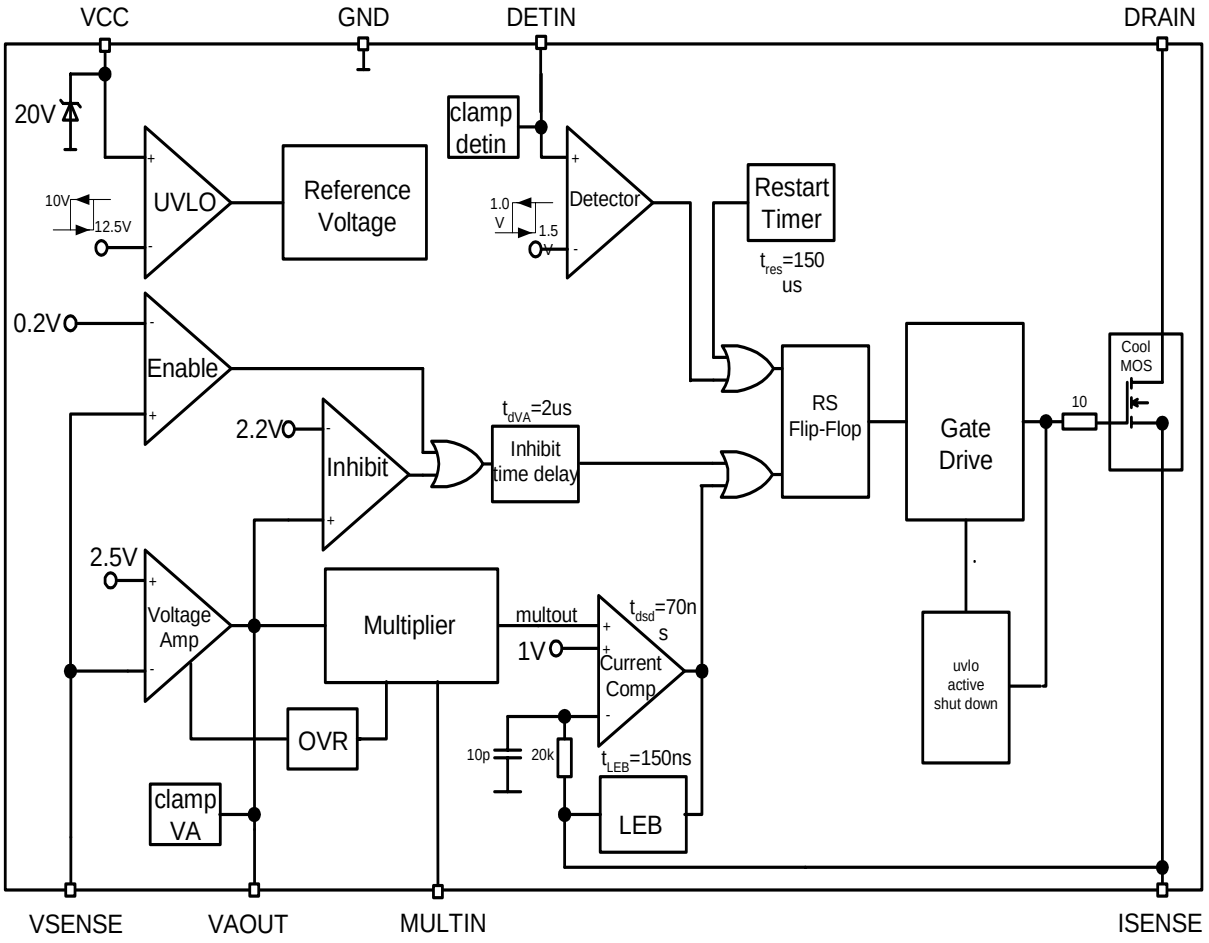
Pin 6,7,8,9,10,11 DRAIN (drain connection of internal CoolMOS)
The DRAIN pins are internally connected via the leadframe. Be aware of 650V input voltage!

Pin 13 ISENSE (current sense input and CoolMOS source)
Controller current sense input and CoolMOS source are internaly connected via bonds.
ISENSE should be connected to an external sense resistor controlling the CoolMOS source current. The input is internally clamped at -0.3V to prevent negative input voltage interaction. A leading edge blanking circuitry suppresses voltage spiks when turning the MOSFET on.

Pin 14 Vcc (Positive voltage supply)
If Vcc exceeds the turn-on threshold the IC is switched on. When Vcc falls below the turn-off threshold it is switched off and power consumption is very low. An auxilliary winding is charging a capacitor which provides the supply current. A second 100nF ceramic capacitor should be added to Vcc to absorbe supply current spikes required to charge the MOSFET gate capacitance.

Pin 15 DETIN (Zero current detector input)
DETIN is connected to an auxiliary winding monitoring the zero crossing of the inductor current.

Block Diagram



Functional Description

Introduction

Conventional electronic ballasts and switching power supplies are designed with a bridge rectifier and a bulk capacitor. Their disadvantage is that the circuit draws power from the line when the instantaneous AC voltage exceeds the capacitors voltage. This occurs near the line voltage peak and causes a high charge current spike with following characteristics: The apparent power is higher than the real power that means low power factor condition, the current spikes are non sinusoidal with a high content of harmonics causing line noise, the rectified voltage depends on load condition and requires a large bulk capacitor, special efforts in noise suppression are necessary.

With the ICE1PD265G preconverter a sinusoidal current is achieved which varies in direct instantaneous proportional to the input voltage half sine wave and so provides a power factor near 1. This is due to the appearence of almost any complex load like a resistive one at the AC line. The harmonic distortions are reduced and comply with the IEC555 standard requirements.

IC Description

The ICE1PD265G contains a wide bandwidth voltage amplifier used in a feedback loop, an overvoltage regulator, an one quadrant multiplier with a wide linear operating range, a current sense comparator, a zero current detector, a PWM and logic circuitry, a totem-pole MOSFET driver, an internal trimmed voltage reference, a restart timer, an undervoltage lockout circuitry and last not least a CoolMOS transistor.

Voltage Amplifier

With an external capacitor between VSENSE and VAOUT the voltage amplifier forms an integrator. The integrator monitors the average output voltage over several line cycles. Typically the integrators bandwidth is set below 20 Hz in order to suppress the 100 Hz ripple of the rectified line voltage. The voltage amplifier is internally compensated and has a gain bandwidth of 3 MHz and a phase margin of 80 degrees. The non-inverting input is biased internally at 2.5V. The output is directly connected to the multiplier input.

The gate drive is disabled when VSENSE voltage is less than 0.2 V or VAOUT voltage is less than 2.2 V.

If the MOSFET is placed nearby the controller switching inteferences have to be taken into account. The output of the voltage amplifier is designed in a way to minimize these inteferences.

Overvoltage Regulator

Because of the integrators low bandwidth fast changes of the output voltage can’t be regulated whithin an adequate time. Fast output changes occure during initial start-up, sudden load removal, or output arcing. While the integrators differential input voltage remains zero during this fast changes a peak current is flowing through the external capacitor into pin VAOUT. If this current exceeds an internal defined margin the overvoltage regulator circuitry reduces the multiplier output voltage. As a result the on time of the MOSFET is reduced.

Multiplier

The one quadrant multiplier regulates the gate driver with respect of the DC output voltage and the AC half wave rectified input voltage. Both inputs are designed to achieve good linearity over a wide dynamic range to represent an AC line free from distortion. Special efforts are made to assure universal line applications with respect to a 90 to 270 V AC range.

The multiplier output is internally clamped at 1.0V. So the MOSFET is protected against critical operating during start up.

Current sense comparator, LEB and RS Flip-Flop

An external sense resistor transferes the source current of the MOSFET into a sense voltage.The multiplier output voltage is compared with this sense voltage.

To protect the current comparator input from negative pulses a current source is inserted which sends current out of the ISENSE pin every time when ISENSE is falling below ground potential. The switch-on current peak of the MOSFET is blanked out via a resistor-capacitor circuit with a blanking time of typically 220ns. Therefore better THD is achieved at low load conditions.

The RS Flip-Flop ensures that only one single switch-on and switch-off pulse appears at the gate drive output during a given cycle (double pulse suppression).

Zero Current Detector

The zero current detector senses the inductor current via an auxiliary winding and ensures that the next on-time of the MOSFET is initiated immediately when the inductor current has reached zero. This diminishes the revers recovery losses of the boost converter diode. The MOSFET is switched off when the voltage drop of the shunt resistor reaches the voltage level of the multipler output. So the boost current waveform has a triangular shape and there are no deadtime gaps between the cycles. This leads to a continuous AC line current limiting the peak current to twice of the average current.

To prevent false tripping the zero current detector is designed as a Schmitt-Trigger with a hysteresis of 0.5V. An internal 5V clamp protects the input from overvoltage breadkdown, a 0.6V clamp prevents substrate injection. An external resistor has to be used in series with the auxiliary winding to limit the current through the clamps.

Restart Timer

If the MOS is off for more than 150us a restart impulse is generated by the restart timer.

Undervoltage Lockout

An undervoltage lockout circuitry switches the IC on when Vcc reaches the upper threshold V_{CCH} and switches the IC off when Vcc is falling below the lower threshold V_{CCL}. During start up the supply current is less then 100uA.

An internal voltage clamp has been added to protect the IC from Vcc overvoltage condition. When using this clamp special care must be taken on power dissipation.

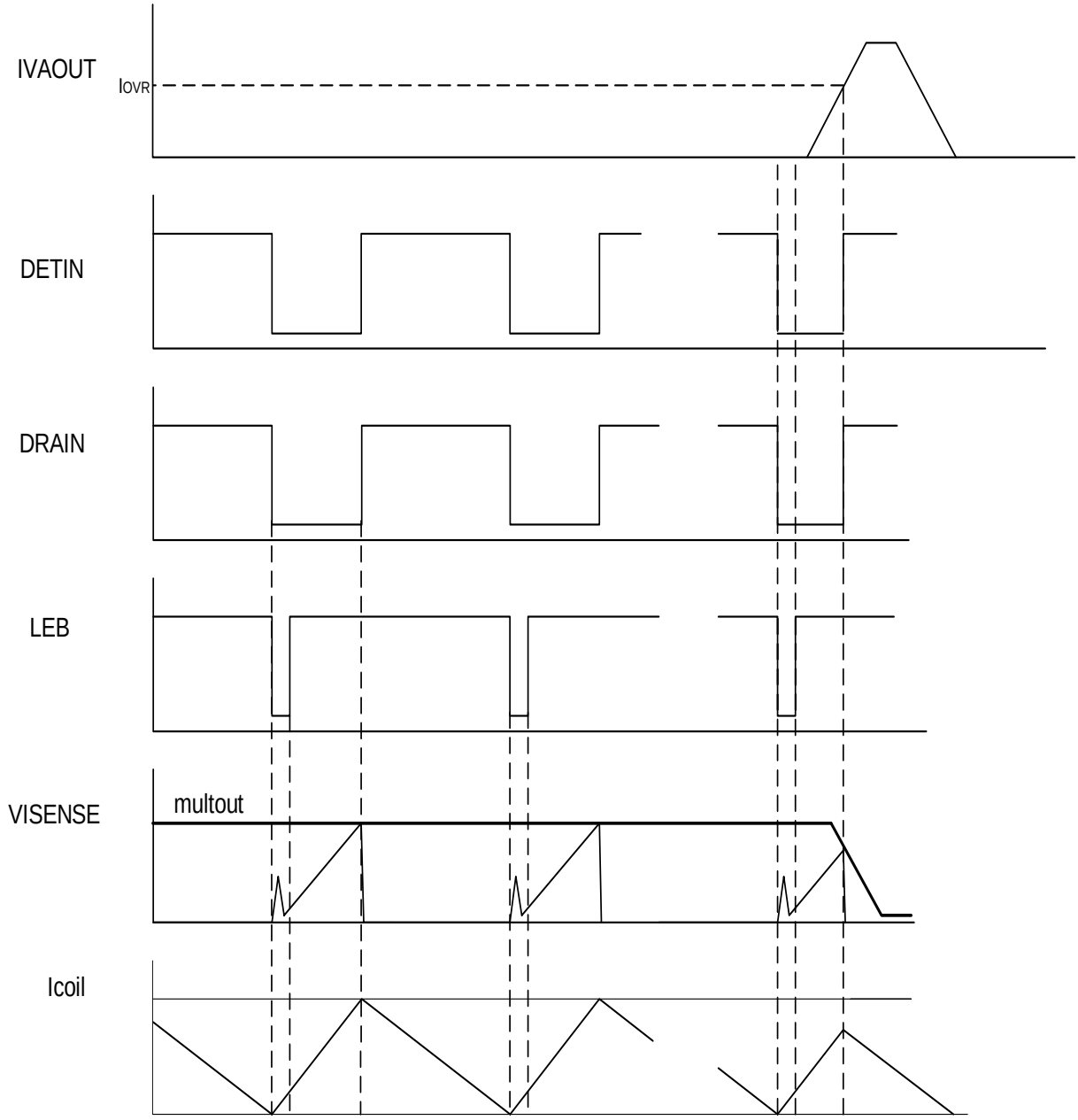
Start up current is provided by an external start up resistor which is connected from the AC line to the input supply voltage Vcc and a storage capacitor which is connected from Vcc to ground. Be aware that this capacitor is discharged befor the IC is plugged into the application board. Otherwise the IC can be destroyed due to the high capacitor voltage.

Bootstrap power supply is created with the previous mentioned auxiliary winding and a diode (see application circuit).

CoolMOS

The CoolMOS is designed for very low R_{DSon} to reduce power dissipation.

Signal Diagrams



Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit	Remark
Supply + Zener Current	Icc+Iz	-	20	mA	
Supply Voltage	V_{CC}	-0.3	Vz	V	Vz=Zener Voltage Icc+Iz=20mA
Voltage at Pin 2,4,13		-0.3	6.5	V	
Current into Pin 3	I_{VAOUT}	 -10	30	mA mA	VAOUT=4V,VSENSE=2.8V VAOUT=0V,VSENSE=2.3V t<1ms
Current into Pin 15	I_{DETIN}	 -10	10	mA mA	DETIN > 6V DETIN< 0.4V
Voltage at Pin 6- 11	V_{DRAIN}		650		T_J=115°C
Continuous Drain Current	I_D		3.2 2	A A	T_C=25°C T_C=100°C
Avalanche Energy	E_{Ar}		0.2	mJ	repetitive
ESD Protection			2000	V	MIL STD 883C method 3015.6, 100pF,1500Ω
Storage Temperature	T_{stg}	-50	150	°C	
Operating Junction Temperature	T_J	-25	150	°C	
Thermal Resistance Junction-Ambient	R_{thJA}		120	K/W	P-DSO-16-10

Characteristics

Unless otherwise stated, -40°C<T_j <150 °C, V_{CC} = 14.5V

Parameter	Symbol	min.	typ.	max.	Unit	Test Condition
Start-Up circuit						
Zener Voltage	Vz	18	20	22	V	Icc+Iz=18mA
Start-up supply current	I_{CCL}		20	100	uA	Vcc=10V
Operating supply current	I_{CCH}		4	6	mA	Output low
Vcc Turn-ON threshold	$V_{CC\ ON}$	12	12.5	13	V	
Vcc Turn-OFF threshold	$V_{CC\ OFF}$	9.5	10	10.5	V	
Vcc Hysteresis	V_{CCHY}		2.5			
Voltage Amplifier						
Voltage feedback Input Threshold	V_{FB}	2.45	2.5	2.55	V	Pin1 connected with Pin2
Line regulation	V_{FBLR}		2	5	mV	V_{CC}=12V to 16V
Open Loop Voltage Gain[1])	G_V		100		dB	
Unity Gain Bandwidth[1])	B_W		5		MHz	
Phase Margin[1)]	M		80		Degr	
Bias current VSENSE	$I_{BVSENSE}$	-1.0	-0.3		uA	
Enable Threshold	$V_{VSENSEE}$		0.2		V	
Inhibit Threshold Voltage	V_{VAOUTI}		2.2		V	V_{ISENSE}= -0.1V
Inhibit Time Delay	t_{dVA}		3		us	V_{ISENSE}= -0.1V
Output Current Source	I_{VAOUTH}		-6		mA	VAOUT=0V VSENSE=2.3V,t<1ms
Output Current Sink	I_{VAOUTL}		30		mA	VAOUT=4V VSENSE=2.8V, t<1ms
Upper Clamp Voltage	V_{VAOUTH}		5.4		V	VSENSE=2.3V, I= -0.2mA
Lower Clamp Voltage	V_{VAOUTL}		1.1		V	VSENSE=2.8V, I=0.5mA
Overvoltage Regulator						
Threshold Current	I_{OVR}	35	40	45	uA	Tj=25°C
1) not tested, guaranteed by design						

Parameter	Symbol	min.	typ.	max.	Unit	Test Condition
Current Comparator						
Input Bias Current	$I_{BISENSE}$	-1			uA	
Input Offset Voltage	$V_{ISENSEO}$ $V_{ISENSEO}$		150 20		mV mV	V_{MULTIN}=0V, VAOUT=2.4V V_{MULTIN}=0V, VAOUT>2.8V
Max Threshold Voltage	$V_{ISENSEM}$	0.95	1.0	1.05	V	
Threshold at OVR	$V_{ISENOVR}$		0.05		V	I_{OVR}=50uA
Shut Down Delay	t_{dISG}		100		ns	
Leading Edge Blanking	t_{LEB}		220		ns	
Detector						
Upper threshold voltage	V_{DETINU}		1.5		V	
Lower threshold voltage	V_{DETINL}		1		V	
Hysteresis	$V_{DETINHY}$		0.5		V	
Input current	I_{BDETIN}	-1			uA	
Input clamp voltage High state Low state	 $V_{DETINHC}$ $V_{DETINLC}$		 5 0.5			 I_{DETIN}=5mA I_{DETIN}=-5mA
Multiplier						
Input bias current	$I_{BMULTIN}$	-1			uA	
Dynamic voltage range MULTIN	V_{MULTIN}		0 to 4		V	V_{VAOUT}=2.75V
Dynamic voltage range VAOUT	V_{VAOUT}		V_{FB} to V_{FB}+1.5			V_{MULTIN}=1V
Multiplier Gain	K_{low} K_{high}		0.18 0.56		V V	V_{VAOUT}<3V V_{VAOUT}>3.5V
Restart Timer						
restart time	t_{RES}		150		us	

Parameter	Symbol	min.	typ.	max.	Unit	Test Condition
CoolMOS						
Drain source breakdown voltage	V_{BRDSS}	600 650			V V	T_J=25°C T_J=115°C
Drain source on-resist-ance	R_{DSon}		1.1	1.4 3.8	Ohm Ohm	T_j=25°C T_j=150°C
Zero gate voltage drain current	IDSS		0.5	1 70	uA uA	U_{GS}=0V, T_j=25° U_{GS}=0V, T_j=150°
Output capacitance 1)	C_{OSS}		150		pF	V_{DS}=25V, f=1MHz
Rise time Fall time	t_{rise} t_{fall}		30 50		ns ns	
1) not tested, guaranteed by design						

Electrical Diagrams

Diagram 1: Icc versus Vcc

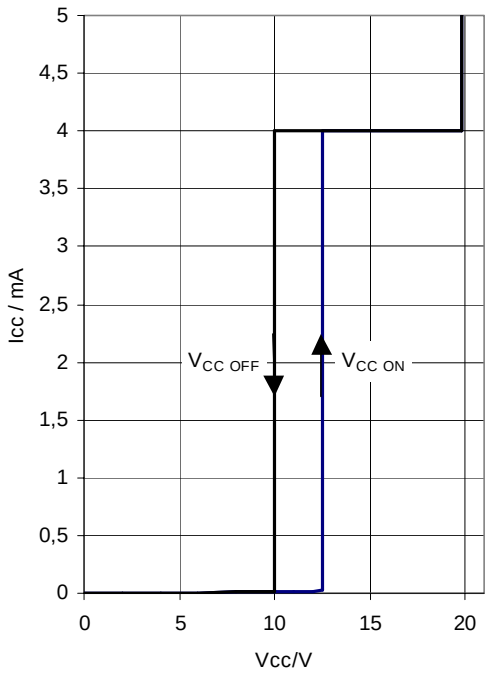


Diagram 2: $V_{CCON/OFF}$ versus Temperature

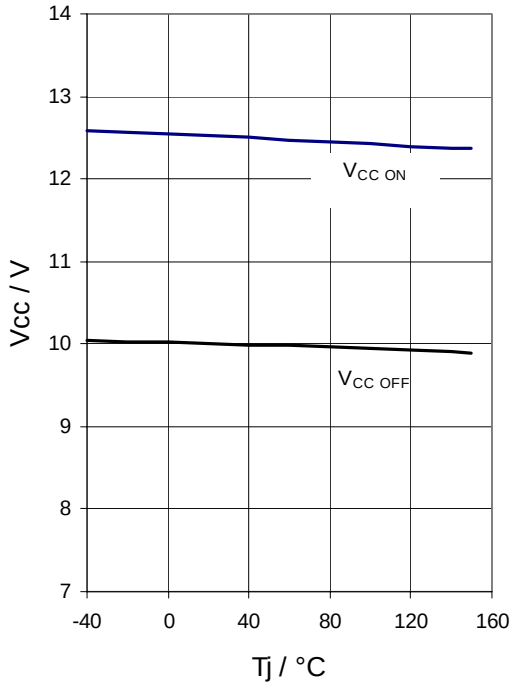


Diagram 3: Iccl versus Vcc

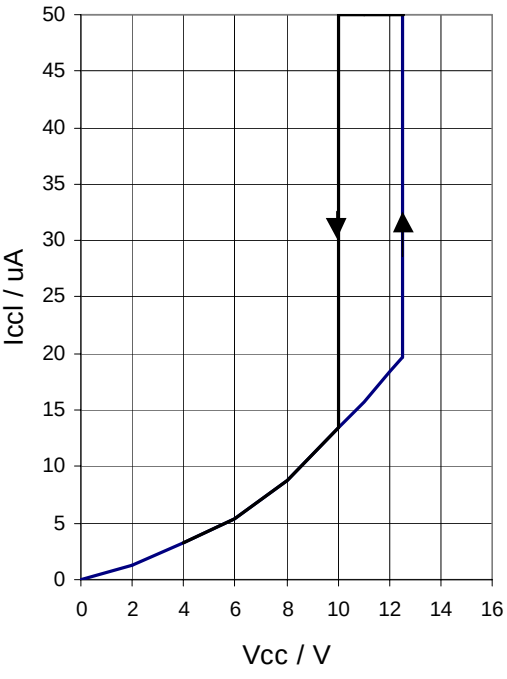


Diagram 4: I_{CCL} versus Temperature, V_{CC}=9V

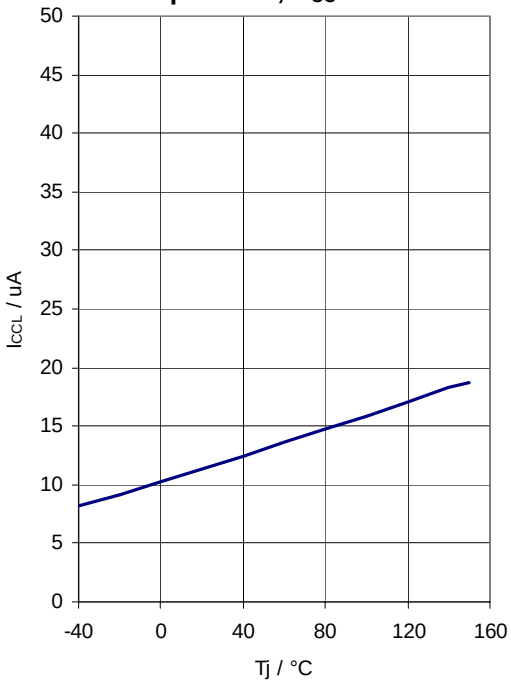


Diagram 5: V_{FB} vers. Temperature
(pin1 connected to pin2)

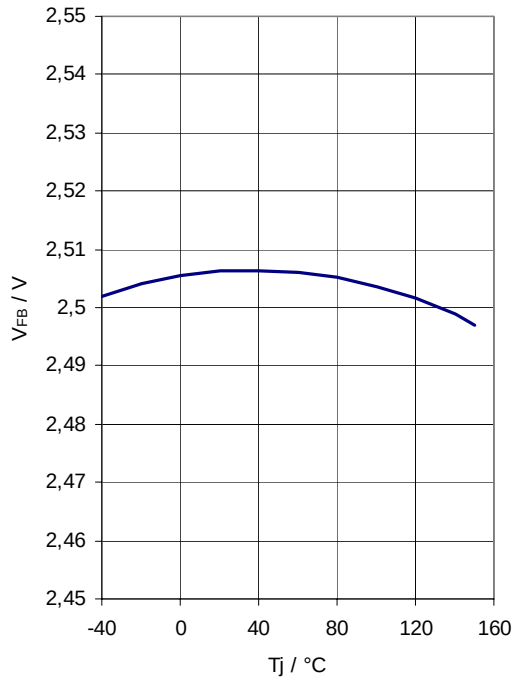


Diagram 6: Voltage Amplifier
Open loop gain and Phase

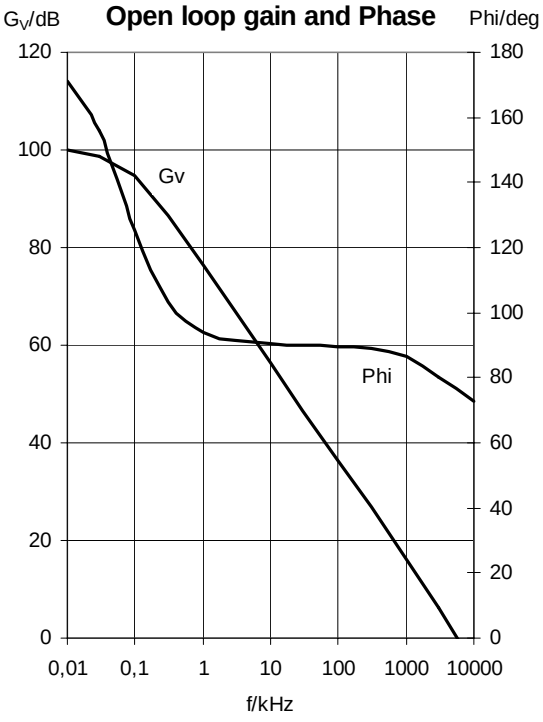


Diagram 7: Overvoltage Regulator
V_{ISENSE} vers. Threshold Voltage

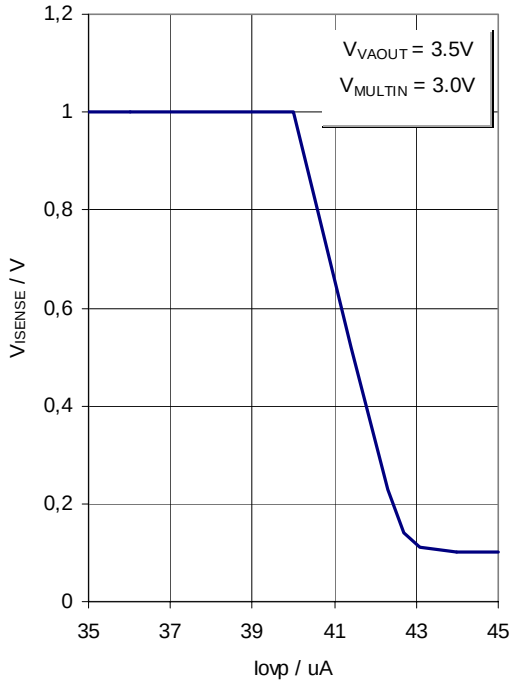


Diagram 8: I_{OVR} versus Temperature

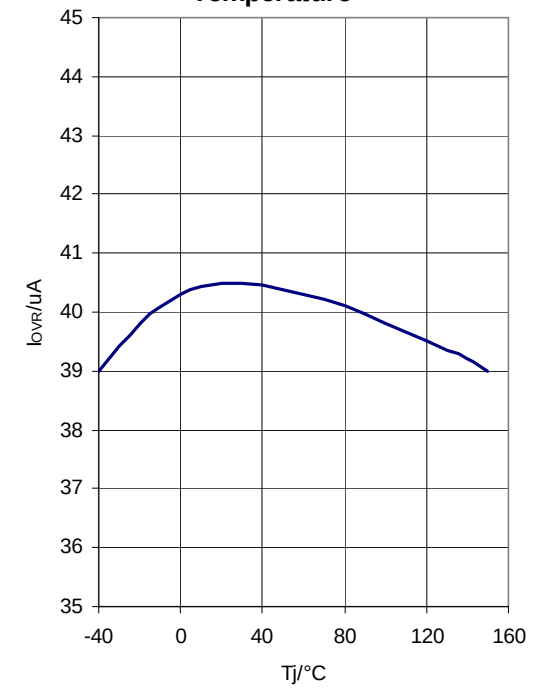


Diagram 9: max Threshold Voltage $V_{ISENSEM}$ vs. Temperature

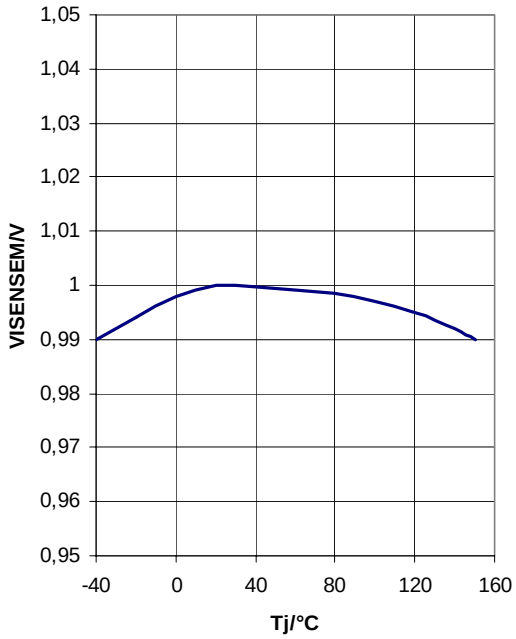


Diagram 10: Leading edge blanking (min on-time) vs. Temp.

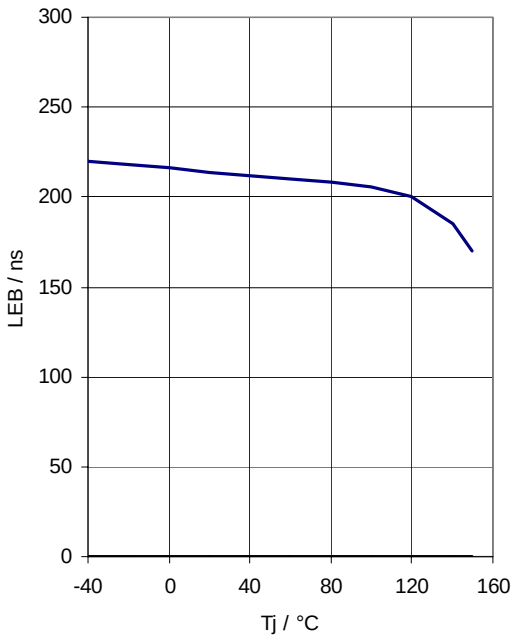


Diagram 11: Current Sense Threshold V_{ISENSE} versus V_{MULTIN}

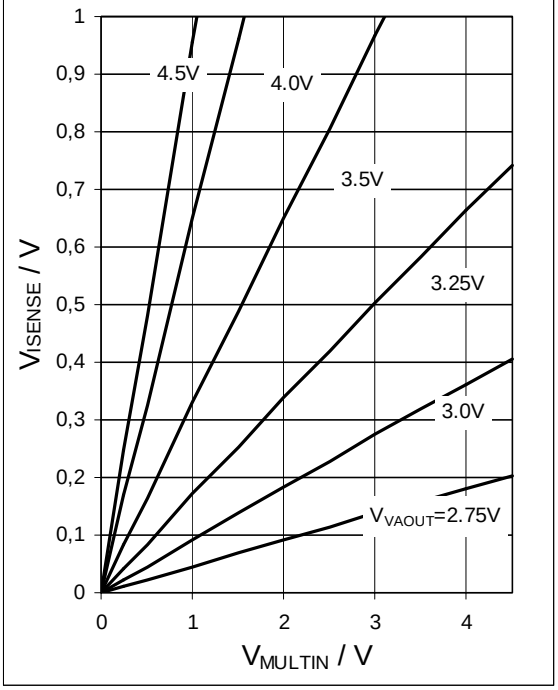


Diagram 12: Current sense threshold V_{ISENSE} versus V_{VAOUT}

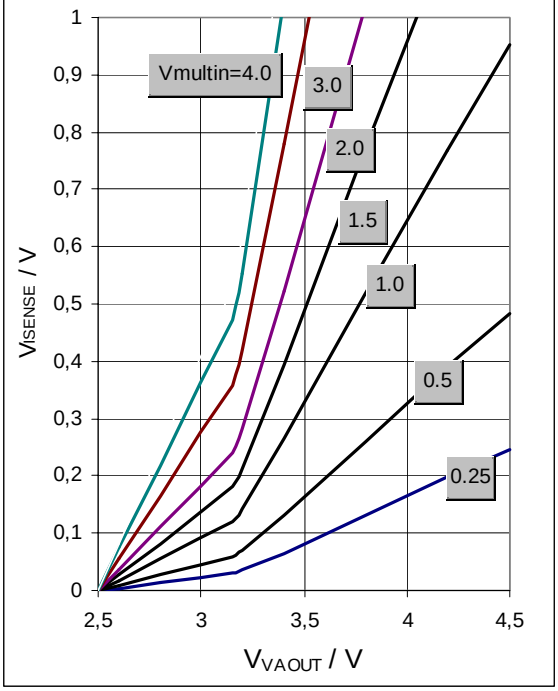


Diagram 13: Restart time versus temperature

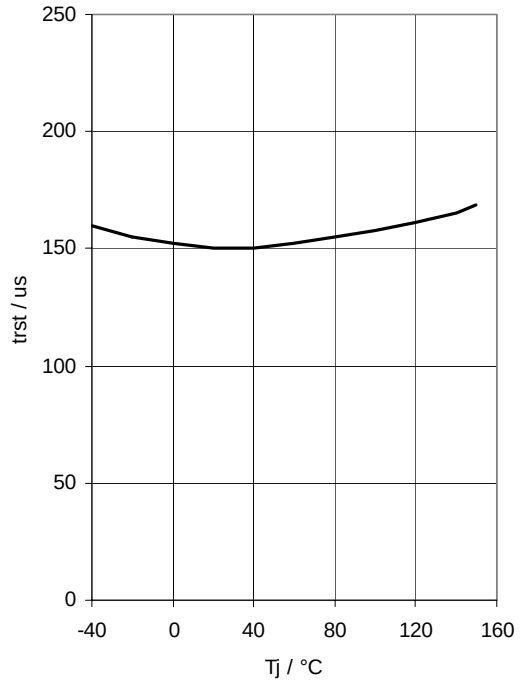


Diagram 14: V_{BRDSS} vs. Temperature

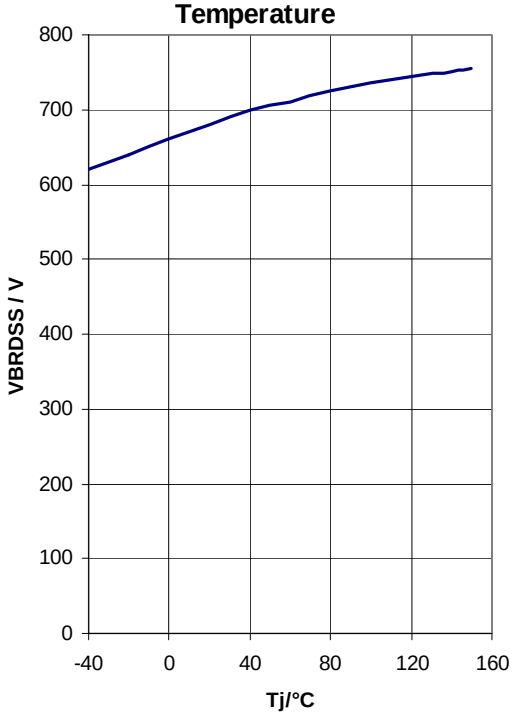
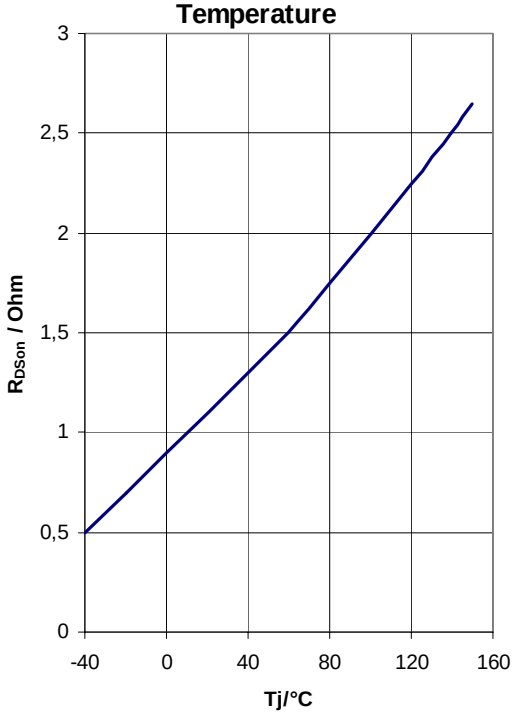
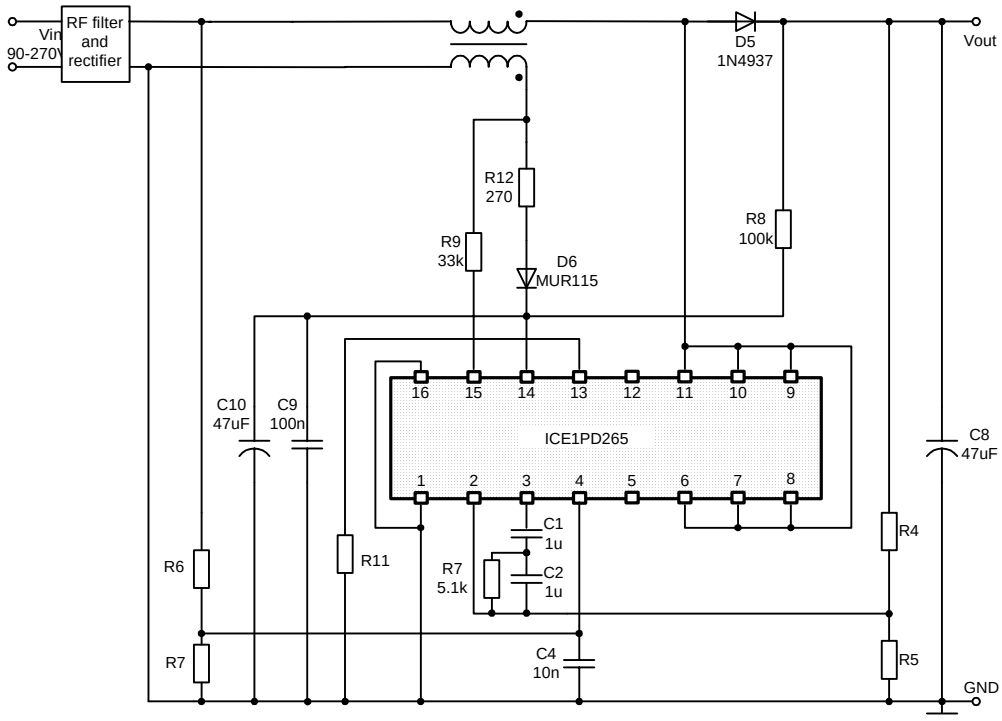


Diagram 15: R_{DSon} vs. Temperature



Application circuit: R_{DSON}=1.1 Ohm
Pout=80W, Vin= 180 - 270V AC
Pout=34W, Vin= 90 - 270 V AC



Total Quality Management

Qualität hat für uns eine umfassende Bedeutung. Wir wollen allen Ihren Ansprüchen in der bestmöglichen Weise gerecht werden. Es geht uns also nicht nur um die Produktqualität – unsere Anstrengungen gelten gleichermaßen der Lieferqualität und Logistik, dem Service und Support sowie allen sonstigen Beratungs- und Betreuungsleistungen.

Dazu gehört eine bestimmte Geisteshaltung unserer Mitarbeiter. Total Quality im Denken und Handeln gegenüber Kollegen, Lieferanten und Ihnen, unserem Kunden. Unsere Leitlinie ist jede Aufgabe mit „Null Fehlern“ zu lösen – in offener Sichtweise auch über den eigenen Arbeitsplatz hinaus – und uns ständig zu verbessern.

Unternehmensweit orientieren wir uns dabei auch an „top“ (Time Optimized Processes), um Ihnen durch größere Schnelligkeit den entscheidenden Wettbewerbsvorsprung zu verschaffen.

Geben Sie uns die Chance, hohe Leistung durch umfassende Qualität zu beweisen.

Wir werden Sie überzeugen.

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Throughout the corporation we also think in terms of Time Optimized Processes (top), greater speed on our part to give you that decisive competitive edge.

Give us the chance to prove the best of performance through the best of quality – you will be convinced.

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