

STB85NF3LL

N-channel 30V - 0.006Ω - 85A - D²PAK Low gate charge STripFET™ II Power MOSFET

General features

Туре	V _{DSS}	R _{DS(on)}	۱ _D
STB85NF3LL	30V	<0.008Ω	85A

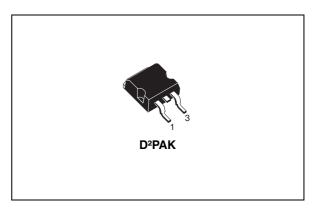
- Optimal R_{DS}(on) x Qg trade-OFF @4.5V
- COnduction losses reduced
- Switching losses reduced

Description

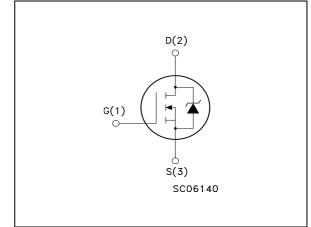
This application specific Power MOSFET is the third genaration of STMicroelectronics unique " Single Feature Size" strip-based process. The resulting transistor shows the best trade-off between on-resistance and gate charge. When used as high and low side in buck regulators, it gives the best performance in terms of both conduction and switching losses. This is extremely important for motherboards where fast switching and high efficiency are of paramount importance.

Applications

Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STB85NF3LLT4	B85NF3LL	D ² PAK	Tape & reel

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Electrical ratings

Table 1.	Absolute	maximum	ratinas
	Absolute	maximum	raunys

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	30	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20K\Omega$)	30	V
V_{GS}	Gate-source voltage	± 16	V
V _{GSM}	Gate-source voltage pulsed (t _p ≤50µs; duty cycle 25%; T _J ≤150°C)	± 20	V
Ι _D	Drain current (continuous) at $T_C = 25^{\circ}C$	85	A
I _D	Drain current (continuous) at $T_C=100^{\circ}C$	60	A
$I_{DM}^{(1)}$	Drain current (pulsed)	340	A
P _{TOT}	Total dissipation at $T_{C} = 25^{\circ}C$	110	W
	Derating factor	0.73	W/°C
T _{stg}	Storage temperature	-65 to 175	°C
ТJ	Max. Operating Junction Temperature	175	°C

1. Pulse width limited by safe operating area

Symbol	Parameter	Value	Unit
R _{thJC}	Thermal resistance junction-case Max	0.36	°C/W
R _{thJA}	Thermal resistance junction-ambient Max	62.5	°C/W
т	Maximum lead temperature for soldering purpose	300	°C

Table 2. Thermal data



2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 250μΑ, V _{GS} = 0	30			V
I _{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	V _{DS} = Max rating, V _{DS} = Max rating @125°C			1 10	μA μA
I _{GSS}	Gate body leakage current (V _{DS} = 0)	$V_{GS} = \pm 16V$			±100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	1			V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10V, I _D = 40A V _{GS} = 4.5V, I _D = 40A		0.006 0.0075	0.008 0.0095	Ω Ω

Table 3. On/off states

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max,}$ $I_D = 40 \text{ A}$		30		S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} =25V, f = 1 MHz, V _{GS} = 0		2210 635 138		pF pF pF
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	V _{DD} =24V, I _D = 60A V _{GS} =4.5V		30 9 12.5	40	nC nC nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%

Table 5.	Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)} t _r t _{d(off)} t _f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 15V, I_D = 30A, R_G =4.7 Ω , V_{GS} =4.5V <i>Figure 12 on page 8</i>		22 130 36.5 36.5		ns ns ns ns
t _{d(off)} t _f t _c	Off-voltage rise time Fall time Cross-over time	Vclamp =24V, I_D =30A R_G = 4.7 Ω , V_{GS} = 4.5V <i>Figure 14 on page 8</i>		32 23 40		ns ns ns

Symbol	Parameter	Test conditions	Min	Тур.	Max	Unit
I _{SD}	Source-drain current				85	А
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)				340	А
V _{SD} ⁽²⁾	Forward on voltage	$I_{SD} = 85A, V_{GS} = 0$			1.3	V
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I _{SD} = 85A, di/dt = 100A/μs, V _{DD} = 15V, T _J = 150°C <i>Figure 14 on page 8</i>		65 105 3.4		ns μC Α

Table 6.Source drain diode

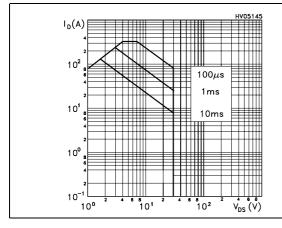
1. Pulse width limited by safe operating area

2. Pulsed: pulse duration=300 μ s, duty cycle 1.5%

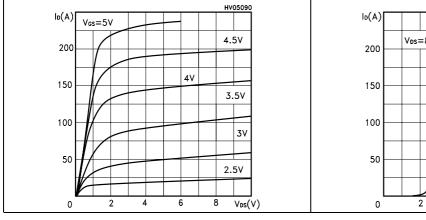


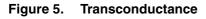
2.1 Electrical characteristics (curves)

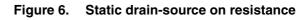
Figure 1. Safe operating area



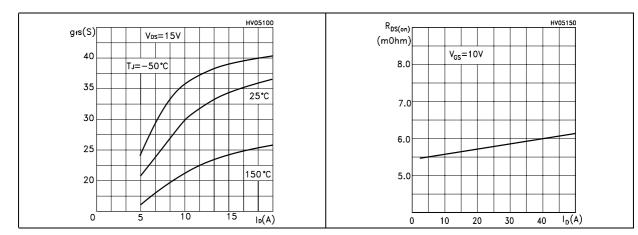


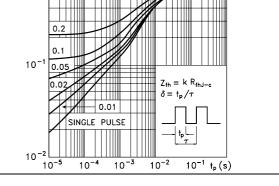






4





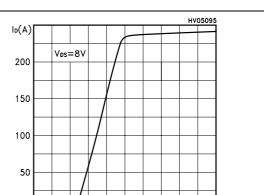
Thermal impedance

Figure 4. Transfer characteristics

Figure 2.

Κ

 $\delta = 0.5$



6

8 V_{GS}(V)

57

Figure 7.

Gate charge vs gate-source voltage Figure 8. Capacitance variations

Figure 9. Normalized gate threshold voltage vs temperature

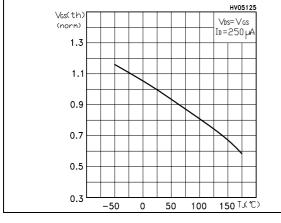
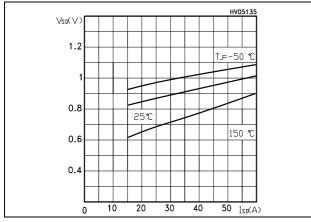


Figure 11. Source-drain diode forward characteristics



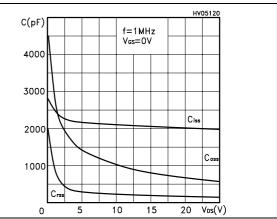
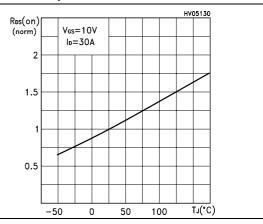


Figure 10. Normalized on resistance vs temperature



3 **Test circuit**

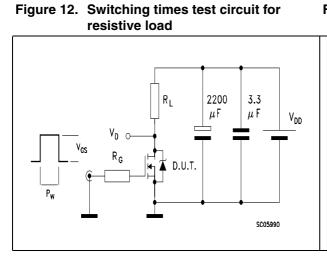
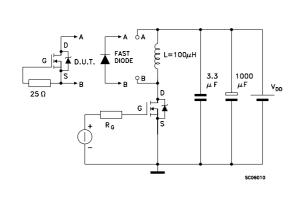


Figure 14. Test circuit for inductive load switching and diode recovery times







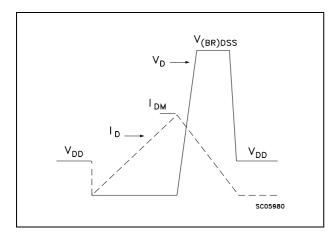
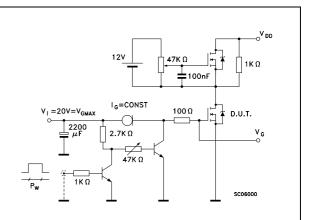
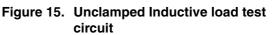
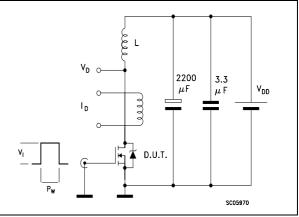


Figure 13. Gate charge test circuit







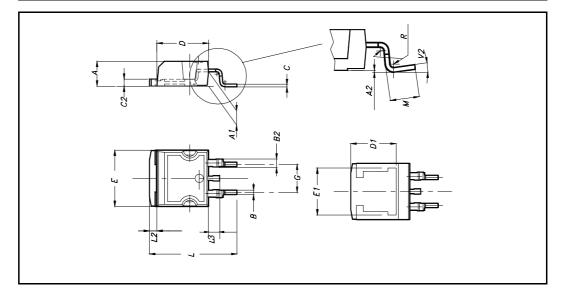
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

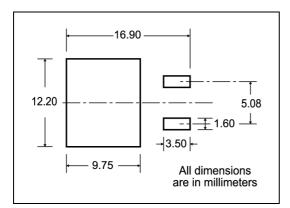


DIM		mm.		inch			
DIM.	MIN.	ТҮР	MAX.	MIN.	TYP.	MAX.	
А	4.4		4.6	0.173		0.181	
A1	2.49		2.69	0.098		0.106	
A2	0.03		0.23	0.001		0.009	
В	0.7		0.93	0.027		0.036	
B2	1.14		1.7	0.044		0.067	
С	0.45		0.6	0.017		0.023	
C2	1.23		1.36	0.048		0.053	
D	8.95		9.35	0.352		0.368	
D1		8			0.315		
Е	10		10.4	0.393			
E1		8.5			0.334		
G	4.88		5.28	0.192		0.208	
L	15		15.85	0.590		0.625	
L2	1.27		1.4	0.050		0.055	
L3	1.4		1.75	0.055		0.068	
М	2.4		3.2	0.094		0.126	
R		0.4			0.015		
V2	0º		4º				

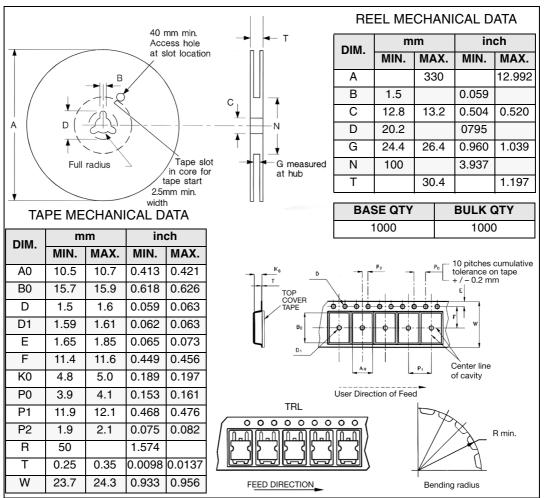
D²PAK MECHANICAL DATA



Packaging mechanical data D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT



* on sales type

6 Revision history

Date	Revision	Changes
09-Sep-2004	3	Complete document
28-Jul-2006	4	New template, SOA updated



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