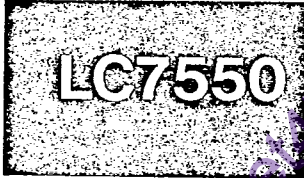


T-74-05-01



3026B

CMOS LSI

# Level Meter with Peak Hold Function

©889B

### Applications

- Peak hold level meter of tape deck
- Peak hold level meter of power amplifier
- General-purpose level meter

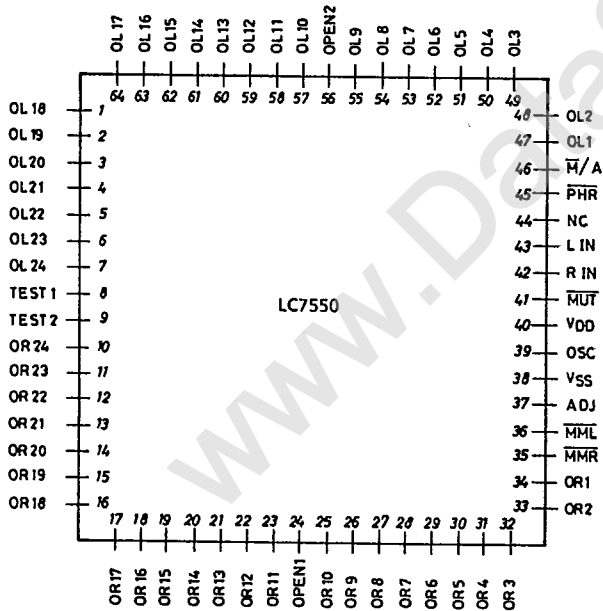
### Features

- CMOS LSI for 2-channel (24 points + 24 points) peak hold level meter
- Capable of driving a static lighting type fluorescent display tube of 23V or less
- Two types of applications are available as follows :
  - a) 2-channel peak hold level meter
  - b) 2-channel level meter

### Functions

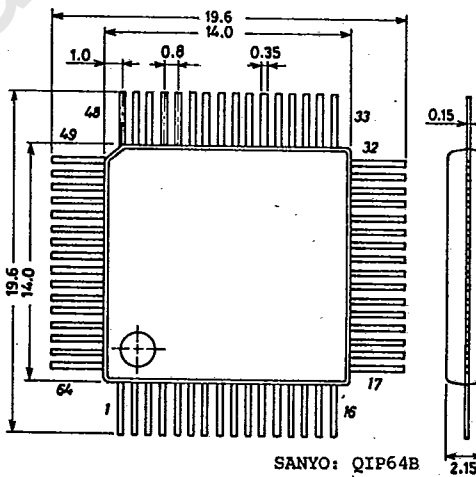
- Peak hold function
  - The peak hold level is indicated by one point lighted.
  - Peak hold comes in 2 types as follows :
    - a) Automatic reset  
Peak hold is reset automatically after lapse of 0.1 to 2 seconds (settable)
    - b) Manual reset  
Peak hold is reset by pushing a reset switch.
- Comparator level : Linear scale
- Input level at full scale : 2.5 to 5V (Adjustable externally)

### Pin Assignment



OPEN pins 1,2/TEST pins 1,2/NC pin : Left open.

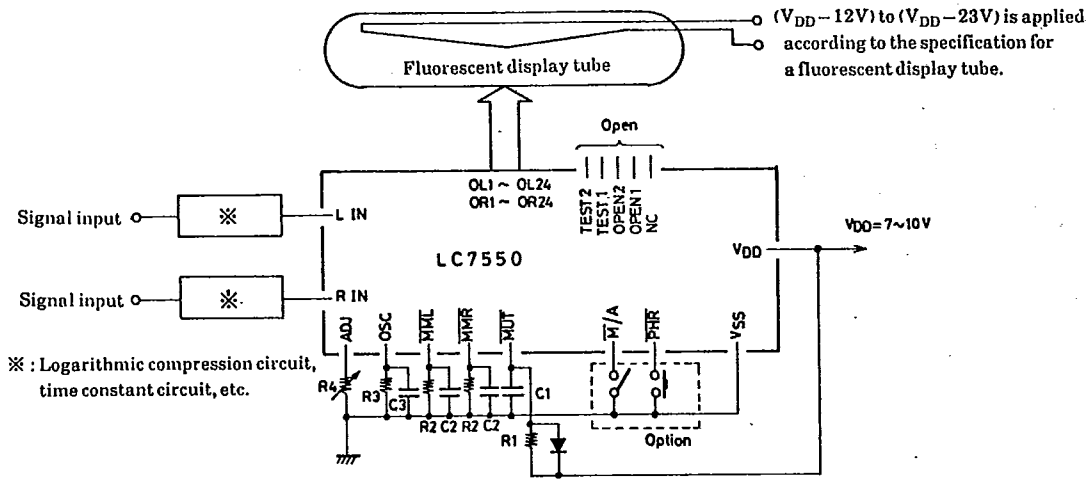
Case Outline 3026B-Q64BIC  
(unit : mm)



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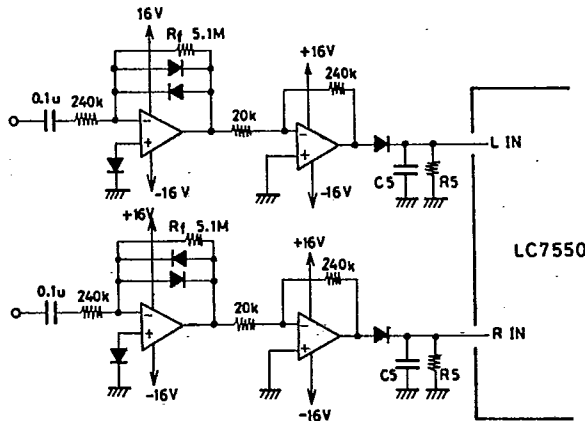
Sample Application Circuit



Reference values of constants

- $(R_1 = 220k\Omega)$  : Values for  $V_{DD}$  rise time of less than 50msec.
- $(C_1 = 0.68\mu F)$
- $(R_2 = 470k\Omega)$  : Values for peak hold time of approximately 1sec.
- $(C_2 = 3.3\mu F)$
- $(R_3 = 56k\Omega)$  : Values for oscillation frequency of approximately 26.7kHz.
- $(C_3 = 1000pF)$  : It is recommended to use a carbon film resistor and a polyester film capacitor so that the variations in frequency with temperature can be minimized.
- $R_4$  : Value to be fixed by referring to the characteristic curve ( $V_{IN\ max} - ADJ$  pin external resistance) shown later.

Example of Logarithmic Compression Circuit and Time Constant Circuit



- OP amp : LA6324
- Diode : DS448
- $(C_5 = 0.33\mu F)$  : time constant to fix decay time
- $(R_5 = 1M\Omega)$

In the Sample Application Circuit, the relation between the input voltage of logarithmic compression circuit and the output voltage of time constant circuit is as shown right. If the full scale input voltage at which up to the 24th point are all lighted is taken as 2.88V and sinusoidal input voltage 295mV is taken as 0dB, the relation between the number of points lighted and the input level becomes as shown below.

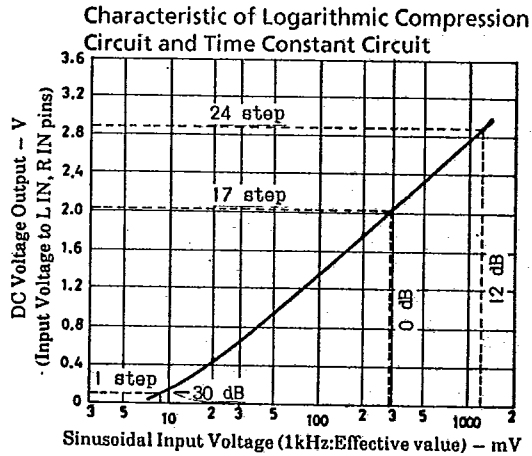
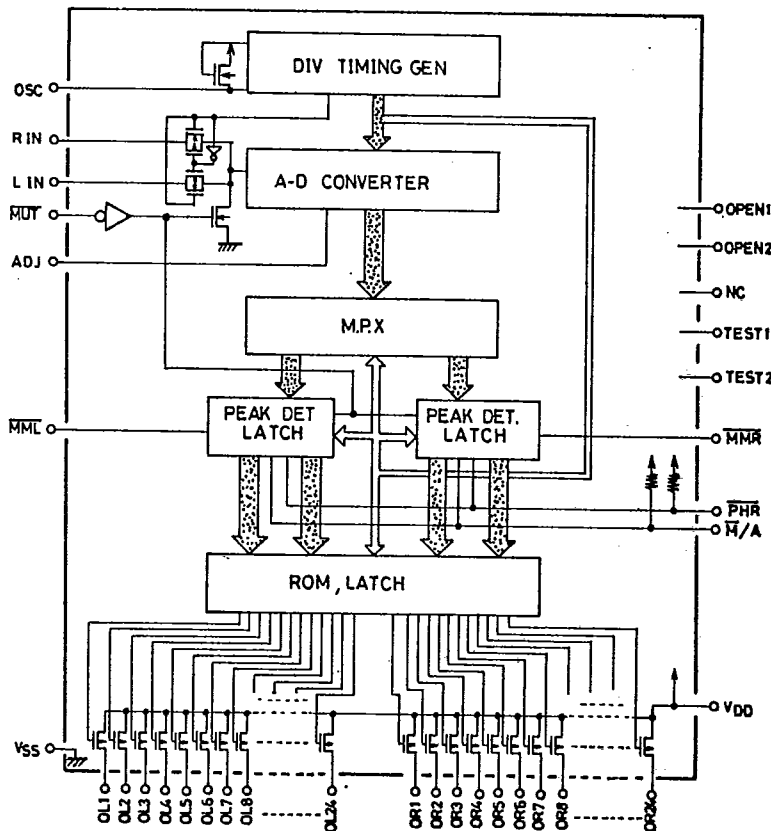


Table 1. Fluorescent Display Tube and Input Level

Number of points lighted	1	2	3	4	5	6	7	8	9	10	11	12
Input level (Approximate value) (dB)	-30	-28	-25	-23	-21	-19	-18	-16	-14	-12	-11	-8
Number of points lighted	13	14	15	16	17	18	19	20	21	22	23	24
Input level (Approximate value) (dB)	-7	-5	-3	-2	0	2	3	5	7	9	10	12

- Note 1. If  $V_{DD}$  is 7.68V, it is seen from the characteristic curve ( $V_{IN\ max}$  - ADJ pin external resistance) that ADJ resistance  $20k\Omega$  causes full scale input voltage 2.88V.
- Note 2. The temperature characteristics and the variations in diode quality, etc. are not considered in this graph.

Equivalent Circuit Block Diagram

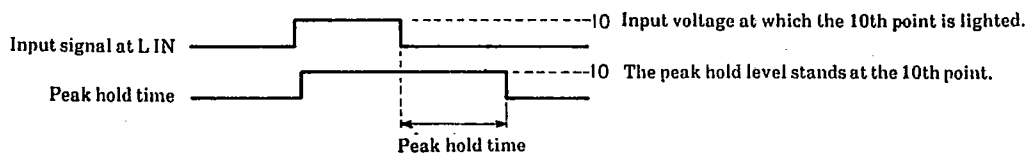


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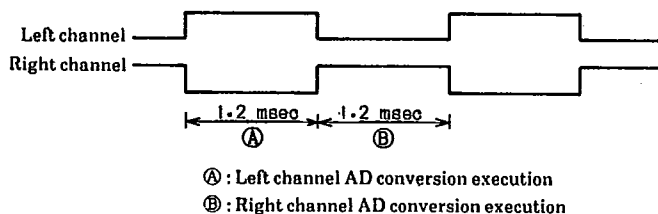
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Pin Description

1. OL<sub>1</sub> to OL<sub>24</sub>, OR<sub>1</sub> to OR<sub>24</sub>
  - Output pins of P channel, open drain type for fluorescent display tube drive.
  - Output withstand voltage (V<sub>DD</sub> - 23V) max
2. L IN, R IN
  - Input pins for display levels of left/right channels
  - The comparator level is of linear scale and if the full scale input voltage (input voltage at which 24 points are all lighted) is taken as 3.6V the number of points lighted will be increased in such a way as 1 point, 2 points, --- each time the voltage is increased by 150mV starting at 0V.
  - The attack, decay circuits to fix the response speed and the logarithmic amplifiers for logarithmic display are connected externally.
3. ADJ
  - Input pin for full scale adjustment
  - The input voltage (full scale input voltage) at which 24 points are all lighted can be adjusted by adjusting external resistor R<sub>4</sub>.
  - The full scale input voltage depends on V<sub>DD</sub>, the internal resistance of LSI, and R<sub>4</sub>.
4. M/A
  - Input pin for controlling changeover of manual/automatic reset of the peak hold point.
  - Automatic reset mode is available when the V<sub>DD</sub> level is applied or the input pins are open; manual reset mode is available when the V<sub>SS</sub> level is applied.
5. PHR
  - Pin for applying the signal to reset the peak hold point at the time of manual reset mode. If the V<sub>SS</sub> level is applied, the peak hold point will be reset.
  - If V<sub>SS</sub> remains applied to the PHR pin at the time of manual reset mode, the ordinary level meter without peak hold function will be result.
6. MML, MMR
  - Pins for externally connecting the time constant circuit of left/right channels to fix the peak hold time at the time of automatic reset mode.



7. MUT
  - Pin for externally connecting the time constant circuit to reset the peak hold function for a specified period of time and also to set the L IN/R IN inputs at the V<sub>SS</sub> level at the time of application of power.
8. OSC
  - Pin for externally connecting C and R to generate control clock inside the LSI.
  - When the oscillation frequency is at 26.6kHz, the L IN/R IN input signals are alternately sampling-processed once in approximately 2.4msec.



9. V<sub>DD</sub>, V<sub>SS</sub>
  - Pins for applying supply voltage

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Operations of Control Pins

Operaiton mode	$\overline{M/A}$	$\overline{PHR}$
With peak hold function		
· Automatic reset of peak hold point	1	×
· Manual reset of peak hold point	0	(1)*
Without peak hold function	0	0

Note) 1 :  $V_{DD}$  level applied or open.  
 0 :  $V_{SS}$  level applied.  
 × : Either  $V_{DD}$  level or  $V_{SS}$  level  
 (1)\* : Normally  $V_{DD}$  level applied or open.  $V_{SS}$  level applied only when resetting.

Absolute Maximum Ratings at  $T_a = 25^\circ\text{C}, V_{SS} = 0\text{V}$

Parameter	Symbol	Conditions	Value	Unit
Supply Voltage	$V_{DD}$		-0.3 to +11	V
Input Voltage	$V_{IN}$	Input/output pins $\overline{OSC}, \overline{MML}, \overline{MMR}, R_{IN}, L_{IN}$ : output OFF	-0.3 to $V_{DD} + 0.3$	V
Output Voltage	$V_{OUT}$	Output OFF, $OL_1$ to $OL_{24}$ , $OR_1$ to $OR_{24}$	$V_{DD} - 23$ to $V_{DD} + 0.3$	V
Allowable Power Dissipation	$P_{d\ max}$	$T_a \leq 70^\circ\text{C}$	230	mW
Allowable Power Dissipation of Segment	$P_{d\ seg}$	$I_O \leq 1.5\text{mA}, OL_1$ to $OL_{24}, OR_1$ to $OR_{24}$	3.5	mW
Operating Temperature	$T_{opg}$		-30 to +70	$^\circ\text{C}$
Storage Temperature	$T_{stg}$		-40 to +125	$^\circ\text{C}$

Allowable Operating Conditions at  $T_a = 25^\circ\text{C}, V_{DD} = 7.0$  to  $10\text{V}, V_{SS} = 0\text{V}$

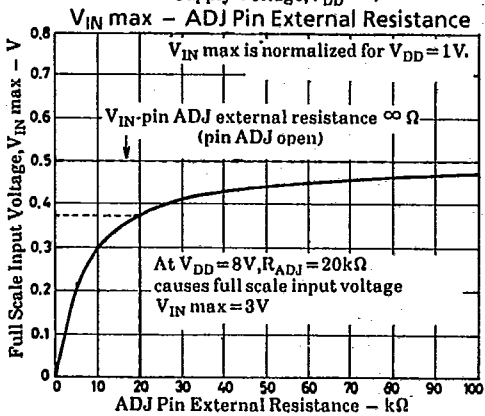
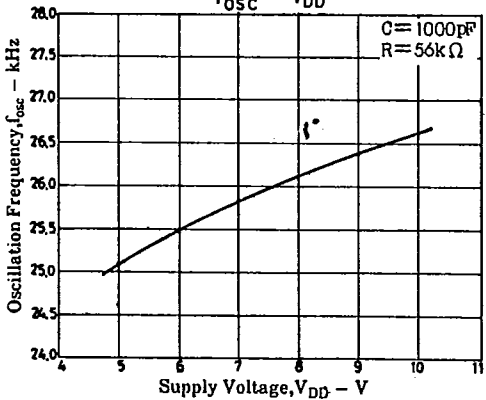
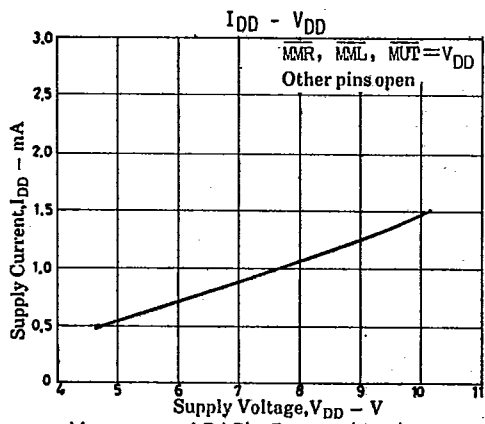
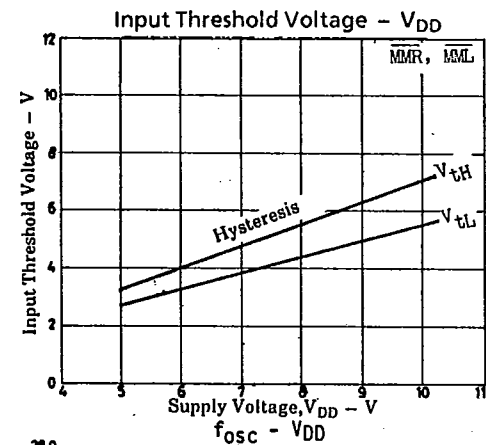
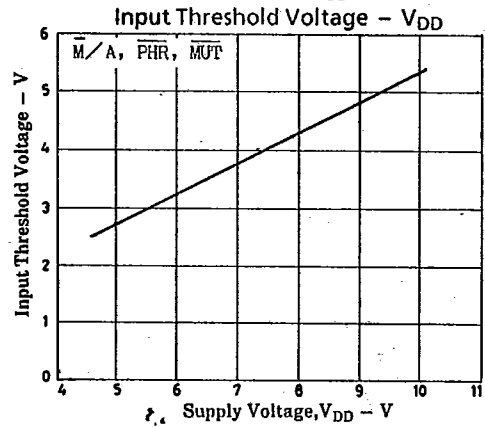
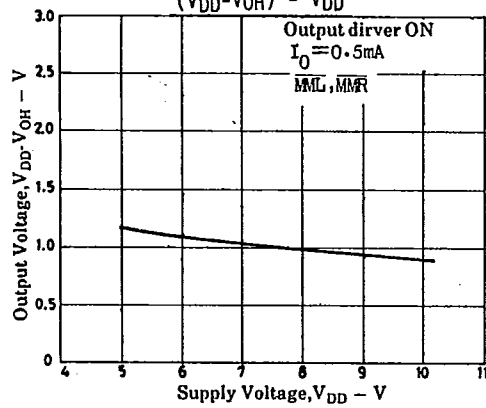
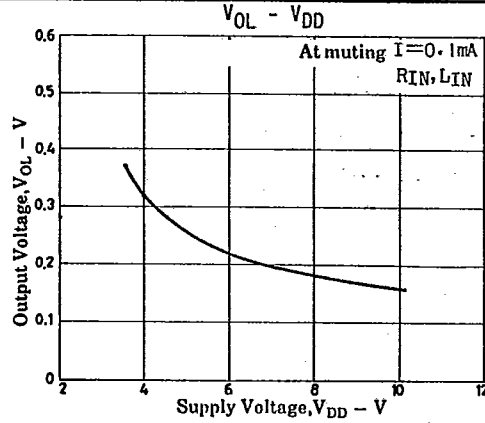
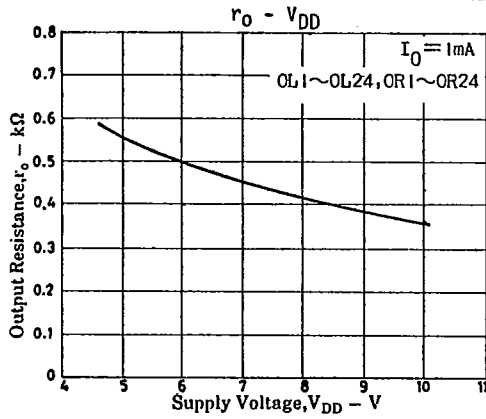
Parameter	Symbol	Conditions	min	typ	max	unit
Supply Voltage	$V_{DD}$		7.0		10.0	V
'H'-Level Input Voltage	$V_{IH(1)}$	$\overline{M/A}, \overline{PHR}$	$V_{DD} - 1.1$		$V_{DD}$	V
'L'-Level Input Voltage	$V_{IL(1)}$	$\overline{M/A}, \overline{PHR}$	0		1.1	V
'H'-Level Input Voltage	$V_{IH(2)}$	$\overline{MUT}$	$0.7V_{DD}$		$V_{DD}$	V
'L'-Level Input Voltage	$V_{IL(2)}$	$\overline{MUT}$	0		$0.3V_{DD}$	V
Input Voltage	$V_{IN}$	$R_{IN}, L_{IN}, V_{IN} \leq V_{DD} - 3\text{V}$	0		5	V

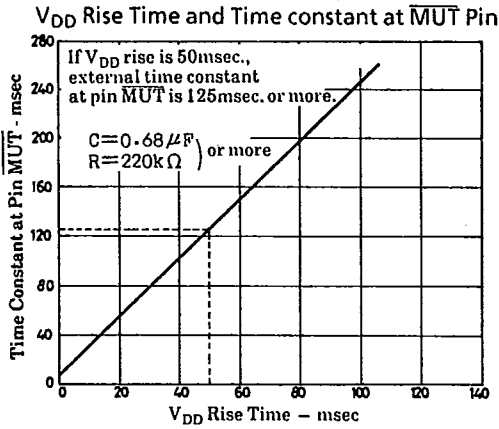
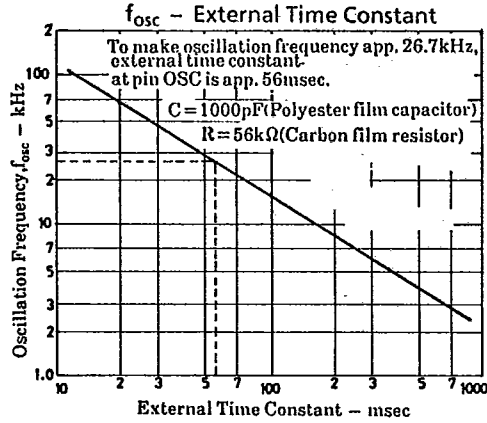
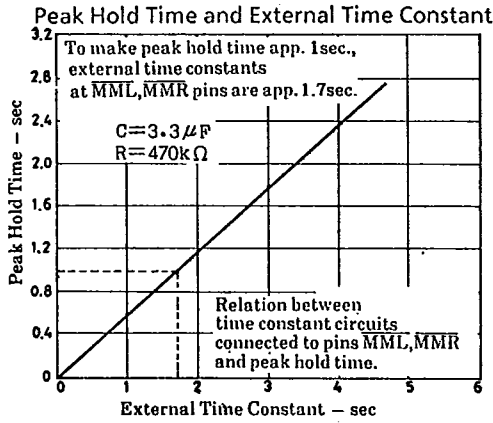
Electrical Characteristics at  $T_a = 25^\circ\text{C}, V_{DD} = 7.0$  to  $10\text{V}, V_{SS} = 0\text{V}$

Parameter	Symbol	Conditions	min	typ	max	unit
Input Current	$I_{IN}$	$\overline{MUT}, V_{IN} = V_{DD}$			3	$\mu\text{A}$
	$I_{IN}$	$\overline{MUT}, V_{IN} = V_{SS}$	-3			$\mu\text{A}$
Input Floating Voltage	$V_{IF}$	$\overline{M/A}, \overline{PHR}$ , input open	$V_{DD} - 0.9$			V
'L'-Level Input Current	$I_{IL(1)}$	$\overline{M/A}, \overline{PHR}, V_{IN} = V_{SS}$	-550		-25	$\mu\text{A}$
'H'-Level Output Voltage	$V_{OH(1)}$	$OL_1$ to $OL_{24}, OR_1$ to $OR_{24}, I_O = 1.5\text{mA}$	$V_{DD} - 2.3$			V
Output OFF Leak Current	$I_{OFF}$	$OL_1$ to $OL_{24}, OR_1$ to $OR_{24}, V_O = V_{DD} - 21\text{V}$	-3			$\mu\text{A}$
Input/Output OFF Leak Current	$I_{I/O(1)}$	$\overline{OSC}, \overline{MML}, \overline{MMR}$ , output OFF			3	$\mu\text{A}$
		$V_{I/O} = V_{DD}$			3	$\mu\text{A}$
		$V_{I/O} = V_{SS}$	-3			$\mu\text{A}$
	$I_{I/O(2)}$	$L_{IN}, R_{IN}, \overline{MUT} = V_{DD}$			3	$\mu\text{A}$
		$V_{I/O} = V_{DD}$			3	$\mu\text{A}$
		$V_{I/O} = V_{SS}$	-3			$\mu\text{A}$
'L'-Level Output Voltage	$V_{OL}$	$L_{IN}, R_{IN}, I_{I/O} = 0.1\text{mA}, \overline{MUT} = V_{SS}$			0.9	V
'H'-Level Output Voltage	$V_{OH(2)}$	$\overline{MML}, \overline{MMR}, I_{I/O} = 0.5\text{mA}$	$V_{DD} - 0.9$			V
Input Offset Voltage	$V_{offset}$	$V_{IN} \leq V_{DD} - 3\text{V}, L_{IN}, R_{IN}, V_{IN} = 0$ to $5\text{V}$	-50		+50	mV
AD Conversion Linear Error		Full scale input voltage = 2.5 to 5V	-1/2		1/2	LSB
Current Dissipation	$I_{DD}$	$f_{osc} = 26.7\text{kHz}, \overline{MUT} = V_{DD}$ , other pins : open			5	mA

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T-90-20

## AUDIO-USE MOS IC CASE OUTLINES

- All of Sanyo audio-use MOS IC case outlines are illustrated below.
- All dimensions are in mm, and dimensions which are not followed by min. or max. are represented by typical values.
- No marking is indicated.

