

Vishay Siliconix

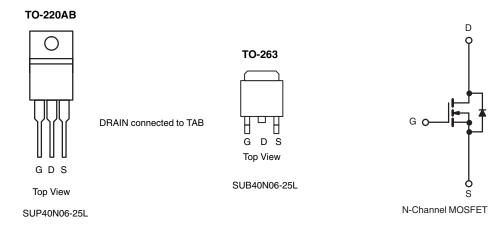
# N-Channel 60-V (D-S), 175 °C MOSFET, Logic Level

PRODUCT SUMMARY			
V <sub>(BR)DSS</sub> (V)	$r_{DS(on)}\left(\Omega\right)$	I <sub>D</sub> (A)	
60	$0.022 \text{ at V}_{GS} = 10 \text{ V}$	40	
	0.025 at V <sub>GS</sub> = 4.5 V	40	

#### **FEATURES**

- TrenchFET<sup>®</sup> Power MOSFETs
- Maximum Junction Temperature: 175 °C Rated





Ordering Information: TO-220AB:

SUP40N06-25L SUP40N06-25L-E3 (Lead (Pb)-free)

TO-263: SUB40N06-25L

SUB40N06-25L-E3 (Lead (Pb)-free)

<b>ABSOLUTE MAXIMUM RAT</b>	<b>INGS</b> $T_C = 25$ °C, unless other	rwise noted			
Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	V <sub>DS</sub>	60	V		
Gate-Source Voltage	$V_{GS}$	± 20	v		
Continuous Drain Current (T <sub>.I</sub> = 175 °C)	T <sub>C</sub> = 25 °C	l <sub>D</sub>	40		
Continuous Diain Current (1 j = 175 C)	T <sub>C</sub> = 100 °C		25		
Pulsed Drain Current	I <sub>DM</sub>	100	A		
Avalanche Current	I <sub>AR</sub>	40			
Repetitive Avalanche Energy <sup>a</sup>	L = 0.1 mH	E <sub>AR</sub>	80	mJ	
Paragraphic attack	T <sub>C</sub> = 25 °C (TO-220AB and TO-263)	В	90 <sup>c</sup>	14/	
Power Dissipation	T <sub>A</sub> = 25 °C (TO-263) <sup>c</sup>	P <sub>D</sub>	3.7	W	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>sta</sub>	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Limit	Unit	
Junction-to-Ambient	PCB Mount (TO-263) <sup>c</sup>	- R <sub>thJA</sub>	40	°C/W	
ounction-to-Ambient	Free Air (TO-220AB)		80		
Junction-to-Case		R <sub>thJC</sub>	1.6		

#### Notes:

- a. Duty cycle  $\leq$  1 %.
- b. See SOA curve for voltage derating.
- c. Surface Mounted on FR4 Board,  $t \le 10$  sec.
- \* Pb containing terminations are not RoHS compliant, exemptions may apply.

# SUP/SUB40N06-25L

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Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	60			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1.0	2.0	3.0	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current		V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V			1	
	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C			50	μΑ
		V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175 °C			150	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	40			Α
Drain-Source On-State Resistance <sup>a</sup>		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A			0.022	Ω
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 125 °C			0.043	
	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 175 °C			0.053	
		$V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$			0.025	
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 20 A				S
Dynamic <sup>b</sup>				<u> </u>	ļ	
Input Capacitance	C <sub>iss</sub>			1800		pF
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 \text{ V}, V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$		350		
Reverse Transfer Capacitance	C <sub>rss</sub>			100		
Total Gate Charge <sup>c</sup>	Qg			40	60	nC
Gate-Source Charge <sup>c</sup>	$Q_{gs}$	$V_{DS} = 30 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 40 \text{ A}$		9		
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			10		
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			10	20	ns
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD}$ = 30 V, $R_L$ = 0.8 $\Omega$ $I_D$ $\cong$ 40 A, $V_{GEN}$ = 10 V, $R_G$ = 2.5 $\Omega$		9	20	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			28	50	
Fall Time <sup>c</sup>	t <sub>f</sub>			7	15	
Source-Drain Diode Ratings and Cha	aracteristics	T <sub>C</sub> = 25 °C <sup>b</sup>		1		
Continuous Current	I <sub>S</sub>				40	^
Pulsed Current	I <sub>SM</sub>				100	A
Forward Voltage <sup>a</sup>	$V_{SD}$	I <sub>F</sub> = 40 A, V <sub>GS</sub> = 0 V		1.0	1.5	V
Reverse Recovery Time	t <sub>rr</sub>			48	100	ns
Peak Reverse Recovery Charge	I <sub>RM(REC)</sub>	$I_F = 40 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$		6		Α
Reverse Recovery Charge	Q <sub>rr</sub>			0.15		μC

#### Notes:

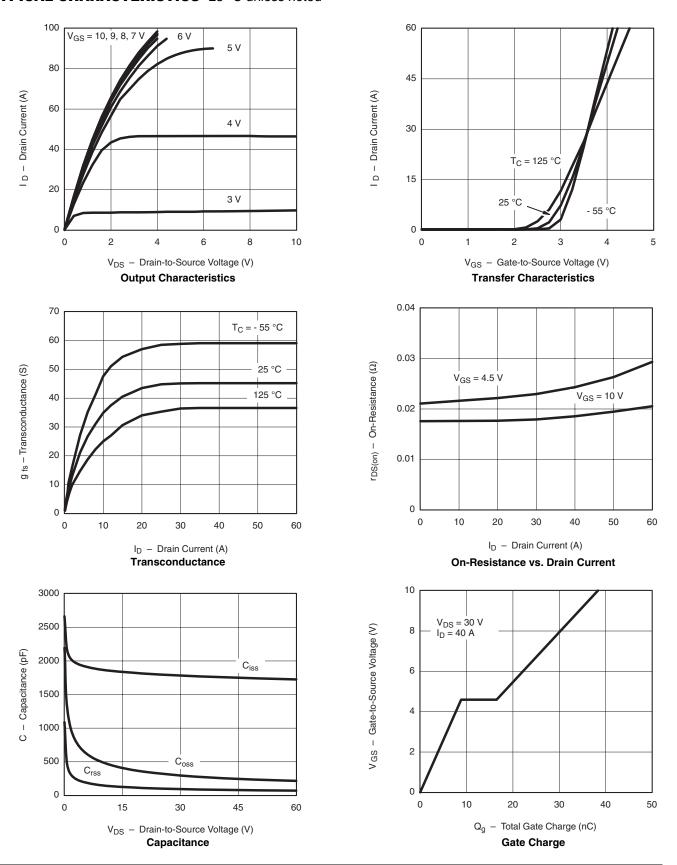
- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



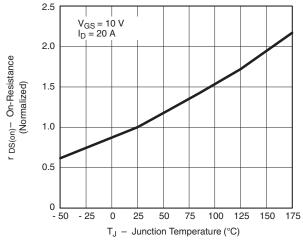


#### TYPICAL CHARACTERISTICS 25 °C unless noted

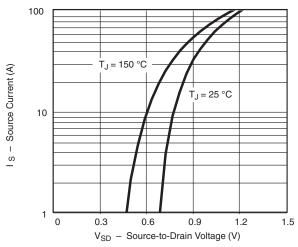


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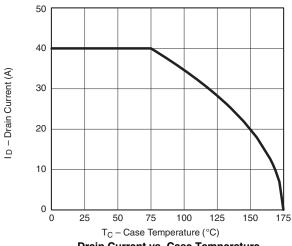


On-Resistance vs. Junction Temperature

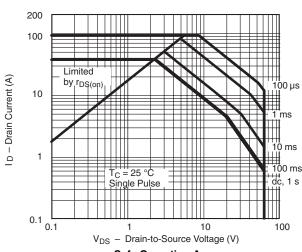


Source-Drain Diode Forward Voltage

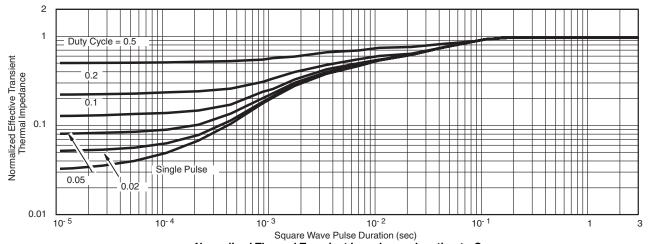
### THERMAL RATINGS



**Drain Current vs. Case Temperature** 



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?70288.



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