HIGH-VOLTAGE, AUTO-ZEROED OPERATIONAL AMPLIFIERS

FEATURES

- **High-Voltage Operation ..... ±15V**
- **Low Offset Voltage ..... 5 μV Max**
- **Low Offset Voltage Drift ..... 0.1 μV/°C**
- **Low Input Bias Current ..... 30 pA Max**
- **High Open-Loop Voltage Gain ..... 140 dB**
- **Wide Common-Mode Voltage Range ..... −15V to +13V**
- **Low Input Voltage Noise (0.1 Hz to 1 Hz) ..... 0.2 μV_{P-P}**
- **Low Supply Current ..... 1 mA**
- **Single Supply Operation ..... 7V to 32V**
- **Output Clamp Speeds Overload Recovery Time**

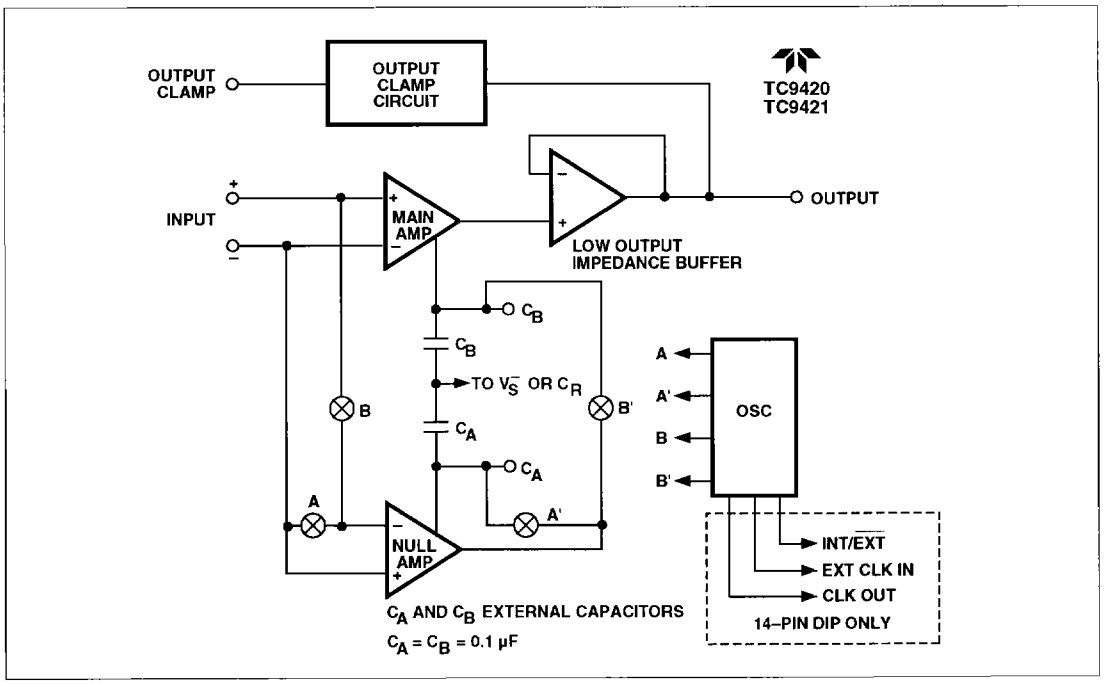
GENERAL DESCRIPTION

The TC9420 and TC9421 are high-voltage, high-performance, CMOS chopper-stabilized operational amplifiers. They can operate from the same ±15V power supplies as commonly used to power bipolar op-amps, such as the OP07 and OP741. Previous CMOS chopper amplifiers, such as the 7650, were limited to operating from ±7.5V supplies.

Maximum V_{OS} for the TC9420/TC9421 is only 5 μV, almost a factor of 14 improvement over the industry-standard OP07E. The maximum V_{OS} drift of 0.1 μV/°C is 12 times less than the OP07E. Input bias and offset currents, both only 30 pA maximum, are factors of 60 improvements.

8

FUNCTIONAL DIAGRAM



TC9420
TC9421

In addition to low initial offset errors, the nulling circuitry ensures excellent performance over time and temperature. Long-term drift, which results in periodic recalibration, is effectively eliminated. The nulling circuitry continues to operate over the full temperature range, whereas laser and "zener zap" trimming are only done at a single temperature. The result is a significant decrease in temperature-induced errors.

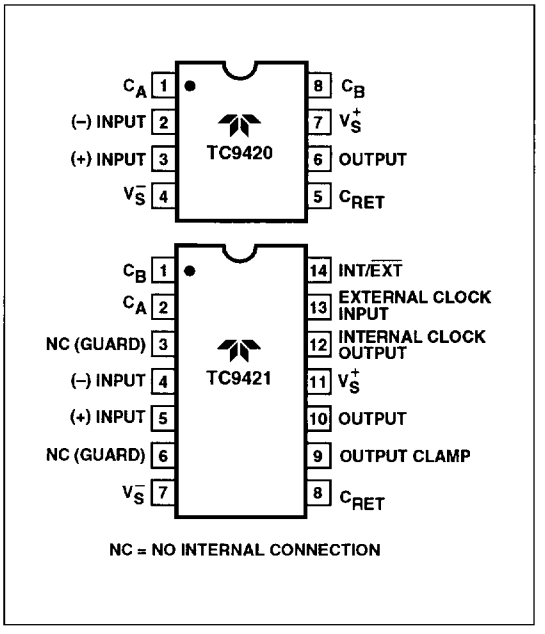
The TC9420/TC9421 operate from dual or single power supplies. Supply current is typically 1 mA with ±15V supplies. Single supply operation extends from +7V to +32V, and the input common-mode range extends to V_S^-. For battery operation, see the low-power TC900 data sheet.

The TC9420/TC9421 open-loop gain is 120 dB minimum. Unlike the 7650, the TC9420/TC9421 gain is independent of load resistance. The low impedance output will drive a 10 kΩ load to ±14V. An output clamp circuit is provided to minimize overload recovery time.

The TC9420/TC9421 use two amplifiers to correct offset voltage errors. A main amplifier is always in the signal path, which prevents switching spikes at the output. A separate nulling amplifier alternately corrects its own V_{OS} error. Only two external capacitors are required to store the nulling error voltages. All active nulling circuitry, including switches and oscillator, are included on the chip.

The TC9420/TC9421 are pin compatible with Maxim's MAX 420/421.

PIN CONFIGURATIONS



ORDERING INFORMATION

Part No.	Package	Temperature Range	Max V_{OS}
TC9420CPA	8-Pin Plastic DIP	0°C to +70°C	10 µV
TC9420EJA	8-Pin CerDIP	–40°C to +85°C	5 µV
TC9420EPA	8-Pin Plastic DIP	–40°C to +85°C	5 µV
TC9421CPD	14-Pin Plastic DIP	0°C to +70°C	10 µV
TC9421EJD	14-Pin CerDIP	–40°C to +85°C	5 µV
TC9421EPD	14-Pin Plastic DIP	–40°C to +85°C	5 µV

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V_S^+ to V_S^-) ..... +36V
Input Voltage ..... (V_S^+ + 0.3V) to (V_S^- – 0.3V)
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Current Into Any Pin ..... 10 mA
Operating Temperature Range
C Device ..... 0°C to +70°C
E Device ..... –40°C to +85°C
Package Power Dissipation (T_A = +25°C)
CerDIP Package ..... 500 mW
Plastic Package ..... 375 mW

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_S^+ = 15V, V_S^- = 15V, T_A = +25°C. Test circuit unless noted.

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
V_{OS}	Input Offset Voltage	T_A = +25°C	C		±1	±10	µV
			E		±1	±5	µV
		Over Temperature Range	C		±2	±20	µV
			E		±2	±10	µV
$\frac{\Delta V_{OS}}{\Delta T}$	Average Temperature Coefficient of Input Offset Voltage	Over Temperature Range	E		0.02	0.1	µV/°C
I_B	Input Bias Current	T_A = +25°C	C		10	100	pA
			E		10	30	pA
		Over Temperature Range	C		30		pA
			E		35		pA
I_{OS}	Input Offset Current	T_A = +25°C	C		15	200	pA
			E		15	60	pA
		Over Temperature Range	C		30		pA
			E		50		pA
R_{IN}	Input Resistance				10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	R_L = 10 kΩ, V_{OUT} = ±10V, T_A = +25°C		120	150		dB
		Over Temperature Range		120	150		dB
V_{OUT}	Output Voltage Swing	CLAMP Not Connected	R_L = 10 kΩ	±12	±14.5		V
			R_L = 100 kΩ		±14.95		V
CMVR	Common-Mode Voltage Range			+12, −15	+13, −15.1		V
CMRR	Common-Mode Rejection Ratio	CMVR = +12V to −15V Over Temperature Range		120	140		dB
PSRR	Power Supply Rejection Ratio	±3V to ±16.5V Over Temperature Range		120	140		dB
e_N	Input Noise Voltage (Peak-to-Peak Value Not Exceeded 95% of Time)	R_S = 100Ω	DC to 1 Hz		0.3		μV_{P-P}
			DC to 10 Hz		1.1		μV_{P-P}
I_N	Input Noise Current	f = 10 Hz			0.01		$pA/\sqrt{Hz}$
UGBW	Unity-Gain Bandwidth				500		kHz
sr	Slew Rate	C_L = 50 pF, R_L = 10 kΩ			0.5		V/µs
t_R	Rise Time				0.7		µs
	Overshoot				20		%
V_S^+, V_S^-	Operating Supply Range (Note 1)			±2.5		±16.5	V
I_S	Supply Current	No Load, T_A = +25°C			1.3	2	mA
		Over Temperature Range				3.5	mA
f_{CH}	Internal Chopping Frequency	Pins 12–14 Open (TC9421)			250		Hz
	Clamp ON Current	R_L = 100 kΩ		25	100		µA
	Clamp OFF Current	−10V ≤ V_{OUT} ≤ +10V			1		pA
	Offset Voltage vs Time				100		$nV/\sqrt{Mo}$

NOTES: 1. Single supply operation: V_S^+ = +7V to +32V.

8

Theory of Operation

Figure 1 shows the major elements of the TC9420/TC9421. There are two amplifiers: the main (signal) amplifier and the nulling amplifier. Both have offset nulling capability. The main amplifier is always connected to the output. The nulling amplifier alternately samples and adjusts its own offset and then the offset of the main amplifier.

A two-phase operation nulls the main amplifier. During the first phase, the A pair of switches close, while the B switches open. Then nulling amp's inputs are shorted and its output is fed back to the nulling input. Capacitor C_A charges to a voltage which will maintain the nulling amp in its nulled state.

During the second phase, the B switches close and the A switches open. The nulling amp's inputs now sample the offset voltage of the main amp. The nulling amp drives the main amp's nulling input to cancel the main amplifier's offset voltage. Capacitor C_B stores the nulling voltage of the main amplifier while the nulling amp is being nulled on the next cycle.

The TC9420/TC9421 design also incorporates an additional output buffer stage. The buffer provides a low impedance output traditionally associated with bipolar op amps. Some CMOS chopper-stabilized amplifiers, such as the 7650, have a high output impedance which makes open-loop gain proportional to load resistance. The TC9420/TC9421 open-loop gain is not dependent on load resistance.

Pin Compatibility

Since the TC9420/9421 operate from the same ±15V power supplies as bipolar op amps, upgrading existing circuits is simple. The bipolar op amp's nulling and compensation components are removed, and the TC9420/TC9421 nulling capacitors are added.

On the 8-pin mini-DIP (TC9420), the external null storage capacitors are connected to pins 1 and 8. On most other op amps they are left open or used for offset potentiometer or compensation capacitor connections.

For OP05 and OP07 operational amplifiers, replacing the offset null pot between pins 1 and 8 with two capacitors from the pins to C_{RET} will convert the OP05/07 pin configuration for TC9420 operation. The 741 is easily upgraded by removing the nulling pot between pin 4 and pins 1 and 5, then connecting capacitors from pin 4 to pins 1 and 8. For LM108 devices, the compensation capacitor is replaced by the external nulling capacitors. The LM101/748/709 pinouts are modified similarly by also removing any circuit connections to pin 5.

The minor modifications needed to retrofit a TC9420 into existing sockets make prototyping and circuit verification straightforward.

Nulling Capacitors

The offset voltage correction capacitors are connected to C_A and C_B. The common capacitor connection is made to C_{RET} (pin 5) on the 8-pin packages and to capacitor return (C_{RET}, pin 8) on the 14-pin packages. The common connection should be made through either a separate pc trace or wire to avoid voltage drops.

Internally, V_S^- is connected to C_{RET}.

C_A and C_B should be 0.1 µF film capacitors. Mylar capacitors are suitable.

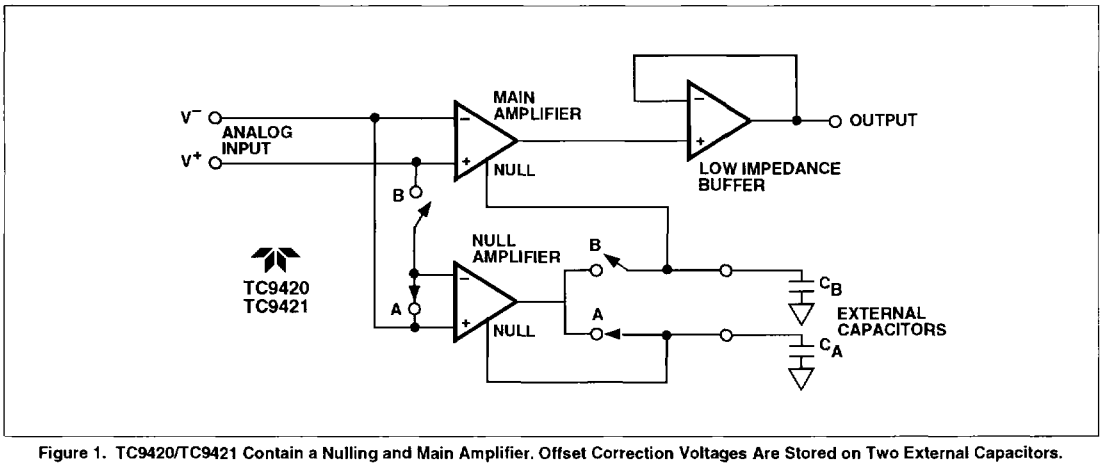


Figure 1. TC9420/TC9421 Contain a Nulling and Main Amplifier. Offset Correction Voltages Are Stored on Two External Capacitors.

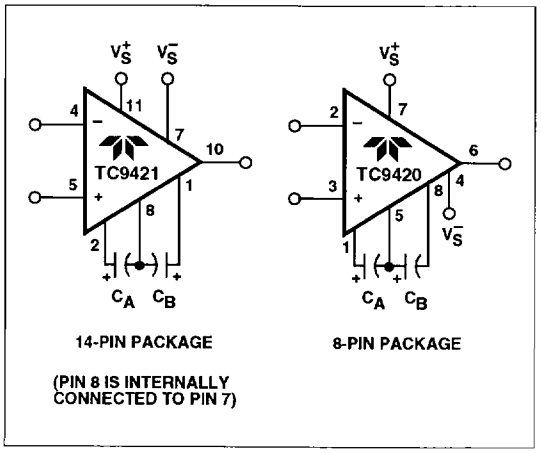


Figure 2. Nulling Capacitor Connection

Component Selection

The two required capacitors, C_A and C_B, have optimum values, depending on the clock or chopping frequency. For the preset internal clock, the correct value is 0.1 µF. To maintain the same relationship between the chopping frequency and nulling time constant, the capacitor values should be scaled in proportion to the external clock, if used. High-quality film-type capacitors (such as Mylar) are preferred. Ceramic or other lower-grade capacitors may be suitable in some applications. For fast settling on initial turn-on, low dielectric absorption capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to 1 µV.

Clock Operation

The internal oscillator is set for a 1000 Hz nominal frequency on both the 8-pin and 14-pin DIPs. With the 14-pin DIP (TC9421), the 250-Hz internal frequency is available at the internal clock output (pin 12). A 1000 Hz nominal signal will be present at the external clock input (pin 13) with INT/$\overline{\text{EXT}}$ high or open. This is the internal clock signal before a ÷4 operation.

The 14-pin device can be driven by an external clock. The INT/$\overline{\text{EXT}}$ input (pin 14) has an internal pull-up and may be left open for internal clock operation. If an external clock is used, INT/$\overline{\text{EXT}}$ must be tied to V_S^- (pin 7) to disable the internal clock. The external clock signal is applied to the external clock input (pin 13).

The external clock amplitude should swing between V_S^+ and ground for power supplies up to ±6V, and between V_S^+ and V_S^+ –6V for higher supply voltages. When the external clock is generated by +5V logic, capacitive coupling to pin 13 (through a 0.1 µF capacitor) will provide adequate drive.

At low frequencies, the external clock duty cycle is not critical, since an internal ÷4 gives the desired 50% switching duty cycle. The offset storage correction capacitors are charged only when the external clock input is high. A 50% to 80% external clock positive duty cycle is desired for frequencies above 500 Hz to guarantee transients settle before the internal switches open.

The external clock input can also be used as a strobe input. If a strobe signal is connected at the external clock input so that it is low during the time an overload signal is applied, neither capacitor will be charged. This function can be used to prevent input transients from overloading the nulling circuitry. Leakage currents at the capacitor pins are very low, so offset voltage drift during strobe operation is minimized.

Output Clamp

Chopper-stabilized systems can show long recovery times from overloads. If the output is driven to either supply rail, output saturation occurs. The inputs are no longer held at a "virtual ground." The V_{OS} null circuit treats the differential signal as an offset and tries to correct it by charging the external capacitors. The nulling circuit also saturates. Once the input signal returns to normal, response time is lengthened by the long recovery time of the nulling amplifier and external capacitors.

Through an external clamp connection, the TC9421 eliminates the overload recovery problem by reducing the feedback network gain before the output voltage reaches either supply rail.

The output clamp circuit is shown in Figure 3, with typical inverting and noninverting circuit connections shown in Figures 4 and 5. For the clamp to be fully effective, the impedance across the clamp output should be >100 kΩ.

When the clamp is used, the clamp "OFF" leakage will add to input bias current. However, clamp leakage in the "OFF" state is typically only 1 pA.

Input Bias Current

The TC9420/TC9421 are never disconnected from the main internal amplifier. The null amplifier samples the input offset voltage and corrects DC errors and drift by storing compensating voltages on external capacitors. The sampling, however, causes charge transfer at the inputs.

The impulse current is not usually a problem because the amount of charge transferred is very small. Care should be exercised, however, when replacing high-input bias current bipolar op amps. Conventional design practice is to cancel bias current by matching the input impedances (Figure 6a). The TC9420/TC9421 have input bias current of

8

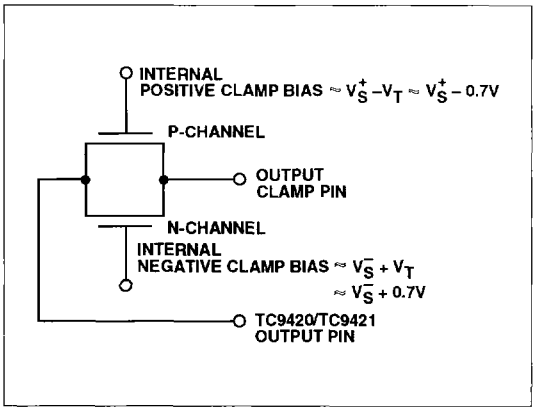


Figure 3. Internal Clamp Circuit

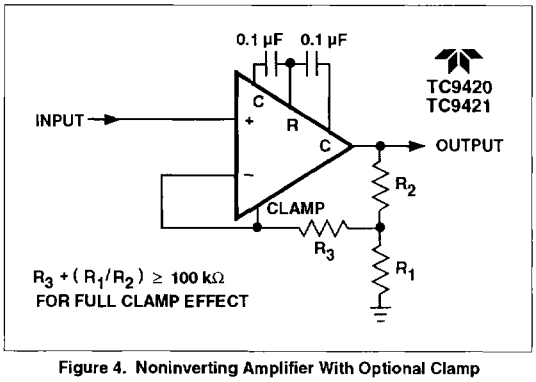


Figure 4. Noninverting Amplifier With Optional Clamp

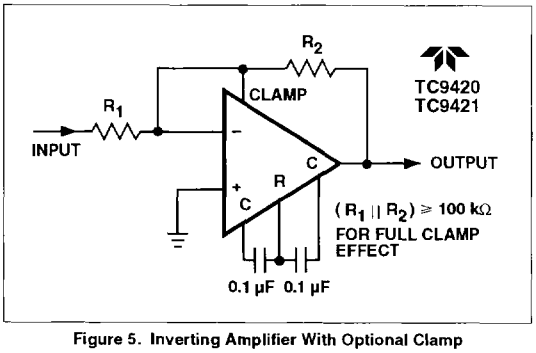


Figure 5. Inverting Amplifier With Optional Clamp

only 100 pA maximum, so the additional resistor is not necessary. In fact, including the resistor makes the charge injection current, passing through the impedance-balancing resistor, appear as a noise source. When replacing an existing op amp with the TC9420/TC9421, omit the resistor or bypass it to ground with a capacitor (Figure 6b).

Latch-Up Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances, this junction may be triggered into a low-impedance state, resulting in excessive supply current. To avoid this condition, voltages greater than 0.3V beyond the supply rails should not be applied to any pin. In general, the amplifier supplies must be established at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 0.1 mA to avoid latch-up.

Static Protection

All device pins are static-protected. Strong static fields and discharges should be avoided, however, as they can degrade diode junction characteristics and increase input-leakage currents.

Many companies are actively involved in providing services, eductional materials, and supplies to aid electronic manufacturers in establishing "static safe" work areas where CMOS components are handled. A partial company listing is:

- 3M
  Static Control Systems Division
  223-25W EM Center
  St. Paul, MN 55101
  (800) 792-1072

- Semtronics
  P.O. Box 592
  Martinsville, NJ 08836
  (210) 561-9520

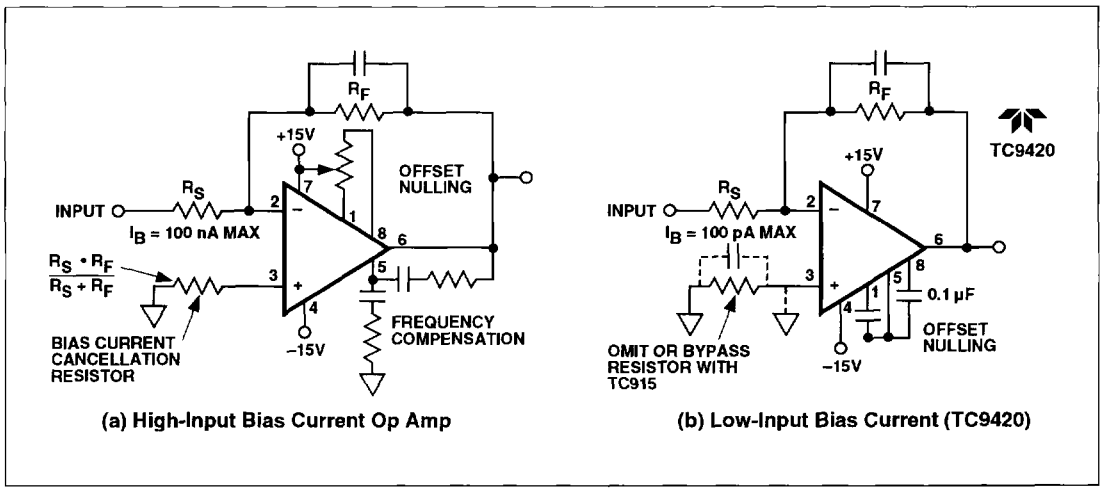
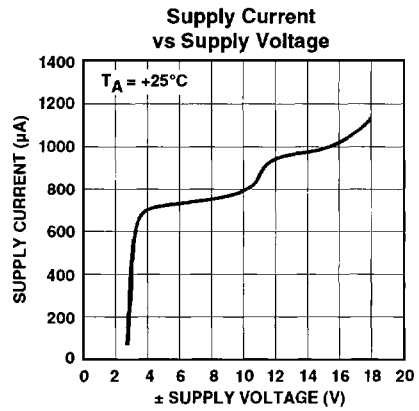
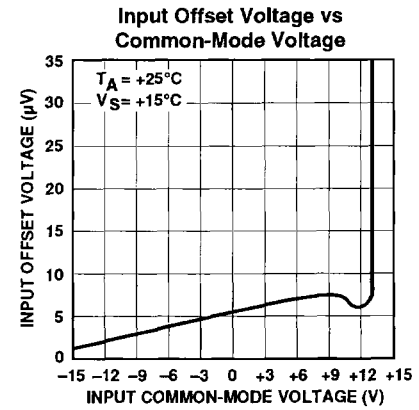


Figure 6. Input Bias Current Cancellation

8

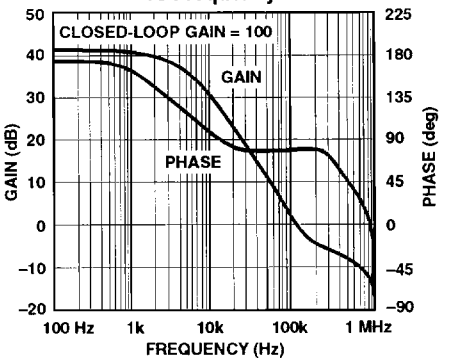
TYPICAL CHARACTERISTICS CURVES



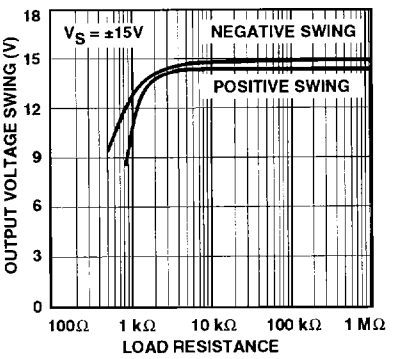


TYPICAL CHARACTERISTICS CURVES (Cont.)

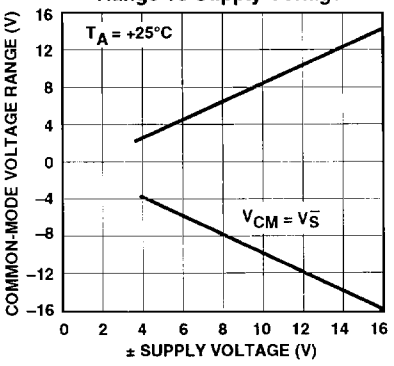
Gain and Phase vs Frequency



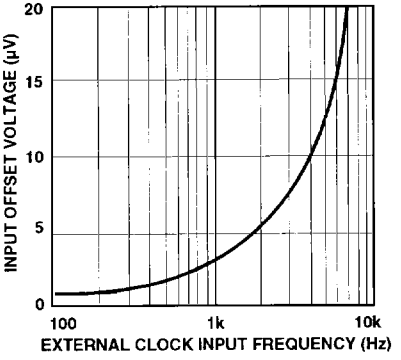
Output Voltage Swing vs Load Resistance



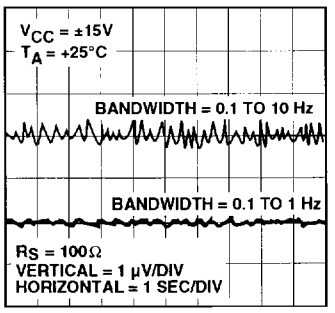
Input Common-Mode Voltage Range vs Supply Voltage



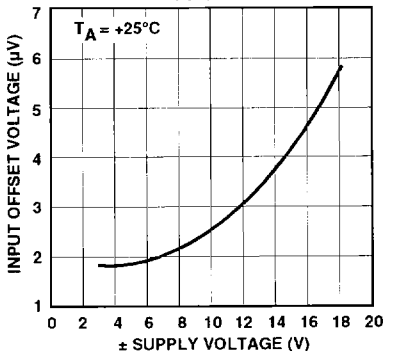
Input Offset Voltage vs Clock Frequency



Input Voltage Noise

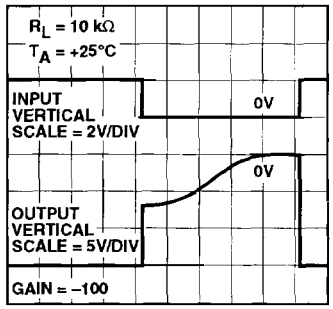


Input Offset Voltage vs Supply Voltage



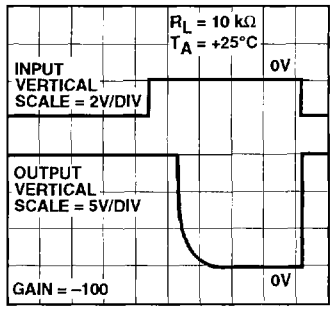
TYPICAL CHARACTERISTICS CURVES (Cont.)

Negative Overload Recovery Time



HORIZONTAL SCALE = 50 ms/DIV

Positive Overload Recovery Time



HORIZONTAL SCALE = 50 ms/DIV

8