

8-INPUT MULTIPLEXER/REGISTER WITH TRANSPARENT LATCHES; 3-STATE

FEATURES

- Transparent data latches
- Transparent address latch
- Easily expanding
- Complementary outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT354 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT354 data selectors/multiplexers contain full on-chip binary decoding, to select one-of-eight data sources. The data select address is stored in transparent latches that are enabled by a LOW on the latch enable input (LE).

The transparent 8-bit data latches are enabled when the active LOW data enable input (\bar{E}) is LOW. When the output enable input $\bar{OE}_1 = \text{HIGH}$, $\bar{OE}_2 = \text{HIGH}$ or $\bar{OE}_3 = \text{LOW}$, the outputs go to the high impedance OFF-state. Operation of these output enable inputs does not affect the state of the latches.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PHL} / t _{PLH}	propagation delay D _n , \bar{E} to Y, \bar{Y} S _n , LE to Y, \bar{Y}	C _L = 15 pF V _{CC} = 5 V	20 24	22 27	ns ns
C _I	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per latch	notes 1 and 2	68	71	pF

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

Notes

1. CPD is used to determine the dynamic power dissipation (P_D in μW):
 $P_D = CPD \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz C_L = output load capacitance in pF
 f_o = output frequency in MHz V_{CC} = supply voltage in V
 Σ (C_L × V_{CC}² × f_o) = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
 For HCT the condition is V_I = GND to V_{CC} - 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

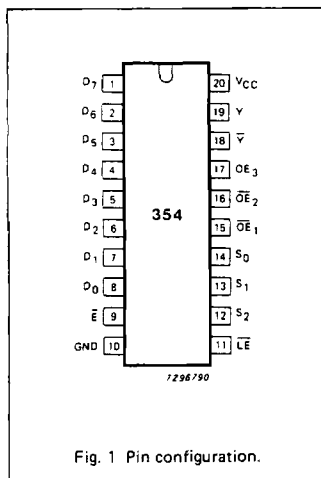


Fig. 1 Pin configuration.

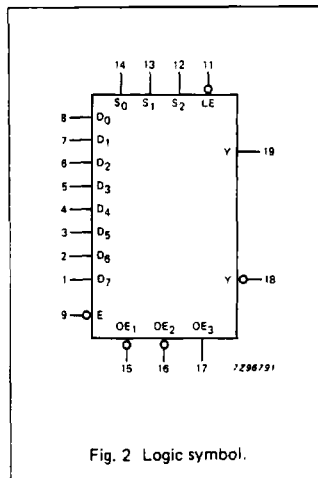


Fig. 2 Logic symbol.

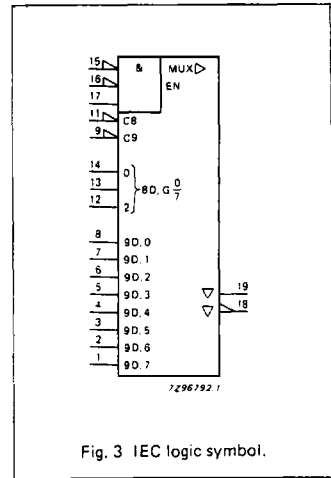


Fig. 3 IEC logic symbol.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8, 7, 6, 5, 4, 3, 2, 1	D ₀ to D ₇	data inputs
9	\bar{E}	data enable input (active LOW)
10	GND	ground (0 V)
11	\bar{LE}	address latch enable input (active LOW)
14, 13, 12	S ₀ , S ₁ , S ₂	select inputs
15, 16	\bar{OE}_1 , \bar{OE}_2	output enable inputs (active LOW)
17	OE ₃	output enable input (active HIGH)
18	\bar{Y}	3-state multiplexer output (active LOW)
19	Y	3-state multiplexer output (active HIGH)
20	VCC	positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUTS				DESCRIPTION	
ADDRESS *			\bar{E}	OUTPUT ENABLE			Y		\bar{Y}
S ₂	S ₁	S ₀		\bar{OE}_1	\bar{OE}_2	OE ₃			
X	X	X	X	H	X	X	Z	Z	outputs in high impedance OFF-state
X	X	X	X	X	X	X	Z	Z	
X	X	X	X	X	X	L	Z	Z	
L	L	L	L	L	L	H	D ₀	\bar{D}_0	data latch is transparent
L	L	H	L	L	L	H	D ₁	\bar{D}_1	
L	H	L	L	L	L	H	D ₂	\bar{D}_2	
L	H	H	L	L	L	H	D ₃	\bar{D}_3	
H	L	L	L	L	L	H	D ₄	\bar{D}_4	
H	L	H	L	L	L	H	D ₅	\bar{D}_5	
H	H	L	L	L	L	H	D ₆	\bar{D}_6	
H	H	H	L	L	L	H	D ₇	\bar{D}_7	
L	L	L	H	L	L	H	D _{0n}	\bar{D}_{0n}	data is latched
L	L	H	H	L	L	H	D _{1n}	\bar{D}_{1n}	
L	H	L	H	L	L	H	D _{2n}	\bar{D}_{2n}	
L	H	H	H	L	L	H	D _{3n}	\bar{D}_{3n}	
H	L	L	H	L	L	H	D _{4n}	\bar{D}_{4n}	
H	L	H	H	L	L	H	D _{5n}	\bar{D}_{5n}	
H	H	L	H	L	L	H	D _{6n}	\bar{D}_{6n}	
H	H	H	H	L	L	H	D _{7n}	\bar{D}_{7n}	

D₀ to D₇ = data at inputs D₀ to D₇D_{0n} to D_{7n} = data at inputs D₀ to D₇ before the most recent LOW-to-HIGH transition of \bar{E}

H = HIGH voltage level

L = LOW voltage level

X = don't care

Z = high impedance OFF-state

* This column shows the input address set-up with \bar{LE} = LOW (address latch is transparent).

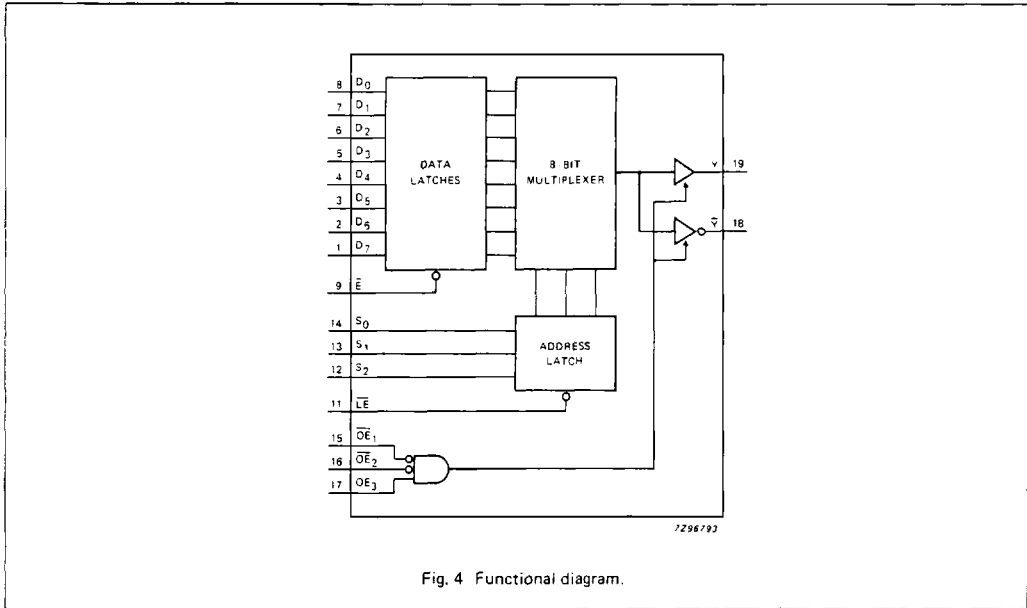


Fig. 4 Functional diagram.

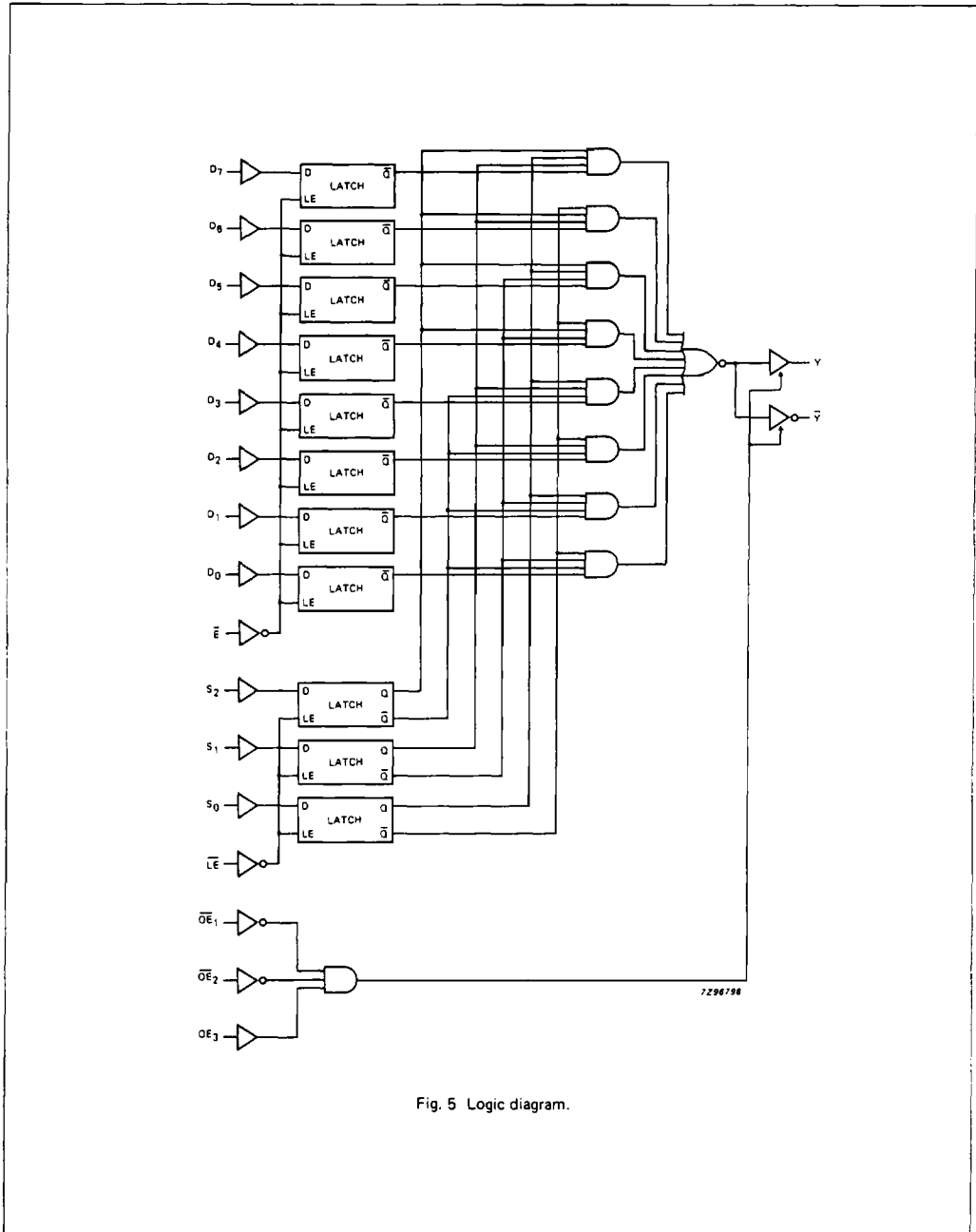


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS	
		74HC									V _{CC} V	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} / t _{PLH}	propagation delay D _n to Y, \bar{Y}		61 22 18	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig. 7	
t _{PHL} / t _{PLH}	propagation delay E to Y, \bar{Y}		63 23 18	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 6	
t _{PHL} / t _{PLH}	propagation delay S _n to Y, \bar{Y}		77 28 22	260 52 44		325 65 55		390 78 66	ns	2.0 4.5 6.0	Fig. 8	
t _{PHL} / t _{PLH}	propagation delay LE to Y, \bar{Y}		77 28 22	290 58 49		365 73 62		435 87 74	ns	2.0 4.5 6.0	Fig. 9	
t _{PZH} / t _{PZL}	3-state output enable time $\bar{O}E_n$ to Y, \bar{Y}		39 14 11	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig. 12	
t _{PZH} / t _{PZL}	3-state output enable time OE ₃ to Y, \bar{Y}		44 16 13	135 27 23		170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig. 12	
t _{PHZ} / t _{PLZ}	3-state output disable time $\bar{O}E_n$ to Y, \bar{Y}		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 12	
t _{PHZ} / t _{PLZ}	3-state output disable time OE ₃ to Y, \bar{Y}		55 20 16	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 12	
t _{THL} / t _{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Figs 7, 8 and 9	
t _w	data enable pulse width \bar{E} LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6	
t _w	latch enable pulse width $\bar{L}E$ LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 9	
t _{su}	set-up time D _n to \bar{E}	50 10 9	11 4 3		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 10	
t _{su}	set-up time S _n to $\bar{L}E$	50 10 9	14 5 4		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 10	

74HC/HCT354
MSI

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HC							V _{CC} V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _h	hold time D _n to \overline{E}	5 5 5	-6 -2 -2		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 11
t _h	hold time S _n to \overline{LE}	5 5 5	-8 -3 -2		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 10

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D _n , S _n	0.2
\overline{OE}_3	0.25
\overline{LE}	0.5
E, \overline{OE}_n	1.0

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)						UNIT	TEST CONDITIONS		
		74HCT							V_{CC} V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t_{PHL}/t_{PLH}	propagation delay D_n to Y, \bar{Y}		25	47		59		71	ns	4.5	Fig. 7
t_{PHL}/t_{PLH}	propagation delay \bar{E} to Y, \bar{Y}		26	54		68		81	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S_n to Y, \bar{Y}		30	59		74		89	ns	4.5	Fig. 8
t_{PHL}/t_{PLH}	propagation delay $\bar{L}E$ to Y, \bar{Y}		31	63		79		95	ns	4.5	Fig. 9
t_{PZH}/t_{PZL}	3-state output enable time \bar{OE}_n to Y, \bar{Y}		18	34		43		51	ns	4.5	Fig. 12
t_{PZH}/t_{PZL}	3-state output enable time OE_3 to Y, \bar{Y}		18	34		43		51	ns	4.5	Fig. 12
t_{PHZ}/t_{PLZ}	3-state output disable time \bar{OE}_n to Y, \bar{Y}		18	33		41		50	ns	4.5	Fig. 12
t_{PHZ}/t_{PLZ}	3-state output disable time OE_3 to Y, \bar{Y}		21	39		49		59	ns	4.5	Fig. 12
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Figs 7, 8 and 9
t_W	data enable pulse width \bar{E} LOW	16	6		20		24		ns	4.5	Fig. 6
t_W	latch enable pulse width $\bar{L}E$ LOW	16	6		20		24		ns	4.5	Fig. 9
t_{su}	set-up time D_n to \bar{E}	10	4		13		15		ns	4.5	Fig. 11
t_{su}	set-up time S_n to $\bar{L}E$	10	5		13		15		ns	4.5	Fig. 10
t_h	hold time D_n to \bar{E}	9	0		11		14		ns	4.5	Fig. 11
t_h	hold time S_n to $\bar{L}E$	9	-3		11		14		ns	4.5	Fig. 10

AC WAVEFORMS

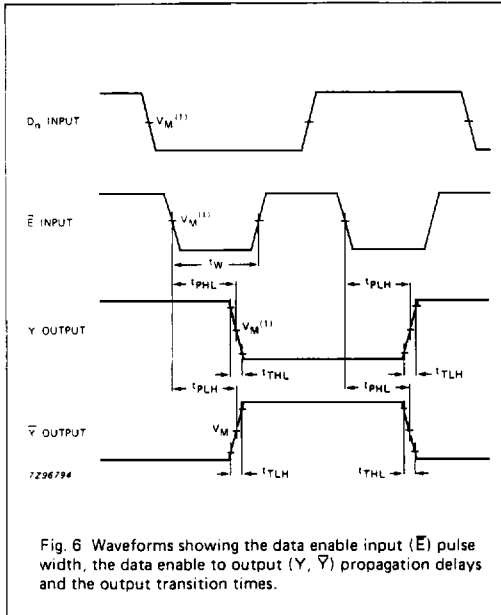


Fig. 6 Waveforms showing the data enable input (\bar{E}) pulse width, the data enable to output (Y, \bar{Y}) propagation delays and the output transition times.

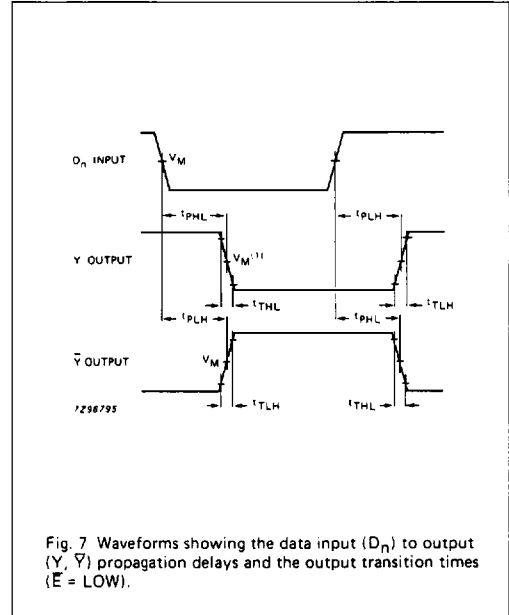


Fig. 7 Waveforms showing the data input (D_n) to output (Y, \bar{Y}) propagation delays and the output transition times ($\bar{E} = \text{LOW}$).

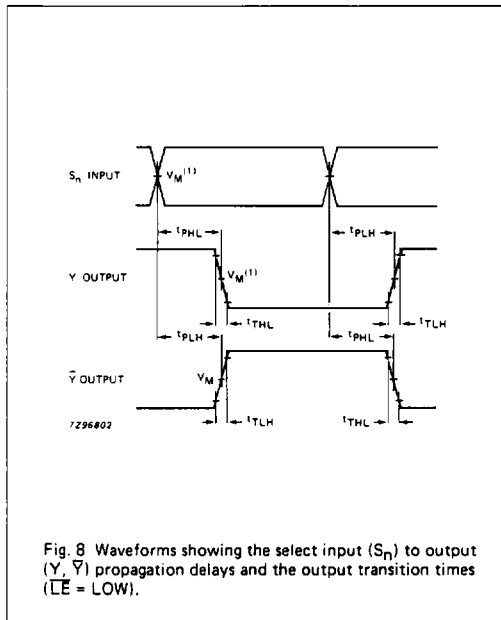


Fig. 8 Waveforms showing the select input (S_n) to output (Y, \bar{Y}) propagation delays and the output transition times ($\bar{LE} = \text{LOW}$).

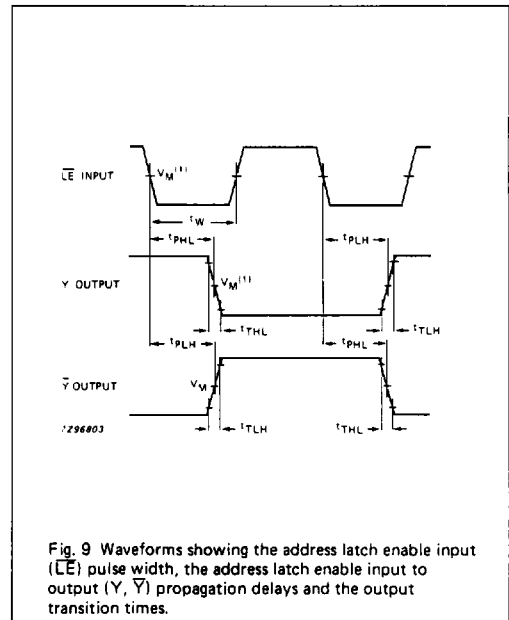


Fig. 9 Waveforms showing the address latch enable input (\bar{LE}) pulse width, the address latch enable input to output (Y, \bar{Y}) propagation delays and the output transition times.

AC WAVEFORMS (Cont'd)

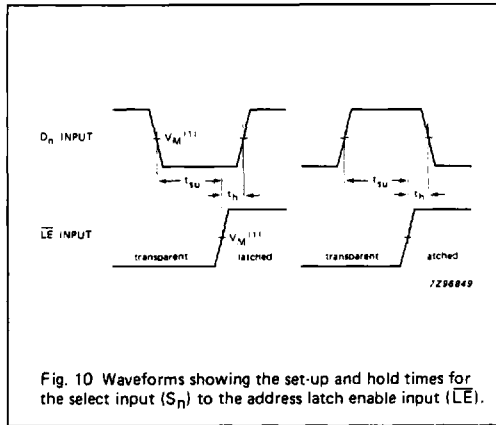


Fig. 10 Waveforms showing the set-up and hold times for the select input (S_n) to the address latch enable input (\overline{LE}).

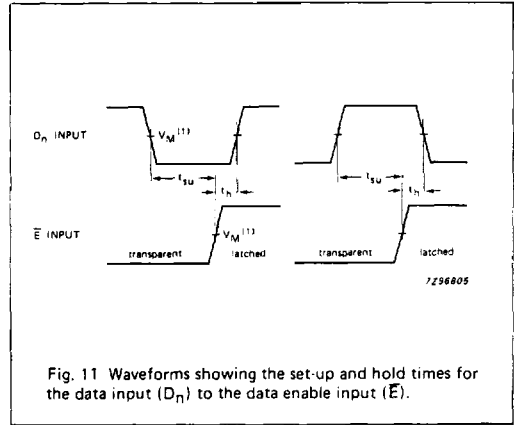


Fig. 11 Waveforms showing the set-up and hold times for the data input (D_n) to the data enable input (E).

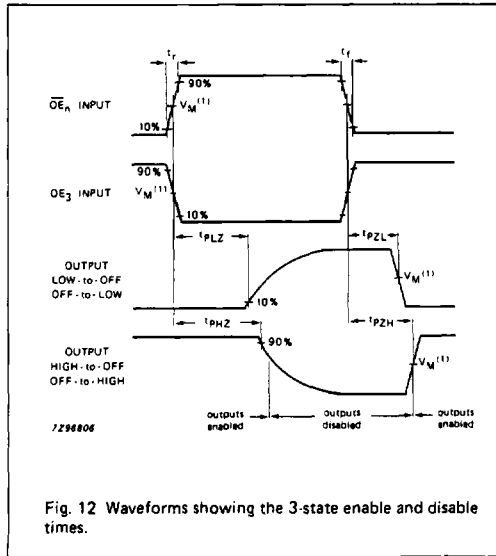


Fig. 12 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$
 HCT: $V_M = 1.3V$; $V_I = \text{GND to } 3V$.