

## ■ General Description

The AME8844 family of positive, linear regulators feature low quiescent current (45µA typ.) with low dropout voltage, making them ideal for battery applications.

Output voltages are set at the factory and trimmed to 1.5% accuracy.

These rugged devices have both Thermal Shutdown, and Current Fold-back to prevent device failure under the "Worst" operating conditions.

An additional feature is a "Power Good" detector, which pulls low when the output is out of regulation.

The AME8844 is stable with an output capacitance of 4.7µF or greater.

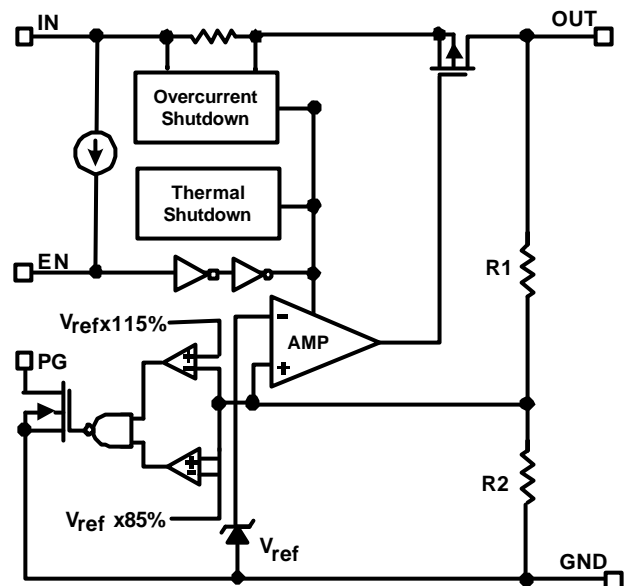
## ■ Features

- Very Low Dropout Voltage
- Guaranteed 750mA Output
- Accurate to within 1.5%
- 45µA Quiescent Current Typically
- Over-Temperature Shutdown
- Current Limiting
- Short Circuit Current Fold-back
- Noise Reduction Bypass Capacitor (Fixed Versions)
- Power-Saving Shutdown Mode
- Space-Saving MSOP-8 Package
- 6 Factory Pre-set Output Voltages
- Low Temperature Coefficient
- Adjustable Version
- Power Good Output Function.
- All AME's Lead Free Products Meet RoHS Standards

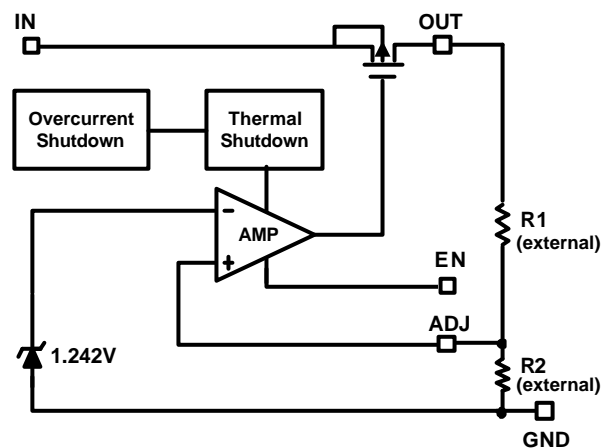
## ■ Applications

- Instrumentation
- Portable Electronics
- Wireless Devices
- PC Peripherals
- Battery Powered Widgets

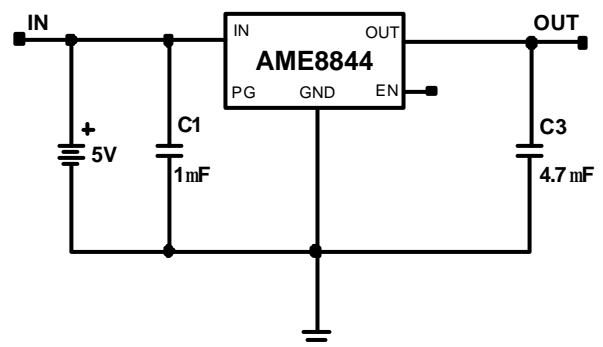
## ■ Functional Block Diagram (Fixed Versions)



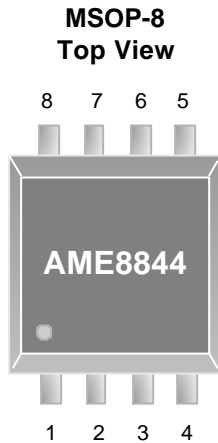
## (Adjustable Version)



## ■ Typical Applications

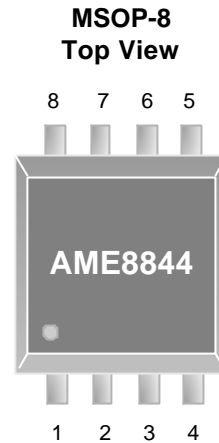


## ■ Pin Configuration


**AME 8844BEQAADJ**

1. EN
2. IN
3. ADJ
4. OUT
5. GND
6. GND
7. GND
8. GND

\* Die Attach:  
Conductive Epoxy

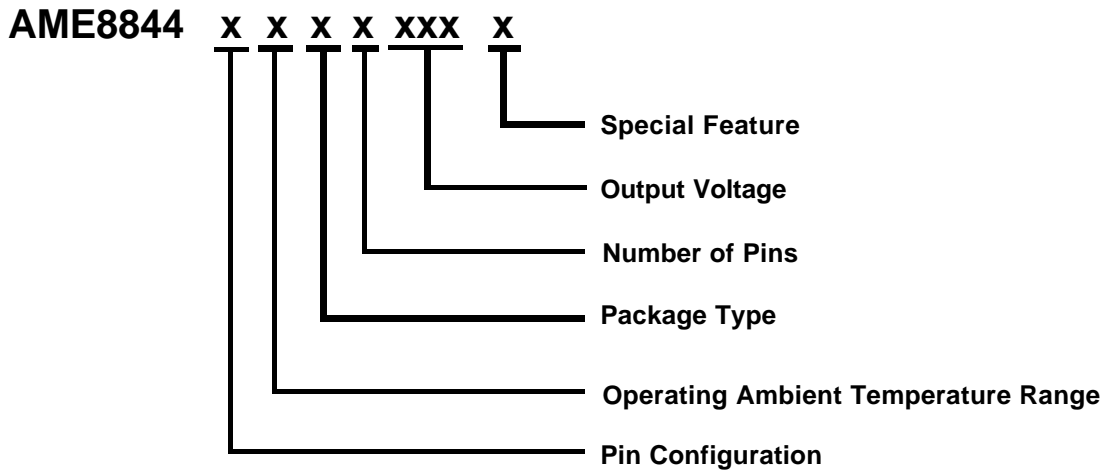

**AME 8844CEQAxXX**

1. EN
2. IN
3. NC
4. OUT
5. GND
6. GND
7. PG
8. GND

\* Die Attach:  
Conductive Epoxy

## ■ Pin Description

Pin Number		Pin Name	Pin Description
AME8844BEQA	AME8844CEQA		
1	1	EN	Enable pin. When pulled low, the PMOS pass transistor turns off, current consuming less than 1µA.
2	2	IN	Input voltage pin. It should be decoupled with 1µF or greater capacitor.
3	N/A	ADJ	Feedback output voltage for adjustable device.
N/A	3	NC	No connection.
4	4	OUT	LDO voltage regulator output pin. It should be decoupled with a 4.7µF or greater value low ESR ceramic capacitor.
N/A	7	PG	Power-Good output. This open-drain output is low when output is out of regulation.
5, 6, 7, 8	5, 6, 8	GND	Ground connection pin.

**■ Ordering Information**


Pin Configuration	Operating Ambient Temperature Range	Package Type	Number of Pins	Output Voltage	Special Feature
B: 1. EN (MSOP-8) 2. IN 3. ADJ 4. OUT 5. GND 6. GND 7. GND 8. GND  C: 1. EN (MSOP-8) 2. IN 3. NC 4. OUT 5. GND 6. GND 7. PG 8. GND	E: -40°C to +85°C	Q: MSOP	A: 8	ADJ: Adjustable 150: V=1.5V 180: V=1.8V 250: V=2.5V 330: V=3.3V	Z: Lead Free



## AME8844

750mA CMOS LDO

### ■ Ordering Information

Part Number	Marking*	Output Voltage	Package	Operating Ambient Temperature Range
AME8844BEQAADJ	8844 Byww	ADJ	MSOP-8	- 40°C to +85°C
AME8844BEQAADJZ	8844 Byww	ADJ	MSOP-8	- 40°C to +85°C
AME8844CEQA250Z	8844 Nyww	2.50	MSOP-8	- 40°C to +85°C

Note: yww represents the date code

\* A line on top of the first character represents lead free plating such as 8844

Please consult AME sales office or authorized Rep./Distributor for the availability of output voltage and package type.

### ■ Absolute Maximum Ratings

Parameter	Maximum	Unit
Input Voltage	-0.3 to +8	V
EN Voltage	-0.3 to +8	V
Output Voltage	-0.3 to $V_{IN} + 0.3$	V
PG Voltage	-0.3 to $V_{IN} + 0.3$	V
Output Current	$P_D / (V_{IN} - V_{OUT})$	mA
ESD Classification	B*	

Caution: Stress above the listed absolute maximum rating may cause permanent damage to the device.

\* HBM B: 2000~3999V

### ■ Recommended Operating Conditions

Parameter	Symbol	Rating	Unit
Ambient Temperature Range	$T_A$	- 40 to +85	°C
Junction Temperature Range	$T_J$	- 40 to +125	°C
Storage Temperature Range	$T_{STG}$	- 65 to +150	°C

### ■ Thermal Information

Parameter	Package	Die Attach	Symbol	Maximum	Unit
Thermal Resistance * (Junction to Case)	MSOP-8	Conductive Epoxy	$\theta_{JC}$	100	°C / W
Thermal Resistance (Junction to Ambient)			$\theta_{JA}$	206	
Internal Power Dissipation			$P_D$	625	mW
Maximum Junction Temperature				150	°C
Solder Iron(10 Sec)**				350	°C

\* Measure  $\theta_{JC}$  on center of molding compound if IC has no tab.

\*\* MIL-STD-202G 210F

## ■ Electrical Specifications

 $V_{IN} = V_{O(NOM)} + 2V$ ,  $V_{EN} = V_{IN}$ ,  $T_A = 25^{\circ}C$  unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	
Input Voltage	$V_{IN}$		Note 1		7	V	
Output Voltage Accuracy	$V_O$	$I_O = 1mA$	-1.5		1.5	%	
Dropout Voltage	$V_{DROPOUT}$	$I_O = 750mA$ $V_O = V_{ONOM} - 2.0\%$	$V_{O(NOM)} = 1.5V$	See chart	1000	mV	
			$V_{O(NOM)} = 1.8V$		650		
			$V_{O(NOM)} \geq 2.0V$		500		
Output Current	$I_O$	$V_O > 1.2V$	750			mA	
Current Limit	$I_{LIM}$	$V_O > 1.2V$	750			mA	
Short Circuit Current	$I_{SC}$	$V_{IN} = V_{O(NOM)} + 1V$ , $V_O < 0.4V$		750		mA	
Quiescent Current	$I_Q$	$I_O = 0mA$		45	70	$\mu A$	
Ground Pin Current	$I_{GND}$	$I_O = 1mA$ to 750mA		45		$\mu A$	
Line Regulation	$REG_{LINE}$	$I_O = 1mA$ $V_{IN} = V_O + 1$ to $V_O + 2$	$V_O < 2.0V$	-0.15		0.15	%
			$4.0 > V_O \geq 2.0V$	-0.1	0.02	0.1	%
			$4.0V \leq V_O$	-0.4		0.4	%
Load Regulation	$REG_{LOAD}$	$I_O = 1mA$ to 750mA	-1	0.2	1	%	
Over Temperature Shutdown	OTS			150		$^{\circ}C$	
Over Temperature Hysteresis	OTH			30		$^{\circ}C$	
$V_O$ Temperature Coefficient	TC			30		ppm/ $^{\circ}C$	
ADJ Input Bias Current	$I_{ADJ}$			1		$\mu A$	
Minimum Load Current	$I_{LOAD}$	$V_{IN} = 2.5V$			70	$\mu A$	
ADJ Reference Voltage	$V_{REF}$		1.221	1.240	1.26	V	
Power Supply Rejection	PSRR	$I_O = 100mA$ $C_O = 4.7\mu F$ ceramic	$f = 1kHz$		75	dB	
			$f = 10kHz$		55		
			$f = 100kHz$		30		
Output Voltage Noise	eN	$f = 10Hz$ to 100kHz $I_O = 10mA$			30	$\mu V_{rms}$	
EN Input Threshold	$V_{EH}$	$V_{IN} = 2.7V$ to 7V	2.0		$V_{in}$	V	
	$V_{EL}$	$V_{IN} = 2.7V$ to 7V	0		0.4	V	
EN Input Bias Current	$I_{EH}$	$V_{EN} = V_{IN}$ , $V_{IN} = 2.7V$ to 7V			1	$\mu A$	
	$I_{EL}$	$V_{EN} = 0V$ , $V_{IN} = 2.7V$ to 7V			1	$\mu A$	



AME8844

750mA CMOS LDO

■ Electrical Specifications (Contd.)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Shutdown Supply Current	$I_{SD}$	$V_{IN}=5V, V_O=0V, V_{EN}<V_{EL}$		0.5	2	$\mu A$
Output Under Voltage	$V_{UV}$	PG goes Low when $V_{OUT}$ too Low			84	$\%V_{O(NOM)}$
Output Over Voltage	$V_{OV}$	PG goes Low when $V_{OUT}$ too High	105			$\%V_{O(NOM)}$
PG Leakage Current	$I_{LC}$	$V_{PG}=7V$			1	$\mu A$
PG Voltage Low	$V_{OL}$	$I_{SINK}=0.25mA$			0.4	V

Note1:  $V_{IN(min)} = V_{OUT} + V_{DROPOUT}$

## ■ Detailed Description

The AME8844 family of CMOS regulators contain a PMOS pass transistor, voltage reference, error amplifier, over-current protection, and thermal shutdown.

The P-channel pass transistor receives data from the error amplifier, over-current shutdown, and thermal protection circuits. During normal operation, the error amplifier compares the output voltage to a precision reference. Over-current and Thermal shutdown circuits become active when the junction temperature exceeds 140°C, or the current exceeds 2.2A. During thermal shutdown, the output voltage remains low. Normal operation is restored when the junction temperature drops below 120°C.

The AME8844 behaves like a current source when the load reaches 2.2A. However, if the load impedance drops below 0.3 ohms, the current drops back to 600mA to prevent excessive power dissipation. Normal operation is restored when the load resistance exceeds 0.75 ohms.

## ■ External Capacitors

The AME8844 is stable with an output capacitor to ground of 4.7µF or greater. Ceramic capacitors have the lowest ESR, and will offer the best AC performance. Conversely, Aluminum Electrolytic capacitors exhibit the highest ESR, resulting in the poorest AC response. Unfortunately, large value ceramic capacitors are comparatively expensive. One option is to parallel a 0.1µF ceramic capacitor with a 10µF Aluminum Electrolytic. The benefit is low ESR, high capacitance, and low overall cost.

A second capacitor is recommended between the input and ground to stabilize  $V_{IN}$ . The input capacitor should be at least 0.1µF to have a beneficial effect.

All capacitors should be placed in close proximity to the pins. A "Quiet" ground termination is desirable. This can be achieved with a "Star" connection.

## ■ Enable

When EN pin is pulled low, the PMOS pass transistor shuts off, and all internal circuits are powered down. In this state, the quiescent current is less than 2µA. This pin behaves much like an electronic switch.

100K ohms resistor is necessary between  $V_{EN}$  source and EN pin when  $V_{EN}$  is higher than  $V_{IN}$ .

*(Note: There is no internal pull-up for EN pin. It can not be floating)*

## ■ Adjustable Version

The adjustable version uses external feedback resistors to generate an output voltage anywhere from 1.5V to 5.0V.  $V_{adj}$  is trimmed to 1.24V and  $V_{OUT}$  is given by the equation:

$$V_{OUT} = V_{adj} ( 1 + R1 / R2 )$$

Feedback resistors R1 and R2 should be high enough to keep quiescent current low, but increasing  $R1 + R2$  will reduce stability. In general, R1 and R2 in the 10 to 30 kΩ will produce adequate stability, given reasonable layout precautions. To improve stability characteristics, keep parasitics on the ADJ pin to a minimum, and lower R1 and R2 values.

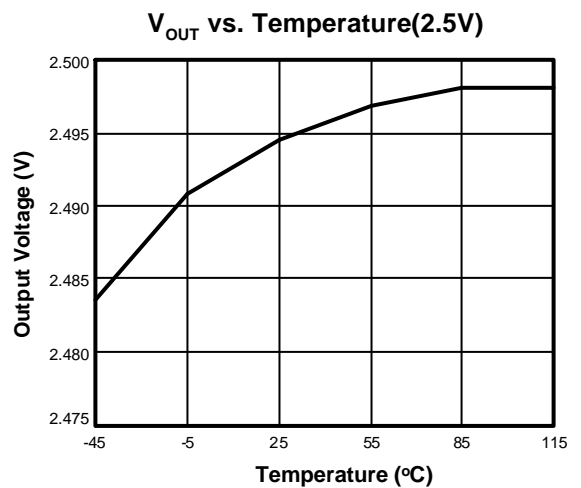
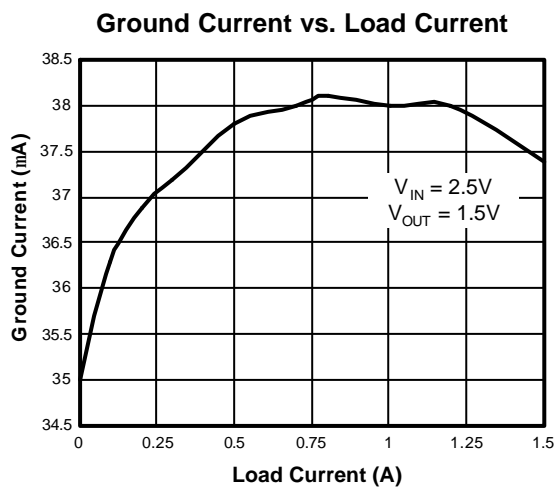
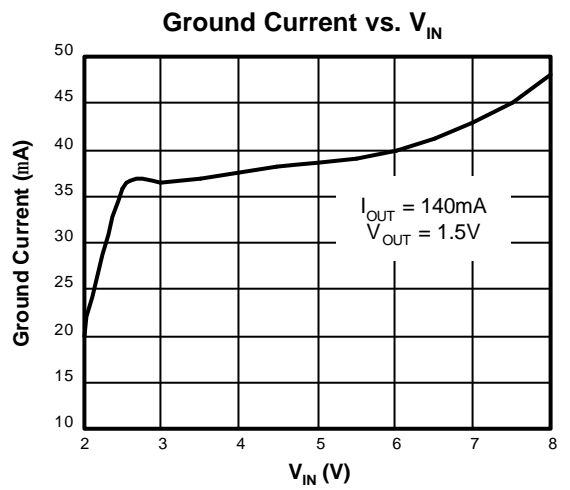
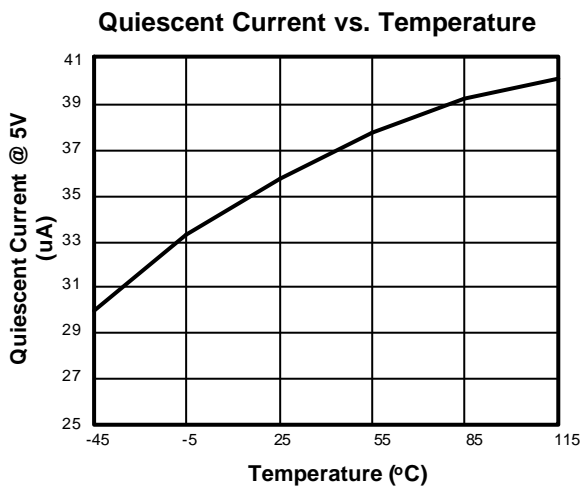
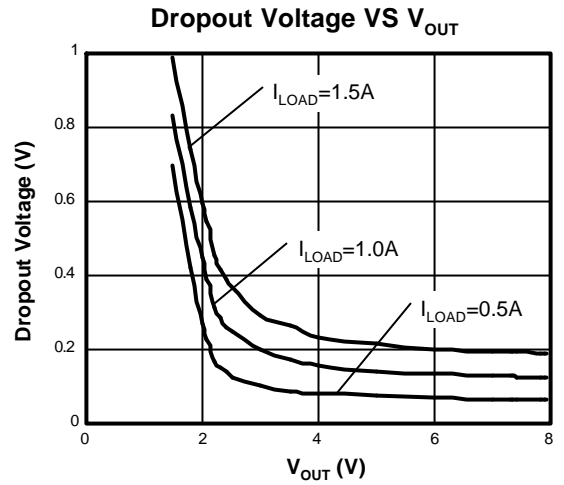
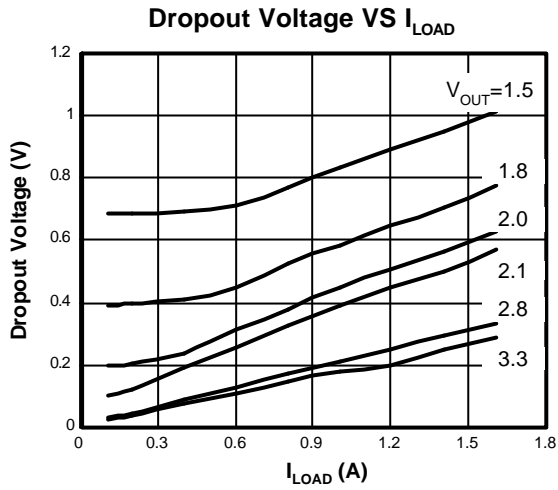
## ■ Power Good

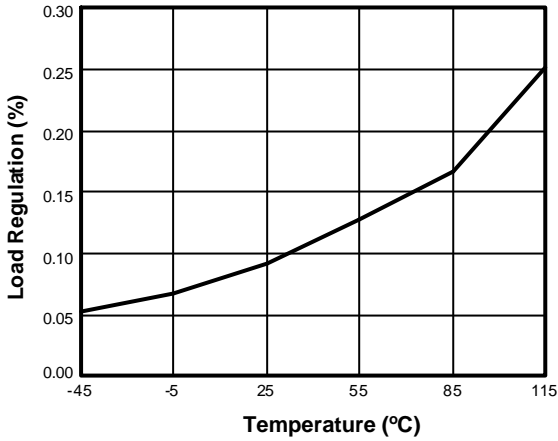
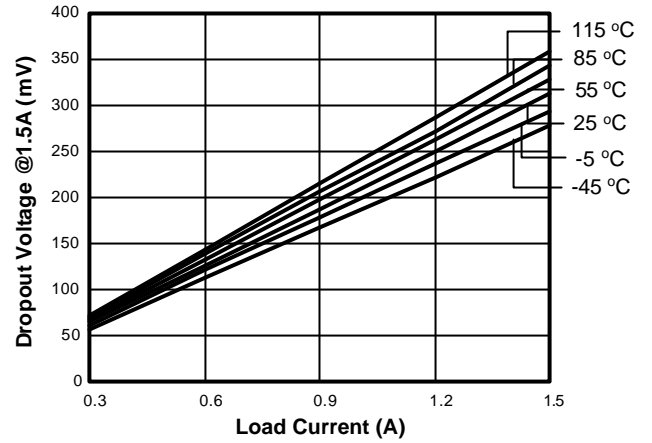
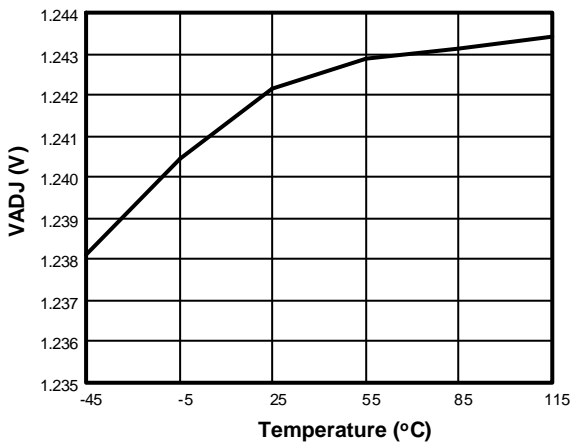
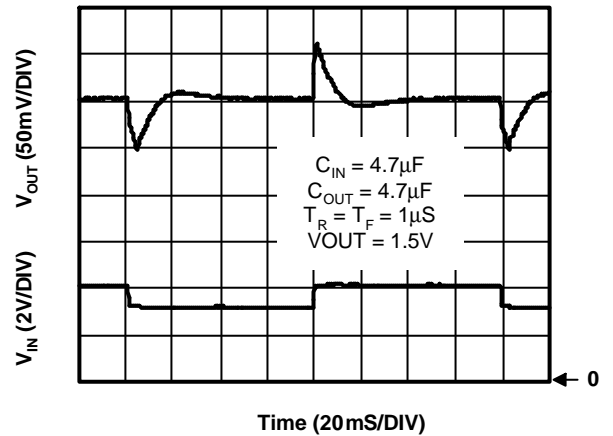
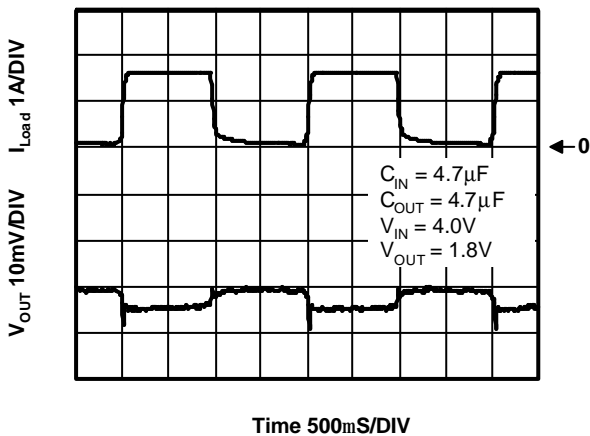
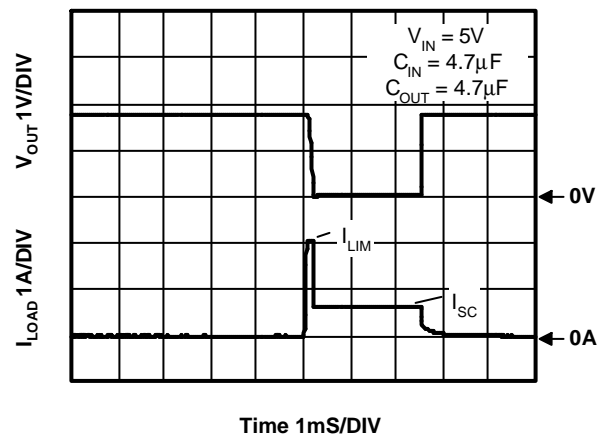
The AME8844 includes the Power Good feature. When the output is not within ± 5% of the specified voltage, it pulls low. This can occur under the following conditions:

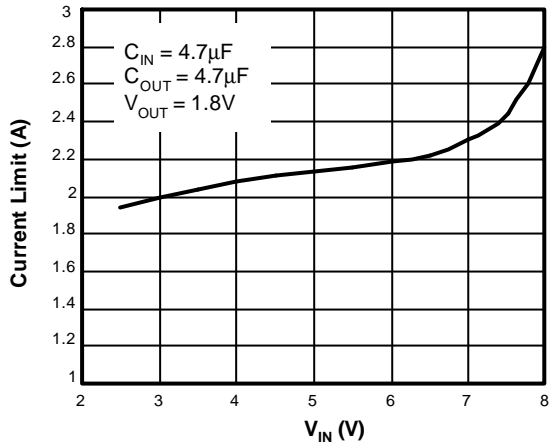
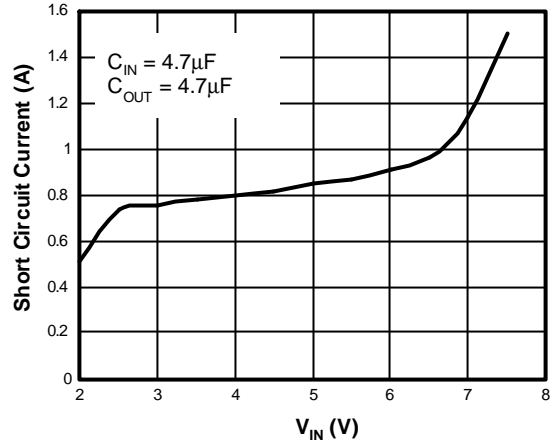
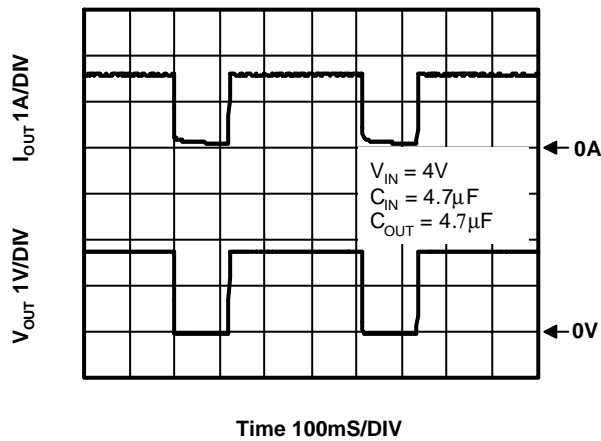
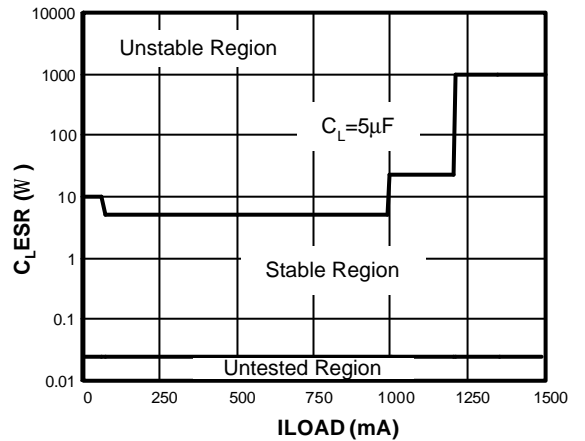
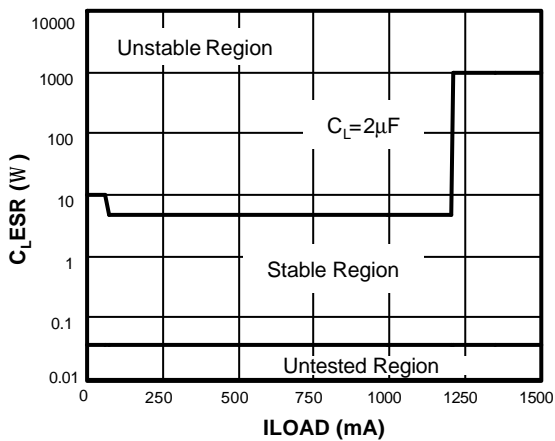
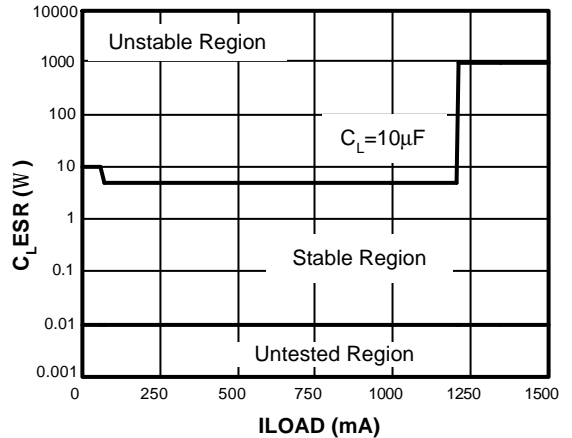
- 1) Input Voltage too low.
- 2) During Over-Temperature.
- 3) During Over-Current.
- 4) If output is pulled up.

*(Note: PG pin is an open-drain output.)*





**Load Regulation vs. Temperature**

**Dropout Voltage vs. Load Current(2.5V)**

**AME8844BEQA VADJ vs. Temperature**

**Line Transient Response**

**Load Step 40mA to 1.5A**

**Current Limit Response**


**Current Limit vs.  $V_{IN}$** 

**Short Circuit Current vs.  $V_{IN}$** 

**Overtemperature Shutdown**

**Stability vs. ESR vs.  $I_{Load}$** 

**Stability vs. ESR vs.  $I_{Load}$** 

**Stability vs. ESR vs.  $I_{Load}$** 


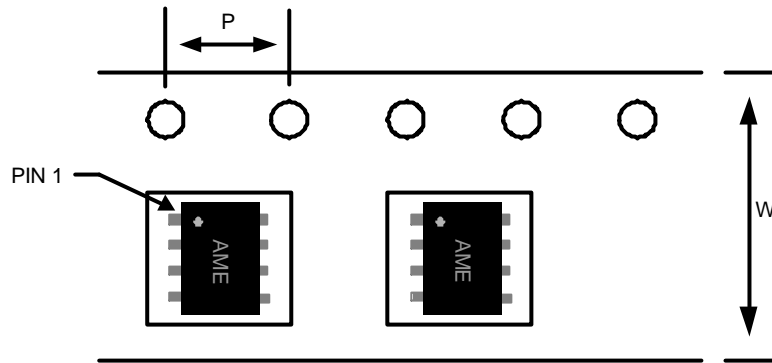
**External Resistor Divider Table**

R1 (K Ohm)	1	2	5	10	20
Vout	$R2(\text{kohm})=(1.24 \cdot R1(\text{kohm})) / (Vout - 1.24)$				
1.30	20.67	41.33	103.33	206.67	413.33
1.35	11.27	22.55	56.36	112.73	225.45
1.40	7.75	15.50	38.75	77.50	155.00
1.45	5.90	11.81	29.52	59.05	118.10
1.50	4.77	9.54	23.85	47.69	95.38
1.55	4.00	8.00	20.00	40.00	80.00
1.60	3.44	6.89	17.22	34.44	68.89
1.65	3.02	6.05	15.12	30.24	60.49
1.70	2.70	5.39	13.48	26.96	53.91
1.75	2.43	4.86	12.16	24.31	48.63
1.80	2.21	4.43	11.07	22.14	44.29
1.85	2.03	4.07	10.16	20.33	40.66
1.90	1.88	3.76	9.39	18.79	37.58
1.95	1.75	3.49	8.73	17.46	34.93
2.00	1.63	3.26	8.16	16.32	32.63
2.05	1.53	3.06	7.65	15.31	30.62
2.10	1.44	2.88	7.21	14.42	28.84
2.15	1.36	2.73	6.81	13.63	27.25
2.20	1.29	2.58	6.46	12.92	25.83
2.25	1.23	2.46	6.14	12.28	24.55
2.30	1.17	2.34	5.85	11.70	23.40
2.35	1.12	2.23	5.59	11.17	22.34
2.40	1.07	2.14	5.34	10.69	21.38
2.45	1.02	2.05	5.12	10.25	20.50
2.50	0.98	1.97	4.92	9.84	19.68
2.55	0.95	1.89	4.73	9.47	18.93
2.60	0.91	1.82	4.56	9.12	18.24
2.65	0.88	1.76	4.40	8.79	17.59
2.70	0.85	1.70	4.25	8.49	16.99
2.75	0.82	1.64	4.11	8.21	16.42
2.80	0.79	1.59	3.97	7.95	15.90
2.85	0.77	1.54	3.85	7.70	15.40
2.90	0.75	1.49	3.73	7.47	14.94
2.95	0.73	1.45	3.63	7.25	14.50
3.00	0.70	1.41	3.52	7.05	14.09
3.05	0.69	1.37	3.43	6.85	13.70
3.10	0.67	1.33	3.33	6.67	13.33

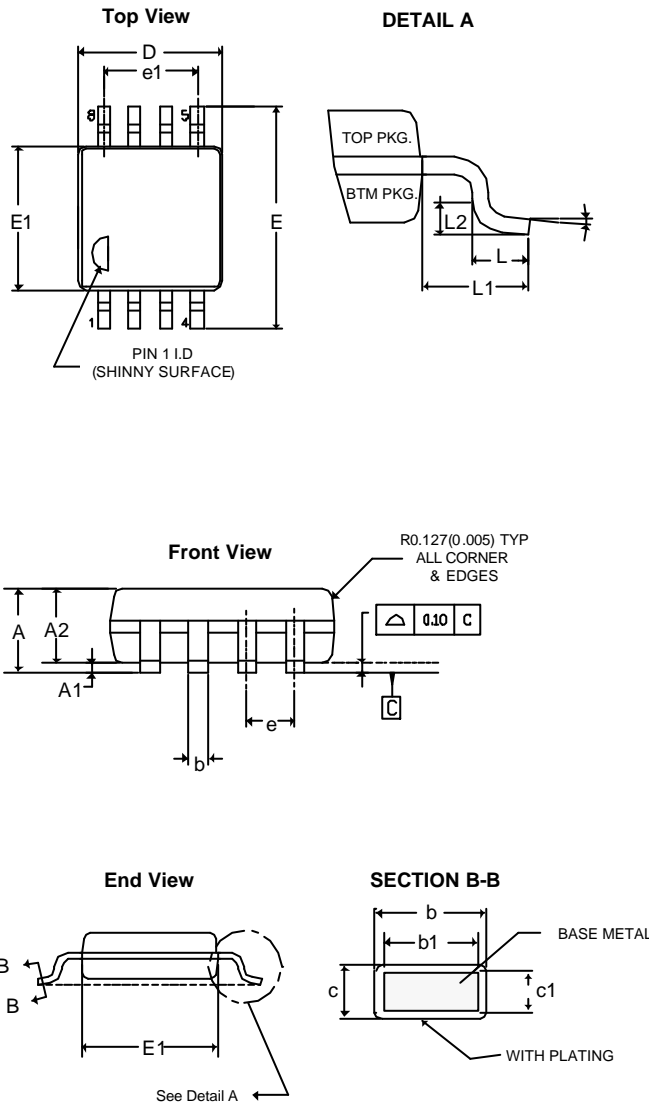
**■ External Resistor Divider Table (contd.)**

R1 (K Ohm)	1	2	5	10	20
Vout	$R2(\text{kohm})=(1.242 \cdot R1(\text{kohm})) / (V_{\text{out}} - 1.242)$				
3.15	0.65	1.30	3.25	6.49	12.98
3.20	0.63	1.27	3.16	6.33	12.65
3.25	0.62	1.23	3.08	6.17	12.34
3.30	0.60	1.20	3.01	6.02	12.04
3.35	0.59	1.18	2.94	5.88	11.75
3.40	0.57	1.15	2.87	5.74	11.48
3.45	0.56	1.12	2.81	5.61	11.22
3.50	0.55	1.10	2.74	5.49	10.97
3.55	0.54	1.07	2.68	5.37	10.74
3.60	0.53	1.05	2.63	5.25	10.51
3.65	0.51	1.03	2.57	5.15	10.29
3.70	0.50	1.01	2.52	5.04	10.08
3.75	0.49	0.99	2.47	4.94	9.88
3.80	0.48	0.97	2.42	4.84	9.69
3.85	0.48	0.95	2.38	4.75	9.50
3.90	0.47	0.93	2.33	4.66	9.32
3.95	0.46	0.92	2.29	4.58	9.15
4.00	0.45	0.90	2.25	4.49	8.99
4.05	0.44	0.88	2.21	4.41	8.83
4.10	0.43	0.87	2.17	4.34	8.67
4.15	0.43	0.85	2.13	4.26	8.52
4.20	0.42	0.84	2.09	4.19	8.38
4.25	0.41	0.82	2.06	4.12	8.24
4.30	0.41	0.81	2.03	4.05	8.10
4.35	0.40	0.80	1.99	3.99	7.97
4.40	0.39	0.78	1.96	3.92	7.85
4.45	0.39	0.77	1.93	3.86	7.73
4.50	0.38	0.76	1.90	3.80	7.61
4.55	0.37	0.75	1.87	3.75	7.49
4.60	0.37	0.74	1.85	3.69	7.38
4.65	0.36	0.73	1.82	3.64	7.27
4.70	0.36	0.72	1.79	3.58	7.17
4.75	0.35	0.71	1.77	3.53	7.07
4.80	0.35	0.70	1.74	3.48	6.97
4.85	0.34	0.69	1.72	3.43	6.87
4.90	0.34	0.68	1.69	3.39	6.78
4.95	0.33	0.67	1.67	3.34	6.68
5.00	0.33	0.66	1.65	3.30	6.60

Note: Small load(greater than 2 mA) is necessary as R1 or R2 is larger than 50 K Ohm. Otherwise, output voltage probably cannot be pulled down to 0 V on disable mode.

**■ Tape and Reel Dimension**
**MSOP-8**

**Carrier Tape, Number of Components Per Reel and Reel Size**

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
MSOP-8	12.0±0.1 mm	4.0±0.1 mm	4000pcs	330±1 mm

**■ Package Dimension**
**MSOP-8**


SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
<b>A</b>	-	1.07	-	0.04197
<b>A<sub>1</sub></b>	0.05	0.20	0.002	0.008
<b>A<sub>2</sub></b>	0.81	0.92	0.032	0.036
<b>b</b>	0.28	0.38	0.011	0.015
<b>b<sub>1</sub></b>	0.28	0.33	0.011	0.013
<b>c</b>	0.13	0.23	0.005	0.009
<b>c<sub>1</sub></b>	0.13	0.17	0.005	0.006
<b>D</b>	2.90	3.10	0.114	0.122
<b>E</b>	4.77	4.98	0.188	0.196
<b>E<sub>1</sub></b>	2.90	3.10	0.114	0.122
<b>e</b>	0.65 TYP		0.0255 TYP	
<b>e<sub>1</sub></b>	1.95 TYP		0.0767 TYP	
<b>L</b>	0.406	0.686	0.01598	0.02701
<b>L<sub>1</sub></b>	0.94 REF		0.037 REF	
<b>L<sub>2</sub></b>	0.254 TYP		0.010 TYP	
<b>q</b>	0°	8°	0°	8°

**NOTE:**

- Controlling dimension : Millimeter, converted inch dimension are not necessarily exact.
- Dimensioning and tolerancing per ANSI Y14.5m-1994.
- Dimension "d" does not include mold flash, protrusion or gate burr. Dimension "e1" does not include inter-lead flash or protrusion, inter-lead flash and protrusion shall not exceed 0.15mm(0.006") per side. Dimension "d" and "e1" are determined at outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
- The package top be smaller than the package bottom. Dimension "d" and "e1" are determined at outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
- Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm(0.0031) total in excess of the "b" dimension at maximum material condition.



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