Le79555

Subscriber Line Interface Circuit
VE580 Series

APPLICATIONS

- **Ideal for high-density, low-power linecard applications**

FEATURES

- **Control states: Active, Reverse Polarity, Tip Open, Ringing, Standby, and Open Circuit**
- **Low Standby power**
- **–40 to –58 V battery operation**
- **On-hook transmission**
- **Two-wire impedance set by single external impedance**
- **Programmable constant-current feed**
- **Low Off-Hook Active Overhead Voltage**
- **Programmable loop-detect threshold**
- **Ground-start detector**
- **Programmable ring-trip detect threshold**
- **No –5 V supply required**
- **Three on-chip relay drivers and relay snubbers, one ringing and two general purpose**
- **Tip Open state for ground-start lines**
- **On-chip switching regulator for Low power dissipation**
- **Supports 30 mA for Active, Norma,l and Reverse Polarity operation**

ORDERING INFORMATION

Standard Packages		
Device	**Performance Grade/Package**	**Packing[2]**
Le79555-1VC Le79555-1QC	52 dB Pol. Rev., 44-pin TQFP 52 dB Pol. Rev., 32-pin QFN	Tray
Le79555-2VC Le79555-2QC	63 dB Pol. Rev., 44-pin TQFP 63 dB Pol. Rev., 32-pin QFN	Tray
Le79555-3VC Le79555-3QC	52 dB No Pol. Rev., 44-pin TQFP 52 dB No Pol. Rev., 32-pin QFN	Tray
Le79555-4VC Le79555-4QC	63 dB No Pol. Rev., 44-pin TQFP 63 dB No Pol. Rev., 32-pin QFN	Tray
Green Packages[1]		
Device	**Performance Grade/Package**	**Packing[2]**
Le79555-1BVC Le79555-1FQC	52 dB Pol. Rev., 44-pin TQFP 52 dB Pol. Rev., 32-pin QFN	Tray
Le79555-2BVC Le79555-2FQC	63 dB Pol. Rev., 44-pin TQFP 63 dB Pol. Rev., 32-pin QFN	Tray
Le79555-3BVC Le79555-3FQC	52 dB No Pol. Rev., 44-pin TQFP 52 dB No Pol. Rev., 32-pin QFN	Tray
Le79555-4BVC Le79555-4FQC	63 dB No Pol. Rev., 44-pin TQFP 63 dB No Pol. Rev., 32-pin QFN	Tray

1. *The green package meets RoHS Directive 2002/95/EC of the European Council to minimize the environmental impact of electrical equipment.*
2. *For delivery using a tape and reel packing system, add a "T" suffix to the OPN (Ordering Part Number) when placing an order.*

DESCRIPTION

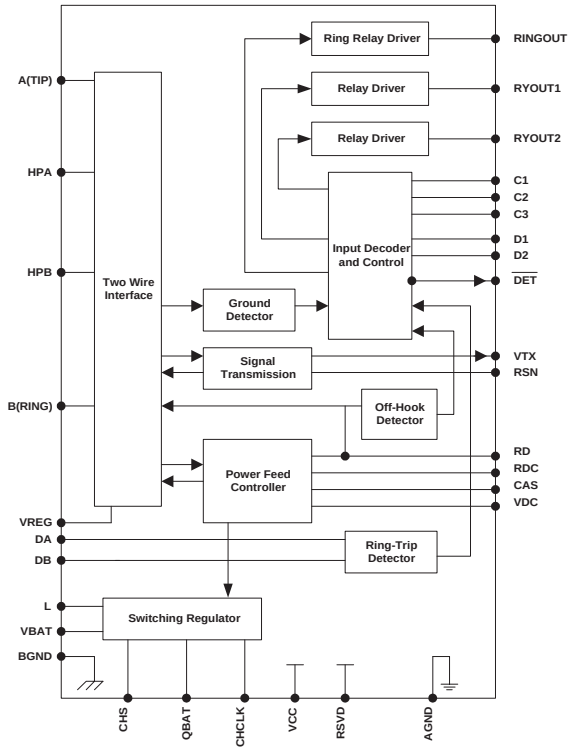
The Le79555 device, part of Legerity's VoiceEdge™ family VE580 series of devices, was designed for high-density POTS applications requiring a power saving, small footprint SLIC device. The new SLIC device fulfills today's requirements for POTS linecard markets requiring a balance of high-performance cost-effective silicon components. The Le79555 device delivers economical linecard solutions by offering power and space savings to linecard designers. The on-chip switching regulator allows for power dissipation to be minimized for the entire system. Another benefit is that the device is offered in a reduced footprint package type, a 44-pin TQFP. This small footprint saves designers board space, thus increasing the density or number of lines on the board.

Legerity offers a range of compatible SLAC™ devices providing a complete line circuit that can be optimized for varying requirements. The SLIC device is designed to operate with a range of SLAC devices from low cost, non-programmable to more advanced, highly programmable options viable for a range of applications.

RELATED LITERATURE

- **080125 SLIC Switcher Circuit Application Note**
- **080725 Le79555 Switching Regulator Applications**
- **080753 Le58QL02/021/031 QLSLAC™ Data Sheet**
- **080754 Le58QL061/063 QLSLAC™ Data Sheet**

BLOCK DIAGRAM



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PRODUCT DESCRIPTION

The Le79555 device is designed for short loop and long loop high-density POTS applications requiring a power saving, small footprint SLIC. The Le79555 device boasts increased power savings over Legerity's other POTS solutions by using an internal switching regulator for each channel to enhance system power management. The switching regulator eliminates the need for a second voltage supply, commonly required for SLIC devices in POTS applications. Such elimination passes on board space and cost savings to the designers. Thus, the smaller footprint and added features of the Le79555 device allows customers to amortize the cost of common hardware across more channels and increase the line density per board. Additionally, the Le79555 device gives line card designers a simple control interface that supports six control states: Active, Ringing, Standby, Disconnect, Reverse Polarity, and Tip Open. The Le79555 device is a low cost, high performance device providing key features required for POTS markets worldwide, including: low power dissipation and ground key detection, as well as all of the features offered currently by Legerity's Transformer SLIC family, Le7920/22.

BLOCK DESCRIPTIONS

Two-Wire Interface

The two-wire interface provides DC current and sends voice signals to a telephone apparatus connected to the line card with a two-wire line. The two-wire interface also receives the returning voice signals from the telephone.

Ground Detector

The ground detector block performs ground start and ground key detection, as well as automatically detects a ring-ground fault. Therefore, when the longitudinal current is greater than the ground key detector threshold, IGK, in either Active, Standby, or Tip Open, the $\overline{\text{DET}}$ will go low. Note that when the device is in Active or Standby, $\overline{\text{DET}}$ may be an indication of off-hook, ground fault, or both.

Signal Transmission

The RSN input current controls the receive current sent to the two-wire interface. The AC line voltage is sensed by differential amplifiers between the A and HPA leads, and between HPB and B leads. The outputs of these amplifiers are equal to the AC metallic components of the line voltages. The transmission circuit also contains a longitudinal feedback circuit to shunt longitudinal signals to a DC bias voltage. The longitudinal feedback does not affect metallic signals.

Power Feed Controller

The power feed controller has three sections: (1) the battery feed circuit, (2) the reverse polarity circuit, and (3) the bias circuit. The battery feed circuit regulates the amount of DC current and voltage supplied to the telephone over a wide range of loop resistance. The reverse polarity circuit provides the capability to reverse the loop current for pay telephone key pad disable and other applications. The bias circuit provides a reference voltage, which is offset from the subscriber line voltage. The reference voltage controls the switched mode regulator, which minimizes SLIC power consumption by providing the minimum supply voltage needed by the line drivers for proper operation.

Switching Regulator

A switching regulator function is implemented on the chip with a few external components. The power feed controller generates a reference voltage which is the minimum voltage required to feed the output line amplifiers. The efficiency of the switching regulator (>80%) minimizes both the on-chip power dissipation and the system power dissipation. This is particularly important for short loops operating at high currents which otherwise cause high power dissipation.

Input Decoder and Control

The input decoder and control block provides a means for a microprocessor or SLAC IC to control such system functions as line activate, on-hook transmission, ringing, and reverse polarity. The input decoder and control block has TTL-compatible inputs, which set the operating states of the SLIC. It also provides the supervision signal sent back to the controller.

Off-Hook Detector

The most important loop monitoring function is off-hook detection. The two-wire interface produces a current equal in magnitude to the loop current divided by a constant, and sends it out on the RD pin. An external resistor and capacitor (RD and CD) connect the RD pin to ground. The value of the voltage across resistor R_D is proportional to the current leaving the RD pin times the value of R_D. The $\overline{\text{DET}}$ pin will show a logic Low when this voltage rises above a threshold.

Ring-Trip Detector

During the Ringing state, the DA pin is more positive than the DB pin, and the $\overline{DET}$ pin will show high to indicate the on hook. When an off hook condition occurs, the DB pin becomes more positive than the DA pin, and the $\overline{DET}$ pin will go low to indicate an off-hook.

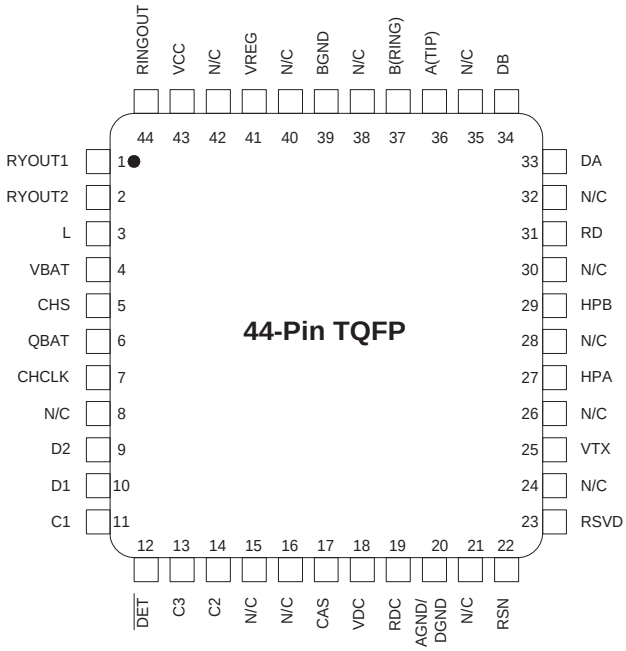
Ring Relay Driver

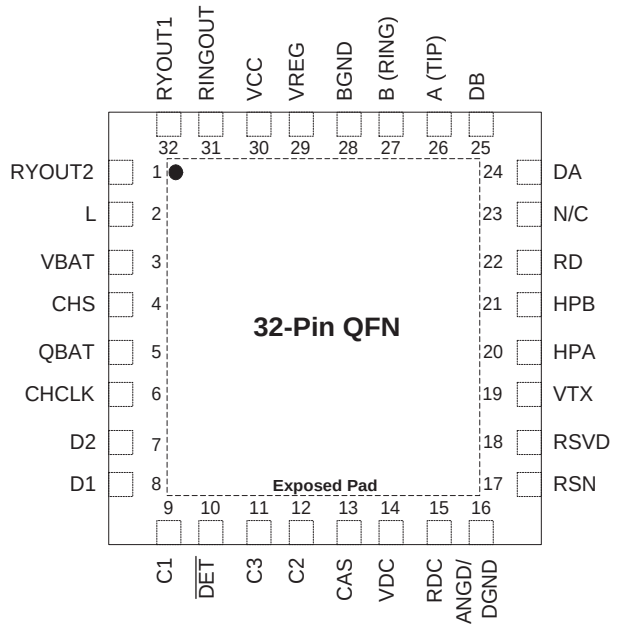
The ring relay driver is active only in the Ringing state.

Relay Driver

A relay driver is activated by logic Low at either input pin, D1, or D2. D1 controls relay driver RYOUT1; D2 controls relay driver RYOUT2.

CONNECTION DIAGRAMS





Note:

1. *Pin 1 is marked for orientation.*
2. *N/C = No Connect*
3. *RSVD = Reserved*
4. *There is VBAT potential on the exposed pad. Do not connect to GND pin.*

PIN DESCRIPTIONS

Pin Name	Type	Description
AGND/ DGND	Ground	Analog and digital ground.
A(TIP)	Output	Output of A(TIP) power amplifier.
BGND	Ground	Battery (power) ground.
B(RING)	Output	Output of B(RING) power amplifier.
C3–C1	Input	SLIC control pins. C3 is MSB and C1 is LSB.
CAS	Capacitor	Anti-Saturation pin for capacitor to filter reference voltage when operating in anti-saturation region.
CHCLK	Input	(Chopper Clock) Input to switching regulator. f = 200 to 600 kHz.
CHS	Input	(Chopper Stabilization) Connection for external stabilization components.
D2–D1	Input	Relay Driver Control. D1 and D2 control the relay drivers RYOUT1 and RYOUT2. Logic Low on D1 activates the RYOUT1 relay driver. Logic Low on D2 activates the RYOUT2 relay driver.
DA	Input	Negative input to ring-trip comparator.
DB	Input	Positive input to ring-trip comparator.
$\overline{\text{DET}}$	Output	Hook-switch detector. A logic Low indicates that selected condition is detected. The detect condition is selected by the logic inputs (C3–C1). The output is open-collector with a built-in 15 kΩ pull-up resistor.
HPA	Capacitor	A (TIP) side of high-pass filter capacitor.
HPB	Capacitor	B (RING) side of high-pass filter capacitor.
L	Output	(Switching Regulator Power Transistor) Connection point for filter inductor and anode of catch diode. This pin will have up to 60 V of pulse waveform on it, and it must be isolated from sensitive circuits. Care must be taken to keep the diode connections short because of the high currents and di/dt.
N/C	—	No Connect. This pin is not internally connected.
QBAT	Battery	(Quiet Battery) Filtered battery supply for the signal-processing circuits.
RD	Resistor	Detector threshold set and filter pin.
RDC	Resistor	Connection point for the DC feed current programming network. The other end of the network connects to the receiver summing node (RSN).
RINGOUT	Output	Ring Relay Driver. Open-collector driver with emitter internally connected to BGND.
RSN	Input	Receive Summing Node. In the Active, Reverse Polarity, and Tip Open states, the metallic current (both AC and DC) between A(TIP) and B(RING) is equal to 500 times the current into this pin. The networks which program receive gain, two-wire impedance, and feed resistance all connect to this node.
RYOUT1	Output	Relay/Switch Driver. Open-collector driver with emitter internally connected to BGND.
RYOUT2	Output	Relay/Switch Driver. Open-collector driver with emitter internally connected to BGND.
VBAT	Battery	Most negative battery.
RSVD	—	This is a reserved pin and must always be left open.
VCC	Power Supply	+5 V power supply.
VDC	Output	Output that is proportional to the line voltage: $VDC = KDC \bullet VAB$. KDC is the VDC scale factor.
VREG	Input	(Regulated Voltage) Provides internal negative power supply and connection point for inductor, filter capacitor, and chopper stabilization.
VTX	Output	Transmit Audio. This output is a 0.50 gain version of the A(TIP) and B(RING) metallic voltage. VTX also sources the two-wire input impedance programming network.
Exposed Pad	Battery	This must be connected to the most negative battery on the SLIC device pin side of D_{VBH} shown on the test and application circuits.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can effect device reliability.

Storage temperature	–55 to +150ºC
V_{CC} with respect to AGND	–0.4 to +7.0 V
V_{BAT} with respect to AGND:	
Continuous	+0.4 to –70 V
10 ms	+0.4 to –75 V
BGND with respect to AGND	+3 to –3 V
A (TIP) or B (RING) to BGND:	
Continuous	V_{BAT} to +1 V
10 ms (f = 0.1 Hz)	–70 to +5 V
1 µs (f = 0.1 Hz)	–80 to +8 V
250 ns (f = 0.1 Hz)	–90 to +12 V
Current from A (TIP) or B (RING)	±150 mA
RINGOUT/RYOUT1,2 current	50 mA
RINGOUT/RYOUT1,2 voltage	BGND to +7 V
RINGOUT/RYOUT1,2 transient	BGND to +10 V
DA and DB inputs:	
Voltage on ring-trip inputs	V_{BAT} to 0 V
Current into ring-trip inputs	±10 mA
C3–C1,D2–D1, CHCLK Input voltage	–0.4 to V_{CC} + 0.4 V
Maximum power dissipation, continuous, T_A = 70°C, No heat sink (See note)	
In 44-pin TQFP package	1.4 W
In 32-pin QFN package	3.0 W
Thermal Data:	θ_{JA}
In 44-pin TQFP package	52°C/W typ
In 32-pin QFN package	25° C/W typ
ESD Immunity (Human Body Model)	JESD22 Class 1C compliant

Notes:

Thermal limiting circuitry on-chip will shut down the circuit at a junction temperature of about 165° C. Operation above 145° C junction temperature may degrade device reliability.

The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Specified performance requires that the exposed thermal pad be soldered to an equally sized exposed copper surface, which, in turn, conducts heat through multiple vias to a large internal copper plane.

Package Assembly

The standard (non-green) package devices are assembled with industry-standard mold compounds, and the leads possess a tin/lead (Sn/Pb) plating. These packages are compatible with conventional SnPb eutectic solder board assembly processes. The peak soldering temperature should not exceed 225°C during printed circuit board assembly.

The green package devices are assembled with enhanced environmental compatible lead (Pb), halogen, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes. The peak soldering temperature should not exceed 245°C during printed circuit board assembly.

Refer to IPC/JEDEC J-Std-020B Table 5-2 for the recommended solder reflow temperature profile.

Operating Ranges

Legerity guarantees the performance of this device over commercial (0 to 70º C) and industrial (-40 to 85ºC) temperature ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore GR-357-CORE Component Reliability Assurance Requirements for Telecommunications Equipment.

Ambient temperature	–40 to +85°C
V_{CC}	4.75 to 5.25 V
V_{BAT}	–40 to –58 V
AGND	0 V
BGND with respect to AGND	–100 to +100 mV
Load resistance on VTX to ground	20 kΩ min

SPECIFICATIONS

Refer to Figure 9, on page 16 for the Le79555 test circuit specifications.

Transmission Performance

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Two-wire return loss	200 Hz to 3.4 kHz	26			dB	1, 4
Analog output (VTX) impedance			1	20	Ω	4
Analog (VTX) output offset voltage		–50		+50	mV	
Overload level, 2-wire	Active state	2.5			Vpk	2a
Overload level	On hook, R_{LAC} = 600 Ω	1.1				2b
THD (Total Harmonic Distortion)	0 dBm +7 dBm		–64 –55	–50 –40	dB	5
THD, On hook	0dBm, R_{LAC} = 600 Ω			–36		5

Longitudinal Capability

(See Figure 6.)

Description	Test Conditions (See Note 1)	Perf. Grade	Min	Typ	Max	Unit	Note
Longitudinal to metallic L-T, L-4 200 Hz to 1 kHz	Normal Polarity: 0ºC to +70ºC -40ºC to +85ºC 0ºC to +70ºC -40ºC to +85ºC Reverse Polarity: -40ºC to +85ºC 0ºC to +70ºC -40ºC to +85ºC	 -2,-4 -2,-4 -1,-3 -1,-3 -2 -1 -1	 63 58 52 50 54 52 50			dB	 4 4 4 4
Longitudinal to metallic L-T, L-4 1 kHz to 3.4 kHz	Normal Polarity: 0ºC to +70ºC -40ºC to +85ºC 0ºC to +70ºC -40ºC to +85ºC Reverse Polarity: -40ºC to +85ºC 0ºC to +70ºC -40ºC to +85ºC	 -2,-4 -2,-4 -1,-3 -1,-3 -2 -1 -1	 58 53 52 50 53 52 50				 4 4 4 4
Longitudinal signal generation 4-L	200 Hz to 3.4 kHz		40				
Longitudinal current per pin (A or B)	Active state		17	27		mArms	4, 8
Longitudinal impedance at A or B	0 to 100 Hz			25		Ω/pin	4

Idle Channel Noise

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
C-message weighted noise	R_L = 600Ω, 0º to +70ºC R_L = 600Ω, –40º to +85ºC		7	+10 +12	dBrnC	4
Psophometric weighted noise	R_L = 600Ω, 0º to +70ºC R_L = 600Ω, –40º to +85ºC		–83	–80 –78	dBmp	

Insertion Loss and Balance Return Signal

(See Figure 4 and Figure 5.)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Gain accuracy, 4- to 2-wire	0 dBm, 1 kHz 0º to +70 ºC	–0.10	0	+0.10	dB	3
	0 dBm, 1 kHz –40º to +85 ºC	–0.15		+0.15		3, 4
Gain accuracy 2- to 4-wire, 4- to 4-wire	0 dBm, 1 kHz 0º to +70 ºC	–6.12	–6.02	–5.92		3
	0 dBm, 1 kHz –40º to +85 ºC	–6.17		–5.87		3, 4
Gain accuracy, 4- to 2-wire	On hook	–0.35		+0.35		3,4
Gain accuracy, 2- to 4-wire, 4- to 4-wire	On hook	–6.37	–6.02	–5.67		
Gain accuracy over frequency	300 to 3.4 kHz relative to 1 kHz 0º to +70 ºC	–0.10		+0.10		3
	300 to 3.4 kHz relative to 1 kHz –40º to +85 ºC	–0.15		+0.15		3, 4
Gain tracking	+3 dBm to –55 dBm relative to 0 dBm 0º to +70 ºC	–0.10		+0.10		3, 4
	+3 dBm to –55 dBm relative to 0 dBm –40º to +85 ºC	–0.15		+0.15		3, 4
Gain tracking On hook	0 dBm to –37 dBm	–0.15		+0.15		3,4
	+3 dBm to 0 dBm	–0.35		+0.35		

Line Characteristics

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
I_L, Short Loops, Active state		22.5	24.5	26.5	mA	
I_L, Long Loops, Active state	R_L = 2010 Ω	20	22.5			
I_L, Standby state	R_L = 2010 Ω T_A = 25 ºC	15				
	R_L = 600 Ω (current limit)	18	30			
I_LLIM	Active, A and B to ground		75	120		
K_{DC} (V_{DC} Scaling)	$K_{DC} = \frac{V_{DC}}{V_{AB}}$ R_L = 300 to 1500 Ω	0.052	0.055	0.058		
V_{AB}, Open Circuit voltage	Active state	42.75	44		V	
I_A, Leakage, Tip Open state	R_L = 0			100	µA	
I_B, Current, Tip Open state	B to GND	15	30	56	mA	
V_A, Active state	RA to BAT = 7 kΩ, RB to GND = 100 Ω	–7.5	–5		V	4

Power Supply Rejection Ratio

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
V_{CC}, ACTIVE STATE	50 Hz to 3.4 kHz (V_{RIPPLE} = 100 MV RMS)	30	40		dB	5
V_{BAT}, ACTIVE STATE	50 Hz to 3.4 kHz Off-hook constant current region (V_{RIPPLE} = 500 MV PP)	28	50			
Effective internal resistance	CAS pin to V_{BAT}	85	170	255	kΩ	4

Power Dissipation

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
On-hook, Standby state	R_L = Open		45	70	mW	
On-hook Active State	R_L = Open		130	190		
Off-hook, Standby state			860	1200		
Off-hook Active State			350	400		

Supply Currents

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
I_{CC}, On-hook V_{CC} supply current	Standby State		2.5	3.2	mA	
	Active/Polarity Reversed States		4.55	6.0		
	Open Circuit, R_L = Open		2.5			
	Ringing, R_L = Open		6.0			
I_{BAT}, On-hook V_{BAT} supply current + V_{REG} supply current	Standby State		0.65	0.9		
	Active/Polarity Reversed States		2.3	4.0		
	Open Circuit, R_L = Open		0.5			
	Ringing, R_L = Open		1.5			

RFI Rejection

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
VAB, RMS	100 kHz to 30 MHz, (See Figure 8)			1.0	mVrms	4

Receive Summing Node (RSN)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
RSN DC voltage	I_{RSN} = 0 mA		0		V	4
RSN impedance	200 Hz to 3.4 kHz		10	20	Ω	

Logic Inputs

(C3-C1, D2-D1, and CHCLK)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
V_{IH}, Input High voltage		2.0			V	
V_{IL}, Input Low voltage				0.8		
I_{IH}, Input High current		–75		40	µA	
I_{IL}, Input Low current		–400				

Logic Output $\overline{\text{DET}}$

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
V_{OL}, Output Low voltage	I_{OUT} = 0.3 mA			0.40	V	
V_{OH}, Output High voltage	I_{OUT} = –0.1 mA	2.4				

Ring-Trip Detector Input

(DA, DB)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Bias Current		–500	–50		nA	
Offset voltage	Source resistance = 2 MΩ	–50	0	+50	mV	6

Loop Detector

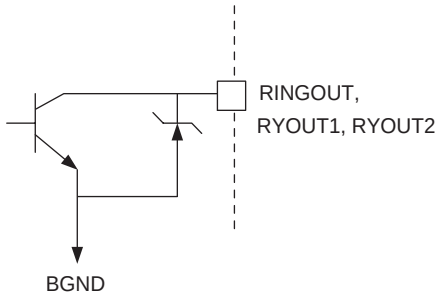
Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Off-hook threshold	R_D = 35.4 kΩ	9.4	11.7	14.0	mA	
On-hook threshold	R_D = 35.4 kΩ	8.8	10.4	12.0		
Hysteresis	R_D = 35.4 kΩ		1.3			
IGK, Ground-key detector threshold	R_L from BX to GND Active, Standby, and Tip open	5	9	13		

Relay Driver Output

(RINGOUT, RYOUT1, RYOUT2)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
On voltage	I_{OL} = 40 mA		+0.3	+0.7	V	
Off leakage	V_{OH} = +5 V			100	µA	
Zener breakover	I_Z = 100 µA	6	7.2		V	
Zener On voltage	I_Z = 30 mA		8			

Figure 1. Relay Driver Schematic



1. *Unless otherwise noted, R_L = 600 Ω. Also, refer to the Le79555 device test circuit in Figure 9, on page 16.*
2.
   a) *Overload level is defined as THD = 1%.*
   b) *Overload level is defined as THD = 1.5%.*
3. *Balance return signal is the signal generated at V_{TX} by V_{RX}. This specification assumes that the two-wire, AC-load impedance matches the programmed impedance.*
4. *Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
5. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*
6. *Tested with 0 Ω source impedance. 2 MΩ is specified for system design only.*
7. *Group delay can be greatly reduced by using a Z_T network such as that shown in Figure 7. The network reduces the group delay to less than 2 µs and increases 2WRL. The effect of group delay on line card performance also may be compensated for by synthesizing complex impedance with the QLSLAC™ device.*
8. *Minimum current level guaranteed not to cause a false loop detect.*

Table 1. SLIC Device Decoding

State	C3	C2	C1	Two-Wire Status	$\overline{\text{DET}}$ Output
0	0	0	0	Reserved	X
1	0	0	1	Reserved	X
2	0	1	0	Active Reverse Polarity (-1, 2 devices)	Loop detector
3	0	1	1	Tip Open	Ring Ground (see note)
4	1	0	0	Open Circuit	Ring trip
5	1	0	1	Ringing	Ring trip
6	1	1	0	Active	Loop detector
7	1	1	1	Standby	Loop detector

Note:

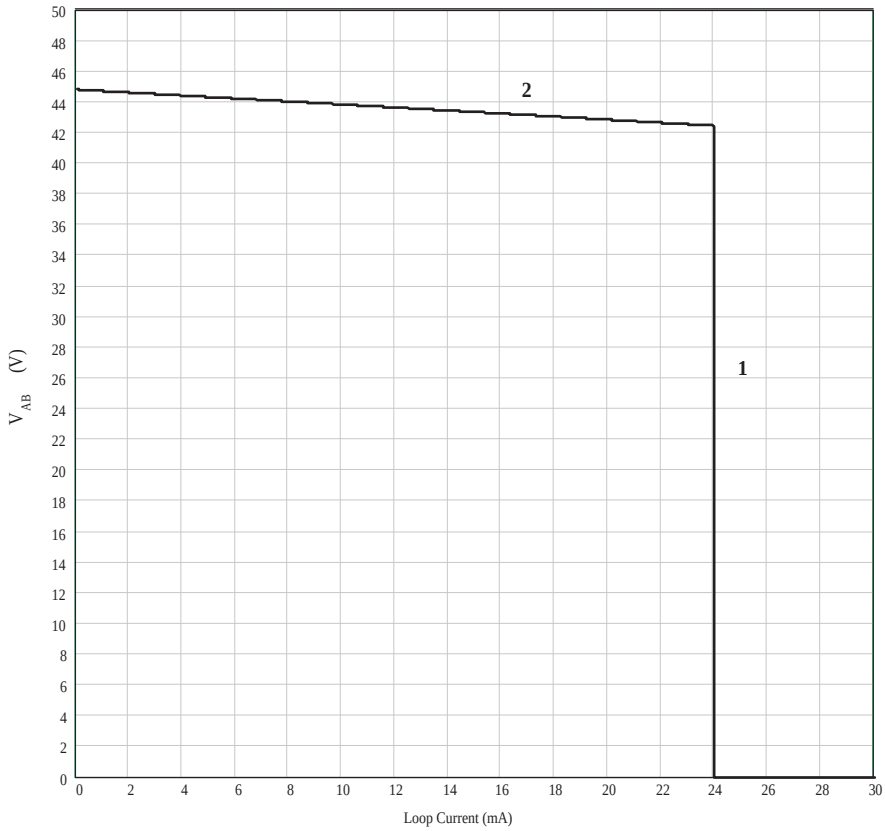
Ring ground detection in Tip Open is automatic. If longitudinal current is greater than IGK in Active, Standby, or Tip Open, the $\overline{DET}$ will go low. Therefore, if in Active or Standby, $\overline{DET}$ may be an indication of off hook, ground fault, or both.

Table 2. User-Programmable Components

$Z_T = 250(Z_{2WIN} - 2R_F)$	Z_T is connected between the VTX and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired 2-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G_{42L}} \bullet \frac{500Z_T}{Z_T + 250(Z_L + 2R_F)}$	Z_{RX} is connected from VRX to RSN. Z_T is defined above, and G_{42L} is the desired receive gain. Z_L = Load Impedance, AD to BD.
$R_{DC1} + R_{DC2} = \frac{625}{I_{LOOP}}$ $C_{DC} = 1.5\ ms \bullet \frac{R_{DC1} + R_{DC2}}{R_{DC1} \bullet R_{DC2}}$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the R_{DC} pin. R_{DC1} and R_{DC2} are approximately equal. $I_{\mathbf{LOOP}}$ is the desired loop current in the constant-current region.
$I_{T_{OFF}} = \frac{414}{R_D}$, $I_{T_{ON}} = \frac{368}{R_D}$, $C_D = \frac{0.5\ ms}{R_D}$ ($I_{Threshold\ on\ to\ off\ hook}$) ($I_{Threshold\ off\ to\ on\ hook}$)	R_D and C_D form the network connected from R_D to AGND/DGND and I_T is the threshold current between on-hook and off-hook.
$C_{CAS} = \frac{1}{170\ k\Omega \bullet 2\pi \bullet f_c}$	C_{CAS} is the regulator filter capacitor and f_c is the desired filter cut-off frequency.
$I_{STANDBY} = \frac{\lvert V_{BAT}\rvert - 3\ V}{400\ \Omega + R_L}$	Standby loop current (resistive region).

DC FEED CHARACTERISTICS

Figure 2. Load Line (Typical)



Regions:

1. *Constant current region:*

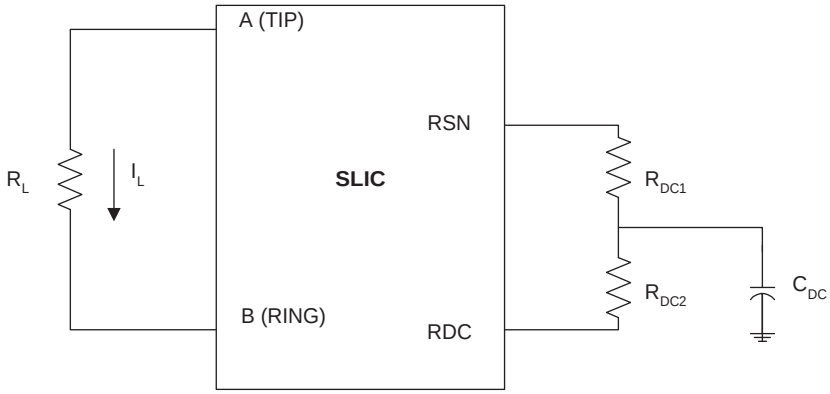
$$V_{AB} = I_L R_L' = \frac{625}{R_{DC}} R_L' \text{ , where } R_L' = R_L + 2R_F$$

$$R_{DC} = R_{DC1} + R_{DC2}$$

2. *Battery tracking anti-sat:*

$$V_{AB} = |BAT| - V_{Diode} - 7.2\ V - I_L(R_{DC}/210)$$

Figure 3. Feed Programming



TEST CIRCUIT SCENARIOS

Figure 4. Two-to-Four-Wire Insertion Loss

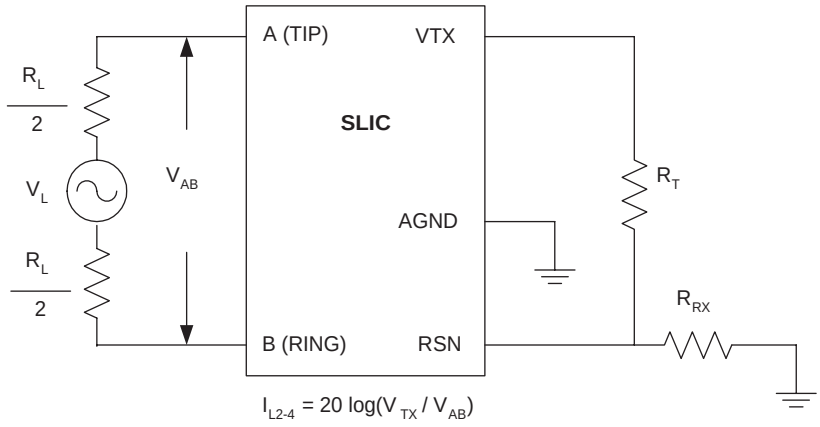


Figure 5. Four-to-Two-Wire Insertion Loss and Balance Return Signal

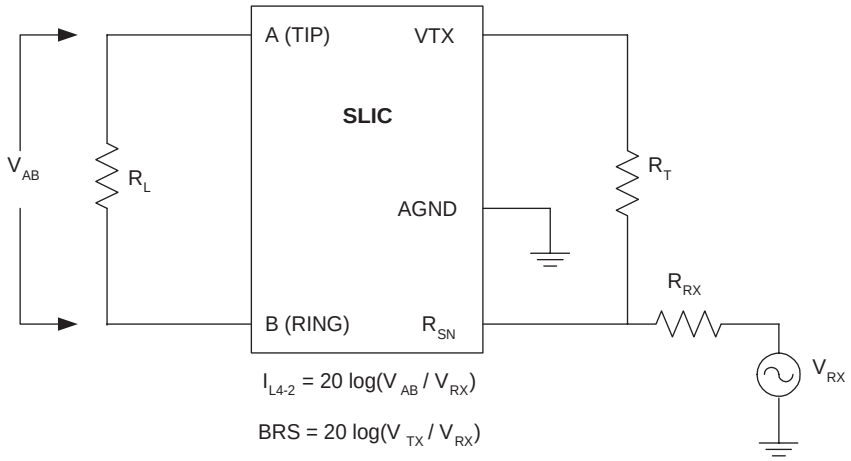
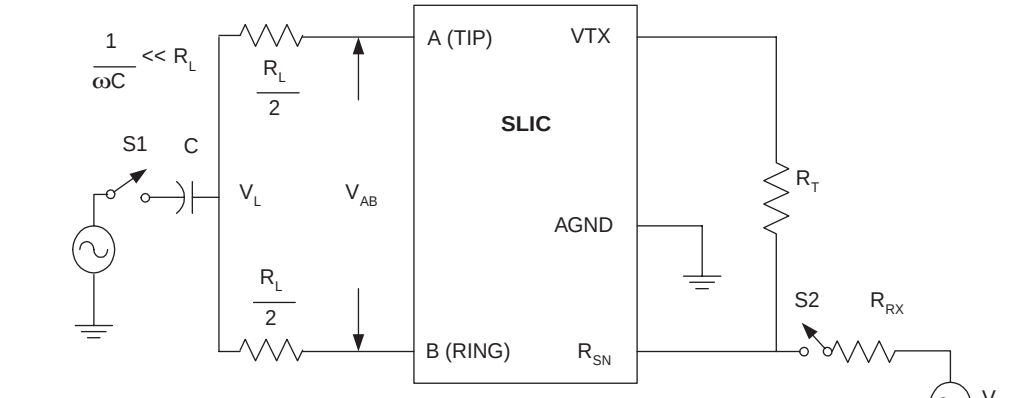


Figure 6. Longitudinal Balance



S2 Open, S1 Closed

L-T Long. Bal. = $20 \log(V_{AB} / V_L)$

L-4 Long. Bal. = $20 \log(V_{TX} / V_L)$

S2 Closed, S1Open

4-L Long. Sig. Gen. = $20 \log(V_L / V_{RX})$

Figure 7. Two-Wire Return Loss

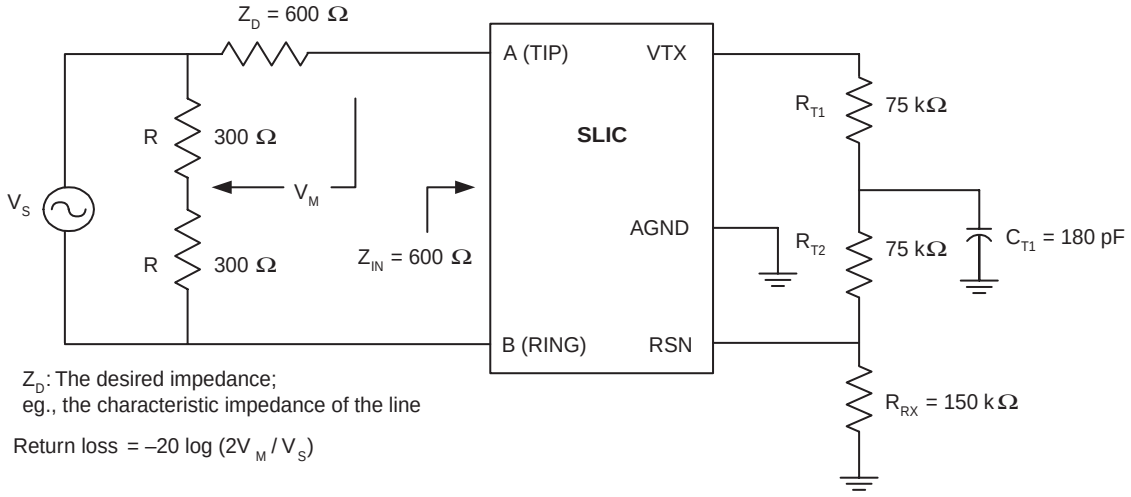


Figure 8. RFI

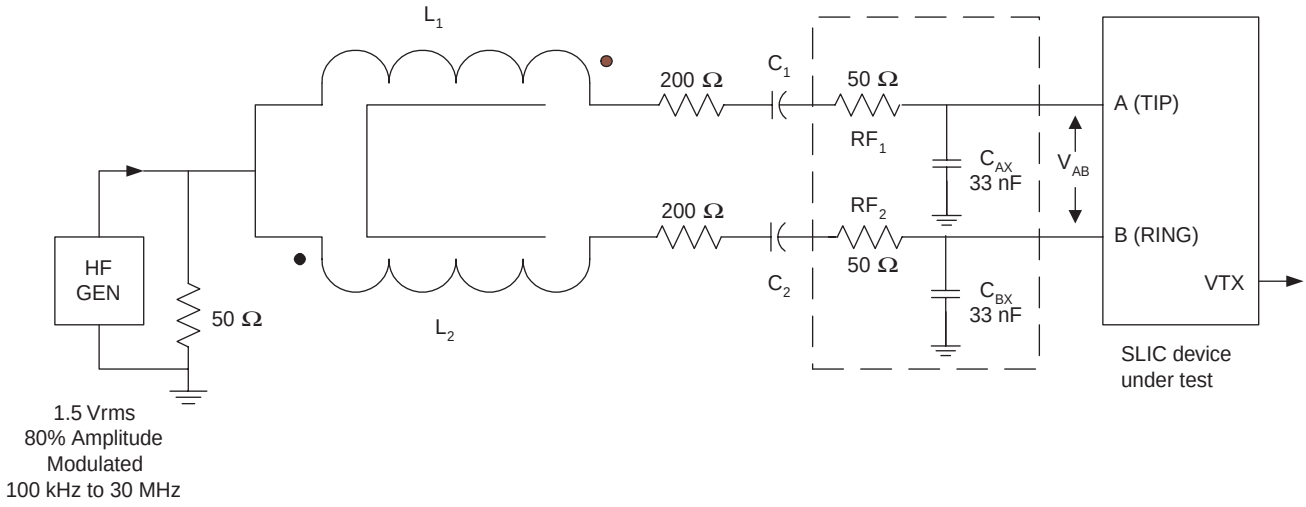
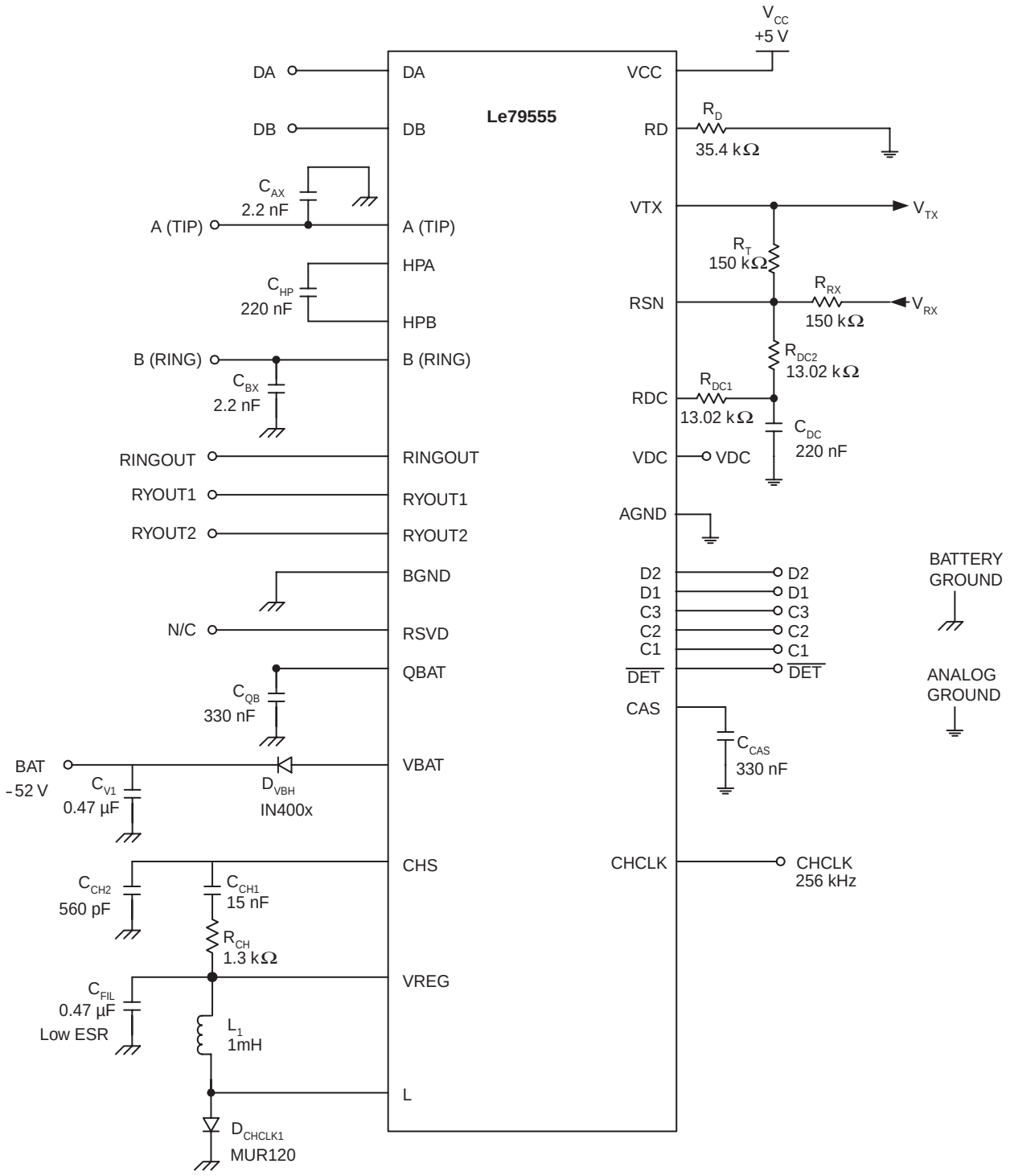
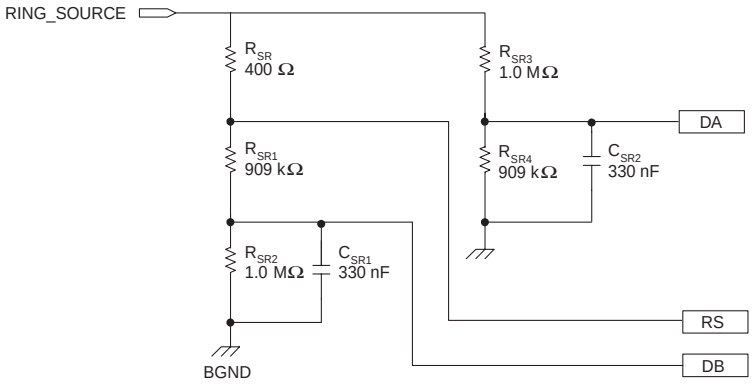
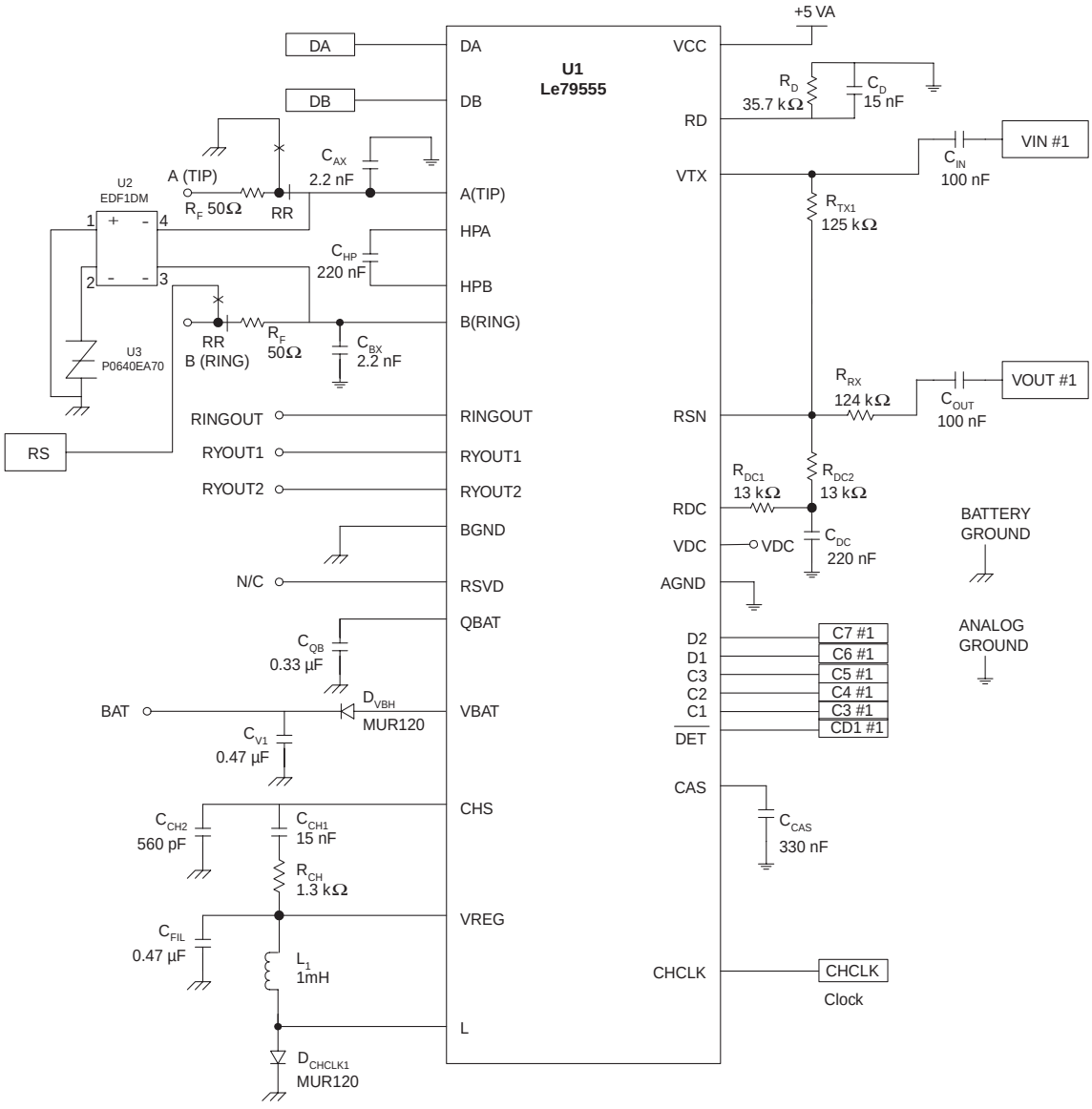


Figure 9. Le79555 Engineering Test Circuit



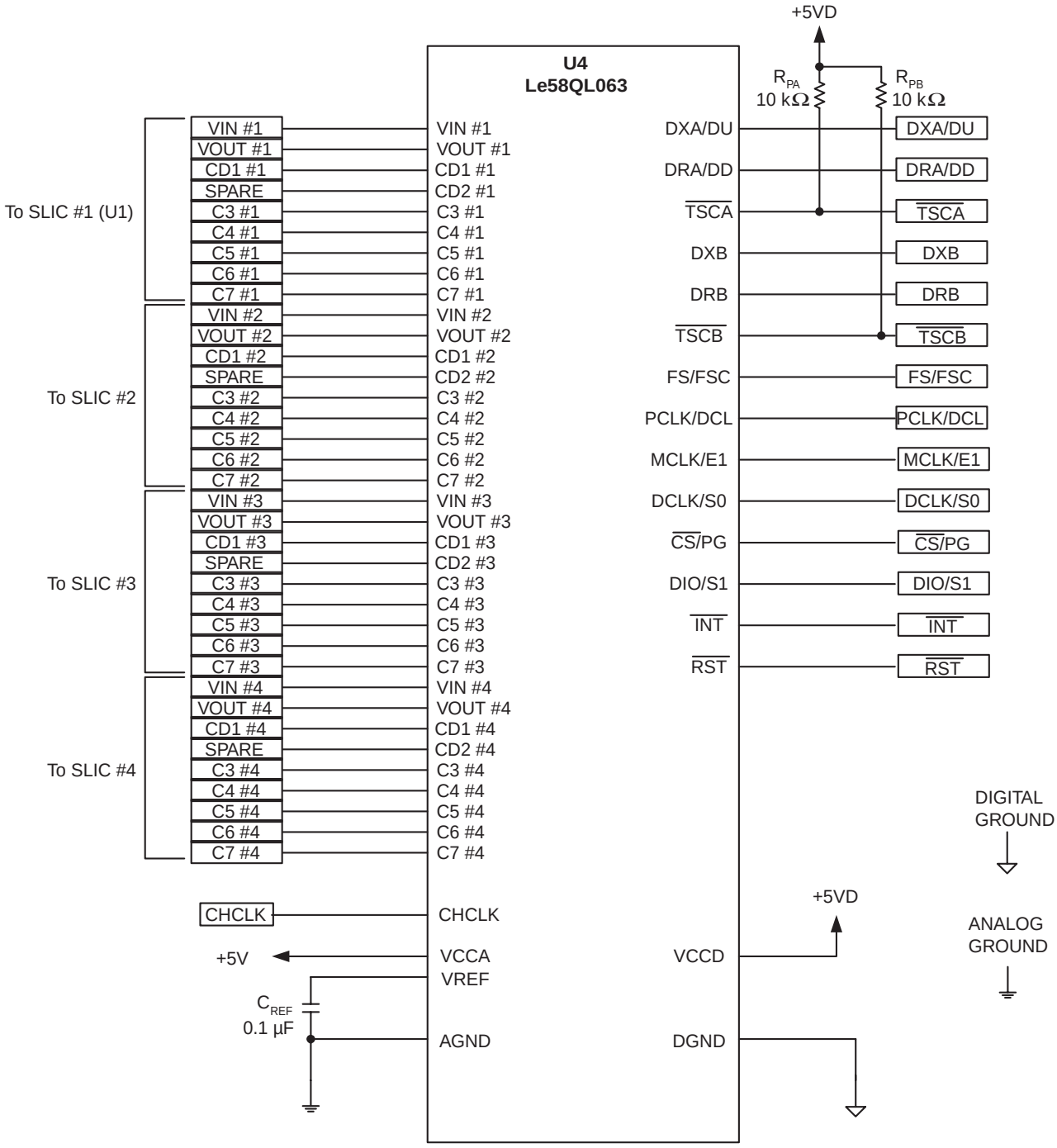
APPLICATION CIRCUITS





Note:

1. *Protection circuitry does not need to be battery tracking.*
2. *For CHCLK operation between 190 kHz and 290 kHz, L1 is recommended to be 2 mH. For CHCLK operation between 290 kHz and 600 kHz, L1 is recommended to be 1 mH.*


+5VD
U4
Le58QL063
R_{PA}
10 kΩ
R_{PB}
10 kΩ
To SLIC #1 (U1)
To SLIC #2
To SLIC #3
To SLIC #4
VIN #1
VOUT #1
CD1 #1
SPARE
C3 #1
C4 #1
C5 #1
C6 #1
C7 #1
VIN #2
VOUT #2
CD1 #2
SPARE
C3 #2
C4 #2
C5 #2
C6 #2
C7 #2
VIN #3
VOUT #3
CD1 #3
SPARE
C3 #3
C4 #3
C5 #3
C6 #3
C7 #3
VIN #4
VOUT #4
CD1 #4
SPARE
C3 #4
C4 #4
C5 #4
C6 #4
C7 #4
CD2 #1
CD2 #2
CD2 #3
CD2 #4
DXA/DU
DRA/DD
TSCA
DXB
DRB
TSCB
FS/FSC
PCLK/DCL
MCLK/E1
DCLK/S0
CS/PG
DIO/S1
INT
RST
CHCLK
+5V
VCCA
VREF
C_{REF}
0.1 µF
AGND
VCCD
DGND
DIGITAL
GROUND
ANALOG
GROUND

LINE CARD PARTS LIST

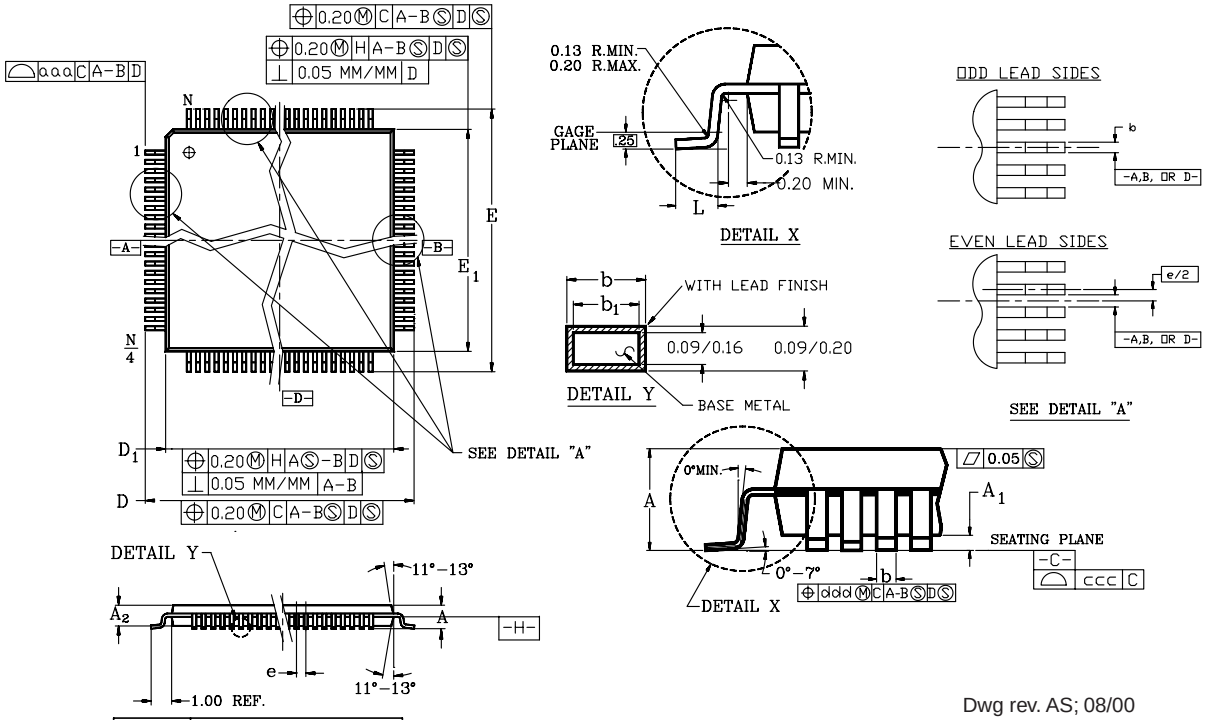
The following list defines the parts and part values required to meet target specification limits for one channel.

Item	Quantity	Type	Value	Tol.	Rating	Comments	Note
C_{CH2}	1	Capacitor (COG)	560 pF	5%	50 V		
C_{AX}, C_{BX}	2	Capacitor (X7R)	2200 pF	20%	100 V		
C_{CH1}	1	Capacitor (X7R)	15 nF	10%	50 V		
C_{HP}	1	Capacitor (X7R)	220 nF	20%	100 V		
C_{DC}	1	Capacitor (X7R)	220 nF	20%	16 V		
C_{CAS}	1	Capacitor (X7R)	330 nF	20%	100 V		
C_{QB}	1	Capacitor (X7R)	330 nF	20%	100 V		
C_{V1}	1	Capacitor (X7R)	470 nF	20%	100 V		
C_{FIL}	1	Capacitor (Low ESR)	470 nF	20%	100 V		
C_D	1	Capacitor (X7R)	15 nF	10%	16 V		
R_F	1	Resistor Hybrid	50	1%			
R_{CH}	1	AXIAL/SMT	1.3 k	1%	0.1 W		
RDC1, RDC2	2	SMT	13.0 k	1%	0.1 W		
RD	1	SMT	35.7 k	1%	0.1 W		
RT	1	SMT	124 k	1%	0.1 W		
RRX	1	SMT	124 k	1%	0.1 W		
D_{VBH}, D_{CHCLK1}	2	**MUR 120 (D0-41) DIODE**			1 A, 100 V		
L1	1	Coiltronics SD25-102 Inductor	1.0 mH	(20 > R > 5)	100 mA		
U3	1	Sidactor P0640EA70					
U2	1	Diode Bridge EDF1DM					
U1	1	Le79555					
U4	1	Le58QL063					
C_{IN}, C_{OUT}, C_{REF}	3	Capacitor (X7R)	100 nF	20%	16 V		
RPA, RPB	2	SMT	10 k	1%	0.25 W		
R_{SR2}, R_{SR3}	2	SMT	1 M	1%	0.25 W		
R_{SR4}, R_{SR1}	2	SMT	909 k	1%	0.25 W		
C_{SR1}, C_{SR2}	2	Capacitor (X7R)	330 nF	20%	100 V		
R_{SR}	1	Resistor Hybrid	400	1%			

PHYSICAL DIMENSIONS

44-Pin TQFP

TQFP 044



Dwg rev. AS; 08/00

PACKAGE	TQFP 044		
JEDEC	MS-026 (C) ACB		
SYMBOL	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	--	0.15
A2	0.95	1.00	1.05
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
L	0.45	0.60	0.75
N	44		
e	0.80 BASIC		
b	0.30	0.37	0.45
b1	0.30	0.35	0.40
TOLERANCES OF FORM AND POSITION			
ccc	0.10		
ddd	0.20		
aaa	0.20		

NOTES:

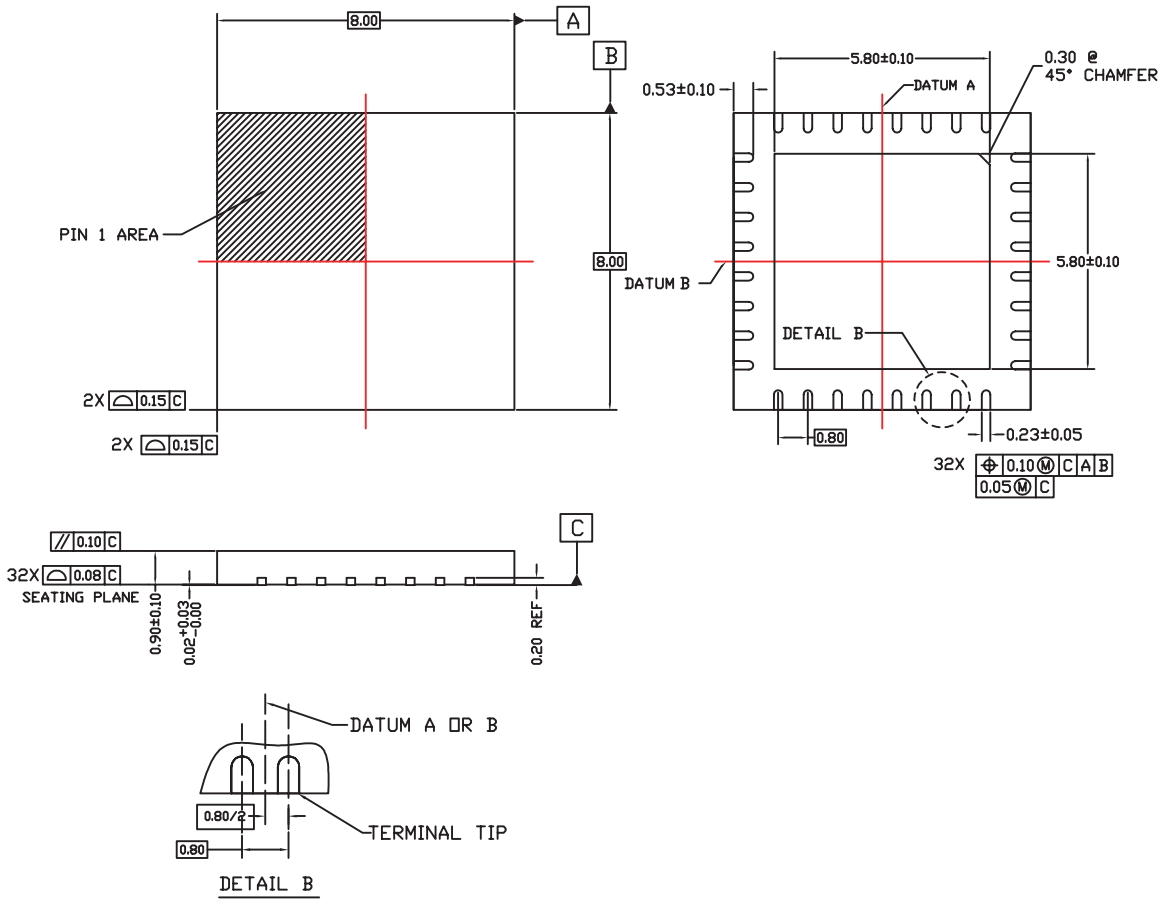
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DATUM PLANE -H- IS LOCATED AT THE MOLD PARTING LINE AND IS COINCIDENT WITH THE BOTTOM OF THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY.
3. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.254mm PER SIDE. DIMENSIONS "D1" AND "E1" INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-
4. DIMENSION "B" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
5. CONTROLLING DIMENSIONS: MILLIMETER.
6. DIMENSIONS "D" AND "E" ARE MEASURED FROM BOTH INNERMOST AND OUTERMOST POINTS.
7. DEVIATION FROM LEAD-TIP TRUE POSITION SHALL BE WITHIN ±0.076 MM. FOR PITCH >0.5mm. AND WITHIN ±0.04 FOR PITCH ≤ 0.5 mm.
8. LEAD COPLANARITY SHALL BE WITHIN: (REFER TO 06-500)
   1- 0.10 mm FOR DEVICES WITH LEAD PITCH OF 0.65-0.80 mm.
   2- 0.076 mm FOR DEVICES WITH LEAD PITCH OF 0.50 mm.
   COPLANARITY IS MEASURED PER SPECIFICATION 06-500.
9. HALF SPAN (CENTER OF PACKAGE TO LEAD TIP) SHALL BE 15.30±.165{.602"±.0065"}
10. "N" IS THE TOTAL NUMBER OF TERMINALS.
11. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF THE PACKAGE BY 0.15 MILLIMETERS.
12. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-026.
13. THE 160 LEAD IS A COMPLIANT DEPOPULATION OF THE 176 LEAD MS-026 VARIATION BGA.

Note:

BSC is an ANSI standard for basic centering. Dimensions are measured in millimeters.

32-Pin QFN (8x8)

32 Lead QFN with Chamfer



Symbol	32 LEAD QFN		
	Min	Nom	Max
A	0.80	0.90	1.00
A2		0.57 REF	
b	0.18	0.23	0.28
D		8.00 BSC	
D2	5.70	5.80	5.90
E		8.00 BSC	
E2	5.70	5.80	5.90
e		0.80 BSC	
L	0.43	0.53	0.63
N		32	
A1	0.00	0.02	0.05
A3		0.20 REF	
aaa		0.20	
bbb		0.10	
ccc		0.10	

NOTES:
1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. ⌖ is in degrees.
3. N is the total number of terminals.
4. The Terminal #1 identifier and terminal numbering convention shall conform to JEP 95-1 and SSP-012. Details of the Terminal #1 identifier are optional, but must be located within the zone indicated. The Terminal #1 identifier may be either a mold or marked feature.
5. Coplanarity applies to the exposed pad as well as the terminals.
6. Reference Document: JEDEC MO-220.
7. Lead width deviates from the JEDEC MO-220 standard.

REVISION HISTORY

Revision A to B

- Updated document format.
- In the "Features" section, the following changes were made:
  - Removed "(45 mW)" from Low standby power (since it's already in the specification).
  - Changed battery voltage range from −16 V to −58 V to −40 V to −58 V.
  - Removed "(6.5 V)" from Low Off-Hook Active Overhead Voltage.
- In "Related Literature", added the "Introduction to the SLIC Family" application note.
- Added the 32-pin PLCC information to the Ordering Information and Absolute Maximum Ratings sections and added the connection diagram.
- Updated the Connection Diagram.
- Updated the Pin Description table to correct inconsistencies; added range for CHCLK.
- In the Electrical Characteristics table:
  - Updated the information in the Line Characteristics section on the Long Loops row and the VDC Accuracy row.
  - Deleted the Disconnect state information in the Power Dissipation and Supply Currents sections.
- In "Specifications", the following changes were made:
  - Added a column for performance grade in the Longitudinal Capability and Insertion Loss and Balance Return Signal tables.
  - Changed test circuit reference in the Longitudinal Capability table
  - Updated the Insertion Loss and Balance Return Signal table.
  - In the Line Characteristics table, I_L Standby state test conditions, changed the equation to R_L = 2.5 k.
  - In the Line Characteristics table, added spec for Overhead Voltage.
  - Made changes to test conditions for I_L, Long Loops, Active State; KDC (V_{DC} Accuracy); VAB, Open Circuit voltage in the Line Characteristics table.
  - Added value for CHCLK in Note 1.
- In the "DC Feed Characteristics" section, revised equations in notes and updated DC Feed Characteristics graphic.
- Changed the equation for Z_{RX} in the User-Programmables table
- Updated Engineering Test Circuit and Application Circuit graphics; added graphic for U4/Am79Q063
- Added Linecard Parts List page
- The physical dimension (PQT044) was added to the Physical Dimension section.

Revision B to C

- Removed current gain feature from the "Features" section
- Updated "Related Literature" section to include the QLSLAC data sheets
- In the "Ordering Information" table, added dashes before performance grades
- Removed package graphic from "Ordering Information" section
- Added OPNs for the QFN package in "Ordering Information"; added note regarding markings on QFN packages
- Edited "Block Descriptions" section
- In "Connection Diagrams," added pinout diagram for 32-pin QFN package; added notes regarding exposed pad and RSVD pin
- In the "Pin Descriptions" table, the following edits were made:
  - Updated the Pin Description table to correct inconsistencies
  - Edited the description of the RSN pin
  - Added range for CHCLK
  - Made minor edits to RSVD description
  - Added a sentence to the description for VDC
  - Added a row to describe the exposed pad
- In "Electrical Characteristics", "Absolute Maximum Ratings" table, the following was added:
  - Max power dissipation of 3.0 W for 32-pin QFN package
  - Thermal data for 32-pin QFN package
- Added a note regarding maximum power dissipation values under the Absolute Maximum Ratings table

- In the "Operating Ranges" table, changed the ambient temperature range to –40º to 85º C
- In "Specifications," the following changes were made:
  - "Transmission Performance" table, Overload level, edited test conditions; changed Min to 1.1; changed units to Vpk.
  - "Transmission Performance" table, THD, On-hook, edited test conditions; changed units to dB
  - "Longitudinal Capability" table, Longitudinal current per pin (A or B), added Note 4 to Note column
  - "Insertion Loss and Balance Return Signal" table, Gain Accuracy, 2-to-4 and 4-to-4 wire, changed Max from -5.82 to -5.87
  - "Insertion Loss and Balance Return Signal" table, deleted the Group delay row
  - "Line Characteristics" table, changed K_{DC} (V_{DC} Accuracy) to K_{DC} (V_{DC} Scaling)
  - "Line Characterisitcs" table, I_L, Long Loops, Active state, edited the test conditions
  - "Line Characterisitcs" table, K_{DC} (V_{DC} Scaling), edited the test conditions
  - "Power Dissipation" table, changed the description "On-hook, Active, Polarity Reversal state" to "On-Hook Active state"
  - "Power Dissipation" table, Changed Max value of Off-hook Active State from 380 mW to 400 mW
  - "Supply Currents" table, added RL = Open to Open Circuit and Ringing test conditions; deleted references to Note 4
  - "Power Dissipation" table, On-hook Standby and On-hook Active, added RL = Open to test conditions
  - Changed "Power Supply Rejection Ratio" to "Power Supply Rejection Ratio at the Two-Wire Interface"
  - "Power Dissipation" table, On-hook, Standby state, changed Max from 60 to 70
  - "Logic Inputs" table, added CHCLK as an input
  - "Logic Inputs" table, edited description of V_{IH}, Input High Voltage
  - "Logic Inputs" table, deleted row for V_{IH}, C3, CHCLK
  - "Logic Inputs" table, edited description of V_{IL}
  - "Logic Output $\overline{DET}$" table, edited test conditions
  - "Loop Detector" table, changed "On threshold" to "Off-hook threshold"
  - "Loop Detector" table, changed "Off threshold" to "On-hook threshold"
  - Extensively edited Note 1; removed Figure 2, "AC Input Impedance Programming Network"
- Made minor formatting edits to SLIC Device Decoding table
- In "User-Programmable Components", the following changes were made:
  - Edited equations for I_{TON} and I_{TOFF}
  - Edited equation for Z_{RX} and C_{CAS}.
- In "DC Feed Characteristics", edited Note 2
- In "Test Circuit Scenarios", the following changes were made:
  - Edited title of graphic "Four-to-Four-Wire Insertion Loss and Balance Return Signal"
  - Modified Longitudinal Balance graphic
  - Modified Two-Wire Return Loss graphic (changed CT1 from 120 pF to 180 pF)
  - Modified RFI graphic
  - Modified Le79555 test circuit graphic
- Modified Application Circuit graphic
- Added Note 2 to "Application Circuit" section
- Updated Linecard Parts List to reflect the updated application circuit

Revision C1 to C2

- Formatting updates made

Revision C2 to D1

- Added green package OPNs to *Ordering Information*, on page 1
- Added *Package Assembly*, on page 7

Revision D1 to E1

- Added "Packing" column and Note 2 to *Ordering Information*, on page 1
- Updated 32QFN drawing in *Physical Dimensions*, on page 20

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