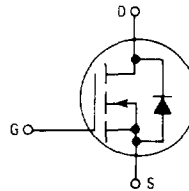


Designer's Data Sheet **Power Field Effect Transistor** **N-Channel Enhancement** **Mode Silicon Gate TMOS**

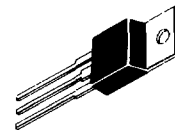
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS} , $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



MTP3N95
MTP3N100
MTP4N85
MTP4N90

TMOS POWER FETs
3 and 4 AMPERES
 $r_{DS(on)} = 4 \text{ OHMS}$
850, 900, 950
and 1000 VOLTS



CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTP				Unit
		4N85	4N90	3N95	3N100	
Drain-Source Voltage	V _{DSS}	850	900	950	1000	V _{dc}
Drain-Gate Voltage (R _{GS} = 1 MΩ)	V _{DGR}	850	900	950	1000	V _{dc}
Gate-Source Voltage — Continuous — Non-repetitive (t _p ≤ 50 μs)	V _{GS} V _{GSM}	± 20 ± 40				V _{dc} V _{pk}
Drain Current Continuous Pulsed	I _D I _{DM}	4 18		3 16		A _{dc}
Gate Current — Pulsed	I _{GM}	1.5				A _{dc}
Total Power Dissipation (at T _C = 25°C Derate above 25°C	P _D			75 0.6		Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	− 65 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

MTP3N95, 100/MTP4N85, 90

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Drain-Source Breakdown Voltage (V _{GS} = 0, I _D = 0.25 mA)	MTP4N85 MTP4N90 MTP3N95 MTP3N100	V _{(BR)DSS}	850 900 950 1000	—	V _{dc}
Zero Gate Voltage Drain Current (V _{DS} = Rated V _{DSS} , V _{GS} = 0) (V _{DS} = 0.8 Rated V _{DSS} , V _{GS} = 0, T _J = 125°C)		I _{DSS}	— —	0.2 1	mAdc
Gate-Body Leakage Current, Forward (V _{GSF} = 20 V _{dc} , V _{DS} = 0)		I _{GSSF}	—	100	nAdc
Gate Body Leakage Current, Reverse (V _{GSR} = 20 V _{dc} , V _{DS} = 0)		I _{GSSR}	—	100	nAdc

ON CHARACTERISTICS

Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1 mA) (T _J = 100°C)		V _{GS(th)}	2 1.5	4.5 4	V _{dc}
Static Drain-Source On-Resistance (V _{GS} = 10 V _{dc} , I _D = 1.5 Adc) (V _{GS} = 10 V _{dc} , I _D = 2 Adc)	MTP3N95:3N100 MTP4N85:4N90	r _{DS(on)}	— —	4 4	Ω
Drain-Source On-Voltage (V _{GS} = 10 V) (I _D = 3 Adc) (I _D = 1.5 Adc, T _J = 100°C) (I _D = 4 Adc) (I _D = 2 Adc, T _C = 100°C)	MTP3N95:3N100 MTP4N85:4N90	V _{DS(on)}	— — — —	12 10 16 14	V _{dc}
Forward Transconductance (V _{DS} = 10 V, I _D = 1.5 A) (V _{DS} = 10 V, I _D = 2 A)	MTP3N95:3N100 MTP4N85:4N90	g _{fs}	2 2	— —	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	iV _{DS} = 25 V, V _{GS} = 0, f = 1 MHz)	C _{iss}	—	1500	pF
Output Capacitance		C _{oss}	—	150	
Reverse Transfer Capacitance		C _{rss}	—	60	

SWITCHING CHARACTERISTICS (T_J = 100°C)

Turn-On Delay Time	(V _{DD} = 25 V, I _D = 0.5 Rated I _D R _{gen} = 50 ohms) See Figs. 8 and 9.	t _{d(on)}	—	40	ns
Rise Time		t _r	—	40	
Turn-Off Delay Time		t _{d(off)}	—	250	
Fall Time		t _f	—	75	
Total Gate Charge	(V _{DS} = 0.8 Rated V _{DSS} , I _D = Rated I _D , V _{GS} = 10 V _{dc}) See Figs. 10 and 11.	Q _g	55 (typ)	85	nC
Gate-Source Charge		Q _{gs}	30 (typ)	—	
Gate-Drain Charge		Q _{gd}	25 (typ)	—	

SOURCE DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I _S = Rated I _D , V _{GS} = 0) See Figs. 16 and 17.	V _{SD}	1.1 (typ)	1.5	V _{dc}
Forward Turn-On Time		t _{on}	200 (typ)	—	ns
Reverse Recovery Time		t _{rr}	1000 (typ)	—	ns

TYPICAL CHARACTERISTICS

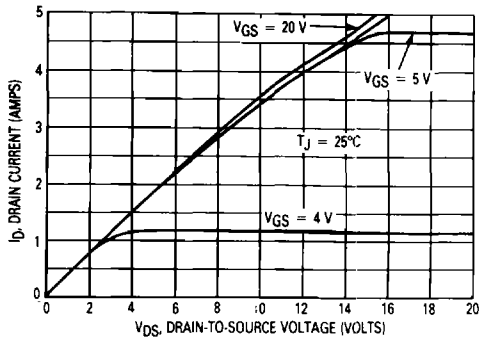


Figure 1. On-Region Characteristics

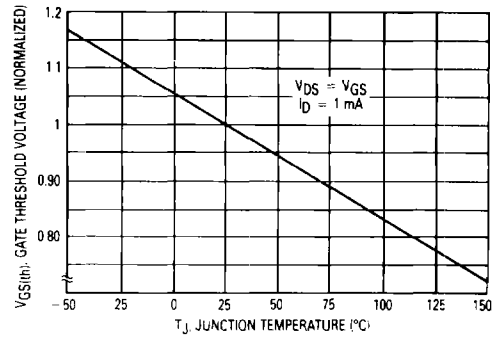


Figure 2. Gate-Threshold Voltage Variation with Temperature

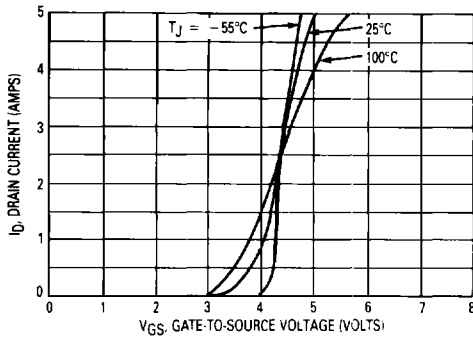


Figure 3. Transfer Characteristics

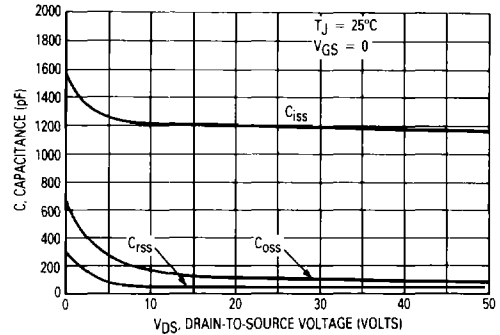


Figure 4. Capacitance Variation

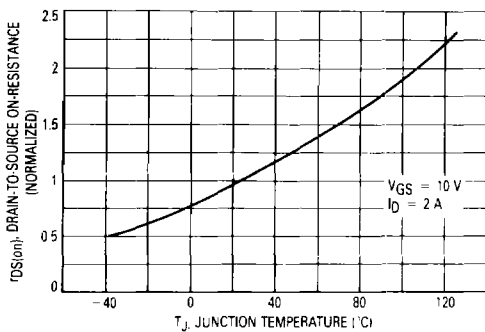


Figure 5. Normalized On-Resistance versus Temperature

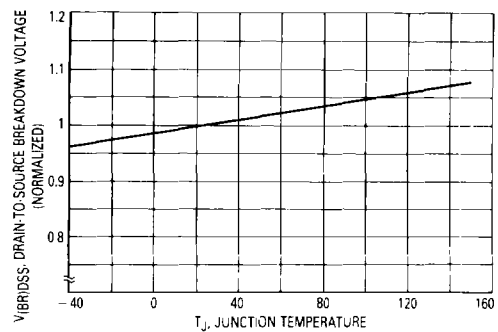


Figure 6. Normalized Breakdown Voltage versus Temperature

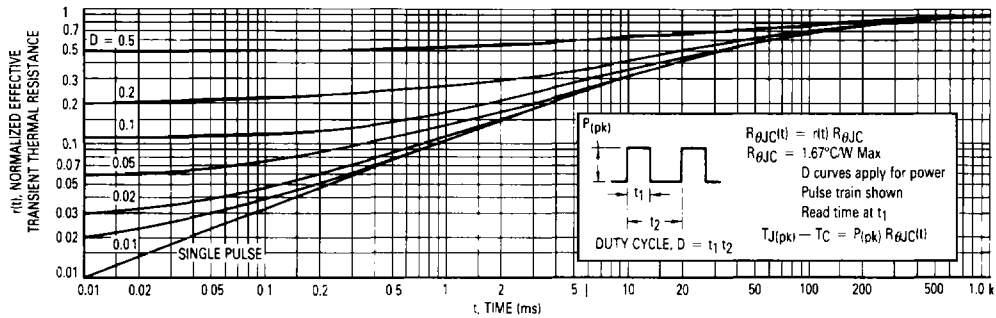


Figure 7. Thermal Response

RESISTIVE SWITCHING

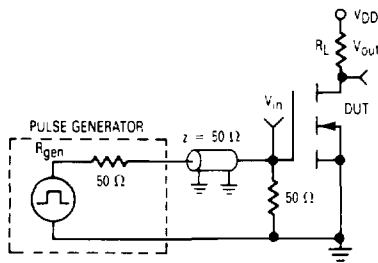


Figure 8. Switching Test Circuit

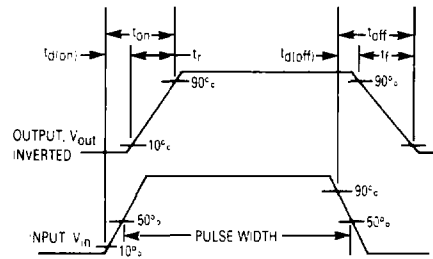


Figure 9. Switching Waveforms

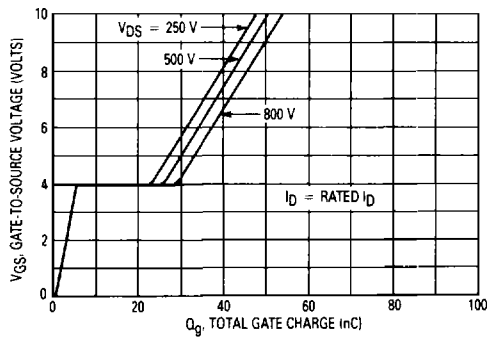
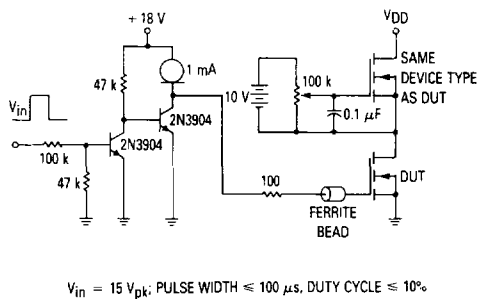


Figure 10. Gate Charge Variation



$V_{in} = 15 \text{ V}_{pk}$; PULSE WIDTH $\leq 100 \mu\text{s}$, DUTY CYCLE $\leq 10\%$

Figure 11. Gate Charge Test Circuit

SAFE OPERATING AREA INFORMATION

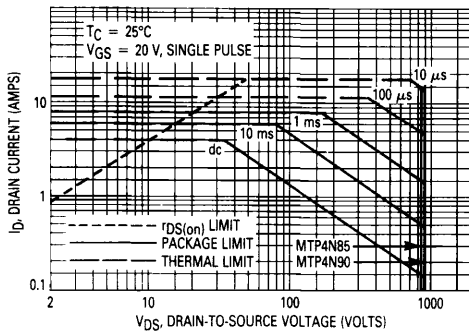


Figure 12. Maximum Rated Forward Biased Safe Operating Area

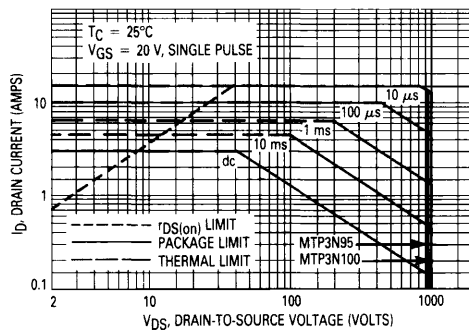


Figure 13. Maximum Rated Forward Biased Safe Operating Area

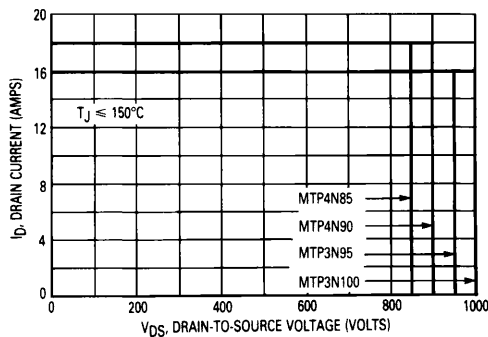


Figure 14. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The dc data of Figures 11 and 12 are based on a case temperature (T_C) of 25°C and a maximum junction temperature ($T_{J(max)}$) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_D(25^\circ\text{C}) \left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)} \right]$$

where

$I_D(25^\circ\text{C})$ = the dc drain current at $T_C = 25^\circ\text{C}$ from Figures 11 and 12

$T_{J(max)}$ = rated maximum junction temperature

T_C = device case temperature

P_D = rated power dissipation at $T_C = 25^\circ\text{C}$

$R_{\theta JC}$ = rated steady state thermal resistance

$r(t)$ = normalized thermal response from Figure 7

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 13 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 13 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

OUTLINE DIMENSIONS

