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PowerPC™

Advance Information

MPC107 Bridge/Memory Controller Hardware Specifications

This document provides an overview of the MPC107 PCI bridge/memory controller (PCIB/MC) for high-performance embedded systems. The MPC107 is a cost-effective, general-purpose PCI bridge/memory controller for applications using PCI in networking infrastructure, telecommunications, and other embedded markets. It can be used in applications such as network routers and switches, mass storage subsystems, network appliances, and print and imaging systems.

This document describes pertinent electrical and physical characteristics of the MPC107. For functional characteristics of the processor, refer to the *MPC107 RISC Bridge/Memory Controller User's Manual* (MPC107UM/D).

This document contains the following topics:

To locate any published errata or updates for this document, refer to the web site at http://www.motorola.com/semiconductors.

1.1 Overview

The MPC107 integrates a PCI bridge, memory controller, DMA controller, EPIC interrupt controller/timers, a message unit with an Intelligent Input/Output (I_2O) message controller, and an Inter-Integrated Circuit (I^2C) controller. The integration reduces the overall packaging requirements and the number of discrete devices required for an embedded system.

Figure 1 shows the major functional units within the MPC107. Note that this is a conceptual block diagram intended to show the basic features rather than an attempt to show how these features are physically implemented.

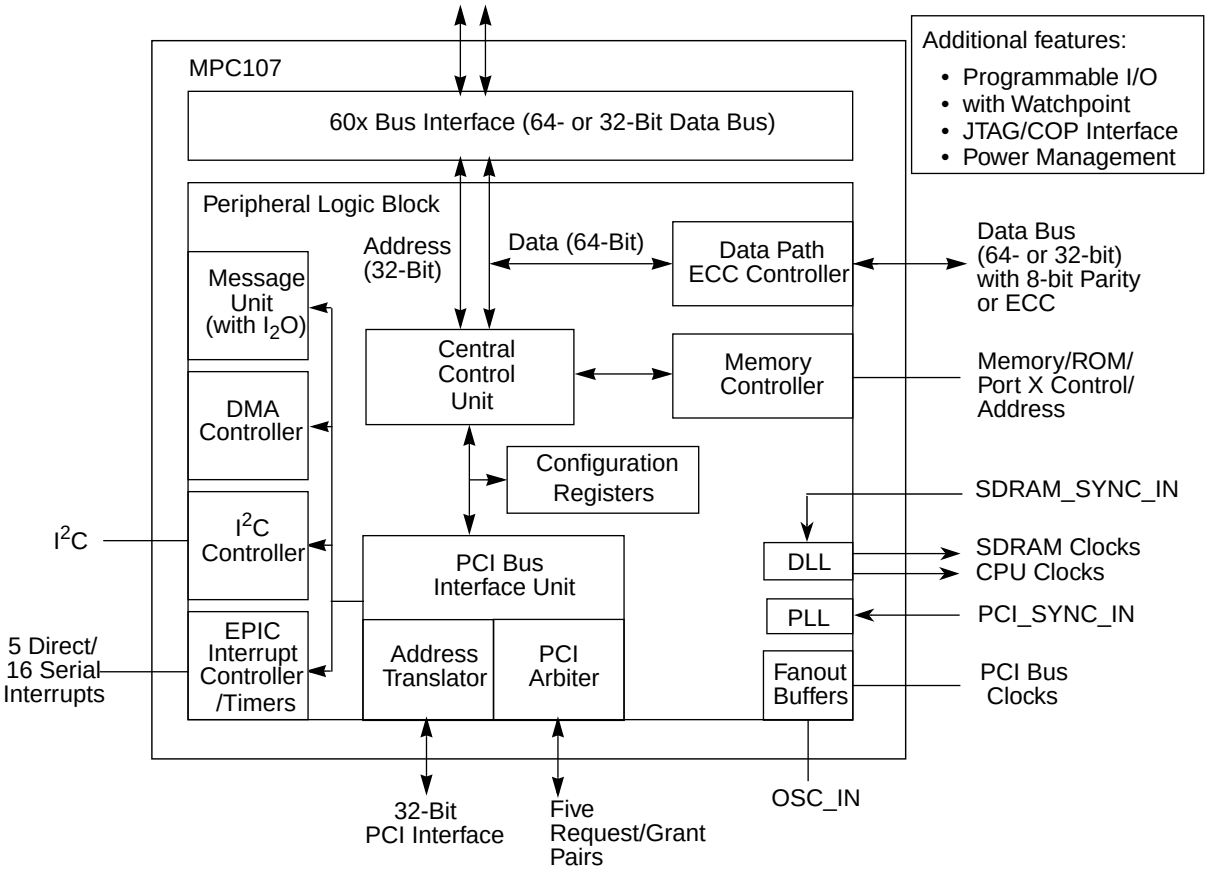


Figure 1. MPC107 Block Diagram

1.2 Features

The MPC107 provides an integrated high-bandwidth, high-performance interface between up to two 60x processors, the PCI bus, and main memory. This section summarizes the major features of the MPC107, as follows:

- Memory interface
  - 64-/32-bit 100-MHz bus
  - Programmable timing supporting either FPM DRAM, EDO DRAM, or SDRAM
  - High-bandwidth bus (32-/64-bit data bus) to DRAM
  - Supports one to eight banks of 4-, 16-, 64-, or 128-Mbit memory devices, and up to four banks of 256-Mbit SDRAM devices
  - Supports 1-Mbyte to 1-Gbyte DRAM memory
  - 144 Mbytes of ROM space
  - 8-, 32-, or 64-bit ROM
  - Write buffering for PCI and processor accesses
  - Supports normal parity, read-modify-write (RMW), or ECC
  - Data-path buffering between memory interface and processor
  - Low-voltage TTL logic (LVTTL) interfaces
  - Port X: 8-, 32-, or 64-bit general-purpose I/O port using ROM controller interface with programmable address strobe timing
- 32-bit PCI interface operating up to 66 MHz
  - PCI 2.1-compliant
  - PCI 5.0-V tolerance
  - Support for PCI locked accesses to memory
  - Support for accesses to PCI memory, I/O, and configuration spaces
  - Selectable big- or little-endian operation
  - Store gathering of processor-to-PCI write and PCI-to-memory write accesses
  - Memory prefetching of PCI read accesses
  - Selectable hardware-enforced coherency
  - PCI bus arbitration unit (five request/grant pairs)
  - PCI agent mode capability
  - Address translation unit
  - Some internal configuration registers accessible from PCI
- Two-channel integrated DMA controller (writes to ROM/Port X not supported)
  - Supports direct mode or chaining mode (automatic linking of DMA transfers)
  - Supports scatter gathering—read or write discontinuous memory
  - Interrupt on completed segment, chain, and error
  - Local-to-local memory
  - PCI-to-PCI memory
  - PCI-to-local memory
  - PCI memory-to-local memory

- Message unit
  - Two doorbell registers
  - An extended doorbell register mechanism that facilitates interprocessor communication through interrupts in a dual-local-processor system
  - Two inbound and two outbound messaging registers
  - I_2O message controller
- I^2C controller with full master/slave support (except broadcast all)
- Embedded programmable interrupt controller (EPIC)
  - Five hardware interrupts (IRQs) or 16 serial interrupts
  - Four programmable timers
- Integrated PCI bus, CPU, and SDRAM clock generation
- Programmable PCI bus, 60x, and memory interface output drivers
- Dynamic power management supporting 60x nap, doze, and sleep modes
- Programmable input and output signals with watchpoint capability
- Built-in PCI bus performance monitor facility
- Debug features
  - Error injection/capture on data path
  - IEEE 1149.1 (JTAG)/test interface
- Processor interface
  - Supports up to two PowerPC™ microprocessors with 60x bus interface
  - Supports various operating frequencies and bus divider ratios
  - 32-bit address bus, 64/32-bit data bus supported at 100 MHz
  - Supports full memory coherency
  - Supports optional local bus slave
  - Decoupled address and data buses for pipelining of 60x accesses
  - Store gathering on 60x-to-PCI writes
  - Concurrent transactions on 60x and PCI buses supported

1.3 General Parameters

The following list provides a summary of the general parameters of the MPC107:

Technology:	0.29 µm CMOS, five-layer metal
Die size:	50 mm^2
Transistor count:	0.96 million
Logic design:	Fully static
Package:	Surface mount 503 Plastic Ball Grid Array (C4/PBGA)
Core power supply:	2.5V ± 5% V DC (nominal; see Table 2 for recommended operating conditions)
I/O power supply:	3.0 to 3.6 V DC

1.4 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC107.

1.4.1 DC Electrical Characteristics

1.4.1.1 Absolute Maximum Ratings

The tables in this section describe the MPC107 DC electrical characteristics. Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings

Characteristic[1]	Symbol	Range	Unit
Supply Voltage - Core	Vdd	-0.3 to 2.75	V
Supply Voltage - Memory Bus Drivers	GVdd	-0.3 to 3.6	V
Supply Voltage - Processor Bus Drivers	BVdd	-0.3 to 3.6	V
Supply Voltage - PCI and Standard I/O Buffers	OVdd	-0.3 to 3.6	V
Supply Voltage - PLLs and DLL	AVdd/LAVdd	-0.3 to 2.75	V
Supply Voltage - PCI Reference	LVdd	-0.3 to 5.4	V
Input Voltage[2]	V_{IN}	-0.3 to 3.6	V
Operational Die-Junction Temperature Range	T_J	0 to 105	°C
Storage Temperature Range	T_{STG}	-55 to 150	°C

Notes:
1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. PCI inputs with LVdd = 5V ± 5% V DC may be correspondingly stressed at voltages exceeding LVdd + 0.5 V DC.

1.4.1.2 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for the MPC107.

Table 2. Recommended Operating Conditions [1]

Characteristic	Symbol	Recommended Value	Unit	Notes
Supply Voltage	Vdd	2.5 ± 5%	V	5
Supply Voltages for Memory Bus Drivers	GVdd	3.3 ± 5%	V	7
Supply Voltages for Processor Bus Drivers	BVdd	3.3 ± 5%	V	7
		2.5 ± 5%		
I/O Buffer supply for PCI and Standard	OVdd	3.3 ± 0.3	V	5
PLL Supply Voltage	AVdd	2.5 ± 5%	V	6
DLL Supply Voltage	LAVdd	2.5 ± 5%	V	6

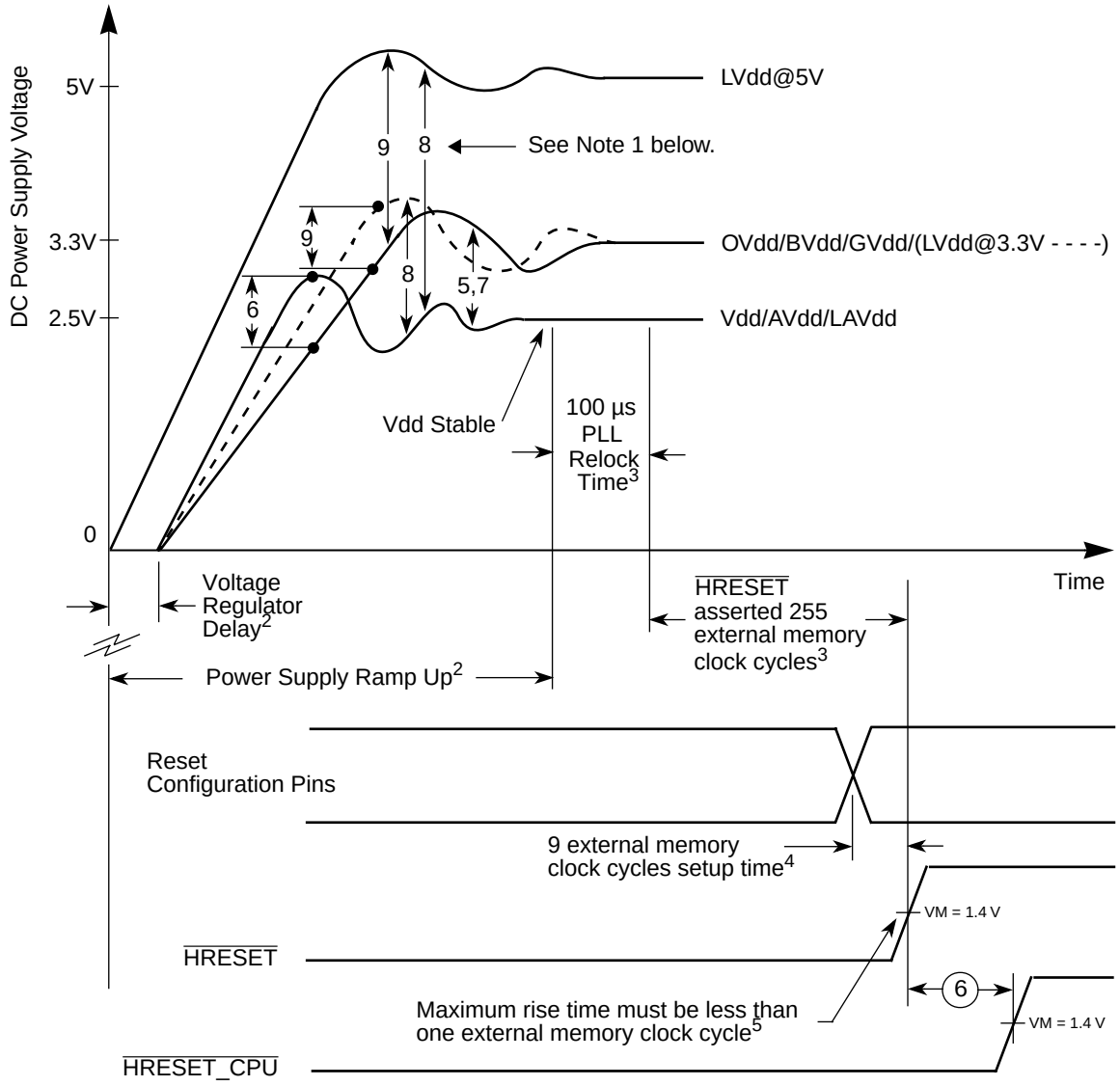
Table 2. Recommended Operating Conditions (Continued)[1]

Characteristic		Symbol	Recommended Value	Unit	Notes
PCI Reference		LVdd	5.0 ± 5%	V	8,9
			3.3 ± 0.3	V	8,9
Input Voltage	PCI Inputs	V_{IN}	0 to 3.6 or 5.75	V	2,3
	All Other Inputs		0 to 3.6	V	4
Die-Junction Temperature		T_J	0 to 105	°C	

Notes:
1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. PCI pins are designed to withstand LVdd + 0.5 V dc when LVdd is connected to a 5.0V DC power supply.
3. PCI pins are designed to withstand LVdd + 0.5 V dc when LVdd is connected to a 3.3 V DC power supply.

Cautions:
4. Input voltage (V_{IN}) must not be greater than the supply voltage (Vdd/AVdd/LAVdd) by more than 2.5 V at all times including during power-on reset.
5. OVdd must not exceed Vdd/AVdd/LAVdd by more than 1.8 V at any time including during power-on reset.
6. Vdd/AVdd/LAVdd must not exceed OVdd by more than 0.6 V at any time including during power-on reset.
7. BVdd/GVdd must not exceed Vdd/AVdd/LAVdd by more than 1.8 V at any time including during power-on reset.
8. LVdd must not exceed Vdd/AVdd/LAVdd by more than 5.4 V at any time including during power-on reset.
9. LVdd must not exceed OVdd by more than 3.6 V at any time including during power-on reset.

Figure 2 shows supply voltage sequencing and separation cautions.



Notes:

1. Numbers associated with waveform separations correspond to caution numbers listed in Table 2.
2. Refer to Section 1.7.2, “Power Supply Voltage Sequencing,” for additional information on this topic.
3. Refer to Table 8 for additional information on PLL Relock and reset signal assertion timing requirements.
4. Refer to Table 9. for additional information on reset configuration pin setup timing requirements.
5. $\overline{\text{HRESET}}$ must transition from a logic 0 to a logic 1 in less than one SDRAM_SYNC_IN clock cycle for the device to be in the non-reset state.
6. $\overline{\text{HRESET\_CPU}}$ negates 2^{17} memory clock cycles after $\overline{\text{HRESET}}$ negates.

Figure 2. Supply Voltage Sequencing and Separation Cautions

Figure 3 shows the undershoot and overshoot voltage of the memory interface of the MPC107.

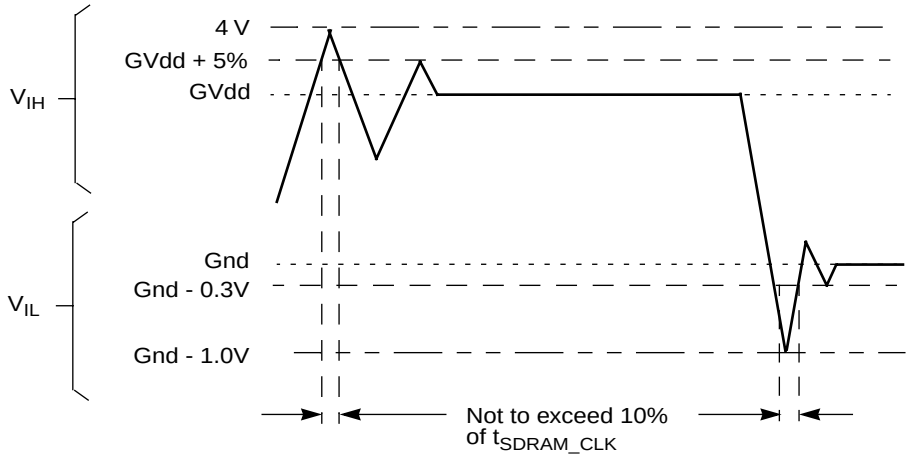


Figure 3. Overshoot/Undershoot Voltage

1.4.1.3 DC Electrical Characteristics

Table 3 provides the DC electrical characteristics for the MPC107.

Table 3. DC Electrical Specifications

At recommended operating conditions (See Table 2)

Characteristics	Conditions[4]	Symbols	Min	Max	Units
Input High Voltage[6]	PCI only	V_{IH}	0.65*OVdd	LVdd	V
Input Low Voltage	PCI only	V_{IL}	—	0.3*OVdd	V
Input High Voltage	All other pins (GVdd = 3.3V)	V_{IH}	2.0	—	V
Input High Voltage	All other pins (BVdd = 2.5V)	V_{IH}	1.7	—	V
Input Low Voltage	All inputs except PCI_SYNC_IN	V_{IL}	GND	0.8	V
PCI_SYNC_IN Input High Voltage		CV_{IH}	2.4	—	V
PCI_SYNC_IN Input Low Voltage		CV_{IL}	GND	0.4	V
Input Leakage Current[5] for pins using DRV_PCI driver.	0.5 V ≤ V_{IN} ≤ 2.7 V @ LVdd = 4.75	I_L	—	± 70	µA
Input Leakage Current[5] all others	LVdd = 3.6 V (GVdd ≤ 3.465)	I_L	—	± 10	µA
Output High Voltage	I_{OH}=Driver Dependent[3] (GVdd = 3.3V)	V_{OH}	2.4	—	V
Output Low Voltage	I_{OL}=Driver Dependent[3] (GVdd = 3.3V)	V_{OL}	—	0.4	V
Output High Voltage	I_{OH}=Driver Dependent[3] (BVdd = 2.5V) All outputs except CPUCLKS[0–2]	V_{OH}	1.85	—	V
	I_{OH}=Driver Dependent[3] (BVdd = 2.5V) CPUCLKS[0–2] Only	V_{OH}	2.0	—	V

Table 3. DC Electrical Specifications (Continued)

At recommended operating conditions (See Table 2)

Output Low Voltage	I_{OL}=Driver Dependent[3] (BVdd = 2.5V) All outputs except CPUCLKS[0–2]	V_{OL}	—	0.4	V
	I_{OL}=Driver Dependent[3] (BVdd = 2.5V) CPUCLKS[0–2] Only	V_{OL}	—	0.3	V
Capacitance[2]	V_{IN}=0 V, f=1MHz	C_{IN}	—	7.0	pF

Notes:
1. See Figure 17 for pins with internal pull-up resistors.
2. Capacitance is periodically sampled rather than 100% tested.
3. See Table 4 for the typical drive capability of a specific signal pin based upon the type of output driver associated with that pin as listed in Table 17.
4. These specifications are for the default driver strengths indicated in Table 4.
5. Leakage current is measured on input pins and on output pins in the high impedance state. The leakage current is measured for nominal OVdd/LVdd and Vdd or both Ovdd/LVdd and Vdd must vary in the same direction.
6. The minimum Input High Voltage is not compliant with the PCI Local Bus Specification (Rev 2.1) which specifies 0.5*OVdd for minimum Input High Voltage.

1.4.1.4 Output Driver Characteristics

Table 4 provides information on the characteristics of the output drivers referenced in Table 17. The values are from the MPC107 IBIS model (v1.1) and are not tested. For additional detailed information, see the complete IBIS model listing at http://www.motorola.com/semiconductors.

Table 4. Drive Capability of MPC107 Output Pins

Driver Type	Programmable Output Impedance (Ohms)	Supply Voltage	I_{OH}	I_{OL}	Units	Notes
DRV_CPU	20	BVdd = 3.3V	36.6	18.1	mA	2, 5
		BVdd = 2.5V	21.4	15.6	mA	3, 6, 7
	40 (default)	BVdd = 3.3V	18.6	9.2	mA	2, 5
		BVdd = 2.5V	10.8	7.9	mA	3, 6, 7
DRV_PCI	25	OVdd = 3.3	12.0	12.4	mA	1, 4
	50 (default)	OVdd = 3.3	6.1	6.3	mA	1, 4
DRV_MEM_ADDR DRV_PCI_CLK	8 (default)	GVdd = 3.3	89.0	42.3	mA	2, 5
	13.3	GVdd = 3.3	55.8	26.4	mA	2, 5
	20	GVdd = 3.3	36.6	18.1	mA	2, 5
	40	GVdd = 3.3	18.6	9.2	mA	2, 5
DRV_MEM_DATA	20 (default)	GVdd = 3.3	36.6	18.1	mA	2, 5
	40	GVdd = 3.3	18.6	9.2	mA	2, 5

Notes:

1. For DRV_PCI, I_{OH} read from the IBIS listing in the pull-up mode, I(Min) column, at the 0.33V label by interpolating between the 0.3 V and 0.4 V table entries' current values which corresponds to the PCI V_{OH} = 2.97 = 0.9*OVdd (OVdd = 3.3 V) where Table Entry Voltage = OVdd - PCI V_{OH}.
2. For all others with GVdd or BVdd = 3.3 V, I_{OH} read from the IBIS listing in the pull-up mode, I(Min) column, at the 0.9 V table entry which corresponds to the V_{OH} = 2.4 V where Table Entry Voltage = G/BVdd - V_{OH}.
3. For all others with BVdd = 2.5 V, I_{OH} read from the IBIS listing in the pull-up mode, I(Min) column, at the 0.65 V table entry by interpolating between the 0.6 V and 0.7 V table entries' current values which corresponds to the V_{OH} = 1.85 V where Table Entry Voltage = BVdd - V_{OH}.
4. For DRV_PCI, I_{OL} read from the IBIS listing in the pull-down mode, I(Min) column, at 0.33 V = PCI V_{OL} = 0.1*OVdd (OVdd = 3.3 V) by interpolating between the 0.3 V and 0.4 V table entries.
5. For all others with GVdd or BVdd = 3.3 V, I_{OL} read from the IBIS listing in the pull-down mode, I(Min) column, at the 0.4 V table entry.
6. For all others with BVdd = 2.5 V, I_{OL} read from the IBIS listing in the pull-down mode, I(Min) column, at the 0.4 V table entry.
7. For BVdd = 2.5 V, the I_{OH} and I_{OL} values are estimated from the io_mem_data_XX_2.5 and io_mem_addr_XX_2.5 sections of the IBIS model where XX = driver output impedance (20 or 40 Ohms).

1.4.1.5 Power Characteristics

Table 5 provides the preliminary power consumption estimates for the MPC107.

Table 5. Power Consumption

Mode	PCI_SYNC_IN/Core Frequency (MHz)								Units	Notes
	25/50		33/33		33/66		66/100			
	Vdd Pwr	I/O Pwr	Vdd Pwr	I/O Pwr	Vdd Pwr	I/O Pwr	Vdd Pwr	I/O Pwr		
Maximum	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mW	
Typical	400	1125	300	925	550	1325	800	1375	mW	1,2
Doze	375	850	250	775	500	975	750	1125	mW	1,2
Nap	375	875	250	825	500	1025	750	1150	mW	1,2
Sleep	175	875	125	825	225	1025	325	1150	mW	1,2
Sleep	125	725	100	650	175	875	275	1025	mW	1,2,3
Sleep	125	575	100	500	175	650	250	675	mW	1,3,4
Sleep	10	400	10	425	10	425	25	500	mW	1,3,4,5
Reset	550	850	350	675	700	975	1050	950	mW	1,2

Notes:

1. Power is measured with Vdd = 2.625V, Gvdd = Ovdd = Bvdd = 3.45 V at 0 °C and one DIMM populated in test system.
2. All clock drivers enabled.
3. Memory refresh off.
4. One PCI_CLK, one CPU_CLK, and one SDRAM_CLK enabled.
5. PLL off.
6. Power consumption on the PLL supply pin (AVdd) and the DLL supply pin (LAVdd) < 15 mW. This parameter is guaranteed by design and is not tested.

1.4.2 Thermal Characteristics

Table 6 provides the package thermal characteristics for the MPC107.

Table 6. PBGA Package Thermal Characteristics

Characteristic[1]	Symbols	Value	Units
Die Junction-to-Case Thermal Resistance	θ_{JC}	< 0.1	°C/W
Die Junction-to-Board Thermal Resistance	θ_{JB}	5.2	°C/W
Package Junction-to-Ambient Thermal Resistance[2]	θ_{JA}	See Figure 25	

Notes:

1. Refer to Section 1.7, “System Design Information,” for more details about thermal management.
2. $T_J = T_A + P_D \times \theta_{JA}$
   - T_J = Die junction temperature
   - T_A = System air ambient temperature near the package
   - P_D = Average power consumed by IC in Watts
   - θ_{JA} = Thermal resistance from die junction to ambient air in °C/W

1.4.3 AC Electrical Characteristics

This section provides the AC electrical characteristics for the MPC107. After fabrication, functional parts are sorted by maximum core frequency as shown in Table 7 and Section 1.4.3.1, “Clock AC Specifications,” and tested for conformance to the AC specifications for that frequency. The core frequency is determined by the bus (PCI_SYNC_IN) clock frequency and the settings of the PLL_CFG[0–3] signals. Parts are sold by maximum processor core frequency; see Section 1.9, “Ordering Information.”

Table 7 provides the operating frequency information for the MPC107.

Table 7. Operating Frequency

At recommended operating conditions (See Table 2) with LVdd = 3.3 V ± 0.3 V

Characteristic[1]	66 MHz		100 MHz		Units
	Min	Max	Min	Max	
Core (memory bus/processor bus) frequency	25	66	25	100	MHz
PCI input frequency (PCI_SYNC_IN)	12.5–66				MHz

Notes:

Caution: The PCI_SYNC_IN frequency and PLL_CFG[0–3] settings must be chosen such that the resulting peripheral logic/memory bus frequency, CPU (core) frequency, and PLL (VCO) frequencies do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0–3] signal description in Section 1.6, “PLL Configuration,” for valid PLL_CFG[0–3] settings and PCI_SYNC_IN frequencies.

1.4.3.1 Clock AC Specifications

Table 8 provides the clock AC timing specifications as defined in Section 1.4.3.2.

Table 8. Clock AC Timing Specifications

At recommended operating conditions (See Table 2.) with LVdd = 3.3 V ± 0.3 V

Num	Characteristics and Conditions [1]	Min	Max	Unit	Notes
1a	Frequency of Operation (PCI_SYNC_IN)	12.5	66	MHz	8
1b	PCI_SYNC_IN Cycle Time	80	15	ns	8
2,3	PCI_SYNC_IN Rise and Fall Times	—	2.0	ns	2
4	PCI_SYNC_IN Duty Cycle Measured at 1.4 V	40	60	%	
5a	PCI_SYNC_IN Pulse Width High Measured at 1.4V	6	9	ns	3
5b	PCI_SYNC_IN Pulse Width Low Measured at 1.4V	6	9	ns	3
7	PCI_SYNC_IN Jitter	—	<150	ps	
9a	PCI_CLK[0–4] Skew (Pin to Pin)	—	500	ps	
9b	SDRAM_CLK[0–3] Skew (Pin to Pin)	—	350	ps	
9c	CPU_CLK[0–2] Skew (Pin to Pin)	—	350	ps	
9d	SDRAM_CLK[0–3]/CPU_CLK[0–2] Jitter	—	150	ps	
10	Internal PLL Relock Time	—	100	µs	3,4,6
15	DLL Lock Range with DLL_EXTEND = 0 disabled	$0 \le (NT_{clk} - t_{loop} - t_{fix0}) \le 7$		ns	7
16	DLL Lock Range with DLL_EXTEND = 1 enabled (Default)	$0 \le (NT_{clk} - T_{clk}/2 - t_{loop} - t_{fix0}) \le 7$		ns	7
17	Frequency of Operation (OSC_IN)	12.5	66	MHz	8
18	OSC_IN Cycle Time	80	15	ns	8
19	OSC_IN Rise and Fall Times	—	5	ns	5
20	OSC_IN Duty Cycle Measured at 1.4 V	40	60	%	
21	OSC_IN Frequency Stability	—	100	ppm	

Notes:

1 These specifications are for the default driver strengths indicated in Table 4.

2 Rise and fall times for the PCI_SYNC_IN input are measured from 0.4 to 2.4 V.

3 Specification value at maximum frequency of operation.

4 Relock time is guaranteed by design and characterization. Relock time is not tested.

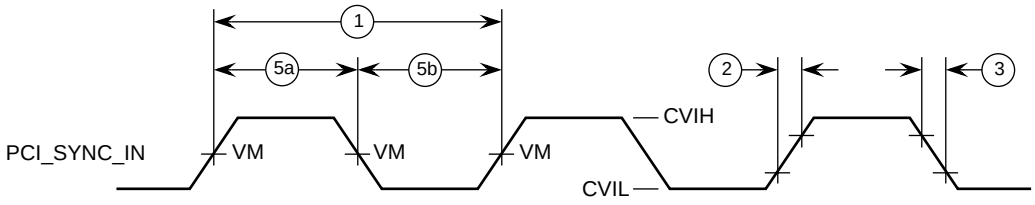
5 Rise and fall times for the OSC_IN input are guaranteed by design and characterization. OSC_IN input rise and fall times are not tested.

6 Relock timing is guaranteed by design. PLL-relock time is the maximum amount of time required for PLL lock after a stable Vdd and PCI_SYNC_IN are reached during the reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the reset sequence.

7 DLL_EXTEND is bit 7 of the PMC2 register <72>. N is a non-zero integer (1 or 2). T_{clk} is the period of one SDRAM_SYNC_OUT clock cycle in ns. t_{loop} is the propagation delay of the DLL synchronization feedback loop (PC board runner) from SDRAM_SYNC_OUT to SDRAM_SYNC_IN in ns; 6.25 inches of loop length (unloaded PC board runner) corresponds to approximately 1 ns of delay. t_{fix0} is a fixed delay inherent in the design when the DLL is at tap point 0 and the DLL is contributing no delay; t_{fix0} equals approximately 3 ns. See Figure 6 for DLL locking ranges.

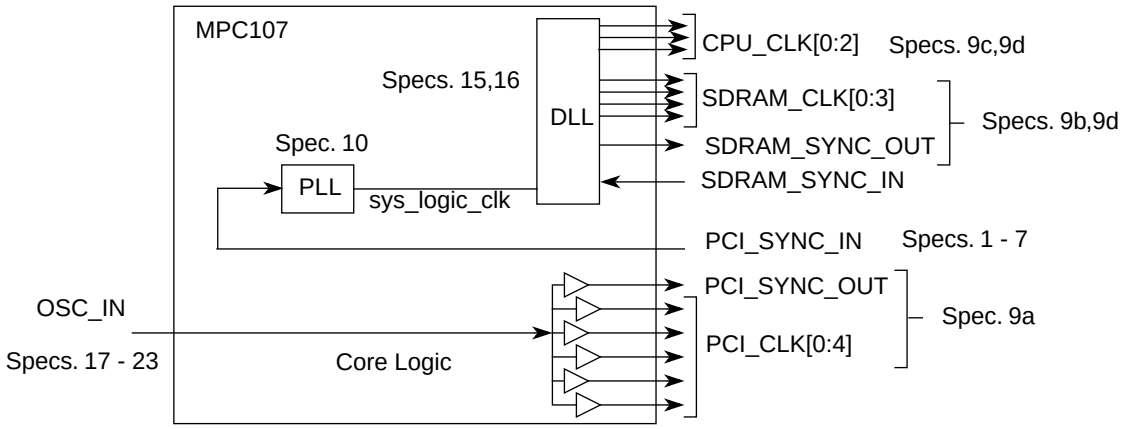
8 See Table 18 for PCI_SYNC_IN input frequency range for specific PLL_CFG[0–3] settings.

Figure 4 shows PCI_SYNC_IN input clock timing, Figure 5 illustrates how the Table 8 clock specifications relate to the MPC107 clocking, and Figure 6 shows the DLL locking range loop delay versus frequency of operation.



VM = Midpoint Voltage (1.4V)

Figure 4. PCI_SYNC_IN Input Clock Timing Diagram



Note: Specification numbers are from Table 8.

Figure 5. Clock Subsystem Block Diagram

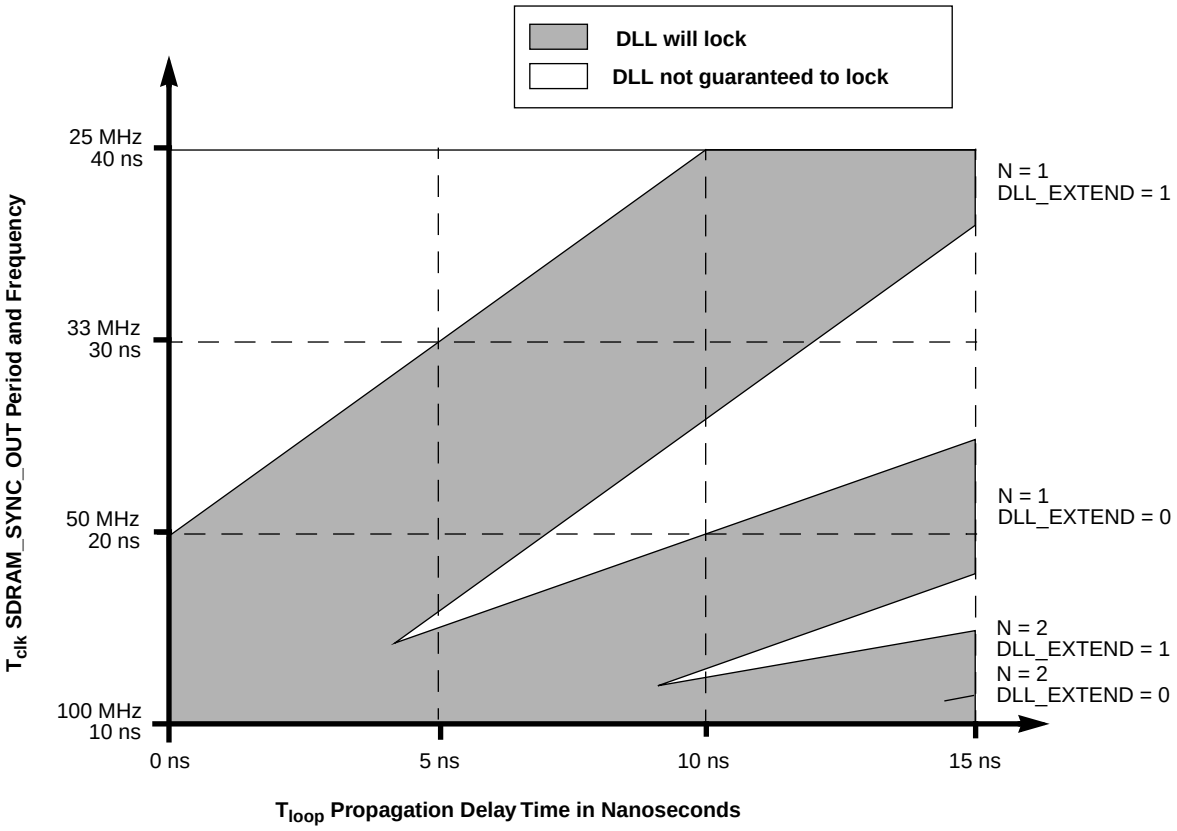


Figure 6. DLL Locking Range Loop Delay vs. Frequency of Operation

1.4.3.2 Input AC Timing Specifications

Table 9 provides the input AC timing specifications. See Figure 7 and Figure 8.

Table 9. Input AC Timing Specifications

At recommended operating conditions (see Table 2) with LVdd = 3.3 V ± 0.3 V

Num	Characteristic	Min	Max	Units	Notes
10a	PCI input signals valid to PCI_SYNC_IN (input setup)	3.0	—	ns	2,3
10b	Memory interface signals Valid to SDRAM_SYNC_IN (Input Setup)	2.0	—	ns	1,3
10c	Epic, misc. debug input signals valid to SDRAM_SYNC_IN (Input Setup)	2.0	—	ns	1,3
10d	I^2C input signals valid to SDRAM_SYNC_IN (input setup)	2.0	—	ns	1,3
10e	Mode select inputs valid to $\overline{\text{HRESET}}$ (input setup)	$9*t_{CLK}$	—	ns	1,3–5
10f	60x processor interface signals Valid to SDRAM_SYNC_IN (input setup)	2.0	—	ns	1,3

Table 9. Input AC Timing Specifications (Continued)

At recommended operating conditions (see Table 2) with LVdd = 3.3 V ± 0.3 V

Num	Characteristic	Min	Max	Units	Notes
11a1	PCI_SYNC_IN (SDRAM_SYNC_IN) to inputs invalid (input hold)	1.0	—	ns	2,3
11a2	Memory interface signals SDRAM_SYNC_IN to inputs invalid (input hold)	0.5	—	ns	1,3
11a3	60x processor interface signals SDRAM_SYNC_IN to inputs invalid (input hold)	0	—	ns	1,3
11b	$\overline{\text{HRESET}}$ to mode select inputs invalid (input hold)	0	—	ns	1,3,5

Notes:

1 All memory, processor, and related interface input signal specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the V_M = 1.4 V of the rising edge of the memory bus clock, SDRAM_SYNC_IN. SDRAM_SYNC_IN is the same as PCI_SYNC_IN in 1:1 mode, but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of PCI_SYNC_IN). See Figure 7.

1 All PCI signals are measured from OVdd/2 of the rising edge of PCI_SYNC_IN to 0.4*OVdd of the signal in question for 3.3 V PCI signaling levels. See Figure 8.

2 Input timings are measured at the pin.

3 t_{CLK} is the time of one SDRAM_SYNC_IN clock cycle.

4 All mode select input signals specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the V_M = 1.4 V of the rising edge of the $\overline{\text{HRESET}}$ signal. See Figure 9.

Figure 7 shows input-output timing referenced to SDRAM_SYNC_IN and Figure 8 the input-output timing referenced to PCI_SYNC_IN.

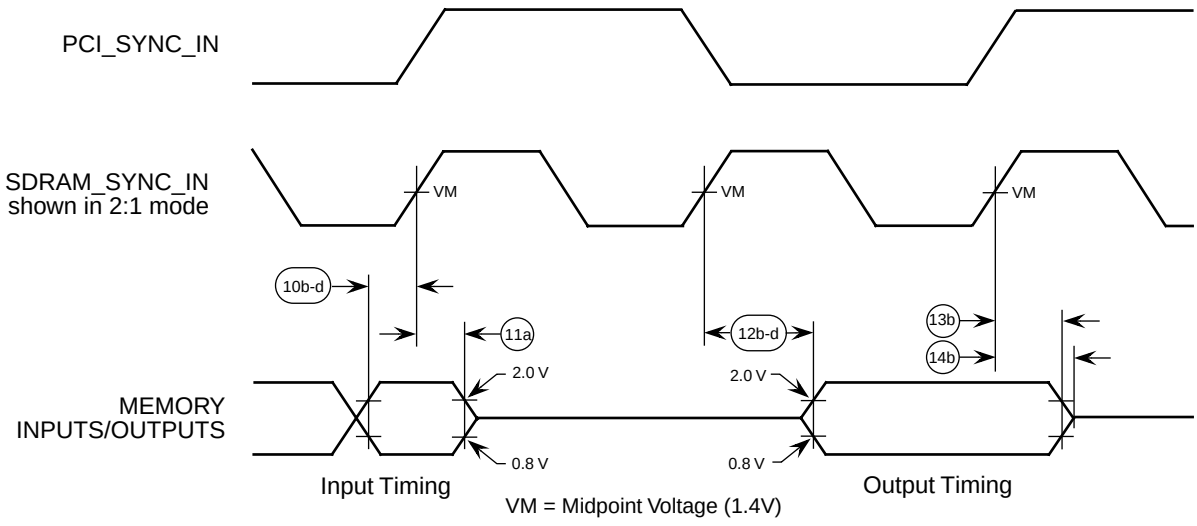


Figure 7. Input - Output Timing Diagram Referenced to SDRAM_SYNC_IN

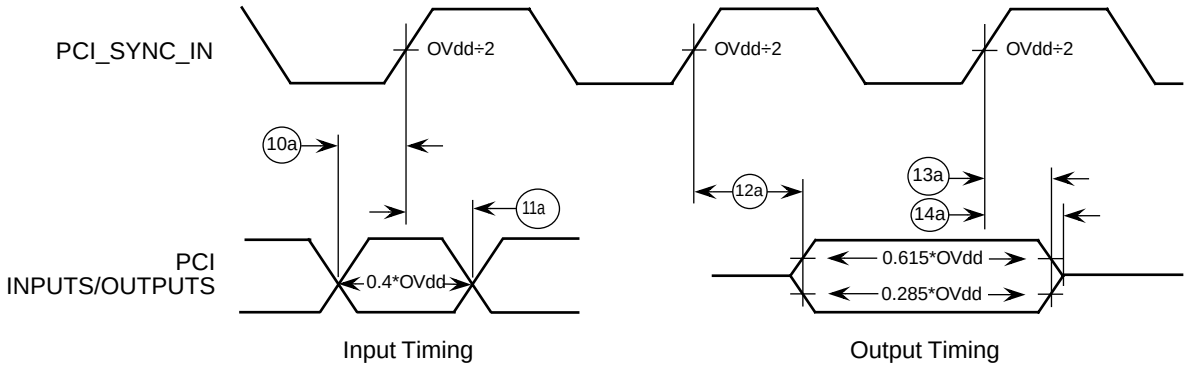


Figure 8. Input - Output Timing Diagram Referenced to PCI_SYNC_IN

Figure 9 shows input timing for mode select signals.

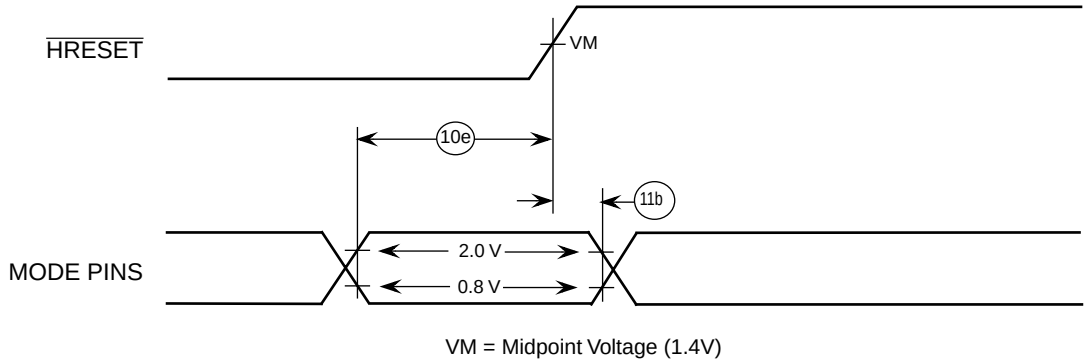


Figure 9. Input Timing Diagram for Mode Select Signals

1.4.3.3 Output AC Timing Specification

Table 10 provides the processor bus AC timing specifications for the MPC107. See Figure 7 and Figure 8.

Table 10. Output AC Timing Specifications

At recommended operating conditions (see Table 2) with LVdd = 3.3 V ± 0.3 V

Num	Characteristic[3,6]	Min	Max	Units	Notes
12a	PCI_SYNC_IN to output valid, 66 MHz PCI, with SDMA4 pulled-down to logic 0 state. See Figure 11.	—	6.0	ns	2,4
	PCI_SYNC_IN to output valid, 33 MHz PCI, with SDMA4 in the default logic 1 state. See Figure 11.	—	11.0	ns	2,4
12b	Memory interface signals, SDRAM_SYNC_IN to output valid	—	5.5	ns	1
12b1	Memory interface signal: CKE (100 MHz device), SDRAM_SYNC_IN to output valid	—	5.5	ns	1
12b2	Memory interface signal: CKE (66 MHz device), SDRAM_SYNC_IN to output valid	—	6.0	ns	1
12c	EPIC, misc. debug signals, SDRAM_SYNC_IN to ¬alid	—	9.0	ns	1
12d	I^2C, SDRAM_SYNC_IN to output valid	—	5.0	ns	1

Table 10. Output AC Timing Specifications (Continued)

At recommended operating conditions (see Table 2) with LVdd = 3.3 V ± 0.3 V

Num	Characteristic[3,6]	Min	Max	Units	Notes
12e	60x Processor interface signals SDRAM_SYNC_IN to output valid	—	5.5	ns	1
13a	Output hold, 66 MHz PCI, with SDMA4 and SDMA3 pulled-down to logic 0 states. See Table 11.	1.0	—	ns	2,4,5
	Output hold, 33 MHz PCI, with SDMA4 in the default logic 1 state and SDMA3 pulled-down to logic 0 state. See Table 11.	2.0	—	ns	2,4,5
13b	Output hold (for all others)	1	—	ns	1
14a	PCI_SYNC_IN to output high impedance (T_{off} for PCI)	—	14.0	ns	2,4
14b	SDRAM_SYNC_IN to output high impedance (for all others)	—	4.0	ns	1

Notes:

1 All memory and related interface output signal specifications are specified from the V_M = 1.4 V of the rising edge of the memory bus clock, SDRAM_SYNC_IN to the TTL level (0.8 or 2.0 V) of the signal in question. SDRAM_SYNC_IN is the same as PCI_SYNC_IN in 1:1 mode, but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of PCI_SYNC_IN). See Figure 7.

2 All PCI signals are measured from OVdd/2 of the rising edge of PCI_SYNC_IN to 0.285*OVdd or 0.615*OVdd of the signal in question for 3.3 V PCI signaling levels. See Figure 8.

3 All output timings assume a purely resistive 50 ohm load (See Figure 10). Output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

4 PCI bussed signals are composed of the following signals: $\overline{\text{LOCK}}$, $\overline{\text{IRDY}}$, $\overline{\text{C/BE}}$[0–3], PAR, $\overline{\text{TRDY}}$, $\overline{\text{FRAME}}$, $\overline{\text{STOP}}$, $\overline{\text{DEVSEL}}$, $\overline{\text{PERR}}$, $\overline{\text{SERR}}$, AD[0–31], $\overline{\text{REQ}}$[4–0], $\overline{\text{GNT}}$[4–0], $\overline{\text{IDSEL}}$, $\overline{\text{INTA}}$.

5 PCI hold times can be varied; see Section 1.4.3.3.1, “PCI Signal Output Hold Timing,” for information on programmable PCI output hold times. The values shown for item 13a are for PCI compliance.

6 These specifications are for the default driver strengths indicated in Table 4.

Figure 10 shows the AC Test Load for the MPC107.

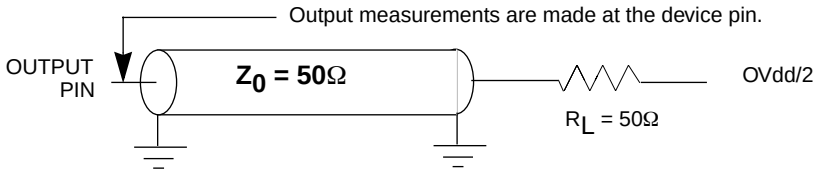


Figure 10. AC Test Load for the MPC107

1.4.3.3.1 PCI Signal Output Hold Timing

In order to meet minimum output hold specifications relative to PCI_SYNC_IN for both 33 MHz and 66 MHz PCI systems, the MPC107 has a programmable output hold delay for PCI signals. The initial value of the output hold delay is determined by the values on the SDMA4 and SDMA3 reset configuration signals. Further output hold delay values are available by programming the PCI_HOLD_DEL value of the PMCR2 configuration register.

Table 11 describes the bit values for the PCI_HOLD_DEL values in PMCR2.

Table 11. Power Management Configuration Register 2—0x72

Bit	Name	Reset Value	Description
6–4	PCI_HOLD_DEL	xx0	PCI output hold delay values relative to PCI_SYNC_IN. The initial values of bits 6 and 5 are determined by the reset configuration pins SDMA4 and SDMA3, respectively. As these two pins have internal pull-up resistors, the default value after reset is 0b110. While the minimum hold times are guaranteed at shown values, changes in the actual hold time can be made by incrementing or decrementing the value in these bit fields of this register via software or hardware configuration. The increment is in approximately 400 picosecond steps. Lowering the value in the three bit field decreases the amount of output hold available. 000 66 MHz PCI. Pull-down SDMA4 configuration pin with a 2KΩ or less value resistor. This setting guarantees the minimum output hold, item 13a, and the maximum output valid, item 12a, times as specified in Figure 10 are met for a 66 MHz PCI system. See Figure 11. 001 010 011 100 33 MHz PCI. This setting guarantees the minimum output hold, item 13a, and the maximum output valid, item 12a, times as specified in Figure 10 are met for a 33 MHz PCI system. See Figure 11. 101 110 (Default if reset configuration pins left unconnected) 111

Figure 11 shows the PCI_HOLD_DEL Affect on Output Valid and Hold Time.

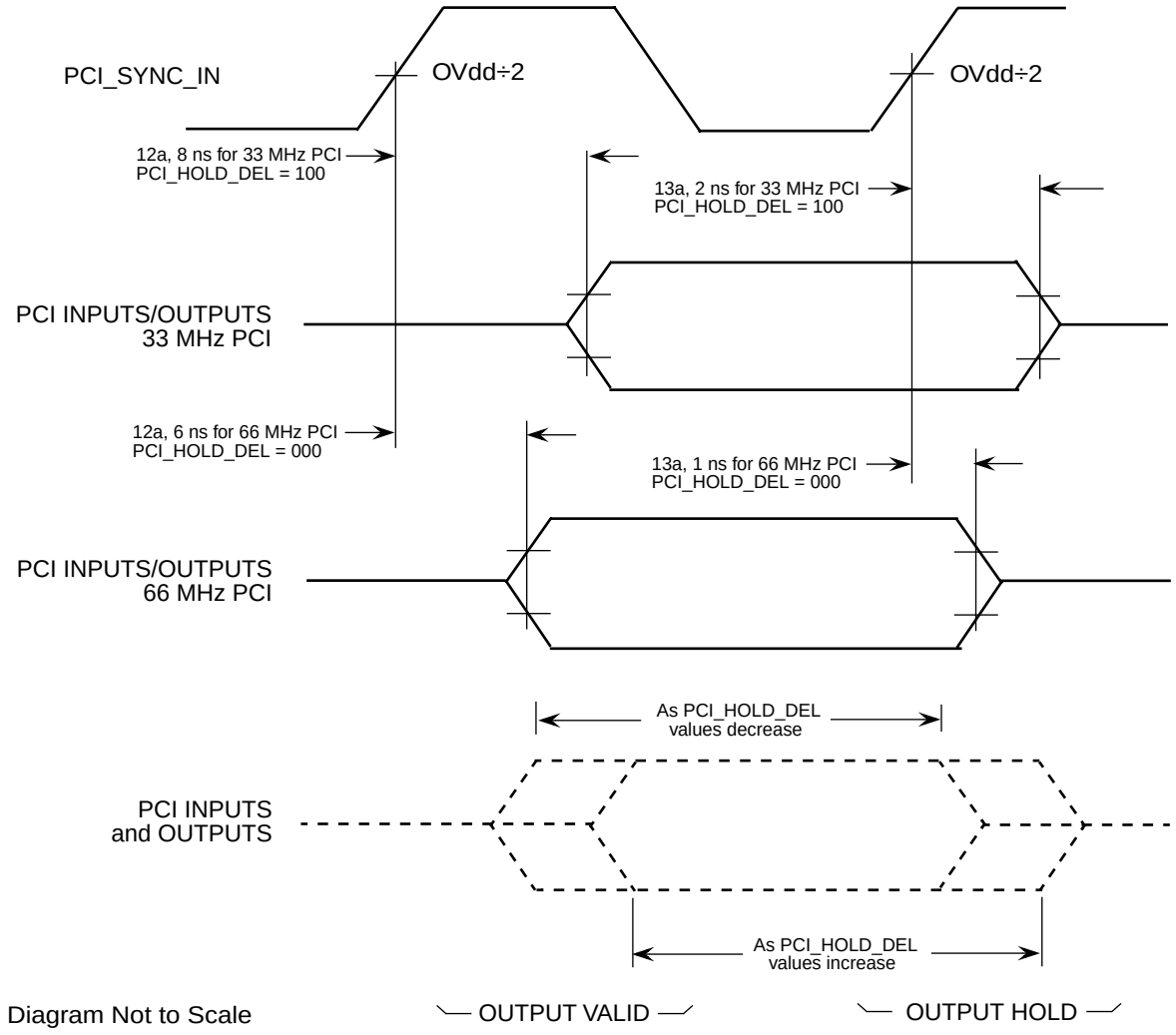


Figure 11. PCI_HOLD_DEL Affect on Output Valid and Hold Time

1.4.3.4 I^2C AC Timing Specifications

Table 12 provides the I^2C input AC timing specifications for the MPC107.

Table 12. I^2C Input AC Timing Specifications

At recommended operating conditions (see Figure 2) with LVdd = 3.3 V ± 0.3 V

Num	Characteristic	Min	Max	Unit	Notes
1	Start condition hold time	4.0	—	CLKs	1,2
2	Clock low period (The time before MPC107 will drive SCL low as a transmitting slave after detecting SCL low as driven by an external master.)	$8.0 + (16 \times 2^{FDR[4:2]}) \times (5 - 4(\{FDR[5],FDR[1]\} == b'10) - 3(\{FDR[5],FDR[1]\} == b'11) - 2(\{FDR[5],FDR[1]\} == b'00) - 1(\{FDR[5],FDR[1]\} == b'01))$	—	CLKs	1,2,4, 5
3	SCL/SDA rise time (from 0.5v to 2.4v)	—	1	ms	
4	Data hold time	0	—	ns	2
5	SCL/SDA fall time (from 2.4 to 0.5v)	—	1	ms	
6	Clock high period (Time needed to either receive a data bit or generate a START or STOP.)	5.0	—	CLKs	1,2, 5
7	Data setup time	3.0	—	ns	3
8	Start condition setup time (for repeated start condition only)	4.0	—	CLKs	1,2
9	Stop condition setup time	4.0	—	CLKs	1,2

Notes:

1 Units for these specifications are in SDRAM_CLK/CPU_CLK units.

2 The actual values depend on the setting of the digital filter frequency sampling rate (DFFSR) bits in the frequency divider register I2CFDR. Therefore, the noted timings in the above table are all relative to qualified signals. The qualified SCL and SDA are delayed signals from what is seen in real time on the I^2C bus. The qualified SCL, SDA signals are delayed by the SDRAM_CLK/CPU_CLK clock times DFFSR times 2 plus 1 SDRAM_CLK/CPU_CLK clock. The resulting delay value is added to the value in the table (where this note is referenced). See Figure 13.

3 Timing is relative to the Sampling Clock (not SCL).

4 FDR[n] refers to the Frequency Divider Register I2CFDR bit n.

5 Input clock low and high periods in combination with the FDR value in the frequency divider register (I2CFDR) determine the maximum I^2C input frequency. See Figure 13.

Table 13 provides the I^2C frequency divider register (I2CFDR) information for the MPC107.

Table 13. MPC107 Maximum I^2C Input Frequency

FDR Hex[2]	Divider[2] (Dec)	Max I^2C Input Frequency[1]			
		SDRAM_CLK/CPU_CLK @ 25 MHz	SDRAM_CLK/CPU_CLK @ 33 MHz	SDRAM_CLK/CPU_CLK @ 50 MHz	SDRAM_CLK/CPU_CLK @ 100 MHz
20, 21	160, 192	862	1.13 MHz	1.72 MHz	3.44 MHz
22, 23, 24, 25	224, 256, 320, 384	555	733	1.11 MHz	2.22 MHz
0, 1	288, 320	409	540	819	1.63 MHz
2, 3, 26, 27, 28, 29	384, 448, 480, 512, 640, 768	324	428	649	1.29 MHz
4, 5	576, 640	229	302	458	917
6, 7, 2A, 2B, 2C, 2D	768, 896, 960, 1024, 1280, 1536	177	234	354	709
8, 9	1152, 1280	121	160	243	487
A, B, 2E, 2F, 30, 31	1536, 1792, 1920, 2048, 2560, 3072	92	122	185	371
C, D	2304, 2560	62	83	125	251
E, F, 32, 33, 34, 35	3072, 3584, 3840, 4096, 5120, 6144	47	62	95	190
10, 11	4608, 5120	32	42	64	128
12, 13, 36, 37, 38, 39	6144, 7168, 7680, 8192, 10240, 12288	24	31	48	96
14, 15	9216, 10240	16	21	32	64
16, 17, 3A, 3B, 3C, 3D	12288, 14336, 15360, 16384, 20480, 24576	12	16	24	48
18, 19	18432, 20480	8	10	16	32
1A, 1B, 3E, 3F	24576, 28672, 30720, 32768	6	8	12	24
1C, 1D	36864, 40960	4	5	8	16
1E, 1F	49152, 61440	3	4	6	12

Notes:

1 Values are in KHz unless otherwise specified.

2 FDR Hex and Divider (Dec) values are listed in corresponding order.

3 Multiple Divider (Dec) values will generate the same input frequency but each Divider (Dec) value will generate a unique output frequency as shown in Table 14.

Table 14 provides the I^2C output AC timing specifications for the MPC107.

Table 14. I^2C Output AC Timing Specifications

At recommended operating conditions (see Figure 2) with LVdd = 3.3 V ± 0.3 V

Num	Characteristic	Min	Max	Unit	Notes
1	Start condition hold time	(FDR[5] == 0) x (D_{FDR}/16) / 2N + (FDR[5] == 1) x (D_{FDR}/16) / 2M	—	CLKs	1,2,5
2	Clock low period	D_{FDR} / 2	—	CLKs	1,2,5
3	SCL/SDA rise time (from 0.5 V to 2.4 V)	—	—	ms	3
4	Data hold time	8.0 + (16 x $2^{FDR[4:2]}$) x (5 - 4({FDR[5],FDR[1]} == b'10) - 3({FDR[5],FDR[1]} == b'11) - 2({FDR[5],FDR[1]} == b'00) - 1({FDR[5],FDR[1]} == b'01))	—	CLKs	1,2,5
5	SCL/SDA fall time (from 2.4 V to 0.5 V)	—	< 5	ns	4
6	Clock high time	D_{FDR} / 2	—	CLKs	1,2,5
7	Data setup time (MPC107 as a master only.)	(D_{FDR} / 2) - (Output data hold time)	—	CLKs	1,5
8	Start condition setup time (for repeated start condition only)	D_{FDR} + (Output start condition hold time)	—	CLKs	1,2,5
9	Stop condition setup time	4.0	—	CLKs	1,2

Notes:

1. Units for these specifications are in SDRAM_CLK/CPU_CLK units.
2. The actual values depend on the setting of the digital filter frequency sampling rate (DFFSR) bits in the frequency divider register I2CFDR. Therefore, the noted timings in the above table are all relative to qualified signals. The qualified SCL and SDA are delayed signals from what is seen in real time on the I^2C bus. The qualified SCL, SDA signals are delayed by the SDRAM_CLK/CPU_CLK clock times DFFS times 2 plus 1 SDRAM_CLK/CPU_CLK clock. The resulting delay value is added to the value in the table (where this note is referenced). See Figure 13.
3. Since SCL and SDA are open-drain type outputs, which the MPC107 can only drive low, the time required for SCL or SDA to reach a high level depends on external signal capacitance and pull-up resistor values.
4. Specified at a nominal 50pF load
5. D_{FDR} is the decimal divider number indexed by FDR[5:0] value. Refer to the I^2C Interface chapter's serial bit clock frequency divider selections table. FDR[x] refers to the frequency divider register I2CFDR bit x. N is equal to a variable number that would make the result of the divide (data hold time value) equal to a number less than 16. M is equal to a variable number that would make the result of the divide (data hold time value) equal to a number less than 9.

Figure 12 through Figure 15 show the I^2C timing diagrams I, II, III, and IV respectively.

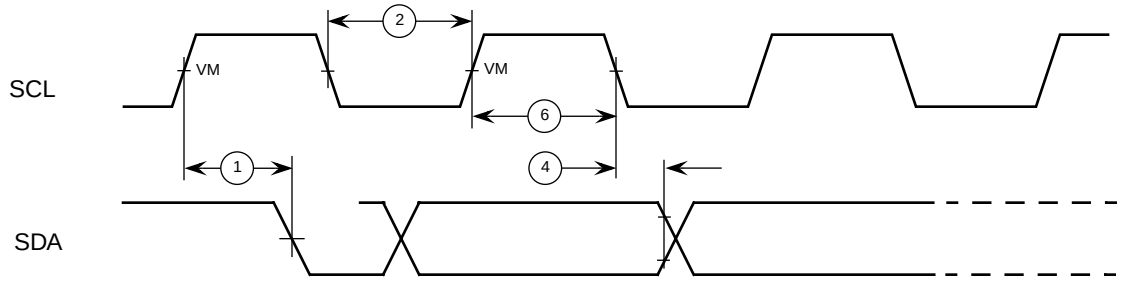


Figure 12. I²C Timing Diagram I

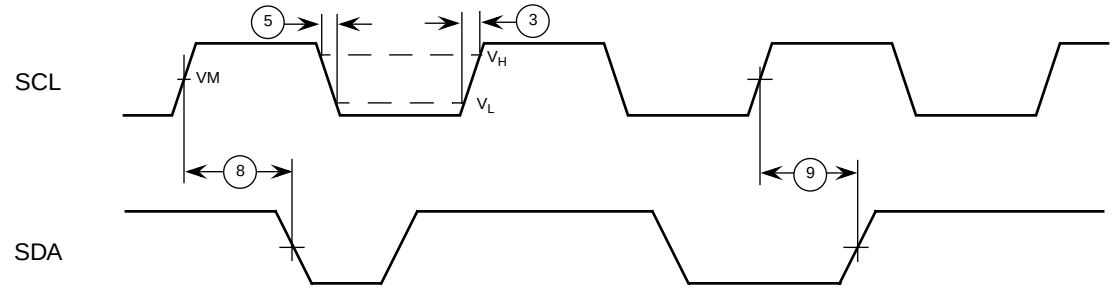
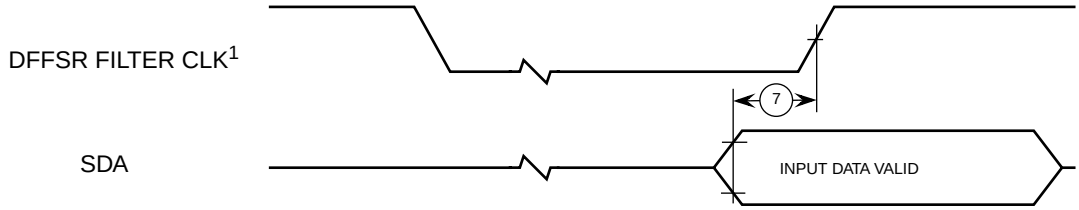


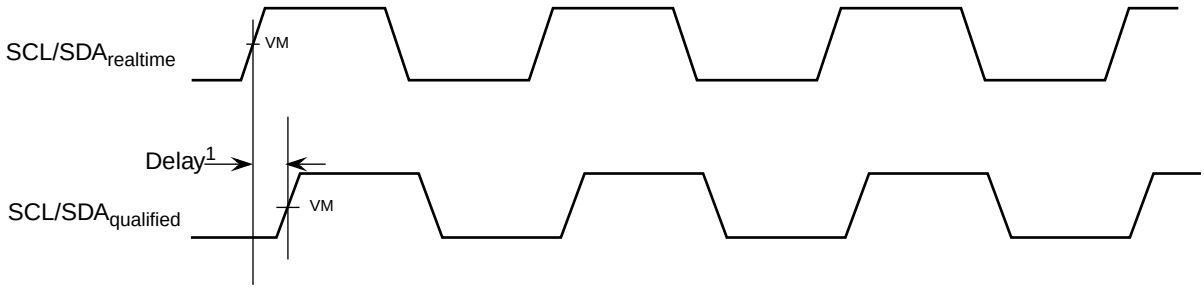
Figure 13. I²C Timing Diagram II



Notes:

1 DFFSR filter clock is the SDRAM_CLK/CPU_CLK clock times DFFSR value.

Figure 14. I²C Timing Diagram III



Notes:

1 The delay is the local memory clock times DFFSR times 2 plus 1 local memory clock.

Figure 15. I²C Timing Diagram IV (Qualified Signal)

1.4.3.5 EPIC Serial Interrupt Mode AC Timing Specifications

Table 15 provides the EPIC serial interrupt mode AC timing specifications for the MPC107.

Table 15. EPIC Serial Interrupt Mode AC Timing Specifications

At recommended operating conditions (see Figure 2) with LVdd = 3.3 V ± 0.3 V

Num	Characteristic	Min	Max	Unit	Notes
1	S_CLK frequency	1/14 SDRAM_SYNC_IN	1/2 SDRAM_SYNC_IN	MHz	1
2	S_CLK duty cycle	40	60	%	
3	S_CLK output valid time	–	6	ns	
4	Output hold time	0	–	ns	
5	$\overline{\text{S\_FRAME}}$, S_RST output valid time	–	1 sys_logic_clk period + 6	ns	2
6	S_INT input setup time to S_CLK	1 sys_logic_clk period + 2	–	ns	2
7	S_INT inputs invalid (hold time) to S_CLK	–	0	ns	2

Notes:

1 See the MPC107 User's Manual for a description of the EPIC interrupt control register (EICR) describing S_CLK frequency programming.

2 S_RST, $\overline{\text{S\_FRAME}}$, and S_INT shown in Figure 16 and Figure 17 depict timing relationships to sys_logic_clk and S_CLK and do not describe functional relationships between S_RST, $\overline{\text{S\_FRAME}}$, and S_INT. See the MPC107 User's Manual for a complete description of the functional relationships between these signals.

3 The sys_logic_clk waveform is the clocking signal of the internal peripheral logic from the output of the peripheral logic PLL; sys_logic_clk is the same as SDRAM_SYNC_IN when the SDRAM_SYNC_OUT to SDRAM_SYNC_IN feedback loop is implemented and the DLL is locked. See the MPC107 User's Manual for a complete clocking description.

Figure 15 and Figure 16 show the EPIC serial interrupt mode output and input timing diagrams respectively.

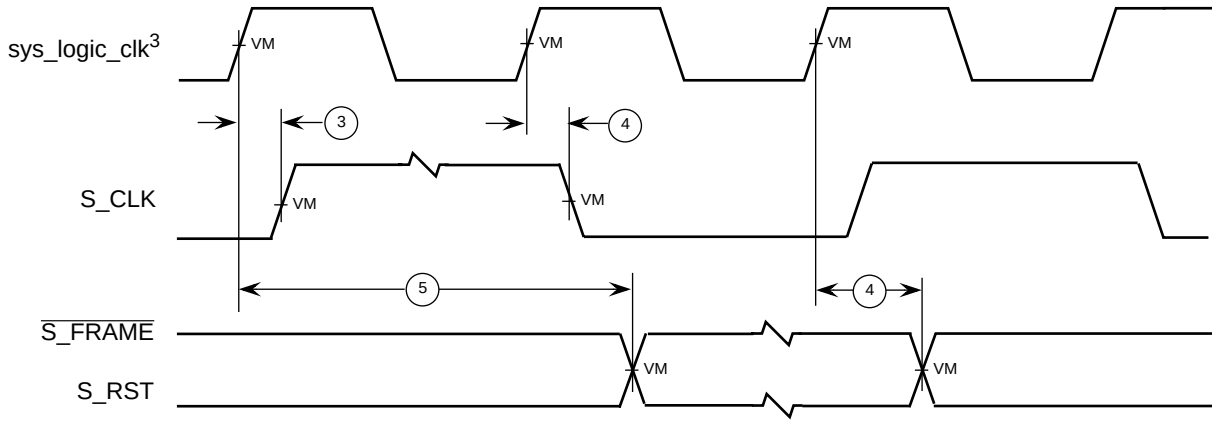


Figure 16. EPIC Serial Interrupt Mode Output Timing Diagram

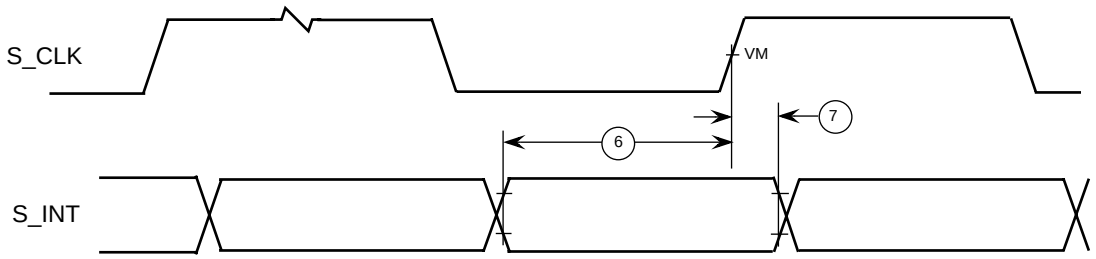


Figure 17. EPIC Serial Interrupt Mode Input Timing Diagram

1.4.3.6 IEEE 1149.1 (JTAG) AC Timing Specifications

Table 16 provides the JTAG AC timing specifications for the MPC107 while in the JTAG operating mode.

Table 16. JTAG AC Timing Specification (Independent of PCI_SYNC_IN)

At recommended operating conditions (see Figure 2) with LVdd = 3.3 V ± 0.3 V

Num	Characteristic[4]	Min	Max	Unit	Notes
	TCK Frequency of Operation	0	25	MHz	
1	TCK Cycle Time	40	—	ns	
2	TCK Clock Pulse Width Measured at 1.5 V	20	—	ns	
3	TCK Rise and Fall Times	0	3	ns	
4	TRST_ Setup Time to TCK Falling Edge	10	—	ns	1
5	TRST_ Assert Time	10	—	ns	
6	Boundary Scan Input Data Setup Time	5	—	ns	2
7	Boundary Scan Input Data Hold Time	15	—	ns	2
8	TCK to Output Data Valid	0	30	ns	3
9	TCK to Output High Impedance	0	30	ns	3
10	TMS, TDI Data Setup Time	5	—	ns	
11	TMS, TDI Data Hold Time	15	—	ns	
12	TCK to TDO Data Valid	0	15	ns	
13	TCK to TDO High Impedance	0	15	ns	

Notes:

1 $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes only.
2 Non-test (other than TDI and TMS) signal input timing with respect to TCK
3 Non-test (other than TDO) signal output timing with respect to TCK
4 Timings are independent of the system clock (PCI_SYNC_IN).

Figure 18 shows the JTAG clock input timing diagram.

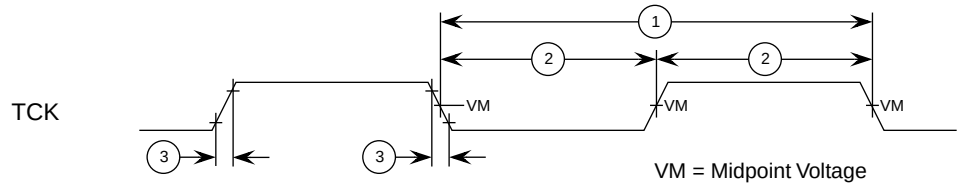


Figure 18. JTAG Clock Input Timing Diagram

Figure 19 shows the JTAG $\overline{\text{TRST}}$ timing diagram, Figure 20 the JTAG boundary scan timing diagram, and Figure 21 the test access port timing diagram.

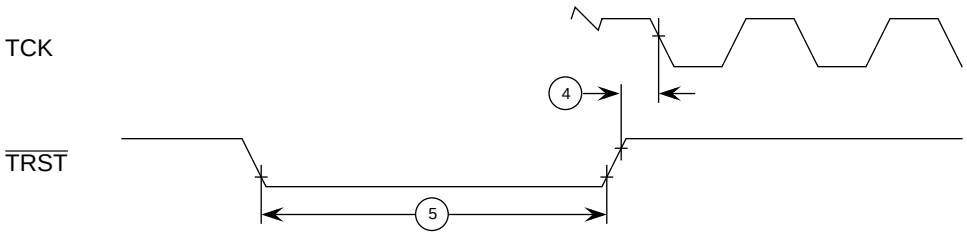


Figure 19. JTAG TRST Timing Diagram

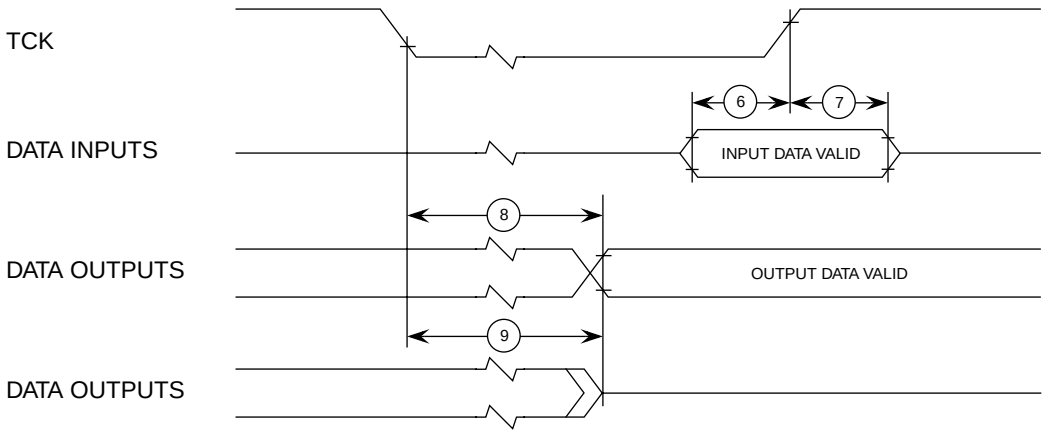


Figure 20. JTAG Boundary Scan Timing Diagram

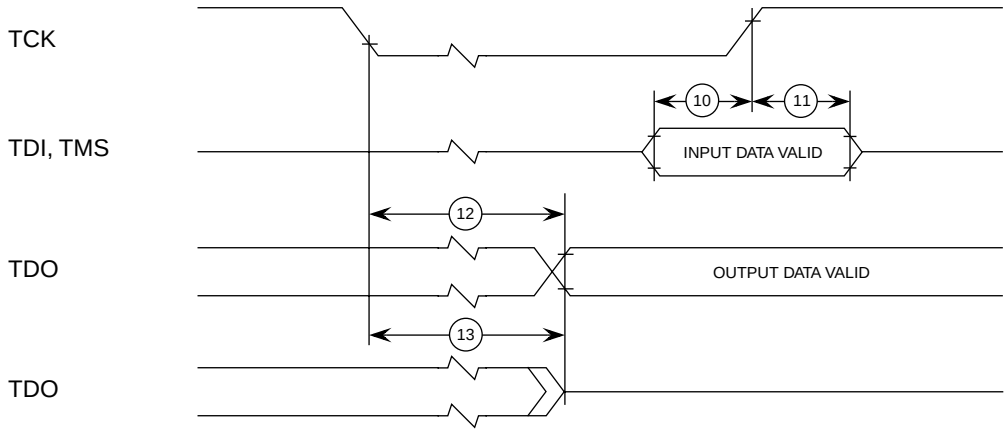


Figure 21. Test Access Port Timing Diagram

1.5 Package Description

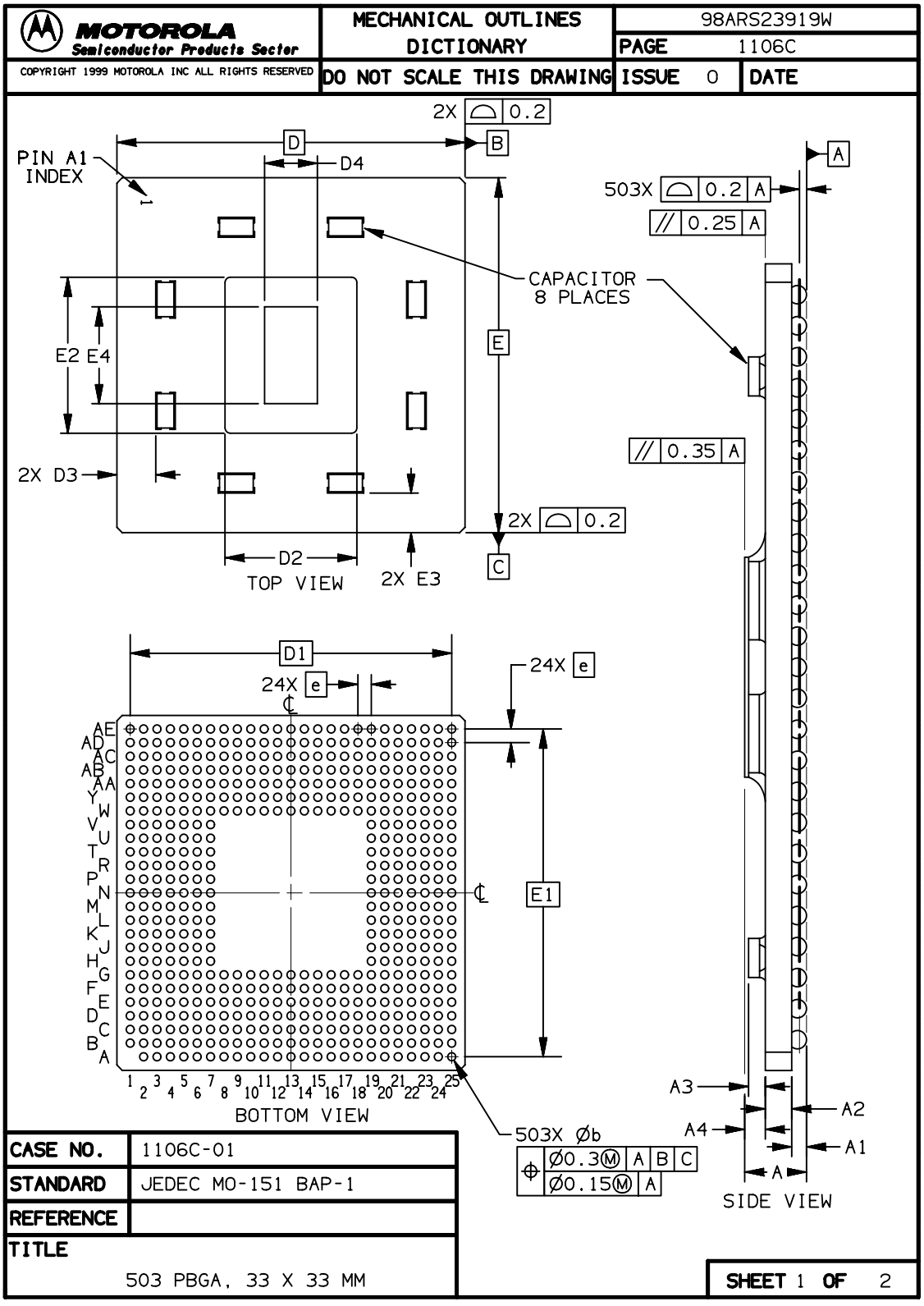
1.5.1 Package Parameters for the MPC107

The MPC107 uses a 33 mm x 33 mm, 503 pin Plastic Ball Grid Array (PBGA) package. The plastic package parameters are as provided in the following list.

Package Outline:	33 mm x 33 mm
Interconnects:	503
Pitch:	1.27 mm
Solder Attach:	63/37 Sn/Pb
Solder Balls:	63/37 Sn/Pb
Solder Ball Diameter:	0.60 - 0.90 mm
Maximum Module Height:	2.75 mm
Co-planarity Specification:	0.20 mm
Maximum Force:	6.0 lbs. total, uniformly distributed over package (5.4 grams/ball)

1.5.2 Pin Assignments and Package Dimensions

Figure 22 shows the top surface, side profile, and pinout of the MPC107, 503 PBGA package.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NOTES

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b IS THE MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. D2 AND E2 DEFINE THE AREA OCCUPIED BY THE DIE AND UNDERFILL. ACTUAL SIZE OF THIS AREA MAY BE SMALLER THAN SHOWN. D3 AND E3 ARE THE MINIMUM CLEARANCE FROM THE PACKAGE EDGE TO THE CHIP CAPACITORS.
5. CAPACITORS MAY NOT BE PRESENT ON ALL DEVICES.
6. CAUTION MUST BE TAKEN NOT TO SHORT EXPOSED METAL CAPACITOR PADS ON PACKAGE TOP.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX	DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	--	2.75							
A1	0.50	0.70							
A2	1.00	1.20							
A3	--	0.80							
A4	0.82	0.90							
b	0.60	0.90							
D	33 BSC								
D1	30.48 BSC								
D2	--	12.50							
D3	3.43	--							
D4	5.00	--							
e	1.27 BSC								
E	33 BSC								
E1	30.48 BSC								
E2	--	14.50							
E3	3.43	--							
E4	9.00	--							

CASE NO.	1106C-01
STANDARD	JEDEC MO-151 BAP-1
REFERENCE	
TITLE	503 PBGA, 33 X 33 MM
	SHEET 2 OF 2

Figure 22. MPC107 Package Dimensions and Pinout Assignments

1.5.3 Pinout Listings

Table 17 provides the pinout listing for the MPC107, 503 PBGA package.

Table 17. MPC107 Pinout Listing

Signal Name	Package Pin Number	Pin Type	Supply Voltage	Output Driver Type	Notes
60x Processor Interface Signals					
A[0–31]	AE22, AE16, AA14, AE17, AD21, AD14, AD20, AB16, AB20, AB15, AA20, AD13, Y15, AE12, AD15, AB9, AB14, AA8, AC13, Y12, Y11, AE15, AE13, AA16, Y13, AB8, AD12, AE10, AB13, Y9, Y8, AD9	I/O	BVDD	DRV_CPU	4
$\overline{\text{AACK}}$	AC7	Output	BVDD	DRV_CPU	—
$\overline{\text{ARTRY}}$	Y7	I/O	BVDD	DRV_CPU	15
$\overline{\text{BG0}}$	AE11	Output	BVDD	DRV_CPU	—
$\overline{\text{BG1}}$	AD11	Output	BVDD	DRV_CPU	—
$\overline{\text{BR0}}$	AB17	Input	BVDD	—	—
$\overline{\text{BR1}}$	Y14	Input	BVDD	—	10
$\overline{\text{CI}}$	AD16	I/O	BVDD	DRV_CPU	—
$\overline{\text{DBG0}}$	AC10	Output	BVDD	DRV_MEM_ADDR	—
$\overline{\text{DBG1}}$	AD10	Output	BVDD	DRV_MEM_ADDR	—
$\overline{\text{DBGLB}}$	AB10	Output	BVDD	DRV_MEM_ADDR	—
DH[0–31]	P1, R1, P2, T4, T1, T3, R4, P6, U6, V5, V2, T5, U1, R6, W1, V4, W2, U4, T2, V6, W3, W5, Y1, Y2, Y4, Y5, AA1, AA2, AA4, AB1, AB3, AB4	I/O	BVDD	DRV_CPU	4
DL[0–31]	AA7, W6, AB6, AA6, AB5, AC4, AD3, AB7, AE1, W4, N6, M1, N3, N4, N5, N1, M2, R2, V1, P5, P4, N2, U2, AE4, AE6, AE2, AE3, AE7, AD5, AB2, AC2, AC1	I/O	BVDD	DRV_CPU	4
DP[0–7]	AE9, AD6, AD8, AD1, AE8, AD7, AD4, AE5	I/O	BVDD	DRV_CPU	4
$\overline{\text{GBL}}$	AD17	I/O	BVDD	DRV_CPU	—
$\overline{\text{LBCLAIM}}$	Y17	Input	BVDD	—	—
$\overline{\text{TA}}$	AE14	I/O	BVDD	DRV_CPU	15
$\overline{\text{TBST}}$	AE21	I/O	BVDD	DRV_CPU	—
$\overline{\text{TEA}}$	AB11	Output	BVDD	DRV_CPU	—
$\overline{\text{TS}}$	AA10	I/O	BVDD	DRV_CPU	15
TSIZ[0–2]	AE19,AD18,AB18	I/O	BVDD	DRV_CPU	4
TT[0–4]	AD19,AC19,AB19,AA19,AA18	I/O	BVDD	DRV_CPU	4

Table 17. MPC107 Pinout Listing (Continued)

Signal Name	Package Pin Number	Pin Type	Supply Voltage	Output Driver Type	Notes
$\overline{WT}$	AC16	I/O	BVDD	DRV_CPU	—
PCI Interface Signals					
AD[31–0]	N23, N21, M20, M21, M22, M24, M25, L20, L22, K25, K24, K23, K21, J20, J24, J25, H20, F24, E25, F21, E24, E22, D25, A25, B25, A23, B23, B22, C22, C25, D23, D21	I/O	OVDD	DRV_PCI	4,11
$\overline{C/BE}$[3–0]	L24, J22, G22, A24,	I/O	OVDD	DRV_PCI	4,11
$\overline{DEVSEL}$	G23	I/O	OVDD	DRV_PCI	6,11
$\overline{FRAME}$	G20	I/O	OVDD	DRV_PCI	6,11
$\overline{GNT}$[4–0]	T24, P22, P21, R22, N20	Output	OVDD	DRV_PCI	4,11
IDSEL	L25	Input	OVDD	—	—
$\overline{INTA}$	V21	Output	OVDD	DRV_PCI	6,11,12
$\overline{IRDY}$	H24	I/O	OVDD	DRV_PCI	6,11
$\overline{LOCK}$	G21	Input	OVDD	—	6
PAR	G24	I/O	OVDD	DRV_PCI	11
$\overline{PERR}$	G25	I/O	OVDD	DRV_PCI	6,11,13
$\overline{REQ}$[4–0]	W25, V25, U25, T25, T23	Input	OVDD	—	10
$\overline{SERR}$	F25	I/O	OVDD	DRV_PCI	6,11,12
$\overline{STOP}$	H21	I/O	OVDD	DRV_PCI	6,11
$\overline{TRDY}$	H25	I/O	OVDD	DRV_PCI	6,11
Memory Interface Signals					
$\overline{AS}$	A4	Output	GVDD	DRV_MEM_ADDR	—
$\overline{CAS}$/DQM[0–7]	A2, B1, A11, A10, B3, C2, F12, D11	Output	GVDD	DRV_MEM_ADDR	4
CKE	A12	Output	GVDD	DRV_MEM_ADDR	1
$\overline{FOE}$	A13	I/O	GVDD	DRV_MEM_ADDR	1,2
MDH[0–31]	M6, L4, L6, K2, K4, K5, J4, J6, H4, H5, G3, G5, G6, F5, F1, E1, B14, D15, B15, E16, D16, C16, D18, D17, B17, F18, E19, E20, B19, B20, B21, A22	I/O	GVDD	DRV_MEM_DATA	4
MDL[0–31]	M5, L1, L2, K1, K3, J1, J2, H1, H2, H6, G2, G4, F4, G1, F2, E2, F14, F15, A16, F17, B16, A17, A18, A19, B18, E18, D19, F19, A20, C19, D20, A21	I/O	GVDD	DRV_MEM_DATA	3,4
PAR/AR[0–7]	D2, C1, A15, A14, D1, D3, F13, C13	I/O	GVDD	DRV_MEM_DATA	4

Table 17. MPC107 Pinout Listing (Continued)

Signal Name	Package Pin Number	Pin Type	Supply Voltage	Output Driver Type	Notes
RAS/$\overline{CS}$[0–7]	E6, C4, D5, E4, C10, F11, B10, B11	Output	GVDD	DRV_MEM_ADDR	4
$\overline{RCS0}$	D10	I/O	GVDD	DRV_MEM_ADDR	1,2
$\overline{RCS1}$	B9	Output	GVDD	DRV_MEM_DATA	—
$\overline{RCS2}$	B5	Output	GVDD	DRV_MEM_ADDR	—
$\overline{RCS3}$	D7	Output	GVDD	DRV_MEM_ADDR	—
SDBA0	A9	Output	GVDD	DRV_MEM_ADDR	1,2
SDBA1	A8	Output	GVDD	DRV_MEM_ADDR	—
$\overline{SDCAS}$	D4	Output	GVDD	DRV_MEM_ADDR	1
SDMA [13–0]	E10, F9, D9, F8, E8, D8, B8, E7, C7, B7, A7, B6, A6, A5	Output	GVDD	DRV_MEM_ADDR	4,5
$\overline{SDRAS}$	B4	Output	GVDD	DRV_MEM_ADDR	1
$\overline{WE}$	A3	Output	GVDD	DRV_MEM_ADDR	—
EPIC Control Signals					
$\overline{INT}$	Y22	Output	OVDD	DRV_CPU	16
IRQ_0 /S_INT	U24	Input	OVDD	—	—
IRQ_1 / S_CLK	C24	I/O	OVDD	DRV_PCI	—
IRQ_2 / S_RST	T21	I/O	OVDD	DRV_PCI	—
IRQ_3 / S_FRAME	U20	I/O	OVDD	DRV_PCI	—
IRQ_4/ L_INT	V22	I/O	OVDD	DRV_PCI	—
I^2C Control Signals					
SCL	AB25	I/O	OVDD	DRV_CPU	8,12
SDA	AB24	I/O	OVDD	DRV_CPU	8,12
Clock Signals					
CKO	V20	Output	OVDD	DRV_PCI	—
CPUCLK[0–2]	AA12, AA13, AB12	Output	BVDD	DRV_MEM_ADDR	4
OSC_IN	U22	Input	OVDD	—	—
PCI_CLK [0–4]	R25, P24, R24, N24, N25	Output	OVDD	DRV_MEM_ADDR	4
PCI_SYNC_IN	P20	Input	OVDD	—	—
PCI_SYNC_OUT	P25	Output	OVDD	DRV_MEM_ADDR	—
SDRAM_CLK [0–3]	D14, D13, E12, E14	Output	GVDD	DRV_MEM_ADDR	4
SDRAM_SYNC_IN	E13	Input	GVDD	—	—
SDRAM_SYNC_OUT	D12	Output	GVDD	DRV_MEM_ADDR	—

Table 17. MPC107 Pinout Listing (Continued)

Signal Name	Package Pin Number	Pin Type	Supply Voltage	Output Driver Type	Notes
Miscellaneous Signals					
$\overline{\text{HRESET}}$	AA23	Input	OVDD	—	—
$\overline{\text{HRESET\_CPU}}$	AB21	Output	BVDD	DRV_CPU	10,12
$\overline{\text{MCP}}$	AE20	Output	BVDD	DRV_CPU	10
NMI	AC25	Input	OVDD	—	—
$\overline{\text{QACK}}$	AE18	Output	BVDD	DRV_CPU	10
$\overline{\text{QREQ}}$	M4	Input	BVDD	—	—
$\overline{\text{SRESET}}$	Y18	Output	BVDD	DRV_CPU	10
Test/Configuration Signals					
PLL_CFG[0–3]	AC22, AD23, AD22, AE23	Input	OVDD	—	2,4
TCK	W24	Input	OVDD	—	7,10
TDI	Y25	Input	OVDD	—	7,10
TDO	W23	Output	OVDD	DRV_PCI	
$\overline{\text{TEST}}$	AA25	Input	OVDD	—	7,10
$\overline{\text{TEST1}}$	V24	Input	OVDD	—	8
$\overline{\text{TEST2}}$	D6	Input	GVDD	—	9
TMS	Y24	Input	OVDD	—	7,10
TRIG_IN	W22	Input	OVDD	—	
TRIG_OUT	W21	Output	OVDD	DRV_CPU	10
$\overline{\text{TRST}}$	AA24	Input	OVDD	—	7,10,14
Power and Ground Signals					
AVdd	AE24	Input	—	—	—
GND	AA21, AB22, AC11, AC14, AC17, AC20, AC23, AC3, AC5, AC8, AD24, AE25, C12, C15, C18, C21, C23, C3, C6, C9, E3, F10, F16, F20, F23, F6, G11, G13, G15, G18, G8, H19, H3, H7, J23, K20, K6, L19, L3, L7, M23, N19, N7, P3, R19, R23, R7, T20, T6, U3, V19, V23, V7, W11, W13, W15, W18, W8, Y10, Y16, Y19, Y20, Y3, Y6	Input	—	—	—
GVdd	B2, C5, C8, C11, C14, C17, C20, E5, E9, E11, E15, E17, F3, G7, G9, G12, G14, G17, G19, J3, J5, J7, L5, M3, M7	Input	—	—	—
LAVdd	F7	Input	—	—	—
LVdd	D22, F22, H22, K22, N22, T22	Input	—	—	—

Table 17. MPC107 Pinout Listing (Continued)

Signal Name	Package Pin Number	Pin Type	Supply Voltage	Output Driver Type	Notes
OVdd	B24, E21, E23, H23, J19, J21, L21, L23, M19, P19, P23, R21, U19, U21, U23, Y23	Input	—	—	—
BVdd	P7, R3, R5, U5, U7, V3, W7, W9, W12, W14, W17, AA3, AA5, AA9, AA11, AA15, AA17, AC6, AC9, AC12, AC15, AC18, AC21, AD2	Input	—	—	—
Vdd	K19, W16, T19, G10, G16, K7, T7, W10, W19, W20, Y21, AA22, AB23, AC24, AD25	Input	—	—	—
Manufacturing Pins					
FTP[2–3]	R20, D24	I/O	OVDD	DRV_PCI	4,8
MTP[1–2]	B12, B13	I/O	GVDD	DRV_MEM_ADDR	4,9

Notes:

1 This pin has an internal pull-up resistor which is enabled only when the MPC107 is in the reset state. The value of the internal pull-up resistor is not guaranteed, but is sufficient to ensure that a logic '1' is read into configuration bits during reset.
2 This pin is a reset configuration pin.
3 MDL[0] is a reset configuration pin and has an internal pull-up resistor which is enabled only when the MPC107 is in the reset state.The value of the internal pull-up resistor is not guaranteed, but is sufficient to insure that a logic '1' is read into configuration bits during reset.
4 Multi-pin signals such as AD[0–31] or DL[0–31] have their physical package pin numbers listed in order corresponding to the signal names. Ex: AD0 is on pin D21, AD1 is on pin D23,... AD31 is on pin N23.
5 SDMA[10–1] are reset configuration pins and have internal pull-up resistors which are enabled only when the MPC107 is in the reset state.The values of the internal pull-up resistors is not guaranteed, but are sufficient to ensure that logic '1's are read into the configuration bits during reset.
6 Recommend a weak pull-up resistor (2K – 10K Ohm) be placed on this PCI control pin to LVdd.
7 V_{IH} and V_{IL} for these signals are the same as the PCI V_{IH} and V_{IL} entries in Table 3, “DC Electrical Specifications.”
8 Recommend a weak pull-up resistor (2K – 10K Ohm) be placed on this pin to OVdd.
9 Recommend a weak pull-up resistor (2K – 10K Ohm) be placed on this pin to GVdd.
10 This pin has an internal pull-up resistor; the value of the internal pull-up resistor is not guaranteed, but is sufficient to prevent unused inputs from floating.
11 This pin is affected by programmable PCI_HOLD_DEL parameter, see Section 1.4.3.3.1, “PCI Signal Output Hold Timing.”
12 This pin is an open drain signal.
13 This pin is a sustained tri-state pin as defined by the PCI Local Bus Specification.
14 See Section 1.7.4, “Connection Recommendations,” for additional information on this pin.
15 Recommend a weak pull-up resistor (2K – 10K Ohm) be placed on this pin to BVdd.
16 If BVdd = 2.5 V ± 5%, this microprocessor interface pin needs to be DC voltage level shifted from OVdd (3.3 V ± 0.3 V) to 2.5 V ± 5%; this can typically be accomplished with a two resistor voltage divider circuit since $\overline{INT}$ is an output only signal.

1.6 PLL Configuration

The MPC107’s internal PLL is configured by the PLL_CFG[0–3] signals. For a given PCI_SYNC_IN (PCI bus) frequency, the PLL configuration signals set the Core/Memory/Processor PLL (VCO) frequency of operation for the PCI-to-Core/Memory/Processor frequency multiplying, if any. All valid PLL configurations for the MPC107 are shown in Table 18.

Table 18. MPC107 Microprocessor PLL Configuration

Ref	PLL_CFG[0–3][2]	66 MHz Part		100 MHz Part		PCI:Core Ratio	VCO Multiplier
		PCI_SYNC_IN Range (MHz)	Core/Mem/CPU Range (MHz)	PCI_SYNC_IN Range (MHz)	Core/Mem/CPU Range (MHz)		
1	0001	25[5] – 50[4]	25 – 50	25[5] – 50[4]	25 – 50	1	4
2	0010	12.5[5] – 25[4]	25 – 50	12.5[5] – 25[4]	25 – 50	2	4
3	0011	Bypass		Bypass		Bypass	Bypass
5	0101	25[5] – 33	50 – 66	25[5] – 50	50 – 100	2	2
8	1000	16[5] – 22	50 – 66	16[5] – 33	50 – 100	3	2
9	1001	33[5] – 44	50 – 66	33[5] – 66	50 – 100	1.5	2
C	1100	20[5] – 26	50 – 66	20[5] – 40	50 – 100	2.5	2
D	1101	50[5] – 66	50 – 66	50[5] – 66	50 – 66	1	2
F	1111	Clock off[3]	Not usable	Clock off[3]	Not usable	Off	Off

Notes:

1 PLL_CFG[0–3] settings not listed (0000, 0100, 0110, 0111, 1010, 1011, and 1110) are reserved.

2 In PLL Bypass mode, the PCI_SYNC_IN input signal clocks the internal core directly, the PLL is disabled, and the PCI:core mode is set for 1:1 mode operation. The AC timing specifications given in this document do not apply in PLL bypass mode.

3 In Clock Off mode, no clocking occurs inside the MPC107 regardless of the PCI_SYNC_IN input.

4 Limited due to maximum memory VCO = 200 MHz.

5 Limited due to minimum memory VCO = 100 MHz.

6 Range values are shown rounded down to the nearest whole number (decimal place accuracy removed) for clarity.

1.7 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC107.

1.7.1 PLL Power Supply Filtering

The AVdd and LAVdd power signals are provided on the MPC107 to provide power to the peripheral logic/memory bus PLL and the SDRAM clock delay-locked loop (DLL), respectively. To ensure stability of the internal clocks, the power supplied to the AVdd and LAVdd input signals should be filtered of any noise in the 500kHz to 10MHz resonant frequency range of the PLLs. A separate circuit similar to the one shown in Figure 23 using surface mount capacitors with minimum effective series inductance (ESL) is recommended for each of the AVdd and LAVdd power signal pins. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over using multiple values.

The circuits should be placed as close as possible to the respective input signal pins to minimize noise coupled from nearby circuits. Routing directly as possible from the capacitors to the input signal pins with minimal inductance of vias is important but proportionately less critical for the LAVdd pin.

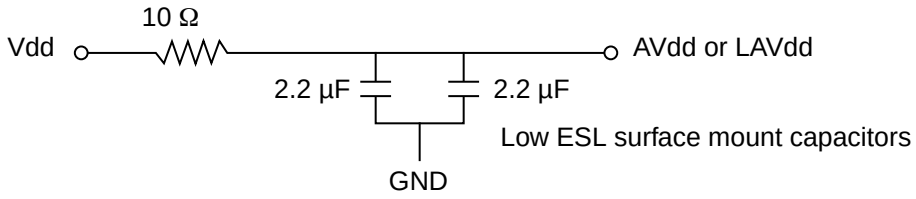

Figure 23. PLL Power Supply Filter Circuit

1.7.2 Power Supply Voltage Sequencing

The notes in Table 2 contain cautions illustrated in Figure 2 about the sequencing of the external bus voltages and internal voltages of the MPC107. These cautions are necessary for the long term reliability of the part. If they are violated, the electrostatic discharge (ESD) protection diodes will be forward biased and excessive current can flow through these diodes. Figure 2 shows a typical ramping voltage sequence where the DC power sources (voltage regulators and/or power supplies) are connected as shown in Figure 24. The voltage regulator delay shown in Figure 2 can be zero if the various DC voltage levels are all applied to the target board at the same time. The ramping voltage sequence shows a scenario in which the Vdd/AVdd/LAVdd power plane is not loaded as much as the OVdd/GVdd power plane and thus Vdd/AVdd/LAVdd ramps at a faster rate than OVdd/GVdd.

If the system power supply design does not control the voltage sequencing, the circuit of Figure 24 can be added to meet these requirements. The MUR420 diodes of Figure 24 control the maximum potential difference between the 3.3V bus and internal voltages on power-up and the 1N5820 Schottky diodes regulate the maximum potential difference on power-down.

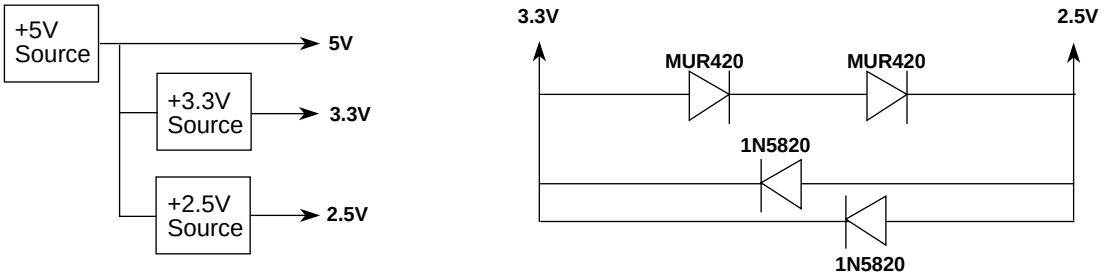

Figure 24. Example Voltage Sequencing Circuits

1.7.3 Decoupling Recommendations

Due to the MPC107's dynamic power management feature, large address and data buses, and high operating frequencies, the MPC107 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC107 system, and the MPC107 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each Vdd, OVdd, GVdd, and LVdd pin of the MPC107. It is also recommended that these decoupling capacitors receive their power from separate Vdd, OVdd, GVdd, and GND power planes in the PCB, utilizing short traces to minimize inductance. These capacitors should have a value of 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0508 or 0603, oriented such that connections are made along the length of the part.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the Vdd, OVdd, GVdd, BVdd, and LVdd planes to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors: 100–330 µF (AVX TPS tantalum or Sanyo OSCON).

1.7.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OVdd. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external Vdd, OVdd, GVdd, LVdd, BVdd, and GND pins of the MPC107.

The PCI_SYNC_OUT signal is intended to be routed halfway out to the PCI devices and then returned to the PCI_SYNC_IN input of the MPC107.

The SDRAM_SYNC_OUT signal is intended to be routed halfway out to the SDRAM devices and then returned to the SDRAM_SYNC_IN input of the MPC107. The trace length may be used to skew or adjust the timing window as needed. See Motorola application note AN1794/D for more information on this topic.

The $\overline{\text{TRST}}$ signal must be asserted during reset to ensure proper initialization and operation of the MPC107. It is recommended that the $\overline{\text{TRST}}$ signal be connected to the system $\overline{\text{HRESET}}$ signal or pulled down with a 100- to 1K-Ohm resistor.

1.7.5 Pull-up/Pull-down Resistor Requirements

The data bus input receivers are normally turned off when no read operation is in progress; therefore, they do not require pull-up resistors on the bus. The processor data bus signals are: DH[0–31], DL[0–31], and DP[0–7]. The memory data bus signals are: MDH[0–31], MDL[0–31], and PAR/AR[0–7].

If the 32-bit data bus mode is selected, the input receivers of the unused data and parity bits (DL[0–31], DP[4–7], MDL[0–31], and PAR[4–7]) will be disabled, and their outputs will drive logic zeros when they would otherwise normally be driven. For this mode, these pins do not require pull-up resistors, and should be left unconnected by the system to minimize possible output switching.

It is recommended that $\overline{\text{ARTRY}}$, $\overline{\text{TA}}$, and $\overline{\text{TS}}$ have weak pull-up resistors (2K – 10K Ohms) connected to BVdd.

It is recommended that MTP[1–2] and $\overline{\text{TEST2}}$ have weak pull-up resistors (2K – 10K Ohms) connected to GVdd.

It is recommended that the following signals be pulled up to OVdd with weak pull-up resistors (2K – 10K Ohms): SDA, SCL, $\overline{\text{TEST1}}$, and FTP[2–3].

It is recommended that the following PCI control signals be pulled up to LVdd with weak pull-up resistors (2K – 10K Ohms): $\overline{\text{DEVSEL}}$, $\overline{\text{FRAME}}$, $\overline{\text{IRDY}}$, $\overline{\text{LOCK}}$, $\overline{\text{PERR}}$, $\overline{\text{SERR}}$, $\overline{\text{STOP}}$, $\overline{\text{TRDY}}$, and $\overline{\text{INTA}}$. The resistor values may need to be adjusted stronger to reduce induced noise on specific board designs.

The following pins have internal pull-up resistors enabled at all times: $\overline{\text{REQ}}$[0–4], TCK, TDI, TMS, $\overline{\text{TRST}}$, $\overline{\text{BR1}}$, $\overline{\text{HRESET\_CPU}}$, $\overline{\text{MCP}}$, $\overline{\text{QACK}}$, $\overline{\text{SRESET}}$, $\overline{\text{TEST}}$ and $\overline{\text{TRIG\_OUT}}$. See Table 17, “MPC107 Pinout Listing,” for more information.

The following pins have internal pull-up resistors enabled only while device is in the reset state: MDL0, $\overline{\text{FOE}}$, $\overline{\text{RCS0}}$, $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, CKE, SDBAO, and SDMA[10–1]. See Table 17, “MPC107 Pinout Listing,” for more information.

The following pins are reset configuration pins: MDL0, $\overline{\text{FOE}}$, $\overline{\text{RCS0}}$, SDBAO, SDMA[10–1], and PLL_CFG[0–3]. These pins are sampled during reset to configure the device.

Any other unused active-low input pins should be tied to a logic one level via weak pull-up resistors (2K – 10K Ohms) to the appropriate power supply listed in Figure 17. Unused active-high input pins should be tied to GND via weak pull-down resistors (2K – 10K Ohms).

1.7.6 Thermal Management Information

This section provides thermal management information for the plastic ball grid array (PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent upon the system-level design: the heat sink, airflow and thermal interface material. Figure 25 depicts the die junction-to-ambient thermal resistance for two typical cases:

1. A heat sink is not attached to the PBGA package and there exists high board-level thermal loading of adjacent components. See “Typical Upper Limit” curve in Figure 25.
2. A heat sink is not attached to the PBGA package and there exists low board-level thermal loading of adjacent components. See “Typical Lower Limit” curve in Figure 25.

Figure 25 shows the die junction-to-ambient resistance.

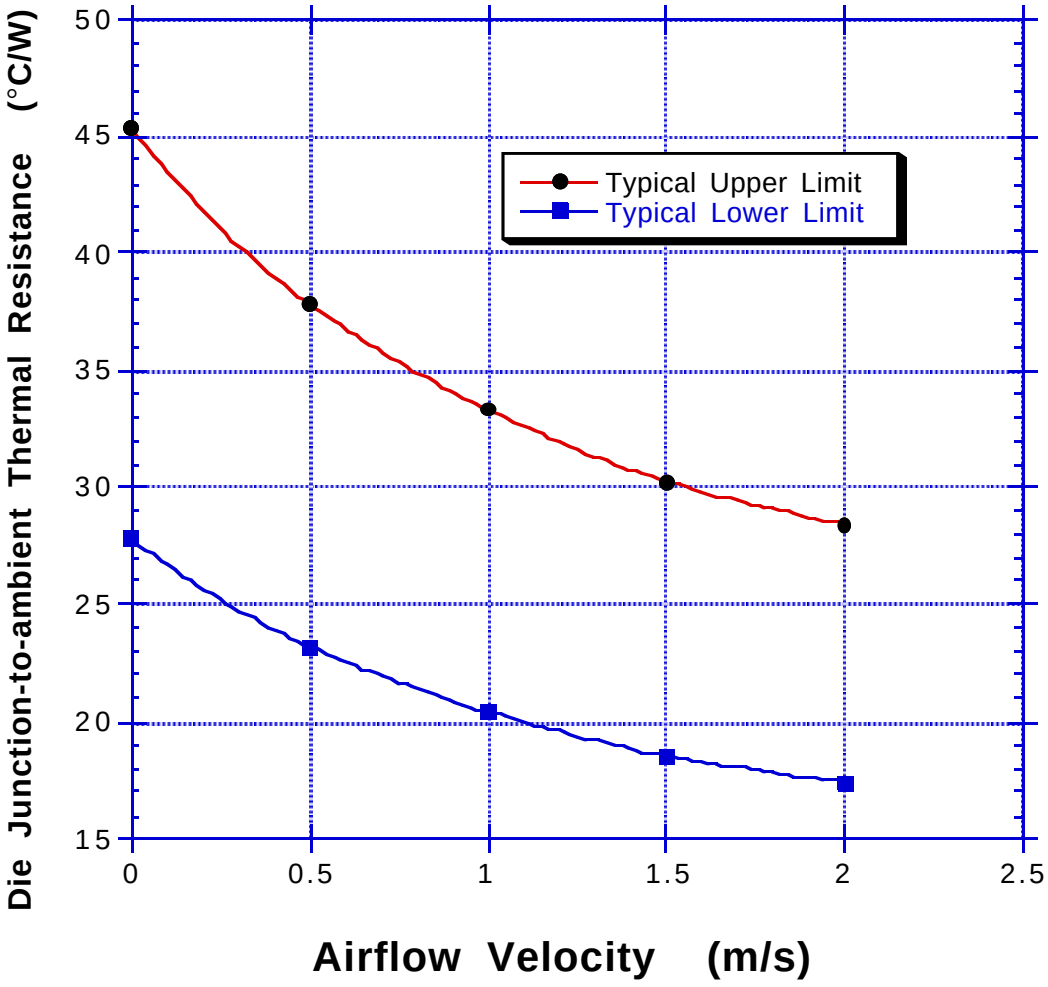

Figure 25. Die Junction-to-Ambient Thermal Resistance

1.7.6.1 Internal Package Conduction Resistance

For the PBGA packaging technology, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-ball thermal resistance

Figure 26 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

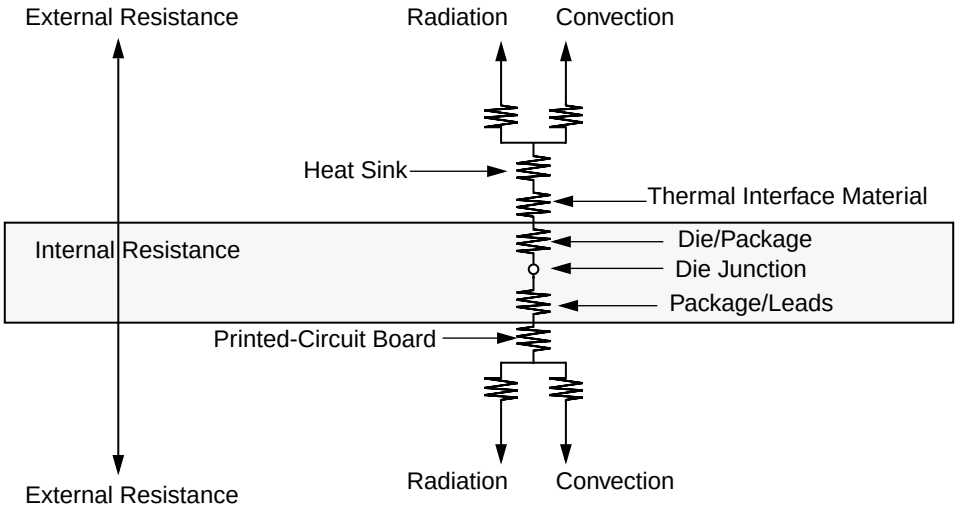

Figure 26. C4 Package with Heat Sink Mounted to a Printed-Circuit Board

For this PBGA package, heat is dissipated from the component via several concurrent paths. Heat is conducted through the silicon and may be removed to the ambient air by convection or radiation. In addition, a second, parallel heat flow path exists by conduction in parallel through the C4 bumps and the epoxy under-fill to the plastic substrate for further convection cooling off the edges. Then from the plastic substrate, heat is conducted via the leads/balls to the next-level interconnect (printed-circuit board), whereupon the primary mode of heat transfer is by convection or radiation.

1.8 Document Revision History

Table 19 provides a revision history for this hardware specification.

Table 19. Document Revision History

Document Revision	Substantive Change(s)
0	Preliminary release with some TBDs in the spec tables.
0.1	Removed references to CBGA packaging. Removed references to BVdd = 2.5V and GVdd = 2.5V until device characterization is complete. Corrected “Power Supply Ramp Up” range in Figure 2 to show Vdd being stable BEFORE 100 microsecond PLL Relock time. Modified Table 4: • Filled in current values from IBIS model. • Changed “DRV_STD” to “DRV_CPU” and changed “OVdd” to “BVdd”. Added Note 10 referencing power consumption on PLL supply voltage pins to Table 5. Updated Table 6 PBGA package thermal characteristics. Corrected DLL Lock Range (DLL_EXTEND=1) equation in Table 8. Modified Figure 6 reducing T_{loop} Propagation Delay Time from 40 ns to 15 ns. Modified Figure 22 for PBGA packaging. Updated Table 17, the table’s notes, and the corresponding text in Section 1.7.5, “Pull-up/Pull-down Resistor Requirements.” Modified Note 5 of Table 18 reducing maximum memory VCO frequency from 225 MHz to 200 MHz. Updated the affected PLL_CFG[0-3] entries (0001 and 0010) in the table. Revised Section 1.7.6, “Thermal Management Information,” for PBGA packaging.
0.2	Lowered PCI Input Frequency (PCI_SYNC_IN) in Table 7 from 25 MHz to 12.5 MHz, see Table 18 for specific details on applicability of lower input frequency. Modified Table 8: • Completed specification numbering. • Combined PCI_SYNC_IN jitter specifications, 7 and 8, into specification 7. • Added specification 9d. • Updated values for specifications 7, 9b, and 9c. • Deleted OSC_IN Jitter (Cycle-to-Cycle) specification. • Added Note 8 to specifications 1a, 1b, 17, and 18; updated the “Min” part of these specifications to correspond to the lower PCI 12.5 MHz input frequency. Added Figure 5. Replaced Input AC Timing TBDs in Table 9 with values. Replaced Output AC Timing TBDs for specifications 12c, 12d, 12e, and 14a in Table 10 with values. Replaced Figure 22 with Motorola standard packaging drawing for 503 pin PBGA. Updated Table 18: • Lowered input frequency on Refs 2 and C. • Ref A changed to reserved. • Ref 8 is changed to usable for 66 MHz devices.

Table 19. Document Revision History (Continued)

Document Revision	Substantive Change(s)
0.3	Removed references to the suspend (power-saving) mode. Section 1.3 technology reference updated from 0.35 µm to 0.29 µm CMOS. Updated Figure 2 and Note 5 to indicate only $\overline{\text{HRESET}}$ must transition to a logic 1 in one clock cycle for the device to be in the non-reset state. Table 3: Changed minimum “Input High Voltage,” for “PCI only” from 0.5*OVdd to 0.65*OVdd and added Note 6. Changed condition on “Input Low Voltage,” V_{IL}, from “All inputs except OSC_IN” to “All inputs except PCI_SYNC_IN.” Replaced minimum CV_{IH} formula, 0.5*OVdd, with 2.4V value. Replaced maximum CV_{IL} formula, 0.3*OVdd, with 0.4V value. Updated IBIS model version from v1.0 to v1.1, changed LVdd references to OVdd in Table 4 and notes, changed Notes 3 and 4 for the values to be read from the IBIS model’s I(Min) column, and updated the I_{OL} column values. Replaced most TBDs in Table 5 for with new preliminary power consumption estimates. Deleted specs 22 and 23 from Table 8; they were DC levels covered in Table 3. Replaced TBDs in Table 10 for spec 14b. Separated CKE output valid timing from specification 12b (added 12b1 and 12b2) dependent upon device’s maximum operating frequency; see Table 10. Replaced TBDs in Table 15 for specs 3, 5, & 6. Modified Table 17: • Renamed SUSPEND pin (V24) to $\overline{\text{TEST1}}$ and moved it from Miscellaneous Signals group to Test/Configuration Signals group. Added notes about pulling it up to OVdd. • Renamed RTC pin (D6) to $\overline{\text{TEST2}}$ and moved it from Memory Interface Signals group to Test/Configuration Signals group. Added notes about pulling it up to GVdd. • Added Note 14 for $\overline{\text{TRST}}$ pin. • Added Note 6 for $\overline{\text{INTA}}$ pin. Also added $\overline{\text{INTA}}$ to LVdd pull-up list in Section 1.7.5. Deleted Note 1 from Table 18; adjusted remaining note numbers. Added paragraph in Section 1.7.4 for $\overline{\text{TRST}}$ connection.

Table 19. Document Revision History (Continued)

Document Revision	Substantive Change(s)
0.4	Added BVdd = 2.5 V information to document: Table 2, Table 3, and Table 4. Updated Table 4 and the associated notes. Updated specific operating conditions at the top of the following tables: Table 7 – Table 10, Table 12, Table 14 – Table 16. Replaced Figure 22, “MPC107 Package Dimensions and Pinout Assignments,” with a clearer diagram of the 503 PBGA package. Modified Table 17: • Added Note 15 for BVdd pull-ups to the following pins: $\overline{\text{ARTRY}}$, $\overline{\text{TA}}$, and $\overline{\text{TS}}$. • Added Note 16 for $\overline{\text{INT}}$ signal in BVdd = 2.5 V applications. • Changed $\overline{\text{AACK}}$ pin type from I/O to output. • Changed Output Driver Type from DRV_MEM_DATA to DRV_MEM_ADDR on the following pins: $\overline{\text{FOE}}$, $\overline{\text{RCS0}}$, $\overline{\text{RCS2}}$, and $\overline{\text{RCS3}}$. • Deleted RTC signal (D6) from Memory Interface Signals group since it is now $\overline{\text{TEST2}}$ in the Test/Configuration Signals group. Added PLL_CFG[0-3] = 0000 to Note 1 of Table 18 for reserved settings. Added BVdd pull-up information to Section 1.7.5, “Pull-up/Pull-down Resistor Requirements.”
0.5	Separated V_{OH} and V_{OL} DC specs for CPUCLK[0–2] signals at BVdd = 2.5V from the other output pins’ DC levels. Updated Table 8 with correct DLL_extend default value. Reversed vector ordering for the PCI Interface Signals in Table 17: $\overline{\text{C/BE}}$[0–3] changed to $\overline{\text{C/BE}}$[3–0], AD[0–31] changed to AD[31–0], $\overline{\text{GNT}}$[0–3] changed to $\overline{\text{GNT}}$[3–0], and $\overline{\text{REQ}}$[0–3] changed to $\overline{\text{REQ}}$[3–0]. The package pin number orderings were also reversed, meaning that pin functionality did NOT change. For example, AD0 is still on signal D21, AD1 is still on signal D23, ... AD31 is still on signal N23. This change makes the vectored PCI signals in the MPC107 Hardware Specification consistent with the PCI Local Bus Specification and the MPC107 User Manual vector ordering.

1.9 Ordering Information

This section provides the part numbering nomenclature for the MPC107. Note that the individual part numbers correspond to a maximum core/memory/processor frequency. For available frequencies, contact your local Motorola sales office.

Figure 27 provides the Motorola part numbering nomenclature for the MPC107. Each part number also contains a revision code. This refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only.

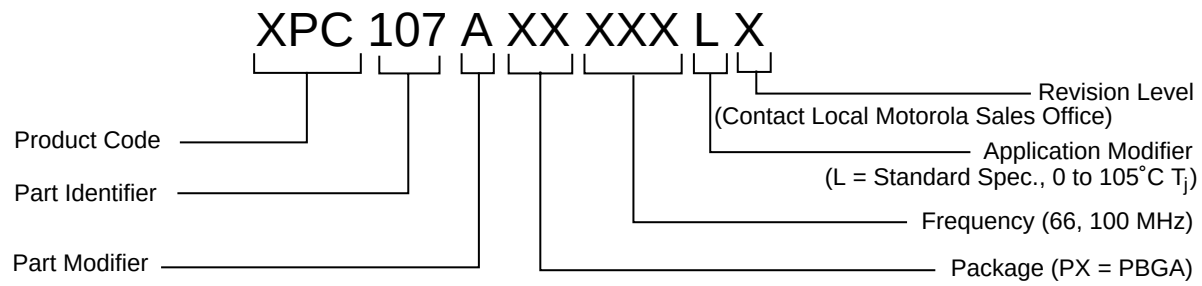

Figure 27. Motorola Part Number Key

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