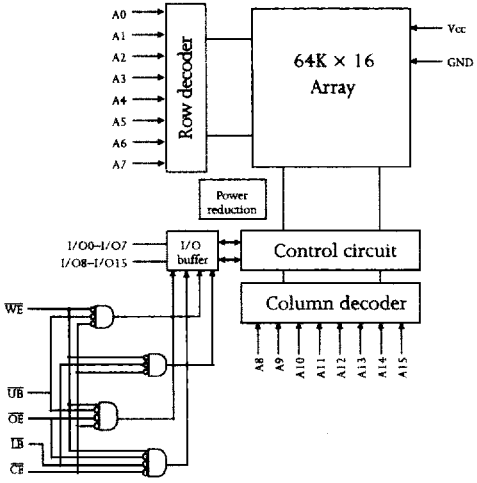
64K × 16 IntelliWatt™ low power CMOS SRAM

Advance information

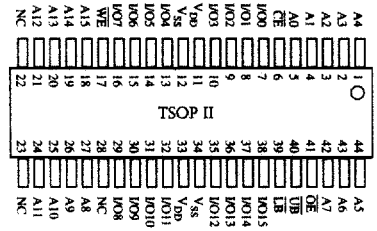
Features

- Optimized design for battery operated portable systems
- Intelliwatt™ active power reduction circuitry
- Organization: 65,536 words × 16 bits
- 2.3V to 3.0V operating range (JESD 8-5)
- High speed
  - 55/70/100 ns address access time
- Low power consumption
  - Active: 54 mW max (100 ns cycle)
  - Typical: <15 mW (100 ns cycle)
  - Standby: 3.0 µW max
  - Very low DC component in active power
- 1.5V data retention
- Equal access and cycle times
- Easy memory expansion with $\overline{CE}$, $\overline{OE}$ inputs
- LVTTL/LVCMOS-compatible, three-state I/O
- JEDEC registered packaging
  - 44-pin TSOP II package
  - 48-ball csp 8mm × 6mm BGA
- Center power and ground pins for low noise
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA
- Industrial and commercial temperature available
- Other voltage versions available
  - 1.65V to 1.95V (AS7C181026LL)
  - 2.7V to 3.3V (AS7C31026LL)

Logic block diagram



Pin arrangement



48-CSP Ball-Grid-Array Package (shading indicates no ball)

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A_0	A_1	A_2	NC
B	I/O_8	$\overline{UB}$	A_3	A_4	$\overline{CE}$	I/O_0
C	I/O_9	I/O_{10}	A_5	A_6	I/O_1	I/O_2
D	V_{SS}	I/O_{11}	NC	A_7	I/O_3	V_{DD}
E	V_{DD}	I/O_{12}	NC	NC	I/O_4	V_{SS}
F	I/O_{14}	I/O_{13}	A_{14}	A_{15}	I/O_5	I/O_6
G	I/O_{15}	NC	A_{12}	A_{13}	$\overline{WE}$	I/O_7
H	no ball	A_8	A_9	A_{10}	A_{11}	no ball

Selection guide

	7C251026LL-55	7C251026LL-70	7C251026LL-100	Unit
Maximum address access time	55	70	100	ns
Maximum output enable access time	25	35	50	ns
Maximum operating current	25	20	15	mA
Maximum standby current	1	1	1	µA

Functional description

The AS7C251026LL is a high performance CMOS 1,048,576-bit Static Random Access Memory (SRAM) organized as 65,536 words × 16 bits. It is designed for portable applications where fast data access, long battery life, low heat dissipation, and simple interfacing are desired.

Equal address access and cycle times (t_{AA}, t_{RO} t_{WC}) of 55/70/100 ns are ideal for high performance applications. The chip enable input $\overline{CE}$ permits easy memory expansion with multiple-bank memory systems.

When $\overline{CE}$ is High, or when $\overline{UB}$ and $\overline{LB}$ are simultaneously pulled Low, the device enters standby mode. The AS7C251026LL is guaranteed not to exceed 3.0 µW power consumption in CMOS standby mode. This device also offers data retention down to 1.5V.

A write cycle is accomplished by asserting write enable ($\overline{WE}$) and chip enable ($\overline{CE}$). Data on the input pins I/O0-I/O15 is written on the rising edge of $\overline{WE}$ (write cycle 1) or $\overline{CE}$ (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and chip enable ($\overline{CE}$), with write enable ($\overline{WE}$) High. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

The device provides multiple center power and ground pins, and separate byte enable controls, allowing individual bytes to be written and read. $\overline{LB}$ controls the lower bits, I/O0–I/O7, and $\overline{UB}$ controls the higher bits, I/O8–I/O15.

The device is packaged in common industry standard packages. Chip scale BGA packaging, easy to use in manufacturing, provides the smallest possible footprint. This 48-ball JEDEC registered package has a ball pitch of 0.75 mm and external dimensions of 8 mm × 6 mm.

Low power design

In the AS7C251026LL design, priority was placed on low power, while maintaining moderately high performance. To reduce standby and data retention current, a 6-transistor memory cell was utilized. Active power was reduced considerably over traditional designs by using Intelliwatt™ power reduction circuitry. With Intelliwatt, SRAM powers down unused circuits between access operations, providing incremental power savings. During periods of inactivity, Intelliwatt SRAM power consumption approaches fully deactivated standby power, even though the chip is enabled. This power savings, both in active and inactive modes, results in longer battery life, and better system marketability. All chip inputs and outputs are TTL-compatible, and operation is from a single power supply. The supply voltage range for the AS7C251026LL conforms to JEDEC standard JESD8-5.

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