LF3370
High-Definition Video Format Converter

LOGIC DEVICES INCORPORATED

FEATURES

- 83 MHz Data Rate for HDTV Applications
- Supports Multiple Video Formats Bi-Directional Conversions:
  - 4:2:2:4
  - 4:4:4:4
  - R/G/B/Key
  - Y/U/V/Key
- Multiplexed and Non-multiplexed I/O Data
- User-Programmable:
  - 3 x 3 Colorspace Converter
  - LUT for Gamma Correction
  - I/O Bias Compensation
  - Bypass Capability
- 13-bit Data Path, Colorspace Converter Coefficients and Key Channel Scaling Coefficients
- 160-lead PQFP

DESCRIPTION

The LF3370 is a video format converter capable of operating at HDTV data rates. This device converts to and from any of the various SDTV/HDTV digital video formats by utilizing an internal 3 x 3 Matrix Multiplier and two 1:2 Interpolation/2:1 Decimation Half-Band Filters.

Using the Input Demultiplexer and Output Multiplexer, the LF3370 can accept and output interleaved or non-interleaved video. For example, R/G/B/Key data can be color space converted to Y/U/V/Key and down-converted to 4:2:2:4. By re-arranging the order of the functional sections, the opposite conversion can be achieved. The coefficients for the 3 x 3 Matrix Multiplier are fully user programmable to support a wide range of color space conversions. The two Interpolation/Decimation Half-Band Filters are fully compliant with SMPTE 260M.

Input and Output Bias Adders are included for removing or adding a user-defined bias into the video signal. In addition, three programmable 1K x 13-bit Look-Up Tables (LUTs) have also been included for various uses such as gamma correction. A Scaler has been included on the Key Channel for scaling to a desired magnitude using user programmable coefficients.

Input signals can also be forced to user-defined levels for horizontal blanking. Furthermore, a Round/Select/Limit (RSL) circuitry is provided at the end of various stages to provide the best possible conversions without color violations. For additional flexibility, all sections can be individually bypassed using an internal programmable length delay. All control and coefficient registers are loaded through the LF Interface™.

This device operates at 3.3 V (5 V tolerant I/O) and is available in 160-lead PQFP package.

LF3370 BLOCK DIAGRAM

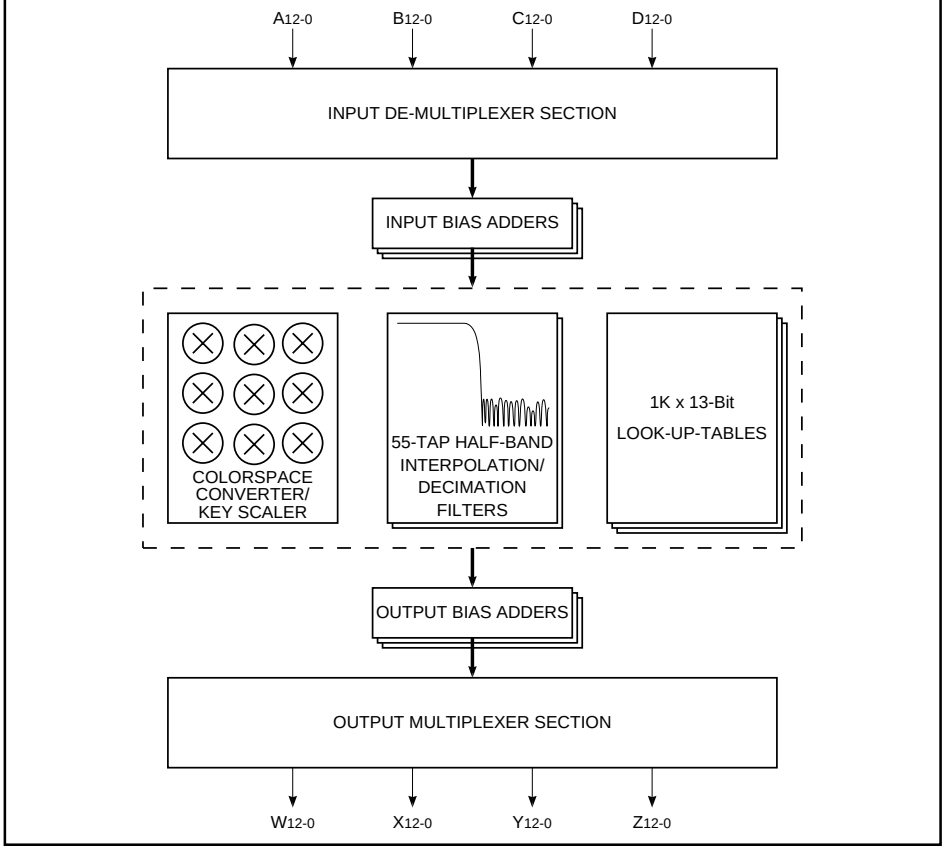


FIGURE 1. LF3370 FUNCTIONAL BLOCK DIAGRAM (HALF-BAND FILTER TO COLORSPACE ARRANGEMENT)

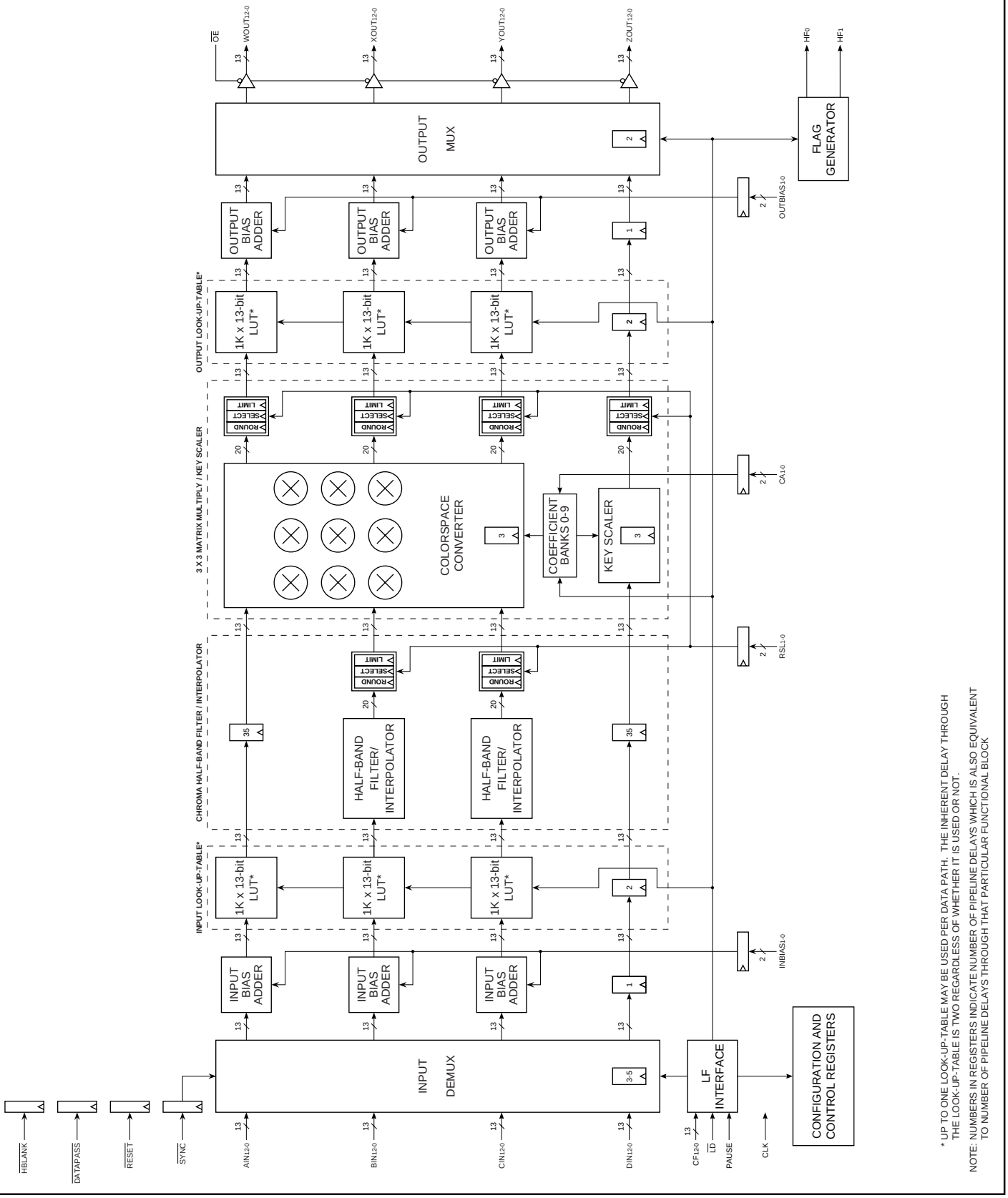
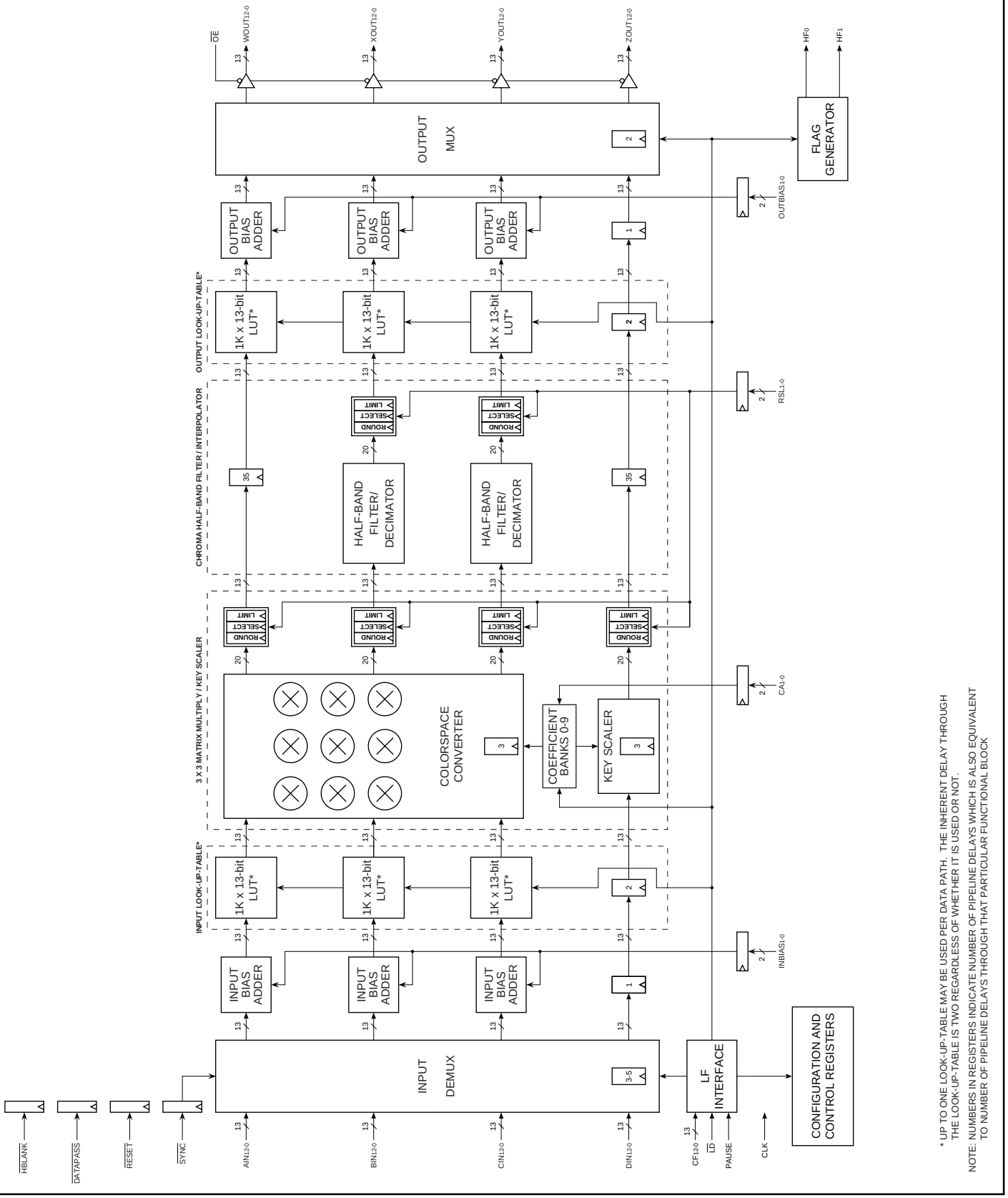


FIGURE 2. LF3370 FUNCTIONAL BLOCK DIAGRAM (COLORSPACE TO HALF-BAND FILTER ARRANGEMENT)



SIGNAL DEFINITIONS

Power

VCC and GND

+3.3 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all enabled registers. To guarantee data integrity, a minimum of 10KHz must be maintained.

Inputs

A12-0, B12-0, C12-0, D12-0 — Data Inputs

A12-0, B12-0, C12-0, and D12-0 are the 13-bit registered data input ports. Data is latched on the rising edge of CLK.

CF12-0 — Coefficient Input

CF12-0 is used to address and load Colorspace / Key Scaler coefficient banks, Round / Select / Limit registers, and Configuration registers. Data present on $\overline{\text{CF}}$12-0 is latched into the LF Interface™ on the rising edge of CLK when LD is LOW.

CA1-0 — Coefficient Address

CA1-0 determines which of the four user-programmable Colorspace / Key Scaler Coefficients are used.

Outputs

W12-0 , X12-0 , Y12-0 , Z12-0 — Data Outputs

W12-0, X12-0, Y12-0, and Z12-0 are the 13-bit registered data output ports. The data present on the output ports will correspond to the appropiate input data, based on the user-progammable configuration.

Controls

$\overline{\text{LD}}$ — Coefficient Load

When $\overline{\text{LD}}$ is LOW, data on CF12-0 is latched into the LF3370 LF Interface™ on the rising edge of CLK. When $\overline{\text{LD}}$ is HIGH, data is not loaded into the LF Interface™. When enabling the LF Interface™ for data input, a HIGH to LOW transition of $\overline{\text{LD}}$ is required in order for the input circuitry to function properly. Therefore, $\overline{\text{LD}}$ must be set HIGH immediately after power up to ensure proper operation of the input circuitry.

$\overline{\text{SYNC}}$ — Synchronization for data alignment

$\overline{\text{SYNC}}$ control signal is required to properly synchronize the input demultiplexer, output multiplexer, and halfband filters to the data flowing through the LF3370. A HIGH to LOW transition tells the core which sample corresponds to a Cb / Cr sample for proper de-multiplexing and multiplexing. This signal will also synchronize the half-band filters into a decimation / interpolation sequence.

$\overline{\text{DATAPASS}}$ — Datapass Mode

$\overline{\text{DATAPASS}}$ is used to place the LF3370 in a mode of operation that allows the user to pass data through the core (Input / Output Bias Adders, LUTs, Hafband Interpolator / Decimator, Colorspace / Key Scaler) without any processing.

$\overline{\text{HBLANK}}$ — Horizontal Blanking Control

$\overline{\text{HBLANK}}$ is used for data replacement corresponding to user-selectable blanking levels. A HIGH to LOW transition resets the counter and the HFx flags.

HF1/HF0 — HBlank Flags

HF1 and HF0 are two general purpose flags used to indicate when a 20-bit counter reaches its user-defined terminal count; a HIGH to LOW transition of $\overline{\text{HBLANK}}$ and / or $\overline{\text{RESET}}$ will reset the flags.

INBIAS1-0 — Input Bias Control

INBIAS1-0 determines which of the four user-programmable Input Bias registers are used to sum with the input data.

OUTBIAS1-0 — Output Bias Control

OUTBIAS1-0 determines which of the four user-programmable Output Bias registers are used to sum with the output data.

RSL1-0 — Round/Select/Limit Control

RSL1-0 determines which of the user-programmable Round / Select / Limit registers (RSL registers) are used in the RSL circuitry. A value of 00 on RSL1-0 selects RSL register 0. A value of 01 selects RSL register 1 and so on. RSL1-0 is latched on the rising edge of CLK.

$\overline{\text{OE}}$ — Output Enable

When $\overline{\text{OE}}$ is LOW, W12-0, X12-0, Y12-0, and Z12-0 are enabled for output. When $\overline{\text{OE}}$ is HIGH, W12-0, X12-0, Y12-0, and Z12-0 are placed in a high-impedance state.

PAUSE — LF Interface™ Pause

When PAUSE is HIGH, the LF3370 LF Interface™ loading sequence is halted until PAUSE is returned to a LOW state. This effectively allows the user to load coefficients and control registers at a slower rate than the master clock.

$\overline{\text{RESET}}$ — Reset

$\overline{\text{RESET}}$ is used to reset all programmable flags and line up clock edges during single muxed input or single muxed output events. $\overline{\text{RESET}}$ is used at power up or just after device configuration.

LF3370 Device Initialization

This section explains how to initialize the device for proper operation. It also serves as a summary of all conditions that should be considered before using the device or for troubleshooting.

Configuration Register 0 and Configuration Register 1 must be loaded before operation of the device. If Core Bypassing is desired, Configuration Register 2 must be loaded before use. If use of the Half-Band Filters is desired, at least one Half-Band Filter RSL Register Set must be loaded and selected for each Half-Band Filter.

If use of the Matrix Multiplier / Key Scaler is desired, at least one Matrix Multiplier / Key Scaler RSL Register Set and coefficient must be loaded and selected for each channel. If use of the Input Bias Adder is desired, at least one Input Bias Adder Register must be loaded and selected before use. If use of the Output Bias Adder is desired, at least one Output Bias Adder Register must be loaded and selected before use. If use of the Look-Up Table is desired, the Look-Up Table must be loaded before use.

When using a single channel input or output with interleaved video, SYNC and RESET should be used for proper initialization as shown in Figure 4. If 12 bits or less input data is desired, the input data should be shifted so the MSBs are aligned.

Input Demultiplexer

The input demultiplexer section acts as a buffer between the user's datapath and the LF3370's core. Data may be presented on input ports $A_{12\text{-}0}$, $B_{12\text{-}0}$, and $C_{12\text{-}0}$ as three channels of non-interleaved input data, one channel non-interleaved and one channel interleaved input data, or one channel of interleaved data (see Table 1 for various video input schemes). $D_{12\text{-}0}$ is the Key channel input port; the Key channel simply gets passed through the input demultiplexer with a latency that matches the other three channels.

TABLE 1. INPUT/OUTPUT FORMATS

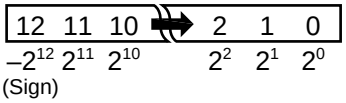
Input Channel	Input Format			
	4:4:4:4*	4:2:2:4*	4:2:2:4	4:2:2:4
$A_{12\text{-}0}$	R	Y	Y	Y/Cr/Cb
$B_{12\text{-}0}$	G	Cr	Cr/Cb	N/A
$C_{12\text{-}0}$	B	Cb	N/A	N/A
$D_{12\text{-}0}$	Key	Key	Key	Key
Output Channel	**Output Format**			
	4:4:4:4*	4:2:2:4*	4:2:2:4	4:2:2:4
$W_{12\text{-}0}$	R	Y	Y	Y/Cr/Cb
$X_{12\text{-}0}$	G	Cr	Cr/Cb	N/A
$Y_{12\text{-}0}$	B	Cb	N/A	N/A
$Z_{12\text{-}0}$	Key	Key	Key	Key

* Not all input/output combinations are valid. If single channel interleaved video is used on either the input or output, the core clock will be running at CLK/2. Thus the maximum input, output, and core data rate must be considered.

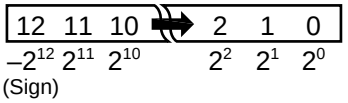
FIGURE 3. INPUT AND OUTPUT FORMATS

INPUT BIAS ADDER/OUTPUT BIAS ADDER

Input Data

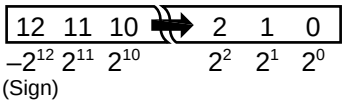


Output Data

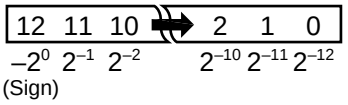


MATRIX MULTIPLIER/KEY SCALER

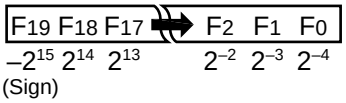
Input Data



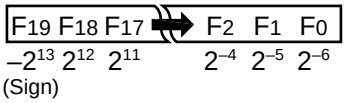
Coefficient Data



***Matrix Multiplier Output**



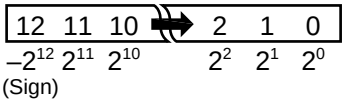
***Key Scaler Output**



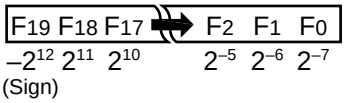
*Format of Matrix Multiplier/Key Scaler ouput feeding the RSL Circuitry. F_{19}-F_0 corresponds to 20 MSBs of which a 13-bit window can be selected from F_{19}-F_4 .

HALF-BAND FILTER

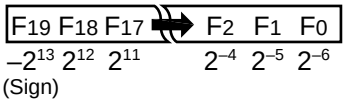
Input Data



****Filter Output (Non-Interpolate)**



****Filter Output (Interpolate)**



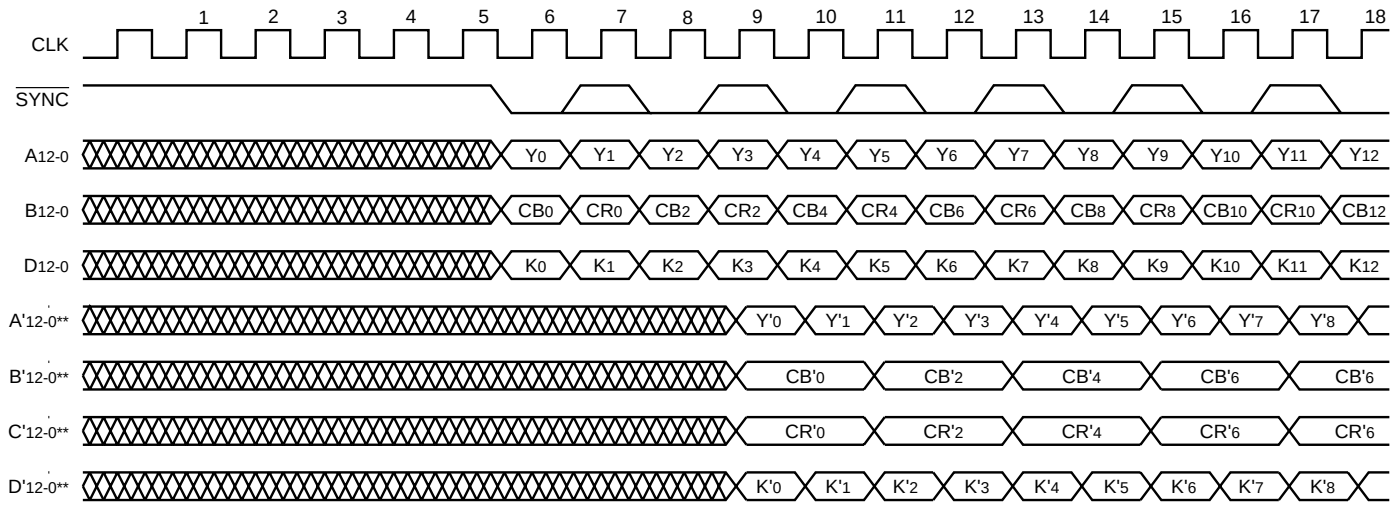
*Format of Half-Band Filter ouput feeding the RSL Circuitry. F_{19}-F_0 corresponds to 20 MSBs of which a 13-bit window can be selected from F_{19}-F_4 (see Table 3).

If video data is non-interleaved and presented to input ports A12-0, B12-0, and C12-0, no demultiplexing is performed. The three channels are passed unmodified into the LF3370 core with a delay of 3 CLK cycles. For this operation, bits 0 and 1 must both be set to 1 in Configuration Register 0 (see Table 5).

If video data is on two channels (see Figure 4), one channel of non-interleaved video and one channel of interleaved video, it is assumed that non-interleaved video is presented to input port A12-0 (i.e., Luma) and interleaved video is presented to input port B12-0 (i.e., Chroma). The input demultiplexer, in this case, separates video data on B12-0 and outputs two channels of separated video into the LF3370 core with a delay of 4 CLK cycles. For this operation, bit 0 must be set to 0 and bit 1 must be set to 1 in Configuration Register 0 (see Table 5).

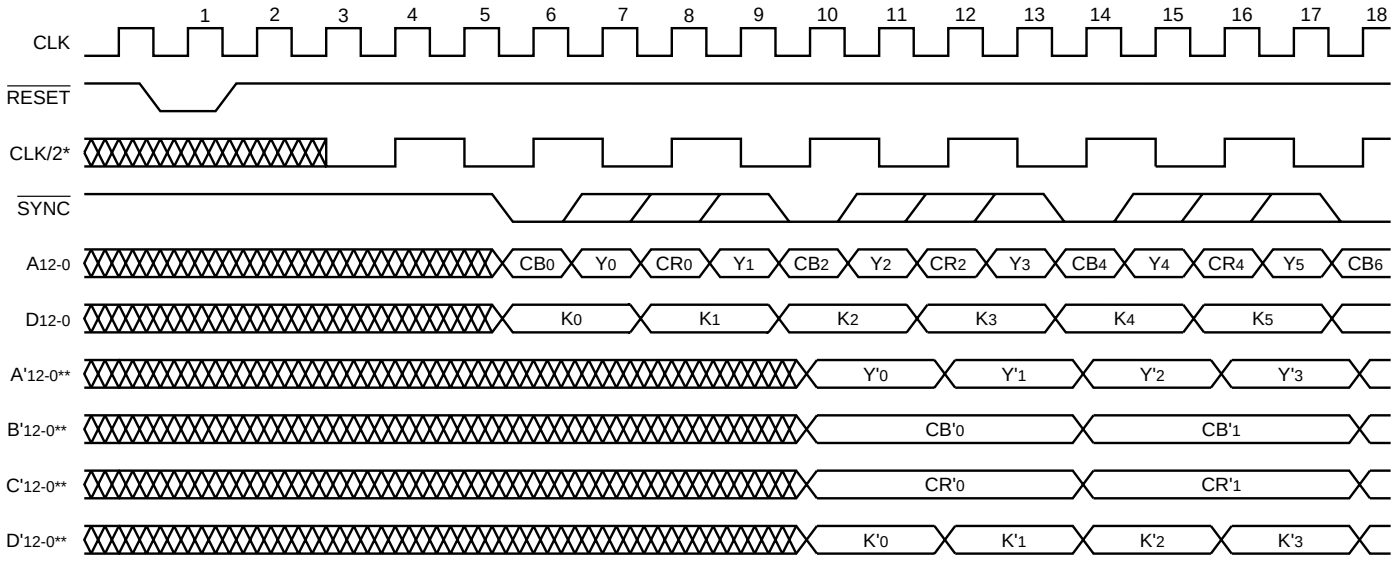
If 4:2:2 video data is on one channel interleaved (see Figure 5), it is assumed that interleaved video is presented to input

FIGURE 4. INPUT PROCESSING 4:2:2:4 (INTERLEAVED CHROMA ON CHANNEL B)



* Demultiplexed Input Data (Output of Demux Section)

FIGURE 5. INPUT PROCESSING 4:2:2:4 (INTERLEAVED LUMA/CHROMA ON CHANNEL A)



* Core Clock (Internally Generated and Synchronized to CLK by $\overline{\text{RESET}}$) Used Only When Single Channel Interleaved Input or Output Video is Used.
** Demultiplexed Input Data (Output of Demux Section)

port A12-0. The input demultiplexer, in this case, separates video data on A12-0 and outputs three channels of separated video into the LF3370 core with a delay of 5 CLK cycles. In this case, the core will run at half of the CLK rate and valid data will be output at at half of the CLK rate. For this operation, bit 0 must be set to 1 and bit 1 must be set to 0 in Configuration Register 0 (see Table 5).

All input demultiplexing operations are controlled by the HIGH to LOW transitions of $\overline{\text{SYNC}}$ which synchronizes the LF3370 core to the multiplexed input data (see $\overline{\text{SYNC}}$ discussion). It is important that unused input ports be set either HIGH or LOW.

Output Multiplexer

The output multiplexer section can be configured in various ways to accommodate the video system. Bits 2 and 3 of Configuration Register 0 determines the number of output channels that the LF3370 will drive. Z12-0 is the Key channel output port; the Key channel simply gets passed through the output multiplexer with a latency that matches the other three channels.

If three separate output channels of non-interleaved video are desired, no multiplexing is performed. The three channels are passed through the output multiplexer unmodified on the output ports W12-0, X12-0, and Y12-0 with a delay of 2 CLK cycles. For this operation, bits 2 and 3 must both be set to 1 in Configuration Register 0 (see Table 5).

If one channel of non-interleaved video (i.e., Luma) and one channel of interleaved video (i.e., Chroma) is desired (see Figure 6), non-interleaved video will be driven to the output port W12-0 and interleaved video will be driven to the output port X12-0 with a delay of 2 CLK cycles. For this operation, bit 2 must be set to 0 and bit 3 must be set to 1 in Configuration Register 0 (see Table 5).

If three channels of interleaved 4:2:2 video is desired (see Figure 7), interleaved video will be driven to the output port W12-0 with a delay of 4 CLK cycles. For this operation, bit 2 must be set to 1 and bit 3 must be set to 0 in Configuration Register 0 (see Table 5).

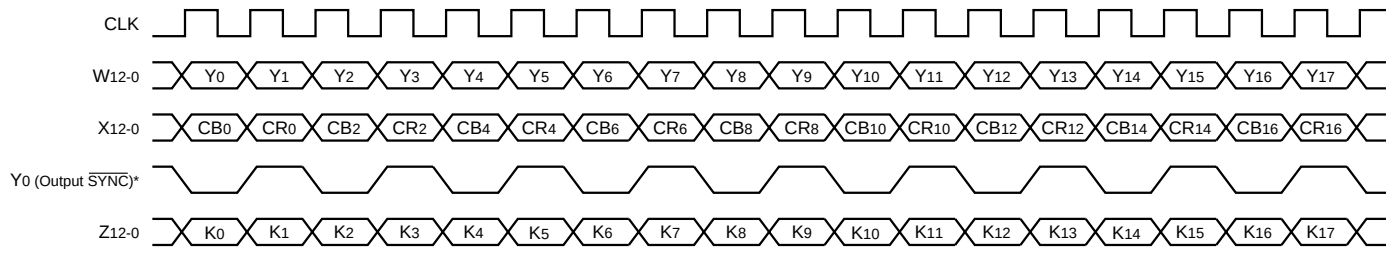
All output multiplexing operations are controlled by the HIGH to LOW transitions of $\overline{\text{SYNC}}$ which synchronizes the multiplexed output data to the LF3370 core (see $\overline{\text{SYNC}}$ discussion).

$\overline{\text{SYNC}}$

$\overline{\text{SYNC}}$ control signal is required to properly synchronize the input demultiplexer, output multiplexer, and halfband filters to the data flowing through the LF3370. A HIGH to LOW transition on $\overline{\text{SYNC}}$ control signal is needed to initialize the device to mark the beginning of valid data.

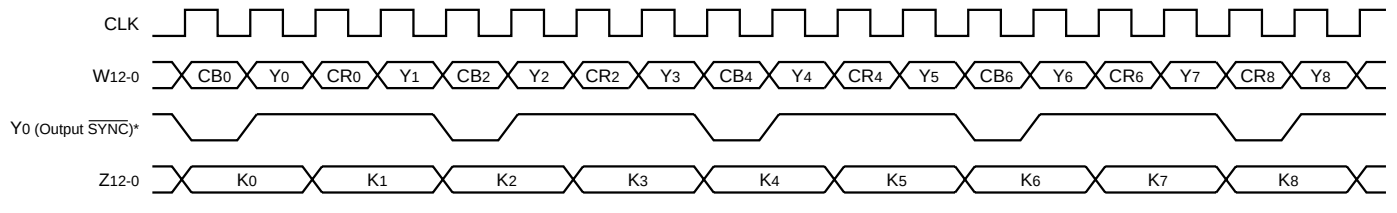
In addition, if 4:2:2 interleaved video data is desired for input or output, a HIGH to LOW transition on $\overline{\text{SYNC}}$ must be registered by a simultaneous rising edge of CLK and CLK/2. CLK/2 is an internal clock that must be synchronized to CLK

FIGURE 6. OUTPUTTING 4:2:2:4 (INTERLEAVED CHROMA ON CHANNEL X)



* There will be a HIGH to LOW transition on every Cb sample

FIGURE 7. OUTPUTTING 4:2:2:4 (INTERLEAVED LUMA/CHROMA ON CHANNEL W)



* There will be a HIGH to LOW transition on every Cb sample

by use of $\overline{\text{RESET}}$ only if the core is running at half the rate of CLK (see $\overline{\text{RESET}}$ discussion).

Furthermore, $\overline{\text{SYNC}}$ is used to identify one interleaved data set from another. For example, in the case of interleaved Chroma, Cb and Cr samples must be properly demultiplexed and synchronized for proper processing.

To differentiate a Cb sample from Cr, there needs to be a HIGH to LOW transition on $\overline{\text{SYNC}}$ on the first Cb sample (see Figure 4 and Figure 5); $\overline{\text{SYNC}}$ can also be toggled on every Cb sample for re-synchronization.

In the case that Cb is the first valid data word, $\overline{\text{SYNC}}$ may be used only once in device initialization and kept low until re-synchronization is desired. Therefore, when there is a HIGH to LOW transition on $\overline{\text{SYNC}}$, the following is assumed: Cb will occur on the next rising clock edge, Cb will occur every two clock cycles if interleaved Chroma is presented to the input port $B_{12\text{-}0}$, Cb will occur every 4 clock cycles if single channel 4:2:2 interleaved video is presented to the input port $A_{12\text{-}0}$.

$\overline{\text{SYNC}}$ control signal is also used to synchronize the interpolation / decimation output data from the Half-Band Filter to the Output Multiplexer.

$\overline{\text{RESET}}$

$\overline{\text{RESET}}$ should be used when initializing the device for proper operation. It is used to synchronize the LF3370 core clock to the master clock. In the case that single channel 4:2:2 interleaved video data is desired either on the input or output, thus using only one input or one output port (not including Key data), the internal clock rate will be half (CLK / 2) of the master clock rate (CLK). In this case, $\overline{\text{RESET}}$ is needed to synchronize the rising edge of CLK / 2 to a known rising edge of CLK (see Figure 4). For example, after configuring the LF3370 and before streaming valid data through the part, a $\overline{\text{RESET}}$ event should be used to align the clock edges (see Figure 5).

Furthermore, $\overline{\text{RESET}}$ will clear HF_0 and HF_1. A LOW state detected on $\overline{\text{RESET}}$ on a rising edge of clock will clear flags HF_0 and HF_1 on the following rising edge of clock. Please note $\overline{\text{HBLANK}}$ should be used to clear HF_0 and HF_1 during normal operation (see $\overline{\text{HBLANK}}$ discussion).

FIGURE 8. INPUT BIAS

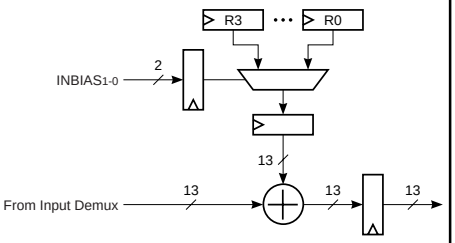
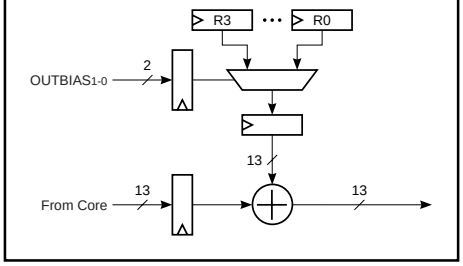


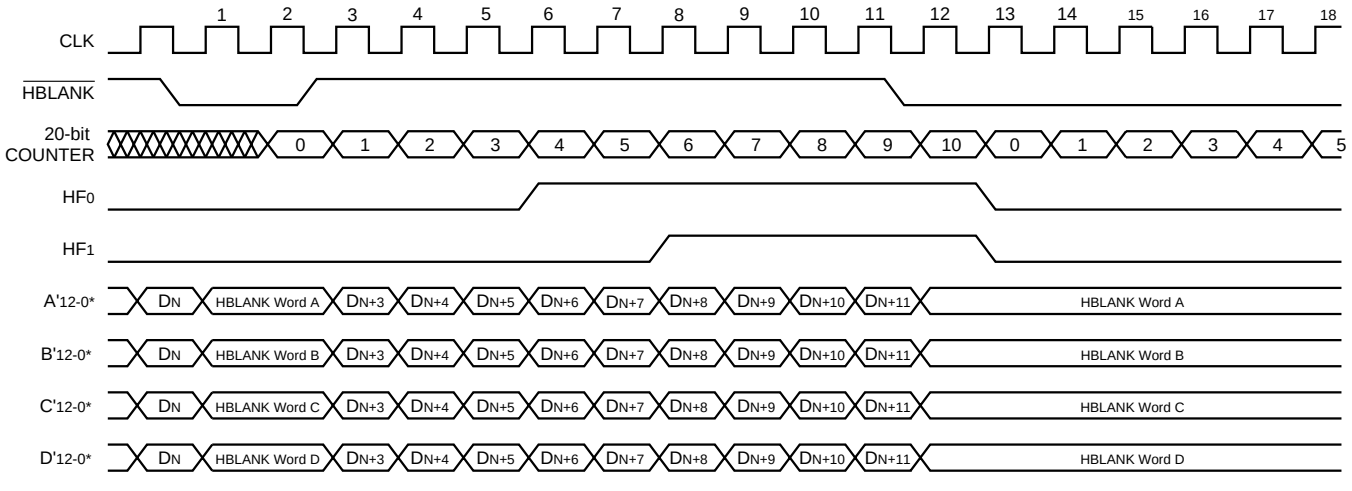
FIGURE 9. OUTPUT BIAS



$\overline{\text{HBLANK}}$

$\overline{\text{HBLANK}}$ is used to replace portions of the input data with user-defined blanking levels. When $\overline{\text{HBLANK}}$ is LOW, blanking level words are injected into the data stream immediately after the Input LUT section regardless of this section being used or not and immediately before the Matrix Multiplier or Half-Band Filter section. During the duration $\overline{\text{HBLANK}}$ is

FIGURE 10. HBLANK AND COUNTER



* Data values at output of Input LUT section
In this example, HF_0 Count Value is set to 3 and HF_1 Count Value is set to 5

LOW, blanking level words are continually injected with user-defined blanking words. Blanking words are injected on the next rising clock edge when $\overline{\text{HBLANK}}$ is LOW. In addition, $\overline{\text{HBLANK}}$ clears flags HF0 and HF1 and resets a 20-bit incrementing counter (0 - 1,048,575). If a HIGH to LOW transition on $\overline{\text{HBLANK}}$ is detected on a rising edge of clock, HF0 and HF1 are cleared and the counter is reset on the following rising edge of clock (see Figure 10). Key Channel blanking may be independently enabled or disabled using Congifuration Register 1 (see Table 6).

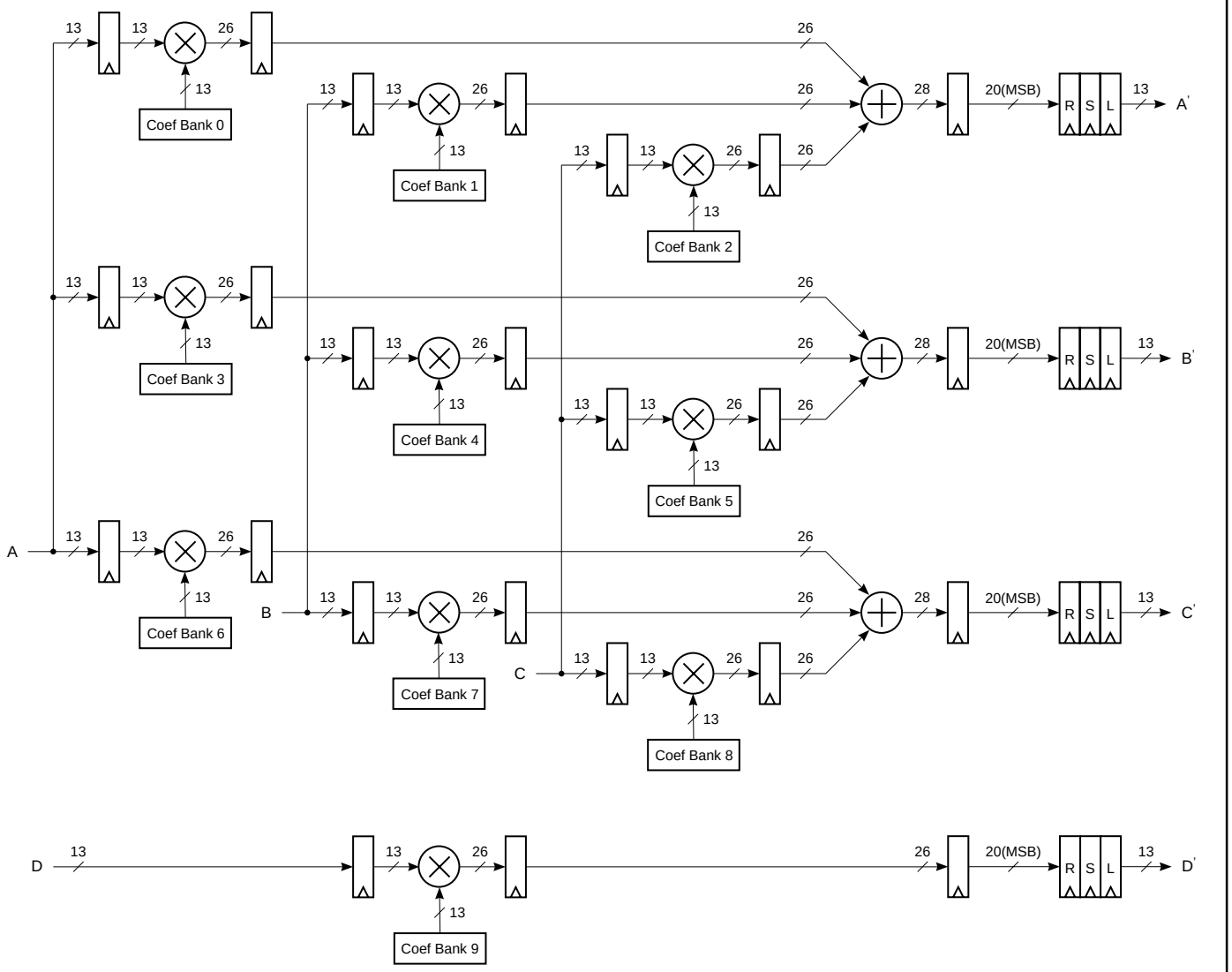
HF0/HF1 and Counter

HF0 and HF1 are two independent flags that are set when the pre-programmed HF0 or HF1 count value is equal to the 20-bit incrementing counter value. For each flag, one user-defined 20-bit count value can be programmed. When HF0 or HF1 count value is equal to the counter value, HF0 or HF1 is set on the next rising edge of clock. Once the flags are set, they must be reset if they are needed again. The counter will increment by one at the rate of CLK and can be reset by $\overline{\text{HBLANK}}$. The counter will continue to loop if not reset. HF0 and HF1 count value register loading is discussed in the LF Interface™. Please note, using $\overline{\text{HBLANK}}$ is the recommended way of clearing HF0 and HF1 flags but they can be cleared by $\overline{\text{RESET}}$, normally performed during device initialization. $\overline{\text{RESET}}$ will not reset the counter.

Input/Output Bias Adder

The programmable Input / Output Bias Adders can be used to subtract or add a 13-bit offset to the data. Input and output data formats for the two sections are

FIGURE 11. MATRIX MULTIPLIER AND KEY SCALER



shown in Figure 3. By using INBIAS1-0, the user may select one of four programmed Input Bias Adder values (see Figure 8). By using OUTBIAS1-0, the user may select one of four programmed Output Bias Adder values (see Figure 9). A value of 00 on INBIAS1-0 / OUTBIAS1-0 selects Input / Output Bias Adder Register 0. A value of 01 selects Input / Output Bias Adder Register 1 and so on. INBIAS1-0 / OUTBIAS1-0 may be changed every clock cycle if desired. If a bias is not desired, then bits 11 & 12 of Configuration Register 1 can be set up to independently disable the input and output bias values. Thus, effectively zeroing the function. The total pipeline latency from the input to the output for each of the two sections is one CLK cycle. Input / Output Bias Adder Register loading is discussed in the LF Interface™ section.

3 x 3 Matrix Multiplier

Processing almost 550 million colors, three simultaneous 13-bit input and output channels are utilized to implement a 3 x 3-matrix multiplication (triple dot product). Each truncated 20-bit output is the sum of all three input words multiplied by the appropriate coefficients (see Figure 11). These outputs are then fed into the RSL circuitry (see Figure 13). Input / Output formats are shown in Figure 3.

For each of the nine multipliers, up to four user-defined 13-bit coefficients can be programmed and selected by CA1-0. A value of 00 on CA1-0 selects Coefficient Set 0 on each of the 9 coefficient banks. A value of 01 selects Coefficient Set 1 and so on. CA1-0 may be changed every clock cycle if desired. Coefficient bank loading is discussed in the LF Interface™.

The total pipeline latency from the input of the Matrix Multiplier to the output of the RSL Circuitry is 6 CLK cycles and new output data is subsequently available every clock cycle thereafter.

If matrix multiplication is not desired, using the appropriate combination of coefficient values while keeping in mind bit weighting, an identity matrix may be set up to bypass the Matrix Multiplier section (see also First Operation Select in the Bypass Options duscussion).

Key Scaler

The Key channel is equiped with a 13 x 13-bit Key Scaler (see Figure 11) producing a truncated 20-bit output which is then fed into the RSL circuitry (see Figure 13). Up to four user-defined 13-bit coefficients can be programmed and selected by CA1-0. Input / Output formats are shown in Figure 3.

The total pipeline latency from the input of the Key Scaler to the output of the RSL Circuitry is 6 CLK cycles and new output data is subsequently available every clock cycle thereafter. If scaling is not desired, load and select a Key Scaler Coefficient value of 1 (see also First Operation Select in the Bypass Options duscussion).

Half-Band Filter

There are two internal Half-Band filters in the LF3370. These Half-Band filters can either interpolate, decimate, or pass through data found on channel B and channel C. Data on channel A and channel D in this section pass through a programmable 127 x 13-bit delay (see Bypass Section). The filter section (as show in Figure 12) is a fixed-coefficient, linear-phase half-band (low-pass) interpolating / decimating digital filter. The filter in this section is a 55-tap transversal FIR with 13-bit coefficients as shown in Table 3. The frequency response (Figure 14) is in full compliance with SMPTE 260M. This section can be configured for 2:1 interpolation, 1:2 decimation, or pass-through mode by setting bits 5-8 in Configuration Register 0 (see Table 5). This section can also be placed before or after the matrix multiplier by setting bit 4 in Configuration Register 0 (see Table 5). The maximum input and output clock rate this section can operate at is the CLK rate. The total internal pipeline latency from the input to the output of this section (including RSL circuitry) as shown in Figure 12 is 6 cycles.

To perform interpolation, the input data rate of this section will be half of CLK rate. Please note the maximum output data rate is the CLK rate. To perform decimation, the output data rate of this section will be half of the input data rate. One output sample is obtained for every two input samples.

FIGURE 12. 1:2 INTERPOLATION / 2:1 DECIMATION HALF-BAND FILTERS

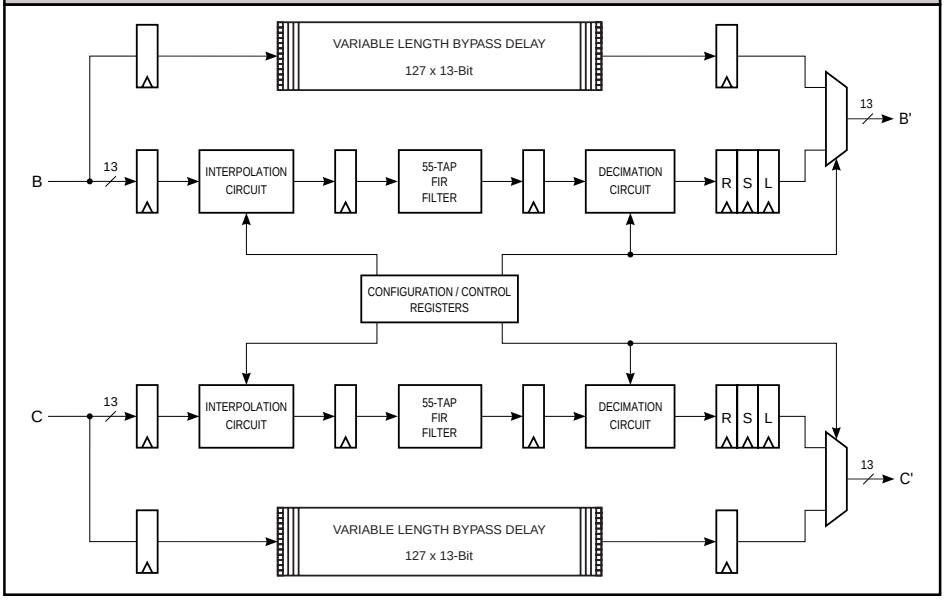


FIGURE 13. RSL CIRCUITRY

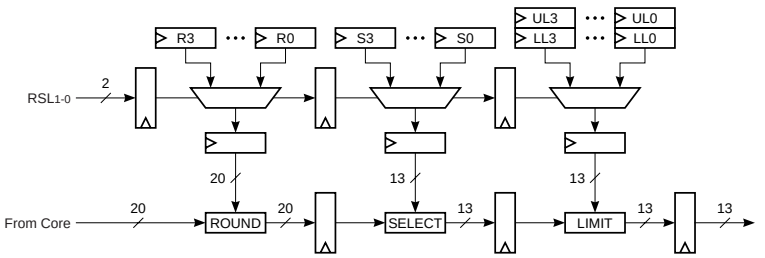


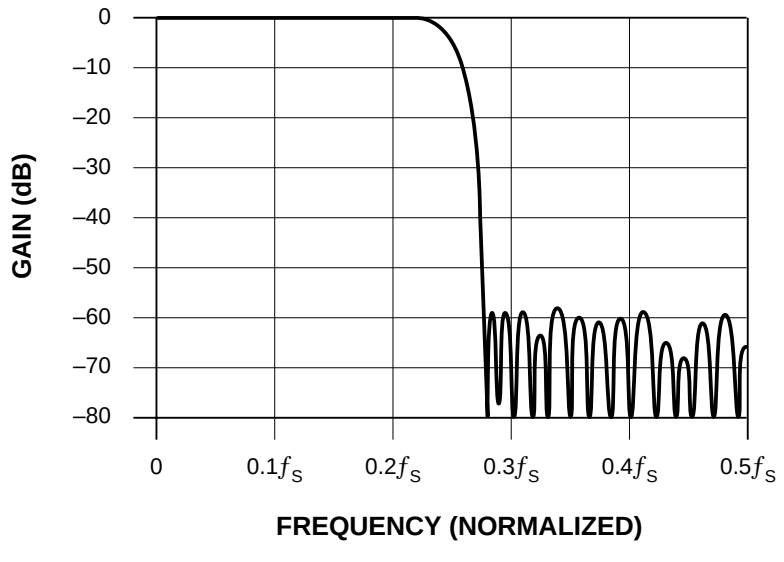
TABLE 2. SELECT FORMATS

SLCT1-0	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
00	F16	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4
01	F17	F16	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5
10	F18	F17	F16	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6
11	F19	F18	F17	F16	F15	F14	F13	F12	F11	F10	F9	F8	F7

Once an impulse is clocked into the Half-Band Filter section, the 55-value output response begins after 8 clock cycles and ends after 62 clock cycles. The pipeline latency from the input of an impulse to its corresponding output peak is 35 clock cycles.

The input / output formats are always in two's complement format as shown in Figure 3. In Interpolate Mode, the gain of the Half-Band Filter is halved (due to half of the input samples being padded with zeros). A right shifted Select window is required to maintain an overall filter gain of 1. It is possible that ringing on the filter's output could cause the high order bit (bit F18 in Figure 3 - Interpolate Filter Output Bit Weighting) to become HIGH. If a right shifted Select window is used, this F18 bit becomes the sign bit of the Selected window – and the output is erroneously considered negative. To ensure that no overflow conditions occur, an internal Limiter within each Half-Band Filter monitors its output. During Interpolate mode, this Limiter clamps the output word to 3FFFFH (20-bit maximum positive value ÷ 2) or C0000H (20-bit maximum negative value ÷ 2) if a positive or negative overflow occurs respectively. The internal 24-bits of the Half-Band Filter are truncated to 20-bits and then passed to the Round section of the RSL circuitry; see RSL section for further details. This section is fully bypassable by use of programmable delays (see Bypass Options section for further details).

FIGURE 14. FREQUENCY RESPONSE OF FILTER



Look-Up Table

Three optional programmable Input / Output 1K x 13-bit LUTs have been provided for Channels A, B, and C for various uses such as Gamma Correction. There are NOT actually two LUTs per channel as shown in Figures 1 and 2; only one LUT per channel can be selected for use at any given time. The latency through a LUT section is 2 cycles, regardless of whether the LUT is in use or not.

When using a LUT, the appropriate addressed value will be passed as an output of the LUT section. The Gamma LUT address can be chosen from any of the 4 possible10-bit words that are 'window' selected from the13-bit Input data bus. Configuring the desired LUT address selector position is accomplished by programming bits 10 & 9 of Configuration Register 1. Once the LUT Select Data position is programmed, it is meant to control all three Gamma LUTs. Therefore, the address selector positions of the three LUTs cannot be independently controlled. LUT loading is discussed in the LF Interface™ section.

Rounding

The rounding circuitry found in the Matrix Multiplier and Half-Band Filter sections work in the same manner. The truncated 20 MSBs from the Matrix Multiplier or Half-Band Filter output may be rounded by being added to the contents of one of the four Round Registers (see Figure 13). Each round register is 20 bits wide and user-programmable. This allows the Matrix Multiplier's or Half-Band Filter's output to be rounded to any precision required. RSL1-0 determines which of the four Round Registers are used in each Rounding Circuitry. A value of 00 on RSL1-0 selects Round Register 0. A value of 01 selects Round Register 1 and so on. RSL1-0 may be changed every clock cycle if desired. If rounding is not desired, the user must load and select a Round Register with value of 0. Round Register loading is discussed in the LF Interface™ section.

Selecting

The selecting circuitry found in the Matrix Multiplier and Half-Band Filter sections work in the same manner. The output word of the Matrix Multiplier and Half-Band Filter feeding the RSL circuitry is the 20 MSBs. However, only 13 bits may be sent to the next section. Therefore, the Select Register determines which 13-bits are passed. There are four select registers; RSL1-0 determines which of the four Select Registers are used in each Select Circuitry (see Table 2). A value of 00 on RSL1-0 selects Select Register 0. A value of 01 selects Select Register 1 and so on. RSL1-0 may be changed every clock cycle if desired. This allows the 13-bit window to be changed every clock cycle. Select Register loading is discussed in the LF Interface™ section.

Limiting

The Limiting Circuitry found in the Matrix Multiplier and Half-Band Filter sections work in the same manner. The Limit Registers determine the valid range of output values for each of these two sections. There are four 13-bit Limit Registers for each section. RSL1-0 determines which of the four Limit Registers are used in each Limiting Circuitry (see Figure 13). A value of 00 on RSL1-0 selects Limit Register 0. A value of 01 selects Limit Register 1 and so on.

Each Limit Register contains an upper and lower limit value. If the value fed to the Limiting Circuitry is less than the lower limit, the lower limit value is passed as the Matrix Multiplier section's or Half-Band filter section's output. If the value fed to the Limiting Circuitry is greater than the upper limit, the upper limit value is passed as the Matrix Multiplier section's or Half-Band filter section's output.

RSL1-0 may be changed every clock cycle if desired thus allowing the limit range to be changed every clock cycle. When loading limit values into the device, the upper limit must be greater than the lower limit. The most negative and most positive values you can load into the Limit Registers are 0FFFH and 1000H. Limit Register loading is discussed in the LF Interface™ section.

LF Interface™

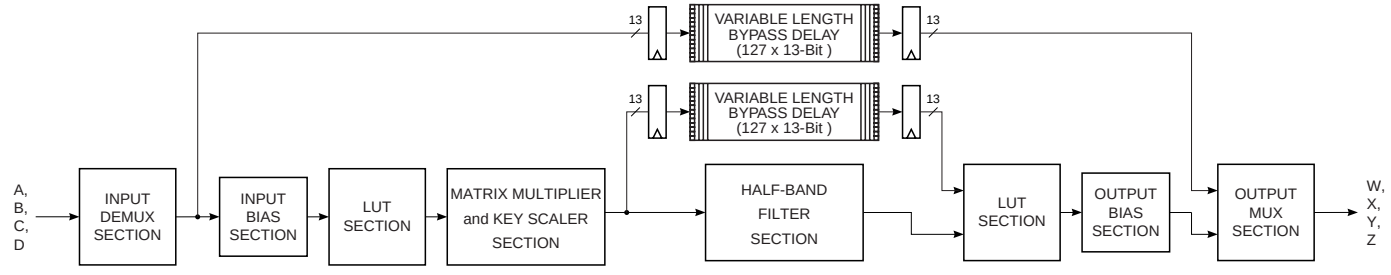
The LF Interface™ is used to load the Configuration Registers, Matrix Multiplier / Key Scaler Coefficient Banks, Look-Up Tables, Input / Output Bias registers, RSL registers, HF0 and HF1 Count Values, and Horizontal Blanking Levels.

LD is used to enable and disable the LF Interface™. When LD goes low, the LF Interface™ is enabled for data input. The first value fed into the interface on CF12-0 is an address which determines what the interface is going to load (see Table 4). For example, to load address Bias Adder Register 2 of the channel B Output Bias Adder, the first data value into the LF Interface™ should be 0A02H. To load RSL Register 1 for the Keyscaler RSL, the first data value should be 1101H. The first address value should be loaded into the interface on the same clock cycle

TABLE 3. HALF-BAND FILTER IMPULSE RESPONSE

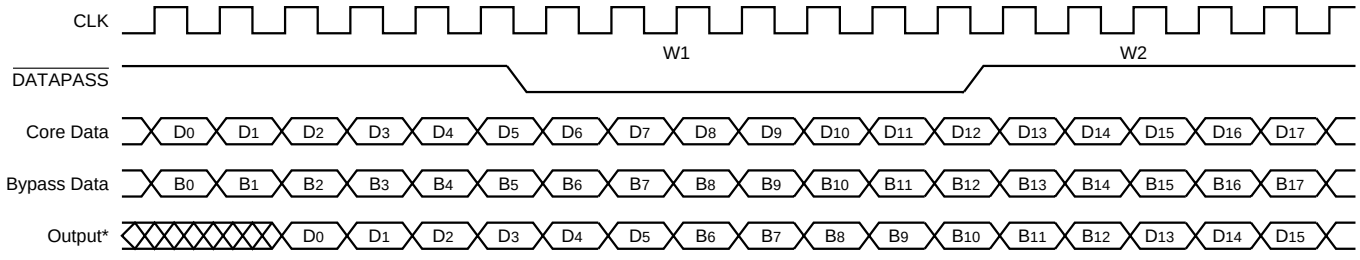
TAP	Impulse Response Out (Non-Interpolated Bit Weighing) 20-bit (MSB) Filter Out (HEX)	Decimal Equivalent
1, 55	FFE35	–0.0008755
2, 54	0	0
3, 53	002D2	0.0013771
4, 52	0	0
5, 51	FFB5C	–0.00226593
6, 50	0	0
7, 49	00725	0.0034885
8, 48	0	0
9, 47	FF508	–0.0053558
10, 46	0	0
11, 45	00F95	0.0076084
12, 44	0	0
13, 43	FEA10	–0.01071167
14, 42	0	0
15, 41	01E59	0.0148182
16, 40	0	0
17, 39	FD6A8	–0.02018738
18, 38	0	0
19, 37	0393E	0.0279503
20, 36	0	0
21, 35	FAF1B	–0.0394993
22, 34	0	0
23, 33	0798D	0.05935097
24, 32	0	0
25, 31	F2BD2	–0.10360334
26, 30	0	0
27, 29	28B30	0.3179626
28 (center)	401BC	0.500846862

FIGURE 15. BYPASS BLOCK DIAGRAM



In this example, the Matrix-Multipler/Key Scaler Section feeds the Half-Band Filter Section. This arrangement is reversible.

FIGURE 16. CORE BYPASS



* In this example, the Output Multiplexer is in a mode where the delay through the section is 2 CLK cycles. Only one channel is shown in this example, however, the other three channels behave in the same manner. The example assumes that the bypass RAM length is set to the length of the core data path.
W1: Bypass data is output to the output port and replaces core data.
W2: Core data is output to the output port and replaces bypass data.

TABLE 4. CONFIGURATION/CONTROL REGISTERS ADDRESSING SUMMARY

DESCRIPTION	ADDRESS RANGE (HEX)
Coefficient Registers	0000 - 0003
Configuration Registers	0200 - 020A
Look-Up Table - Channel 'A'	0300
Look-Up Table - Channel 'B'	0400
Look-Up Table - Channel 'C'	0500
Input Bias Registers - Channel 'A'	0600 - 0603
Input Bias Registers - Channel 'B'	0700 - 0703
Input Bias Registers - Channel 'C'	0800 - 0803
Output Bias Registers - Channel 'A'	0900 - 0903
Output Bias Registers - Channel 'B'	0A00 - 0A03
Output Bias Registers - Channel 'C'	0B00 - 0B03
HF0 Count Value	0C00
HF1 Count Value	0D00
Matrix Mult. RSL Registers - Channel 'A'	0E00 - 0E03
Matrix Mult. RSL Registers - Channel 'B'	0F00 - 0F03
Matrix Mult. RSL Registers - Channel 'C'	1000 - 1003
Key Scaler RSL Registers	1100 - 1103
Half-Band Filter RSL Registers - Channel 'B'	1200 - 1203
Half-Band Filter RSL Registers - Channel 'C'	1300 - 1303

that latches the HIGH to LOW transition of LD. The next value(s) loaded into the interface are the data value(s) which will be stored in the bank or register defined by the address value. When loading coefficient banks, the interface will expect ten values to be loaded into the device after the address value. The ten values are coefficients 0 through 8 and the Keyscale coefficient. When loading Configuration or Bias Registers, the interface will expect one value after the address value. When loading RSL registers, the interface will expect four values after the address value. When loading gamma look-up tables, the interface will expect 1024 values after the address value. When loading HBLANK flag counts, the interface will expect 2 values after the address value.

The coefficient banks, configuration registers, RSL registers, etc., are not loaded with data until all data values for the specified address are loaded into the LF Interface. In other words, the coefficient banks are not written until all ten coefficients have been loaded into the LF

Interface™. A RSL register is not written to until all four data words are loaded. After the last data value is loaded, the interface will expect a new address value on the next clock cycle. After the next address value is loaded, data loading will begin again as previously discussed.

PAUSE allows the user to effectively slow the rate of data loading through the LF Interface™. When PAUSE is HIGH, the LF Interface™is held until PAUSE is returned LOW. Figure 19 shows the effects of PAUSE while loading Matrix Multiplier / Key Scaler coefficients.

Table 28 shows an example of loading a bias value into the Input Bias Adder Register. In this example, a bias value of 007FH is loaded into the Channel 'C' Input Bias Adder Register 1 (0B01H).

Table 29 shows an example of loading a bias value into the Output Bias Adder Register. In this example, a bias value of 0010H is loaded into Channel 'A' Output Bias Adder Register 3 (0903H).

Table 30 shows an example of loading data into the Matrix Multiplier / Key Scaler Coefficient Banks. In this example, the following values are loaded into Coefficient Register Set 2 (0002H): 0000H, 0001H, 0002H, 0003H, 0004H, 0005H, 0006H, 0007H, 0008H, and 0009H.

Table 31 shows an example of loading the HF_0 Flag Count Value. In this example, a 20-bit HF_0 Flag Count Value of B3C27H is loaded into the HF_0 Flag Count Value Register (0C00H). The HF_1 Flag Count Value is loaded in the same manner using the appropriate address.

Table 32 shows an example of loading Round / Select / Limit values. In this example, Channel 'A' Matrix Multiplier Register Set 0 (0E00H) is loaded with a 20-bit Round value of 00020H, a 2-bit Select value of 10H, a 13-bit Upper Limit value of 0FFFH, and a 13-bit Lower Limit value of 1001H. Other RSL registers are loaded in the same manner using the appropriate address.

TABLE 5. CONFIGURATION REGISTER 0 – ADDRESS 200H

BITS	FUNCTION	DESCRIPTION
1-0	Video Input Format	00 : Reserved 01 : Single Channel Interleaved Video 10 : Dual Channel Interleaved Video 11 : 3 Channel Non-Interleaved Video
3-2	Video Output Format	00 : Reserved 01 : Single Channel Interleaved Video 10 : Dual Channel Interleaved Video 11 : 3 Channel Non-Interleaved Video
4	Functional Arrangement	0 : Filter Feeds Matrix Multiplier 1 : Matrix Multiplier Feeds Filter
6-5	Half-Band Filter Control Channel 'B'	00 : Pass Through Filter 01 : Interpolate 10 : Decimate 11 : Bypass Filter
8-7	Half-Band Filter Control Channel 'C'	00 : Pass Through Filter 01 : Interpolate 10 : Decimate 11 : Bypass Filter
9	First Operation Select	0 : Normal Order of Operations 1 : Select First Operation Only
12-10	Reserved	Must be Set to Zero

TABLE 6. CONFIGURATION REGISTER 1 – ADDRESS 201H

BITS	FUNCTION	DESCRIPTION
1-0	Look-Up Table Control Channel 'A'	00 : Disable Look-Up Table 01 : Enable Look-Up Table on Input 10 : Enable Look-Up Table on Output 11 : Reserved
3-2	Look-Up Table Control Channel 'B'	00 : Disable Look-Up Table 01 : Enable Look-Up Table on Input 10 : Enable Look-Up Table on Output 11 : Reserved
5-4	Look-Up Table Control Channel 'C'	00 : Disable Look-Up Table 01 : Enable Look-Up Table on Input 10 : Enable Look-Up Table on Output 11 : Reserved
6	HBLANK Control 'Key' Channel	0 : Disable Horizontal Blanking Option During HBLANK Period 1 : Enable Horizontal Blanking Option During HBLANK Period
8-7	Data Bypass Mode 'W' Output Channel Mux Control	00 : Output Channel 'A' to W_{12-0} 01 : Output Channel 'B' to W_{12-0} 10 : Output Channel 'C' to W_{12-0} 11 : Output Channel 'D' to W_{12-0}
10-9	Look-Up Table Input Address Selection Control	00 : Select Address Data [9:0] 01 : Select Address Data [10:1] 10 : Select Address Data [11:2] 11 : Select Address Data [12:3]
11	Input Bias Disable	0 : Enable Input Bias 1 : Disable Input Bias
12	Output Bias Disable	0 : Enable Output Bias 1 : Disable Output Bias

Table 33 shows an example of loading a Configuration Register. In this example, Configuration Register 0 (0200H) is loaded with 00AEH. This will setup the Input Section to handle Luma on input port A12-0 and interleaved Chroma on the input port B12-0. The Output Section is setup to output RGB on the output ports W12-0, X12-0, Y12-0. The 'functional arrangement' is setup in such a way that the Half-Band Filter section is placed before the Matrix Multiplier section. The Half-Band Filters are setup for 1:2 interpolation and 'normal order of operations' is selected.

BYPASS OPTIONS

Core Bypass

At all times during the normal operation of the LF3370, video data on channels A, B, C, and D are simultaneously being fed from the output of the Input Demultiplexer into the programmable Core Bypass Delay (see Figure 15). This allows users to switch between processed video and unprocessed (bypassed) data on-the-fly.

There is a separate Core Bypass Delay for each channel. Each Core Bypass Delay can be programmed for a length of 2 up to 129 CLK cycles for delay matching between the bypass path and the core as well as other operations. The Core Bypass Delay bypasses the Input Bias, Input LUT, Half-Band Filter, Matrix Multiplier / Key Scaler Section, and Output Bias and feeds the Output Multiplexer. Loading Configuration Register 2 programs the length of all four Core Bypass Delays (see Table 7).

A LOW state detected on $\overline{\text{DATAPASS}}$ on a rising edge of clock will output bypassed data to the output port on the following rising edge of CLK (see Figure X). In addition, any of the four bypassed channels can be passed to the 'W' output channel during a 'bypass' event. For this operation, use bits 7 and 8 of Configuration Register 1 (see Table 6).

TABLE 7. CONFIGURATION REGISTER 2 – ADDRESS 202H

BITS	FUNCTION	DESCRIPTION
6-0	Core Bypass Delay Length	Length of Core Bypass Delay Minus 2
12-7	Reserved	Must be Set to Zero

TABLE 8. CONFIGURATION REGISTER 3 – ADDRESS 203H

BITS	FUNCTION	DESCRIPTION
6-0	Channel 'A' Filter Section Bypass Delay Length	Length of Filter Bypass Delay Minus 2
12-7	Reserved	Must be Set to Zero

TABLE 9. CONFIGURATION REGISTER 4 – ADDRESS 204H

BITS	FUNCTION	DESCRIPTION
6-0	Channel 'B' Filter Section Bypass Delay Length	Length of Filter Bypass Delay Minus 2
12-7	Reserved	Must be Set to Zero

TABLE 10. CONFIGURATION REGISTER 5 – ADDRESS 205H

BITS	FUNCTION	DESCRIPTION
6-0	Channel 'C' Filter Section Bypass Delay Length	Length of Filter Bypass Delay Minus 2
12-7	Reserved	Must be Set to Zero

TABLE 11. CONFIGURATION REGISTER 6 – ADDRESS 206H

BITS	FUNCTION	DESCRIPTION
6-0	Key Channel Filter Section Bypass Delay Length	Length of Filter Bypass Delay Minus 2
12-7	Reserved	Must be Set to Zero

Half-Band Filter Bypass

At all times, while data is being fed into the Half-Band Filter section, channels A, B, C, and Key are fed into programmable length delays. When the Half-Band Filter(s) are set to filter bypass mode, that particular channel passes through a programmable delay and is not filtered. Since there are only two Half-Band Filters in this section found on channels B and C, channels A and Key are passed through their respective programmable delays.

Please note, when using a single channel video input or video output (interleaved 4:2:2), the Core Bypass Delay must be programmed to double the length [(desired length x 2) – 2)] to properly align data due to the core running at half the CLK rate.

First Operation Select

'First Operation Select' is a bypassing option where you select to use the first functional block (Half-Band Filter or Matrix Multiplier / Key Scaler) in any given arrangement. If the device was arranged in such a way that the Half-Band Filter section fed the Matrix Multiplier / Key Scaler section and 'First Operation Select' was enabled, the Half-Band Filter section will be used and the Matrix Multiplier / Key Scaler section will be bypassed.

If the device was arranged in such a way that the Matrix Multiplier / Key Scaler section fed the Half-Band Filter section and 'First Operation Select' was enabled, the Matrix Multiplier / Key Scaler section will be used and the Half-Band Filter section will be bypassed. Unlike in other bypassing options, when a section is bypassed, the total pipeline latency of the device is reduced by the appropriate delay. If the Half-Band Filter section was bypassed by this method, the overall pipeline latency should be reduced by 35 CLK cycles. If the Matrix Multiplier section was bypassed by this method, the overall pipeline latency should be reduced by 6 CLK cycles. This function is implemented by configuring bit 9 of Configuration Register 0. The 'Functional Arrangement' of the device is determined by configuring bit 4 of Configuration Register 0.

Table 12. Channel 'A' Input Bias Registers

REGISTER	ADDRESS (HEX)
0	0600
1	0601
2	0602
3	0603

Table 13. Channel 'B' Input Bias Registers

REGISTER	ADDRESS (HEX)
0	0700
1	0701
2	0702
3	0703

Table 14. Channel 'C' Input Bias Registers

REGISTER	ADDRESS (HEX)
0	0800
1	0801
2	0802
3	0803

Table 15. Channel 'A' Output Bias Registers

REGISTER	ADDRESS (HEX)
0	0900
1	0901
2	0902
3	0903

Table 16. Channel 'B' Output Bias Registers

REGISTER	ADDRESS (HEX)
0	0A00
1	0A01
2	0A02
3	0A03

Table 17. Channel 'C' Output Bias Registers

REGISTER	ADDRESS (HEX)
0	0B00
1	0B01
2	0B02
3	0B03

Table 18. Channel 'A' Matrix Mult. RSL Registers

REGISTER	ADDRESS (HEX)
0	0E00
1	0E01
2	0E02
3	0E03

Table 19. Channel 'B' Matrix Mult. RSL Registers

REGISTER	ADDRESS (HEX)
0	0F00
1	0F01
2	0F02
3	0F03

Table 20. Channel 'C' Matrix Mult. RSL Registers

REGISTER	ADDRESS (HEX)
0	1000
1	1001
2	1002
3	1003

Table 21. 'Key' Channel Matrix Mult. RSL Registers

REGISTER	ADDRESS (HEX)
0	1100
1	1101
2	1102
3	1103

Table 22. Channel 'B' Halfband Filter RSL Registers

REGISTER	ADDRESS (HEX)
0	1200
1	1201
2	1202
3	1203

Table 23. Channel 'C' Halfband Filter RSL Registers

REGISTER	ADDRESS (HEX)
0	1300
1	1301
2	1302
3	1303

Table 24. HFx Count Value Registers

COUNT	ADDRESS (HEX)
0	0C00
1	0D00

Table 25. Horizontal Blanking Level Address

CHANNEL	ADDRESS (HEX)
'A'	0207
'B'	0208
'C'	0209
'D'	020A

Table 26. Matrix Mult. & Scaler Coefficient Registers

REGISTER	ADDRESS (HEX)
0	0000
1	0001
2	0002
3	0003

Table 27. Look-Up Table Addressing

CHANNEL	ADDRESS (HEX)
'A'	0300
'B'	0400
'C'	0500

TABLE 28. INTPUT BIAS ADDER REGISTER LOADING FORMAT

	CF_{12}	CF_{11}	CF_{10}	CF_9	CF_8	CF_7	CF_6	CF_5	CF_4	CF_3	CF_2	CF_1	CF_0
Address	0	1	0	1	1	0	0	0	0	0	0	0	1
Word 0	0	0	0	0	0	0	1	1	1	1	1	1	1

TABLE 29. OUTPUT BIAS ADDER REGISTER LOADING FORMAT

	CF_{12}	CF_{11}	CF_{10}	CF_9	CF_8	CF_7	CF_6	CF_5	CF_4	CF_3	CF_2	CF_1	CF_0
Address	0	1	0	0	1	0	0	0	0	0	0	1	1
Word 0	0	0	0	0	0	0	0	0	1	0	0	0	0

TABLE 30. MATRIX MULTIPLIER/KEY SCALER COEFFICIENT BANK LOADING FORMAT

	CF_{12}	CF_{11}	CF_{10}	CF_9	CF_8	CF_7	CF_6	CF_5	CF_4	CF_3	CF_2	CF_1	CF_0
Address	0	0	0	0	0	0	0	0	0	0	0	1	0
Coef Bank 0	0	0	0	0	0	0	0	0	0	0	0	0	0
Coef Bank 1	0	0	0	0	0	0	0	0	0	0	0	0	1
Coef Bank 2	0	0	0	0	0	0	0	0	0	0	0	1	0
Coef Bank 3	0	0	0	0	0	0	0	0	0	0	0	1	1
Coef Bank 4	0	0	0	0	0	0	0	0	0	0	1	0	0
Coef Bank 5	0	0	0	0	0	0	0	0	0	0	1	0	1
Coef Bank 6	0	0	0	0	0	0	0	0	0	0	1	1	0
Coef Bank 7	0	0	0	0	0	0	0	0	0	0	1	1	1
Coef Bank 8	0	0	0	0	0	0	0	0	0	1	0	0	0
Coef Bank 9	0	0	0	0	0	0	0	0	0	1	0	0	1

TABLE 31. HFX COUNT VALUE LOADING FORMAT

	CF_{12}	CF_{11}	CF_{10}	CF_9	CF_8	CF_7	CF_6	CF_5	CF_4	CF_3	CF_2	CF_1	CF_0
Address	0	1	1	0	0	0	0	0	0	0	0	0	0
Word 0	R	1	1	0	0	0	0	1	0	0	1	1	HF_0
Word 1	R	R	R	R	R	HF_{19}	1	0	1	1	0	0	1	1

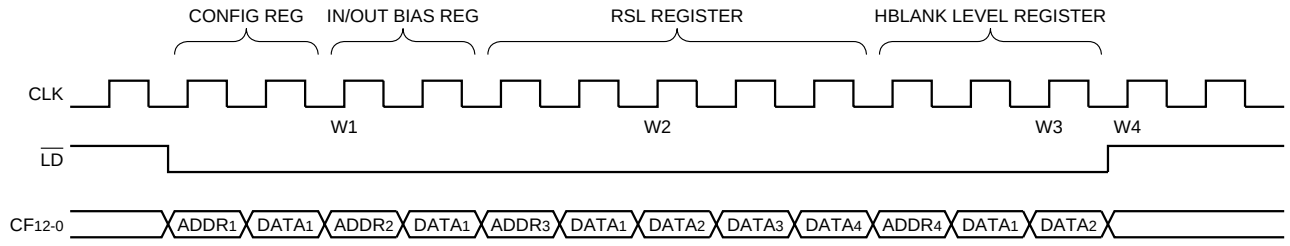
TABLE 32. RSL REGISTER LOADING FORMAT

	CF_{12}	CF_{11}	CF_{10}	CF_9	CF_8	CF_7	CF_6	CF_5	CF_4	CF_3	CF_2	CF_1	CF_0
Address	0	1	1	1	0	0	0	0	0	0	0	0	0
Word 0	R	0	0	0	0	0	0	1	0	0	0	0	R_0
Word 1	R	R	R	S_1	0	1	S_0	R_{19}	0	0	0	0	0	0
Word 2	UL_{12}	0	1	1	1	1	1	1	1	1	1	1	1	UL_0
Word 3	LL_{12}	1	0	0	0	0	0	0	0	0	0	0	1	LL_0

TABLE 33. CONFIGURATION REGISTER LOADING FORMAT

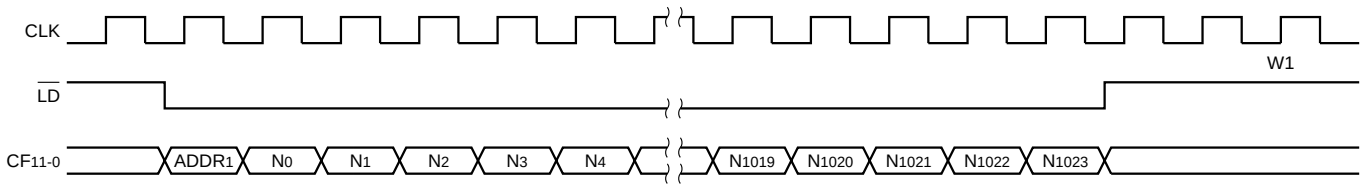
	CF_{12}	CF_{11}	CF_{10}	CF_9	CF_8	CF_7	CF_6	CF_5	CF_4	CF_3	CF_2	CF_1	CF_0
Address	0	0	0	1	0	0	0	0	0	0	0	0	0
Word 0	0	0	0	0	0	1	0	1	0	1	1	1	0

FIGURE 17. CONFIGURATION, INPUT/OUTPUT BIAS ADDER, RSL, AND HBLANK LEVEL REGISTER LOADING SEQUENCE



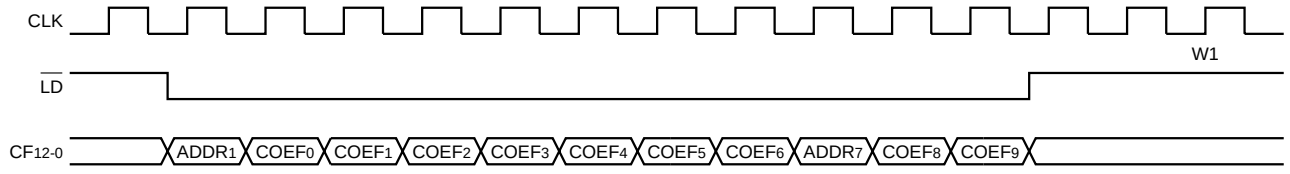
W1: Configuration Register updated and effective on this rising clock edge.
W2: Input or Output Bias Adder Register updated and effective on this rising clock edge.
W3: RSL Register Set updated and effective on this rising clock edge.
W4: Horizontal Blanking Level Register updated and effective on this rising clock edge.

FIGURE 18. LOOK-UP TABLE LOADING SEQUENCE



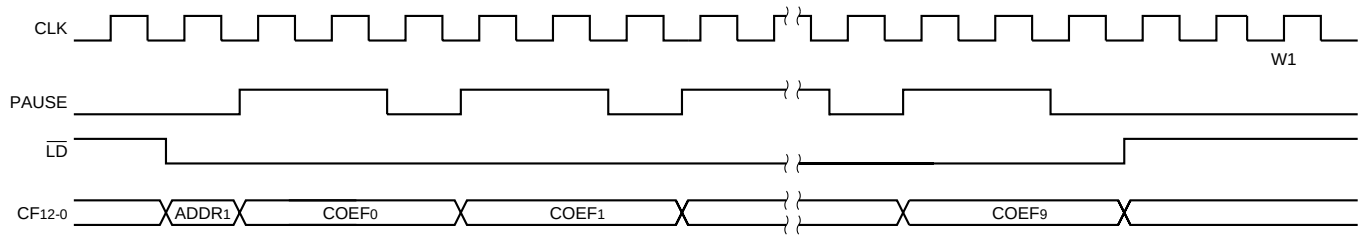
W1: LUT updated and effective on this rising clock edge.

FIGURE 19. MATRIX MULTIPLIER/KEY SCALER COEFFICIENT BANK LOADING SEQUENCE



W1: Matrix Multiplier/Key Scaler Coefficient Set updated and effective on this active rising clock edge.

FIGURE 20. MATRIX MULTIPLIER/KEY SCALER COEFFICIENT BANK LOADING SEQUENCE WITH PAUSE IMPLEMENTATION



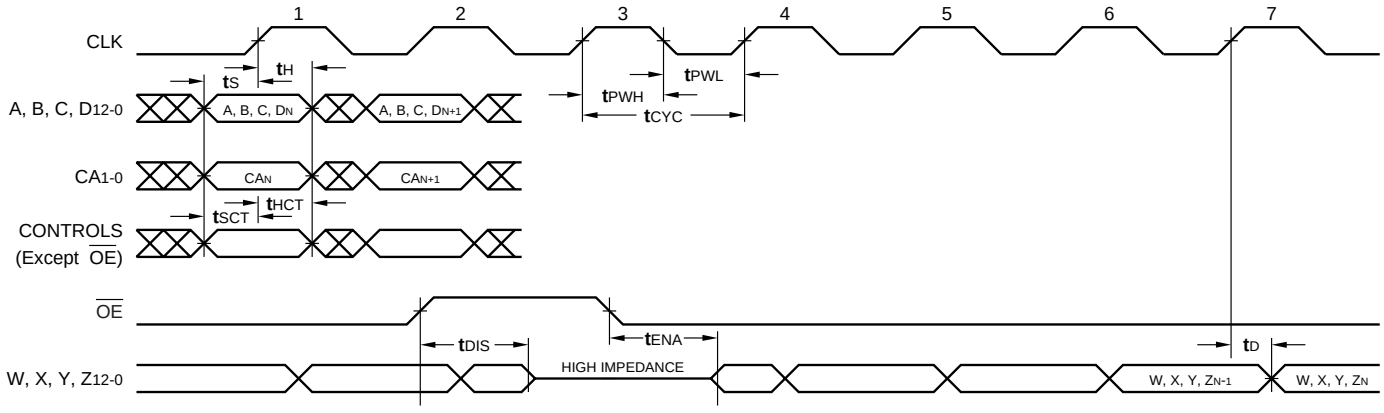
W1: Matrix Multiplier/Key Scaler Coefficient Set updated and effective on this active rising clock edge.

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LF3370–12 Min	LF3370–12 Max
t_{CYC}	Cycle Time	**12**	
t_{PWL}	Clock Pulse Width Low	5	
t_{PWH}	Clock Pulse Width High	5	
t_S	Input Setup Time	4	
t_H	Input Hold Time	0	
t_{SCT}	Setup Time Control Inputs	4	
t_{HCT}	Hold Time Control Inputs	0	
t_D	Output Delay		8
t_{DIS}	Three-State Output Disable Delay (Note 11)		10
t_{ENA}	Three-State Output Enable Delay (Note 11)		10

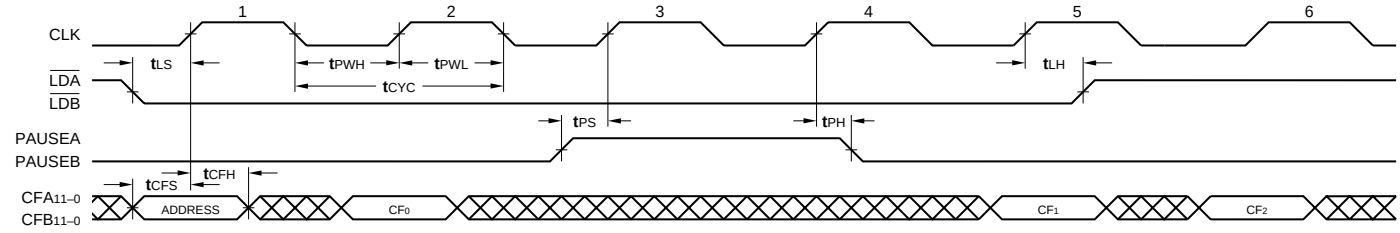
SWITCHING WAVEFORMS: DATA I/O



COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

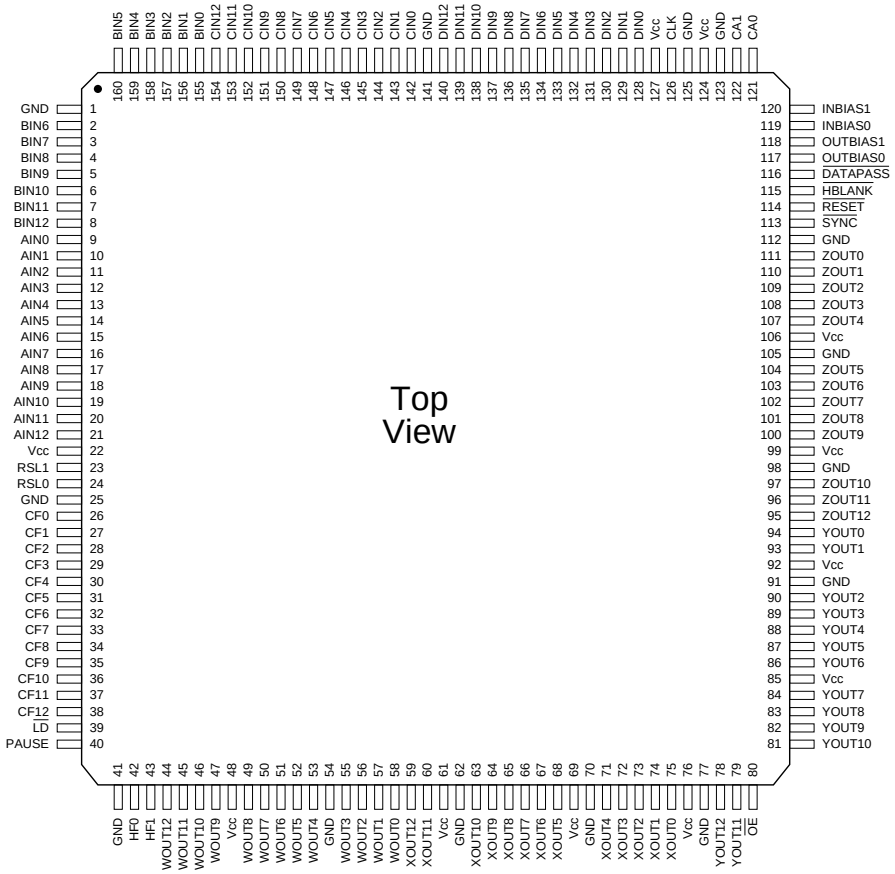
Symbol	Parameter	LF3370–12 Min	LF3370–12 Max
t_{CFS}	Configuration Input Setup	5.5	
t_{CFH}	Configuration Input Hold	0	
t_{LS}	Load Setup Time	4	
t_{LH}	Load Hold Time	0	
t_{PS}	PAUSE Setup Time	4	
t_{PH}	PAUSE Hold Time	0	

SWITCHING WAVEFORMS: LF INTERFACE™



ORDERING INFORMATION

160-pin



Speed	Plastic Quad Flatpack (Q6)
	0°C to +70°C — COMMERCIAL SCREENING
12 ns	LF3370QC12

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