FAIRCHILD SEMICONDUCTOR™

I-Cube®

MSX Family Datasheet

Features

- SRAM-based, in-system programmable
- Configurable I/O Ports
  - Individually programmable as input, output, bi-directional, or Bus Repeater™ mode
  - Control Signals per I/O port: 2 input enables, 2 output enables, 2 Global Clock inputs and Next Neighbor Clock option
  - Output data inversion: capable of inverting output signals in flow through mode
- Non-blocking switch matrix
  - One-to-One and One-to-Many connections
  - Double-buffered configuration RAM cells for simultaneous global updates
- Registered and flow-through data modes
  - Up to 75 MHz clock frequency in registered mode
  - Up to 150 Mb/s in flow-through mode
- 20ns propagation delay in flow-through mode
- 8mA output current
- Dedicated RapidConfigure™ parallel interface or JTAG serial interface available for configuration and readback of MSX devices
- 3.3V operation, LVTTL I/O's (5V tolerant)
- MSX532 is offered in a 792 TBGA package
- MSX340 is offered in a 480 PBGA package

Description

The MSX™ family of SRAM-based bit-oriented switching devices offer flow-through NRZ data rates of up to 150Mb/s and registered clock frequencies of up to 75MHz. The I/O Buffers (IOBs) are individually configurable. The IOBs can be connected to each other through the switch matrix, which supports One-to-One and One-to-Many connections.

The proprietary RapidConfigure parallel interface allows fast configuration of both the IOBs and switch matrix. It also allows readback of the device for test and verification purposes. The MSX devices also support the industry standard JTAG (IEEE 1149.1) interface for boundary scan testing. The JTAG interface can also be used to download configuration data to the device. A functional block diagram of the MSX architecture is shown in Figure 1.

Applications

- Telecom and datacom switching
- Video switches and servers
- Test equipment

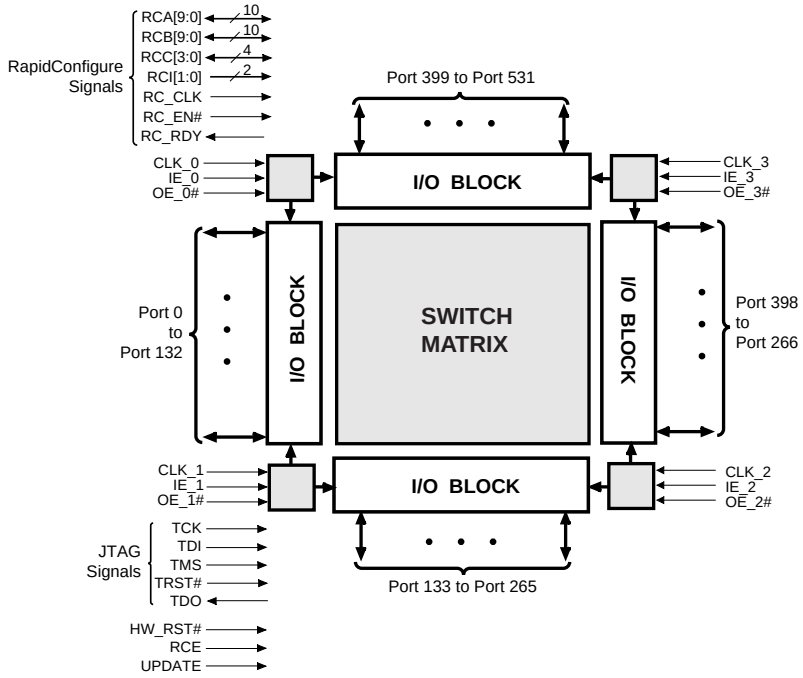

Figure 1 MSX532 Functional Block Diagram

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1. Introduction

1.1 Switch Matrix

The MSX family are SRAM-based, bit-oriented switching devices. The main functional block of the device is a Switch Matrix as shown in Figure 1. The Switch Matrix is an x-y routing structure (or grid). Each horizontal signal trace is hardwired to a corresponding vertical signal trace as shown by the junction dots. An I/O Port pin connects to this horizontal-vertical trace pair through programmable buffer. Signal paths through the Switch Matrix are well balanced, resulting in predictable and uniform pin-to-pin delays.

The two SRAM cells (shown in Figure 2) are arranged so that a double buffered scheme can be employed. The Active SRAM cells are responsible for establishing connections in the switch matrix by turning ON a pass transistor, while the Loading SRAM cell can be used to store a second configuration that can be transferred to the Active SRAM cell at any time. If the UPDATE signal is asserted high, the contents of the Loading SRAM cell are transferred to the Active SRAM cell and the switch matrix connection is either made or broken.

The UPDATE signal can be used to control when the switch matrix is reconfigured. For instance, as long as the UPDATE signal is de-asserted (held low), the Loading SRAM cells for the entire switch matrix could be changed without affecting the current configuration of the switch. When the UPDATE signal is asserted high, the entire switch matrix would be reconfigured simultaneously. If the UPDATE signal is asserted continuously, all crosspoint programming commands (generated by JTAG or RapidConfigure programming cycles) will take effect immediately, since the Loading SRAM cell's contents will be transferred directly to the Active SRAM cell.

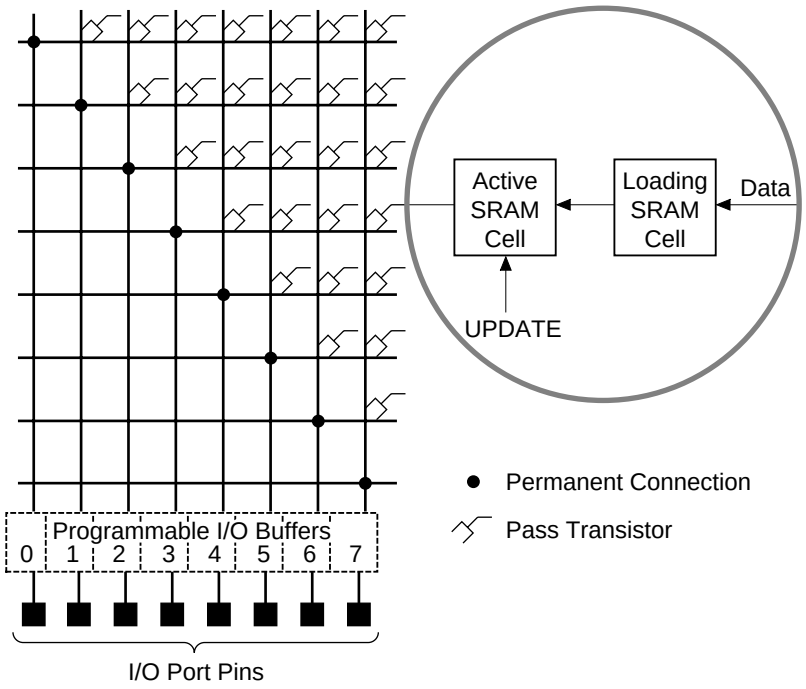

Figure 2 MSX Switch Matrix Diagram

1.2 Input and Output Buffers (IOBs)

Each signal in the switch matrix is connected to a programmable IOB, which is independently configured through either the RapidConfigure or JTAG Interface. The IOB attributes include its signal direction (input, output or bi-directional) and data flow mode (flow-through or registered). The signal can also be inverted at the output. Trickle current source (normally <15 µA) on the pin side and array side for each I/O Port and control pin is used to pull unused or non-driven circuits to a stable high level. Figure 3 shows a basic block diagram of an IOB with the sources for the three control signals (IE, OE and CLK). For any given port number, these three control signals can be selected from one of two sources. The control signals are explained in more detail in the following section.

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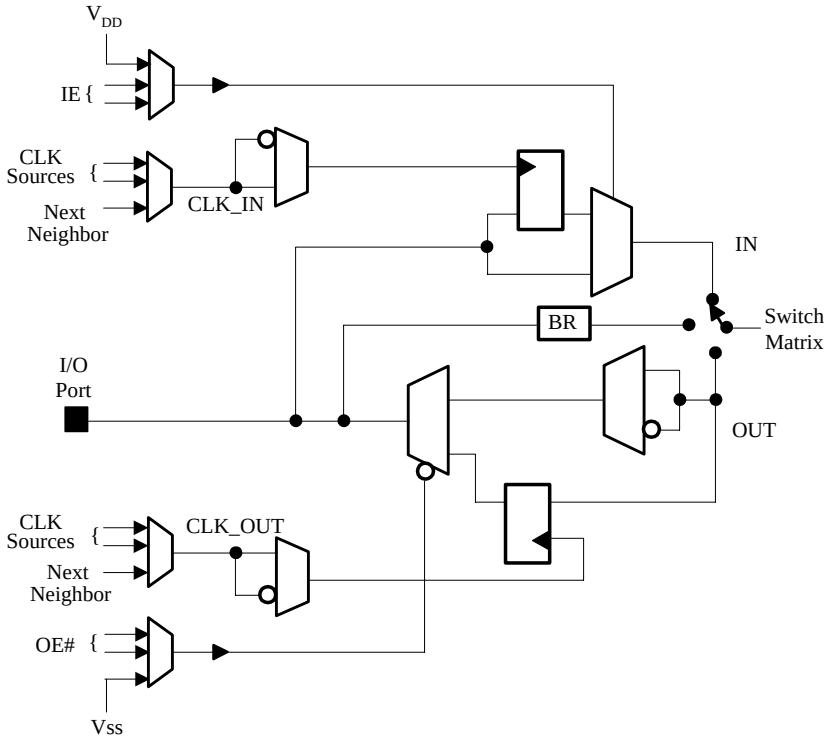


Figure 3 MSX IOB Block Diagram

1.2.1 I/O Port Function Mode

The following legend describes the various modes of the Input or Output Ports and the specification used by the Fairchild Development System Software for bitstream generation.

Legend:

Ax–Switch Matrix Signal

Px–I/O Port Signal

IE–Input Enable

OE#–Output Enable (# means “Active Low”)

CLK–Clock

Table 1 Summary for Programmable I/O Attributes for MSX Devices

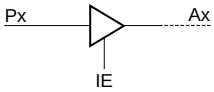
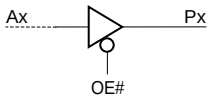
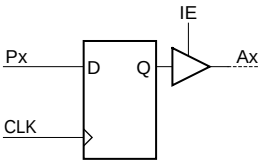
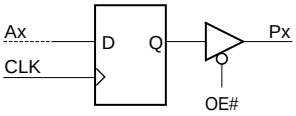
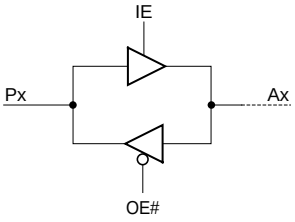
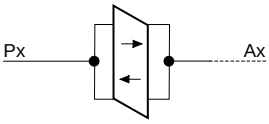
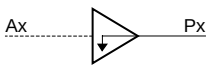
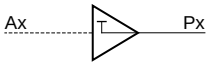
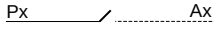
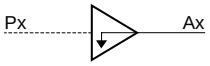
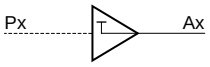
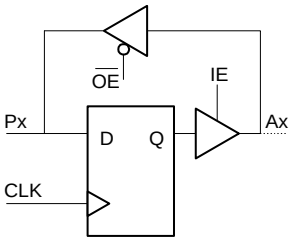
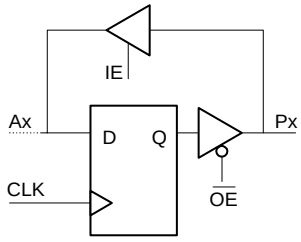
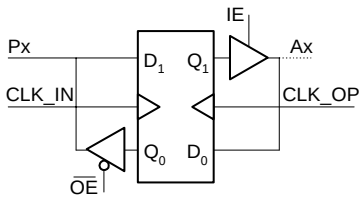
Symbol	I/O Port Function	Mnemonic
	**Input** – The external signal is buffered from the Input Port pin to the corresponding Switch Matrix line.	**IN**
	**Output** – The internal signal is buffered from the corresponding Switch Matrix line to the Output Port pin. In this mode an optional output enable (OE#) can be selected. The default level is logic 0. The output data inversion mode is available to invert the output signal.	**OP**
	**Registered Input** – The external signal at the I/O Port is registered into an edge-triggered register within the I/O Port. A clock source is required in this mode. An input enable (IE) is available but not required.	**RI**
	**Registered Output** – The internal signal on the Switch Matrix line is registered by an edge-triggered register within the I/O Port. A clock source is required in this mode. An output enable (OE#) is available but not required. The output data inversion mode is NOT available to invert the output signal.	**RO**
	**Bidirectional Transceiver** – In this mode, the I/O buffer acts as a bidirectional transceiver between the I/O Port pin and the corresponding Switch Matrix line. This mode requires an input enable (IE) and output enable (OE#). The output data inversion mode is available to invert the output signal.	**BT**
	**Bus Repeater** – In the Bus Repeater mode, the I/O Port behaves as a wire (with a non-zero propagation delay). This unique feature patented by Fairchild incorporates as self-sensing circuit to determine signal direction and does not require a direction control signal. When multiple I/O Ports, configured as “Bus Repeater”, are connected together through the Switch Matrix to form a single internal node, any (open collector or tristatable) “low” (logic “0”) external signal appearing at any one of the I/O Ports gets repeated (or broadcast) to other I/O Ports. For more details, refer to the Technical Note: “The Bus Repeater Mode”	**BR**
	**Pin Side Force 0** – In this output mode, the I/O Port pin is forced low (logic 0), regardless of the signal on the corresponding switch Matrix line. In this mode an optional output enable (OE#) can be selected.	**F0**
	**Pin Side Force 1** – In this output mode, the I/O Port pin is forced high (logic 1), regardless of the signal on the corresponding Switch Matrix line. In this mode an optional output enable (OE#) can be selected.	**F1**
	**No Connect** – In this mode, the I/O Port pin is isolated from the Switch Matrix. This is done by tri-stating both the input and output part of the I/O buffer.	**NC**

Table 1 Summary for Programmable I/O Attributes for MSX Devices *(Continued)*

Symbol	I/O Port Function	Mnemonic
	**Array Side Force 0** – In this input mode, the Switch Matrix line is forced low (logic 0), regardless of the signal on the corresponding I/O Port. In this mode an optional input enable (IE) can be selected.	**A0**
	**Array Side Force 1** – In this input mode, the Switch Matrix line is forced high (logic 1), regardless of the signal on the corresponding I/O Port. In this mode an optional input enable (IE) can be selected.	**A1**
	**Bidirectional Transceiver with Register Input** – This mode combines Registered Input and buffered Output (OP). This mode requires a clock source (CLK), and input enable (IE) and output enable (OE#).	**BT & RI**
	**Bidirectional Transceiver with Register Output** – This mode combines Registered Output (RO) and buffered Input (IE). This mode requires a clock source (CLK), and input enable (IE) and output enable (OE#). The output data inversion mode is NOT available to invert the output signal.	**BT & RO**
	**Bidirectional Transceiver with Register I/O** – This mode combines Registered Input (RI) and Registered Output (RO). This mode requires a clock source (CLK), and input enable (IE) and output enable (OE#). The output data inversion mode is NOT available to invert the output signal.	**BT, RI &RO**

1.3 Control Signals

Every port on the MSX devices has two available global clock inputs, input enables, and output enables. However, not all ports have access to the same global control signals. There are four global clocks (CLK_0 through CLK_3), four global input enables (IE_0 through IE_3), and four global output enables (OE_0# through OE_3#). Each global control signal is available to half of the ports on the MSX device. Table 2 below shows the global control signals that are available to each port.

Table 2 MSX Global Control Signals

MSX340 Port Number	MSX532 Port Number	Input/Output Clock Source 1	Input/Output Clock Source 2	Input Enable 1	Input Enable 2	Output Enable 1	Output Enable 2
Ports 0-84	Ports 0-132	CLK_0	CLK_1	IE_0	IE_1	OE_0#	OE_1#
Ports 85-169	Ports 133-265	CLK_1	CLK_2	IE_1	IE_2	OE_1#	OE_2#
Ports 170-254	Ports 266-398	CLK_2	CLK_3	IE_2	IE_3	OE_2#	OE_3#
Ports 255-339	Ports 399-531	CLK_3	CLK_0	IE_3	IE_0	OE_3#	OE_0#

1.4 RapidConfigure Interface

The MSX family of Digital Crosspoint Switches can be configured in either of two ways. Both the JTAG serial programming interface and the RapidConfigure (RC) parallel interface can assign crosspoint connections and configure I/O Buffers (IOBs), but JTAG is slower. JTAG runs reliably up to 8 MHz and requires over twenty cycles to program a single command. The RapidConfigure interface can run at up to 40 MHz and can send a new command on every clock cycle. Systems requiring frequent reconfiguration should be designed to use the RapidConfigure interface.

RapidConfigure is a 29 signal parallel interface that effectively flattens the serial JTAG bitstream. Rather than consecutively shifting in twenty or so bits of data to configure an IOB or make a crosspoint connection, all of these bits are driven on the RC lines simultaneously and then latched in by the MSX device in a single cycle. Additionally, the MSX RapidConfigure interface has been enhanced to enable reading back of configuration data from the device.

The 29 pins are allocated as follows:

RCA[9:0] = RapidConfigure Address A

RCB[9:0] = RapidConfigure Address B

RCC[3:0] = RapidConfigure Program Variable C

RCI[1:0] = RapidConfigure Instruction Bits

RC_CLK = RapidConfigure Clock

RC_EN# = RapidConfigure Cycle Enable

RC_RDY = Read out IOB and connect/disconnect status

1.4.1 Signal Description

The RC interface supports four types of operations. Two are write operations to the MSX (IOB configuration or crosspoint programming) and two are read operations (IOB and crosspoint configuration read). The RC signals serve different purposes depending upon the type of operation being performed.

Most of the signals on the MSX device's RC interface are bi-directional. These signals receive data during write operations. During read operations these pins receive data during the first part of the cycle, and then drive the interface in the final part of the cycle. RCA[9:0], RCB[9:0], and RCC[0] are bi-directional pins. RCC[3:1], RC_CLK, RC_EN#, and RCI[1:0] are dedicated inputs. RC_RDY is a dedicated output.

The RC_CLK signal is the strobe that latches write data into the MSX device. It synchronizes the signals driven on to the RC interface and determines the rate at which commands can be loaded into the MSX device. The MSX device latches command data on the falling edge of RC_CLK when RC_EN# is asserted. RC Write operations can be repeated on consecutive clocks simply by keeping the RC_EN# signal asserted and providing new commands on the RCA, RCB, RCC, and RCI signals. RC Read operations require four cycles and cannot be performed on back-to-back clocks.

RC_EN# is an active low signal that indicates the beginning of an RC operation. Back-to-back RC Write operations may be performed by keeping the RC_EN# signal asserted. During RC Read operations RC_EN# must remain asserted until the cycle is complete. Back-to-back RC Read operations can be executed simply by keeping RC_EN# asserted.

The MSX device asserts RC_RDY when it has entered the final stage of a read. RC_RDY is asserted on the falling edge of RC_CLK, and de-asserted on the next falling edge. The MSX device will be driving valid read data on the RC interface when RC_RDY is asserted high.

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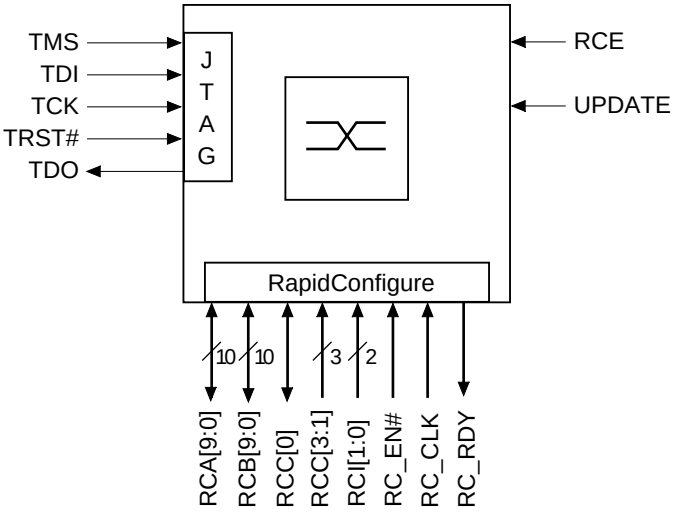


Figure 4 MSX Switch Configuration Signals

The RC interface specifies that the RCI signals be used to determine the type of operation being performed.

Table 3 RapidConfigure Input

RCI[1:0]	Description
00	Force Testing Command. Force commands can force a port to drive either a one or a zero to either the pad or crosspoint array. These commands are generally only used for diagnostic testing.
01	I/O Buffer Programming Command. These commands are used to configure a port as an input or output, registered or not, etc.
10	Crosspoint Array Programming Command. Crosspoint connections can be made or broken, or an individual port can be reset.
11	Read and Reset Commands. This setting is used to read back configuration data from an IOB or crosspoint connection information. It can also be used to reset all of the IOBs and the crosspoint array.

1.4.2 Read and Reset Commands

When RCI[1:0] are equal to 11 a Read or Reset command is executed (see Table 4: Reset Commands).

1.4.2.1 Reset Commands

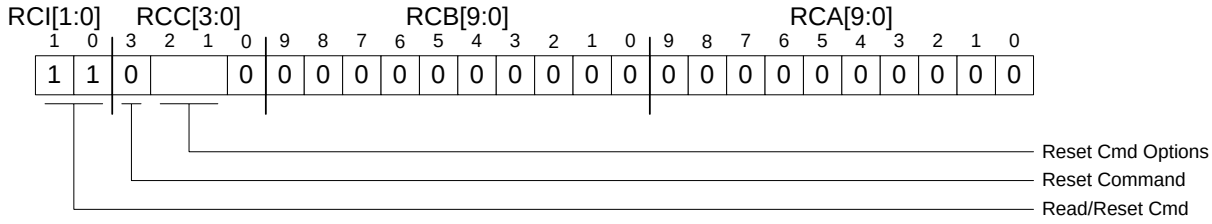


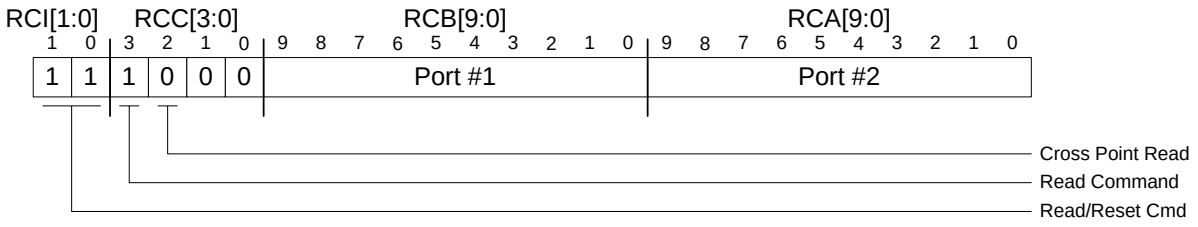
Table 4 Reset Commands

RCC[2:1]	Description
00	Reserved. This is not a valid command.
01	Reserved. This is not a valid command.
10	Crosspoint Array Reset. This command will reset the entire crosspoint array, breaking any previously existing connections.
11	Crosspoint Array and IOB Reset. This command resets both the IOBs and the crosspoint array as described above.

RCC[0], RCB[9:0], and RCA[9:0] have no function during a reset command and must be written as zeroes.

1.4.2.2 Crosspoint Read Commands

A crosspoint read is used to check whether two ports are connected through the crosspoint array. The two ports are addressed using RCA[9:0] and RCB[9:0].



The MSX device uses RCC[0] to show whether the two ports are connected. It drives RCC[0] high if the two ports are connected, and pulls RCC[0] low if the two ports are not connected.

1.4.2.3 IOB Read Commands

I/O Buffer reads are more complicated (see Table 5: I/O Buffer read Commands). The port to be read is addressed using RCA[9:0]. The MSX device uses RCA[9:0] and RCB[9:0] to return all of the configuration data for the particular IOB.

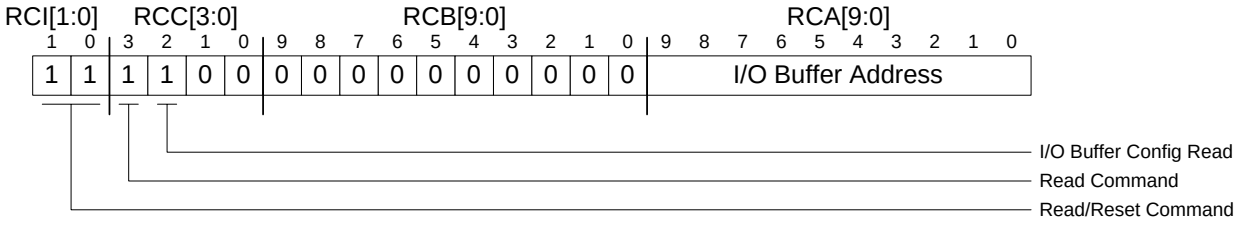


Table 5 I/O Buffer Read Commands

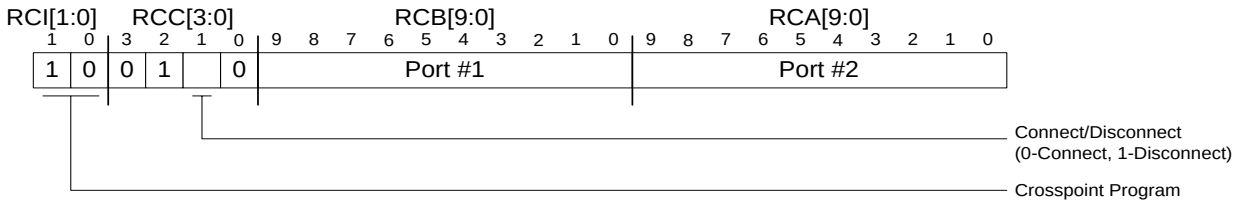
Signal	Description
RCA[0]	RCA[0] is set to one if the IOB is an input. It is zero if the IOB is not configured as an input. Note that an IOB can be configured as an Input, Output, Input and Output (in bi-directional mode), or No Connect. All IOBs default to inputs at power-on reset or following a global IOB Reset command, so RCA[0] will read as a one at reset.
RCA[1]	RCA[1] is set to a one if the IOB is an output. It is zero if the IOB is not configured as an output. If RCA[1:0] equal 00 the IOB is configured as a No Connect. A No Connect means that the I/O pin of the MSX device is not connected to the crosspoint array. RCA[1] will read as a zero at reset.
RCA[2]	RCA[2] is set to a one if the IOB is configured in Bus Repeater Mode. It is zero if the IOB is not in Bus Repeater Mode. Bus Repeater Mode will be disabled by default at reset, so RCA[2] will read as a zero.
RCA[3]	RCA[3] is set to a one if the IOB is configured as a registered input and is assigned to use its Input Clock 1. It is zero if the IOB is not using Input Clock 1. Input Clock 1 for each IOB will vary depending upon the quadrant of the device in which it resides. RCA[3] will read as a zero at reset.
RCA[4]	RCA[4] is set to a one if the IOB is configured as a registered input and is assigned to use its Input Clock 2. It is zero if the IOB is not using Input Clock 2. As with Input Clock 1, the source changes depending upon the quadrant of the device in which the IOB resides. RCA[4] will read as a zero at reset.
RCA[5]	RCA[5] is set to a one if the IOB is configured as a registered input and assigned to use Next Neighbor Clocking. It is zero if Next Neighbor Clocking is disabled. Next Neighbor Clocking allows the IOB to be registered using the next higher numbered Port number signal as its input clock source. Port 100 on the MSX devices can use the signal from Port 101 for its input clock if this mode is enabled. Port 531's Next Neighbor is Port 0. Next Neighbor Clocking will be disabled by default at reset, so RCA[5] will read as a zero.

Table 5 I/O Buffer Read Commands *(Continued)*

Signal	Description
RCA[6]	RCA[6] is set to a one if the IOB is configured as a registered output and is assigned to use its Output Clock 1. It is zero if the IOB is not using Output Clock 1. As with Input Clock 1 and 2, the Output Clocks will vary depending upon the quadrant of the device in which the IOB resides. In the case of the MSX devices, the Output Clock 1 and Input Clock 1 for each IOB have the same source, and the Output Clock 2 and Input Clock 2 do as well. RCA[6] will read as a zero at reset.
RCA[7]	RCA[7] is set to a one if the IOB is configured as a registered output and is assigned to use its Output Clock 2. It is zero if the IOB is not using Output Clock 2. As with Output Clock 1, the source changes depending upon the quadrant of the device in which the IOB resides. RCA[7] will read as a zero at reset.
RCA[8]	RCA[8] is set to a one if the IOB is configured as a registered output and is assigned to use Next Neighbor Clocking. It is zero if Next Neighbor Clocking is disabled. Next Neighbor Clocking allows the IOB to be registered using the next higher numbered Port number signal as its output clock source. Port 100 on the MSX devices can use the signal from Port 101 for its output clock if this mode is enabled. Port 531's Next Neighbor is Port 0. Next Neighbor Clocking will be disabled by default at reset, so RCA[8] will read as a zero.
RCA[9]	RCA[9] is set to a one if the IOB is assigned to use Input Enable 1. It is zero if the IOB is not using Input Enable 1. All bi-directional IOBs must use one of the dedicated input enable pins (IE_0, IE_1, IE_2, or IE_3) to enable the IOB to drive data into the crosspoint array. As with the dedicated clock pins, each IOB can access two input enable signals, which will vary depending upon the quadrant of this chip in which the IOB resides. RCA[9] will read as a zero at reset.
RCB[0]	RCB[0] is set to a one if the IOB is assigned to use Input Enable 2. It is zero if the IOB is not using Input Enable 2. RCB[0] will read as a zero at reset.
RCB[1]	RCB[1] is set to a one if the IOB is assigned to use Output Enable 1. It is zero if the IOB is not using Output Enable 1. All bi-directional IOBs must use one of the dedicated output enable pins (OE_0#, OE_1#, OE_2#, or OE_3#) to enable the IOB to drive the pin of the device. As with the dedicated clock pins, each IOB can access two output enable signals, which will vary depending upon the quadrant of the chip in which the IOB resides. RCB[1] will read as a zero at reset.
RCB[2]	RCB[2] is set to a one if the IOB is assigned to use Output Enable 2. It is zero if the IOB is not using Output Enable 2. RCB[2] will read as a zero at reset.
RCB[6:3]	RCB[6:3] are reserved.
RCB[7]	RCB[7] is set to a one if the IOB is configured as an inverted output. It is zero if the IOB is not configured as an inverted output. The output of any IOB may be inverted so long as it is not a registered output or running in Bus Repeater Mode. RCB[7] will read as a zero at reset.
RCB[8]	RCB[8] is set to a one if the IOB is configured as a registered input and is using an inverted input clock source. It is zero if it is not using an inverted input clock. Inputs can use any of the three clock sources described above and may invert that clock if desired. RCB[8] will read as a zero at reset.
RCB[9]	RCB[9] is set to a one if the IOB is configured as a registered output and is using an inverted output clock source. It is zero if it is not using an inverted output clock. Outputs can use any of the three clock sources described above and may invert that clock if desired. RCB[9] will read as a zero at reset.

1.4.3 Crosspoint Programming

Connections between ports through the crosspoint array can be quickly made or broken using the RC interface. The two ports to be connected or disconnected are addressed using RCA[9:0] and RCB[9:0]. RCC[1] controls whether a connection is made or broken. The two ports are connected when RCC[1] is set to zero, and disconnected when RCC[1] is set to one.



Unlike IOB programming commands, which take effect immediately upon execution of the command, crosspoint connections will only be made if the UPDATE signal is asserted high. The crosspoint programming command loads the Loading SRAM cell in the selected crosspoint array location with a one (in the case of a new connection) or a zero (to break an existing connection). If the UPDATE signal is asserted, the Loading SRAM cells contents are immediately transferred to the Active SRAM cell and the connection is made or broken. However, if the UPDATE signal is held low, the new connection will not be made. The UPDATE signal can be used to control when the switch matrix connections are reconfigured.

1.4.4 IOB Configuration Programming

Each port can be fully configured in a single RapidConfigure cycle. The figure below shows how an IOB is programmed using all of the signals on the RC interface. The following table shows how each control bits (RCC[3:0] and RCB[9:0]) are used. During an IOB programming command the RCA[9:0] signals address the port to be programmed (see Table 6: IOB Programming Commands).

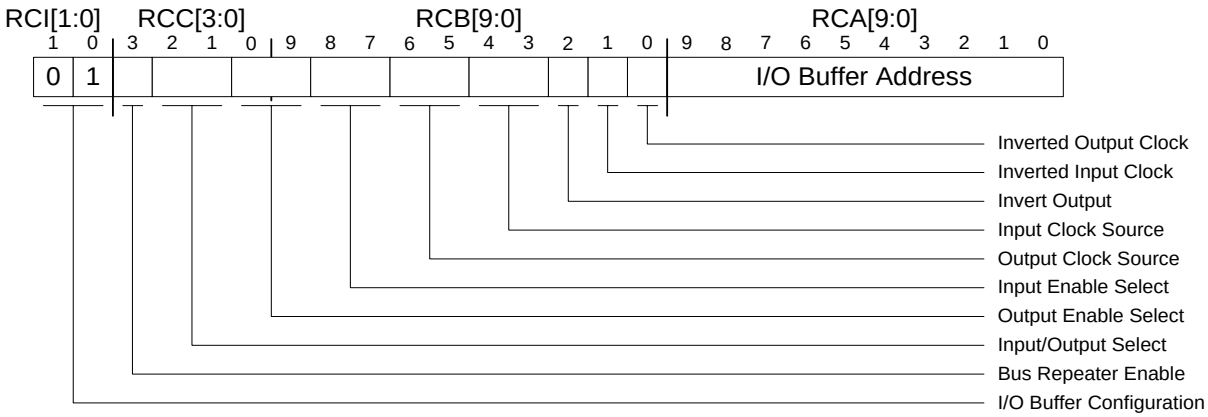


Table 6 IOB Programming Commands

Signal	Description
RCC[3]	Bus Repeater Enable. Setting this bit to a one enables the IOB to operate in Bus Repeater Mode, a special bi-directional mode. When zero the IOB will not operate in Bus Repeater Mode. When programming an IOB to use Bus Repeater Mode, all of the other control bits must be set to zeroes. Attempting to combine other IOB options with Bus Repeater Mode may lead to unpredictable results.
RCC[2:1]	Input/Output Select. These two bits are used to configure the IOB as an input, output, input/output (bi-directional mode), or no connect. When operating in bi-directional mode it is critical that the port be assigned input and output enables so that it can be tri-stated appropriately to avoid contention. RCC[2:1] Function 00 No Connect 01 Input 10 Output 11 Input / Output for Bi-Directional Mode
RCC[0] and RCB[9]	Output Enable Select. These two bits are used to select from the two available active low global output enables. The output will be allowed to drive when its assigned output enable is asserted. An output port will be tri-stated when its assigned output enable is de-asserted. When both output enables are selected, the two available active low output enable signals are AND's together to form the port's combined output enable signal. RCC[0], RCB[9] Function 00 No Output Enable Selected 01 Output Enable 1 10 Output Enable 2 11 Both Output Enables
RCB[8:7]	Input Enable Select. These bits are used to assign a port one of the two available global input enable signals. An input port will drive into the crosspoint array when its assigned input enable is asserted. When both input enables are selected, the two available input enable signals are OR'd together to form the port's combined input enable signal. RCB[8:7] Function 00 No Input Enable Selected 01 Input Enable 1 10 Input Enable 2 11 Both Input Enables
RCB[6:5]	Output Clock Source. These bits are used to select a clock source for a registered output port. Each IOB can select from one of two global clock inputs, or can use Next Neighbor Clocking. Next Neighbor Clocking uses the signal on the next higher numbered port as a clock source. If no clock source is assigned to an output port, it will operate in flow-through mode. RCB[6:5] Function 00 No Output Clock Source Selected 01 Output Clock Source 1 10 Output Clock Source 2 11 Next Neighbor Output Clock Source

Table 6 IOB Programming Commands *(Continued)*

Signal	Description
RCB[4:3]	Input Clock Source. These bits are used to select a clock source for a registered input port. Each IOB can select from one of two global clock inputs, or can use Next Neighbor Clocking. Next Neighbor Clocking uses the signal on the next higher numbered port as a clock source. If no clock source is assigned to an input port, it will operate in flow-through mode. RCB[6:5] Function 00 No Input Clock Source Selected 01 Input Clock Source 1 10 Input Clock Source 2 11 Next Neighbor Input Clock Source
RCB[2]	Invert Output. If an output port is programmed with this bit set to a one, the output of the port will be inverted. If this bit is zero, the output will not be inverted. Outputs may not be inverted when operating in Bus Repeater Mode or in registered output mode.
RCB[1]	Inverted Input Clock. When this bit is set to a one, the registered input port's selected clock source will be inverted. When zero the input clock source will not be inverted.
RCB[0]	Inverted Output Clock. When this bit is set to a one, the registered output port's selected clock source will be inverted. When zero the output clock source will not be inverted.

1.5 JTAG Interface

The dedicated JTAG TAP interface is designed in compliance with the IEEE-1149.1. The standard interface has five pins: Test Data Out (TDO), Test Mode Select (TMS), Test Data In (TDI), Test Reset (TRST#), and Test Clock (TCK) which allow Boundary Scan Testing as well as device configuration and verification. Data on the TDI and TMS pins are clocked into the device on the rising edge of the TCK signal, while the valid data appears on the TDO pin after the falling edge of TCK. For more detailed information on JTAG programming, refer to the *MSX Family Register Programming Manual*.

1.5.1 IOB Programming

The JTAG IOB Data Register where data is held, is used to program the IOB. This register is used with the JTAG interface only. The JTAG IOB Data Register is 20 bits wide. Power on reset, RapidConfigure reset, Hardware reset, and JTAG reset programs all Ports as inputs. JTAG can be reset via the TRST# pin or by clocking five consecutive ones to the TMS pin. The HW_RST# (hardware reset) pin resets and breaks all connections in the Crosspoint Array to all no-connects, and the IOBs to inputs.

Table 7 lists the bits and their function in JTAG mode. These are internal bits as shifted into the IOB Data register for IOB Programming.

Table 7 IOB Programming Bit Functions

Bit Number	IOB Function	Description
0	Input (IN)	Input Pin data to drive Array
1	Output (OP)	Output Array data to Pin
2	Bus Repeater (BR)	Low Array Signal, Drive Pin Low Low Pin Signal, Drive Array Low
3	Reg In Clock 1	Selects Reg. In IOB, Clock 1
4	Reg In Clock 2	Selects Reg. In IOB, Clock 2
5	Reg In Clk Neighbor	Selects Reg. In IOB, Neighbor
6	Reg Out Clock 1	Selects Reg. Out IOB, Clock 1
7	Reg Out Clock 2	Selects Reg. Out IOB, Clock 2
8	Reg Out Clk Neighbor	Selects Reg. Out IOB, Neighbor
9	Input Enable 1 (IE1)	Select Input Enable 1 [1]
10	Input Enable 2 (IE2)	Select Input Enable 2 [1]
11	Output Enable 1 (OE1)	Select Output Enable 1 [2]
12	Output Enable 2 (OE2)	Select Output Enable 2 [2]
13	Force 1	Force IOB output Pin to a 1
14	Force 0	Force IOB output Pin to a 0
15	Array 1	Force IOB Array to a 1
16	Array 0	Force IOB Array to a 0
17	Invert Output	Output data is inverted. This operation is invalid in Bus Repeater mode and Register Output mode
18	Invert Input Clock	Invert the clock to the input register
19	Invert Output Clock	Invert the clock to the output register

NOTES:

1. If both IE1 and IE2 are selected, the two are assigned an OR function to form the IE. Either can be “1” to enable the input.
2. If both OE1# and OE2# are selected, active low signals are assigned an AND function to form the resulting OE#. Either can be “0” to enable the output.

1.5.2 JTAG Architecture and Shift Registers

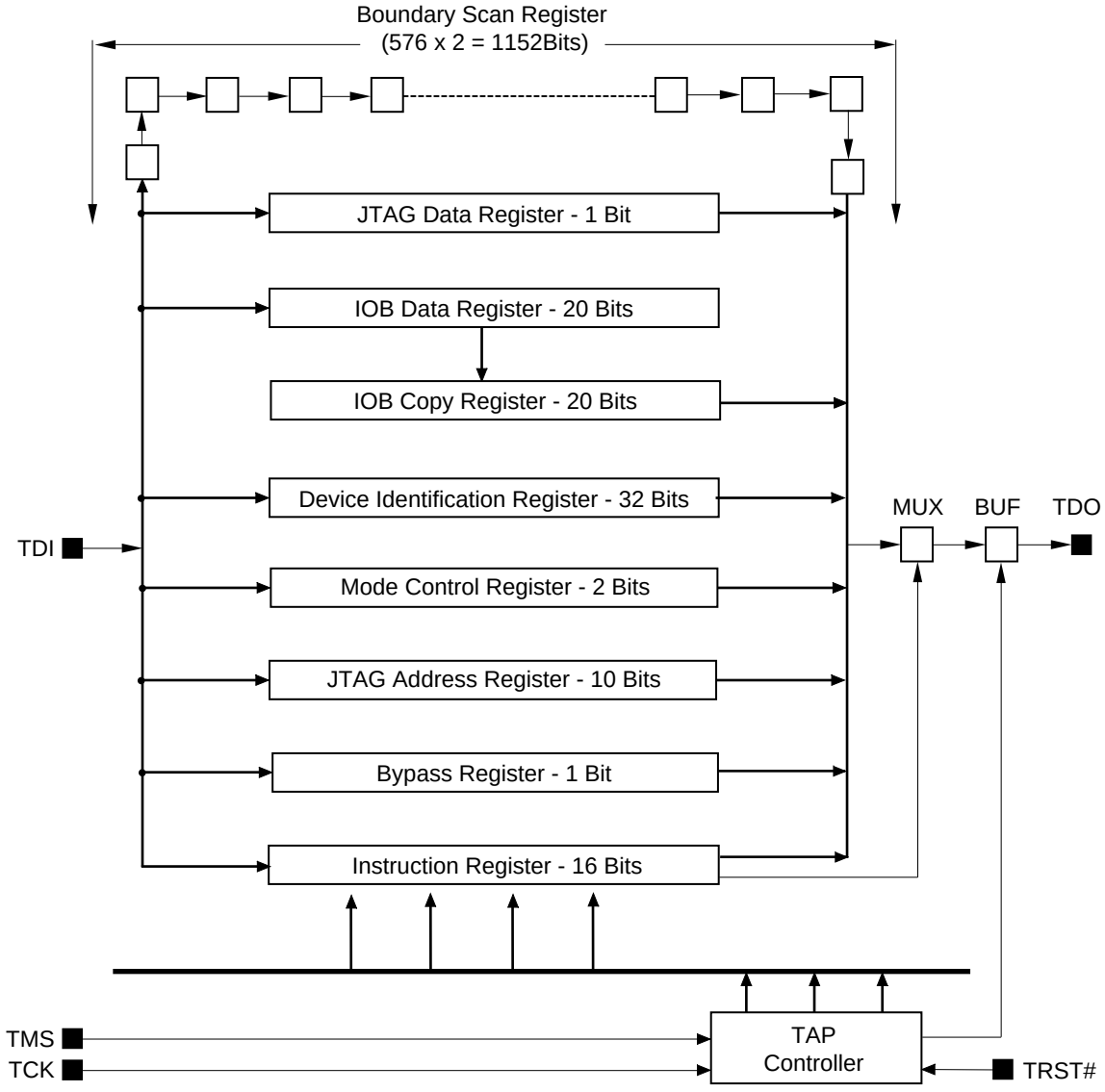


Figure 5 MSX JTAG Architecture

1.5.3 JTAG State Machine

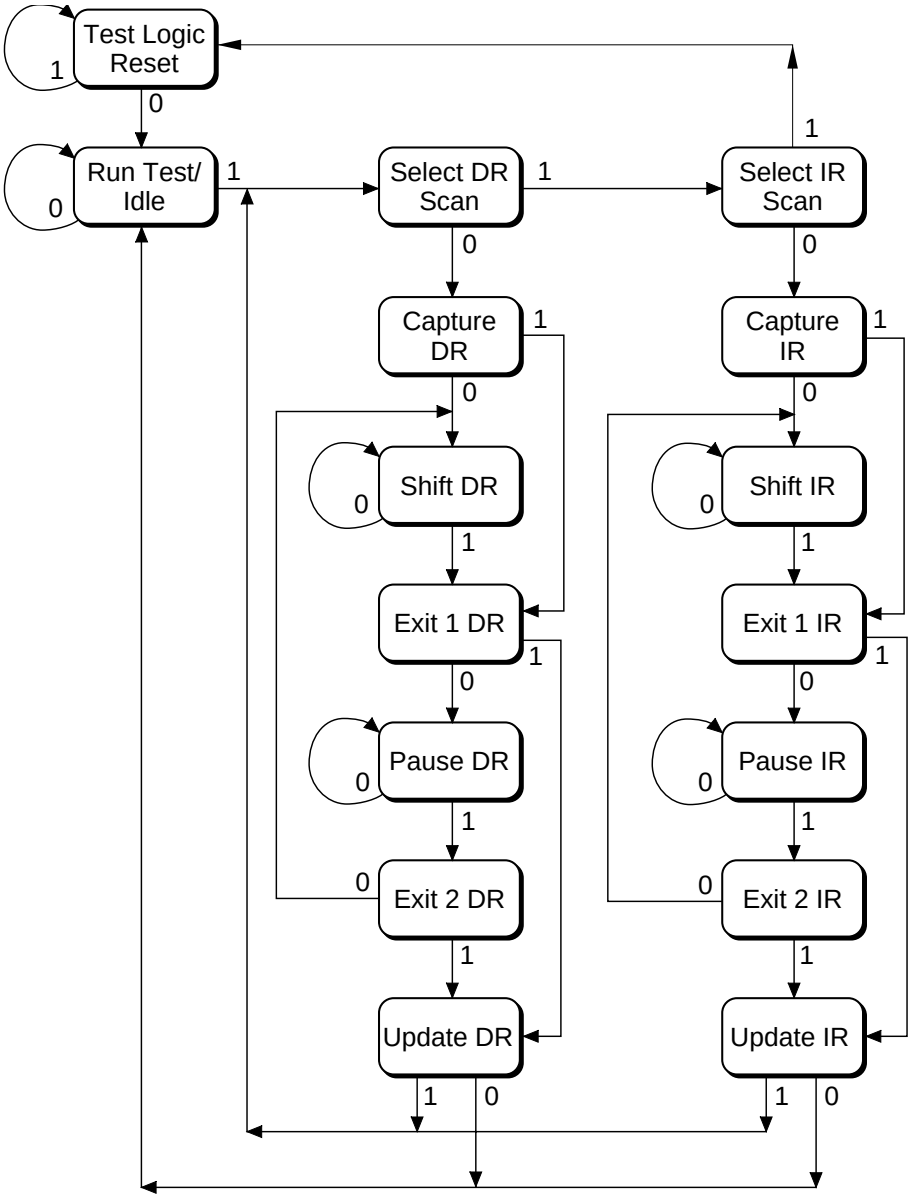


Figure 6 JTAG State Machine

1.5.4 JTAG Input Format

Table 8 JTAG Input Format

	Instruction				Control		Address									
Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	I3	I2	I1	I0	C1	C0	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

1.5.5 JTAG Instructions

Table 9 JTAG Instructions

I3	I2	I1	I0	Instruction	Description
1	1	1	1	Bypass	Places device in a mode to pass TDI data to TDO with one clock delay. Used for programming and testing devices through serial connected JTAG controls.
1	1	1	0	Control Register	Shifts data in and out of the Control Register. Capture, shift, and write the Control Register.
1	1	0	1	IO Buffer and Crosspoint Array Reset, Device ID out	Resets IOBs for the Ports to Input and clear all Ports to Disconnect. The device ID is serialized out to TDO. The Instruction serialized out is the RESET Instruction during the Instruction phase. Update is forced to the crosspoint array.
1	1	0	0	Device ID out	Serialize the device ID and revision history out to TDO. ID for the MSX is **0x0000A89F.**
1	0	1	1	Set the JTAG Address Register	Set the 10-bit JTAG Address Register with the lower ten bits of the JTAG Instruction Register. The lower ten bits of the JTAG Address Register become the 'B' Address for Crosspoint Access.
1	0	1	0	Access the Crosspoint Array and Update Array	Read or Write the crosspoint addressed by the lower ten bits of the JTAG Instruction (A Address) and the JTAG Address Register or Address Counter (B Address). Read data is shifted out on TDO. C1 C0=0 0 Read Switch with A and B Address. Increment 'B' address with each ShiftDR. C1 C0=0 1 Connect switch at location Addressed with A and B. Increment 'B' address with each ShiftDR. Activate with UpdateDR. C1 C0=1 0 Disconnect switch at location Addressed with A and B. Increment 'B' address with each ShiftDR. Activate with UpdateDR. C1 C0=1 1 Force update of Switch Array Shadow register. Activate with UpdateDR.
1	0	0	1	Disconnect a Port in the Crosspoint Array	Disconnect all Ports from the Port Addressed by the lower ten bits of the JTAG Instruction. The addressed port is reset to disconnect. The programmed state of the IOB is not changed.
1	0	0	0	Clear the Crosspoint Array	Clear the crosspoint array at no-connect. Leave the IOBs unchanged.
0	1	1	1	Shift the IO Buffer Data Register	Shift twenty bits of data into and out of the IOB Data register. The data is used to program the IOBs. Parallel shift twenty bits into IOB Copy Register.
0	1	1	0	Shift out the IOB Copy Register	Shifts twenty bits of data out of the IOB Copy Register. Data is either the IOB Data register shifted in by instruction 0111 or the last JTAG IOB Read Data.

Table 9 JTAG Instructions *(Continued)*

I3	I2	I1	I0	Instruction	Description
0	1	0	1	Access an IOB	Read or write the IOB addressed with the lower ten bits of the JTAG Instruction. Read data is placed in the twenty-bit IOB Copy Register. Write Data for the IOB is from the IOB Data Register. C1 C0=0 0 Read an IOB date into the Copy Register. C1 C0=0 1 Write an IOB with data in IOB Data Register.
0	1	0	0		Not used.
0	0	1	1	Test mode only for programming device with RapidConfigure through JTAG	Fairchild only - internal test mode to test RapidConfigure through JTAG.
0	0	1	0	Crosspoint Array Write Testing, Write one location per ShiftDR	Instruction Address=LowerLimit=A, Address Register=Upper Limit=B. C1=1, C0=1 Connect all ports in address range C1=1, C0=0 Connect Pattern=A[1] XOR B[1] C1=0, C0=0 Connect Pattern=A[4] C1=0, C0=1 Connect Pattern=NOT (A[1] XOR B[1]). Compliment address limits, Address is complimented to test A-High Port to B-Low Port connections. Other three patterns test opposite. The number of cycles=(Sum of (X=1), where X=Low Limit to X=High Limit) - 1
0	0	0	0	Sample/Preload EXTEST	External scan tests for interconnect testing.
0	0	0	1	Sample/Preload EXTEST	External scan tests for interconnect testing.

2. Pin Description

Pin Name	Type	Description
P[531:000]	Bi-directional	Input/Output Signals.
OE[3:0]#	Input	Global Output Enables. Each output enable can control two of the four I/O banks. Signal — MSX532 Connected I/O's — MSX340 Connected I/O's OE_0# — P399-P531, P000-P132 — P255-P339, P000-P084 OE_1# — P000-P132, P133-P265 — P000-P084, P085-P169 OE_2# — P133-P265, P266-P398 — P085-P169, P170-P254 OE_3# — P266-P398, P399-P531 — P170-P254, P255-P339
IE[3:0]	Input	Global Input Enables. Each input enable can control two of the four I/O banks. Signal — MSX532 Connected I/O's — MSX340 Connected I/O's IE_0 — P399-P531, P000-P132 — P255-P339, P000-P084 IE_1 — P000-P132, P133-P265 — P000-P084, P085-P169 IE_2 — P133-P265, P266-P398 — P085-P169, P170-P254 IE_3 — P266-P398, P399-P531 — P170-P254, P255-P339
UPDATE	Input	Global Update
CLK[3:0]	Input	Global Clocks. Each clock can control two of the four I/O banks. Signal — MSX532 Connected I/O's — MSX340 Connected I/O's CLK_0 — P399-P531, P000-P132 — P255-P339, P000-P084 CLK_1 — P000-P132, P133-P265 — P000-P084, P085-P169 CLK_2 — P133-P265, P266-P398 — P085-P169, P170-P254 CLK_3 — P266-P398, P399-P531 — P170-P254, P255-P339
HW_RST#	Input	Hardware Reset.
RCE	Input	RapidConfigure Mode Select. Determines which programming mode that the device powers up in. 0 = JTAG mode (RapidConfigure disabled) 1 = RapidConfigure mode (JTAG, IOB, Crosspoint programming disabled)
RC Pins		
RC_CLK	Input	RapidConfigure Clock.
RC_EN#	Input	RapidConfigure Cycle Enable.
RCA[9:0]	Bi-directional	RapidConfigure Address A.
RCB[9:0]	Bi-directional	RapidConfigure Address B.
RCC[0]	Bi-directional	RapidConfigure Program Variable C.
RCC[3:1]	Input	RapidConfigure Program Variable C.
RCI[1:0]	Input	RapidConfigure Instruction Bits.
RC_RDY	Output	Read out IOB and connect/disconnect status.
JTAG Pins		
TCK	Input	JTAG Test Clock.
TDI	Input	JTAG Test Data In.
TDO	Output	JTAG Test Data Out.
TMS	Input	JTAG Test Mode Select.
TRST#	Input	JTAG Test Reset.
Power and Ground Pins		
V_{DD}	Power	+3.3V power for the chip.
V_{SS}	Ground	Ground for the chip. Tie these pins to system ground.

3. Electrical Specifications

3.1 Absolute Maximum Ratings

Table 10 Absolute Maximum Ratings [1]

Symbol	Parameter	Limits	Units
V_{DD}	Supply Voltage	-0.3 to +3.6	V
V_{IN} [2]	Supply Voltage (inputs)	-0.3 to +5.5 [3]	V
T_J	Junction Temperature	+150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_{MAX}	Maximum Power Dissipation	10.5	W
ESD [5]	Electrostatic Discharge	1500	V

3.2 Recommended Operating Conditions

Table 11 Recommended Operating Conditions

Symbol	Parameter	Limits	Units
V_{DD}	Supply Voltage	+3.0 to +3.6	V
T_A	Operating Temperature	0 to +70	°C

3.3 Pin Capacitance

Table 12 Pin Capacitance [4]

Symbol	Parameter	Limits	Units
C_{CLK}	Input Capacitance	10	pF
C_{PORT}	I/O Signal Port Capacitance	8	pF

1. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. A maximum undershoot of 2V for a maximum duration of 20 ns is acceptable. Overshoot to 5.5V is acceptable.
3. All inputs are 5V tolerant with the V_{DD} pin at 3.3V.
4. Capacitance measured at 25°C. Sample tested only.
5. Measured using Human Body Model.

3.4 DC Electrical Specifications

(T_A = 0°C to 70°C, V_{DD} = 3.3V ±10%)

Table 13 LVTTL DC Electrical Specifications

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	High-level Input	Ports are 5V tolerant	2.0	5.25	V
V_{IL}	Low-level Input	Ports are 5V tolerant	-0.3	0.8	V
V_{OH}	High-level Output	V_{DD} = Min V_{DD} = 3.00 I_{OH} = -4mA	2.4	V_{DD} + 0.3	V
V_{OL}	Low-level Output	V_{DD} = Min V_{DD} = 3.00 I_{OL} = 8mA		0.4	V
IL_{IH}, IL_{IL}	Input Leakage for non-programmable I/O pins	V_{DD} = Max 0.0 < In < V_{DD}		+5 -100	µA
IL_{OZ}	Tristate Leakage Output OFF State	V_{DD} = Max 0.0 < In < V_{DD}		+5 -100	µA
I_{OSH}	Short Circuit Current, Out = High	V_{DD} = Max V_0 = Gnd		-80	mA
I_{OSL}	Short Circuit Current, Out = Low	V_{DD} = Max V_0 = V_{DD}		50	mA
Supply Current					
I_{DDQ}	Quiescent Supply Current	V_{DD} = Max		50	mA
Q_{DDD} [1]	Dynamic Supply Current	V_{DD} = Max. No Load, one input cycling @ 50% duty cycle		0.25	mA/MHz

1. See section 5 for dynamic power consumption calculation.

3.5 AC Electrical Specifications

(T_A = 0°C to 70°C, V_{DD} = 3.3V ±10%)

Table 14 AC Electrical Specifications for MSX532 and MSX340

Symbol	Parameter	–20		Units
		Min	Max	
R_{DATA}	NRZ Data Rate		150	Mb/s
f_{RIO}	Registered Input/Output Clock Frequency		75	MHz
t_{W_RIO}	Registered Clock Pulse Width, High or Low	2		ns
t_{S_RI}	Registered Input Setup Time to Clock	3.5		ns
t_{S_RO}	Registered Output Setup Time to Clock	9.5		ns
t_{H_RI}	Registered Input Clock to Hold Data	0		ns
t_{H_RO}	Registered Output Clock to Hold Data	0		ns
t_{CO_RO}	Registered Output Clock to Data Out Valid		11	ns
t_{CO_RI}	Registered Input Clock to Data Out Valid		24	ns
t_{PHL}, t_{PLH}	One Way Signal Propagation Delay, Fanout = 1		20	ns
t_{MC} Delta	Additional Delay Per Output Multicast (MC) Mode		2	ns
t_{W+}	Input Flow-through Positive Pulse Width	6		
t_{W-}	Input Flow-through Negative Pulse Width	6		
t_{SK}	Skew		2	ns
t_{PZH_IT}, t_{PZL_IT}	Input Enable to Valid Data		20	ns
t_{PZH_OT}, t_{PZL_OT}	Output Enable to Valid Data		7.5	ns
t_{PZH_OT}, t_{PZL_OT}	Output Enable to High Z State		7.5	ns
t_{RC}	RapidConfigure Clock Period	20		ns
t_{W+_RC} t_{W-_RC}	RapidConfigure Clock Pulse Width	5		ns
t_{S_RC}	RapidConfigure Address Setup to RC Clock	1		ns
t_{H_RC}	RapidConfigure Address Hold Time to RC Clock	4		ns
t_{P_RC}	Read Back Access Time		9	ns
t_{P_RD}	RC_RDY to Readback Data		4	ns
t_{P_UD}	Update of Crosspoint to Data Out		10	ns
f_{JTAG}	JTAG Clock Frequency (TCK)		8	MHz
t_{W_JTAG}	JTAG Clock Pulse Width (TCK) at 20 MHz Cycle	40	60	ns
t_{S_JTAG}	JTAG Setup Time	4		ns
t_{H_JTAG}	JTAG Hold Time	0		ns
t_{P_JTAG}	JTAG Clock to Output Data Valid (TDO)		10	ns

Note – Refer to Figure 7 for AC test conditions.

3.6 Test Circuit and Timing Diagrams

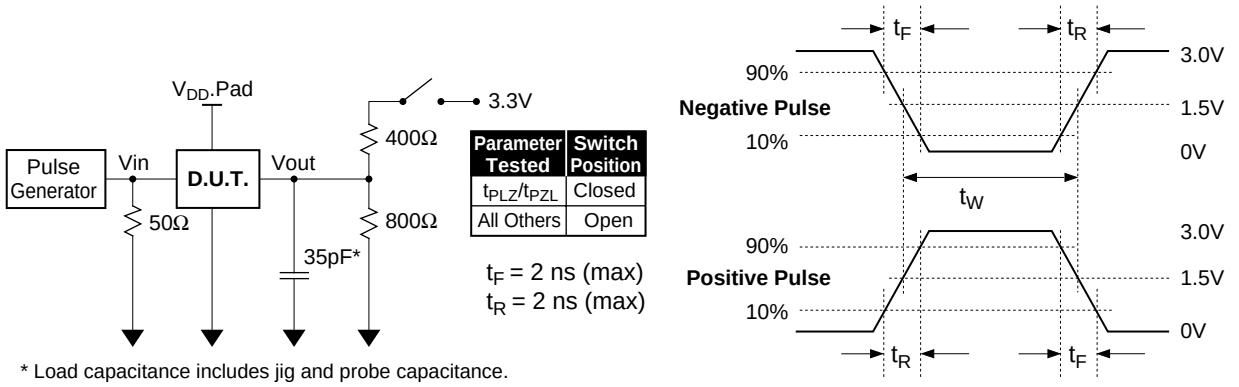


Figure 7 Test Circuit and Waveform Definition

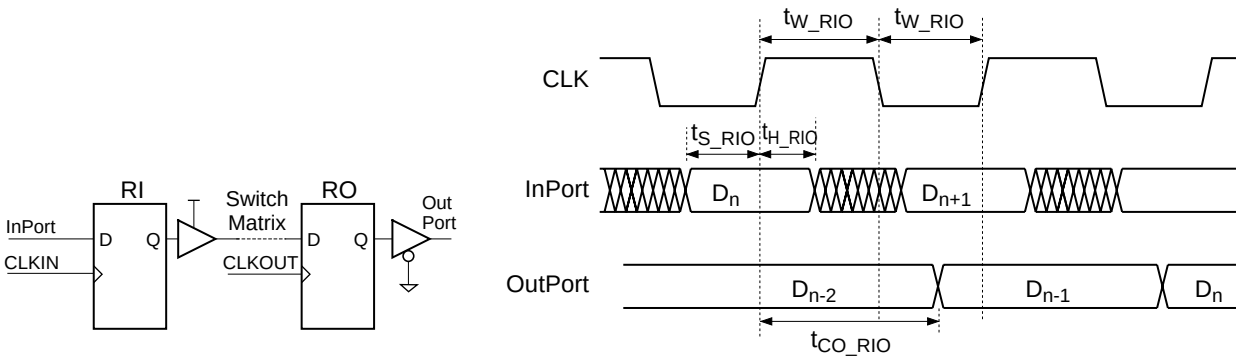


Figure 8 Registered Input and Registered Output Mode Timing (ICLK and OCLK Synchronized)

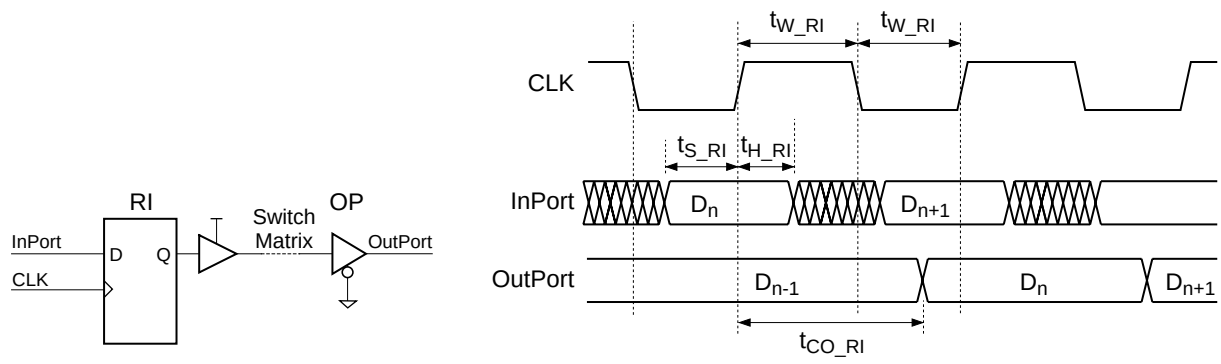


Figure 9 Registered Input Timing Mode

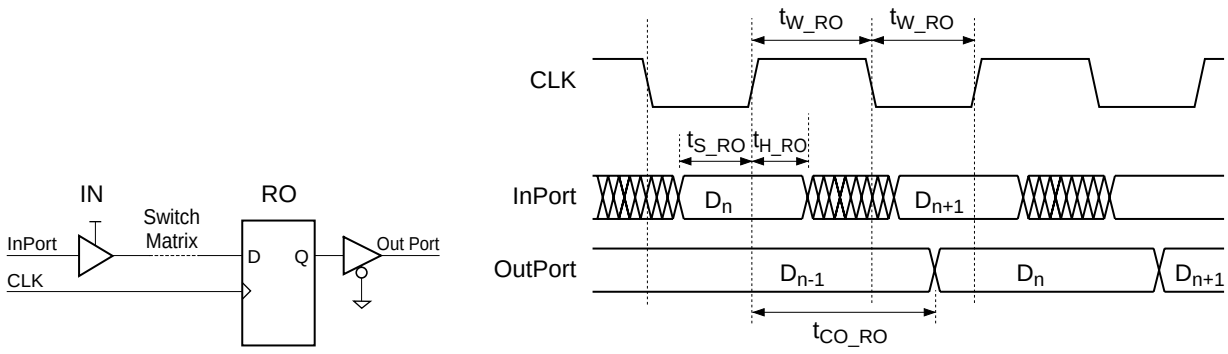


Figure 10 Registered Output Timing Mode

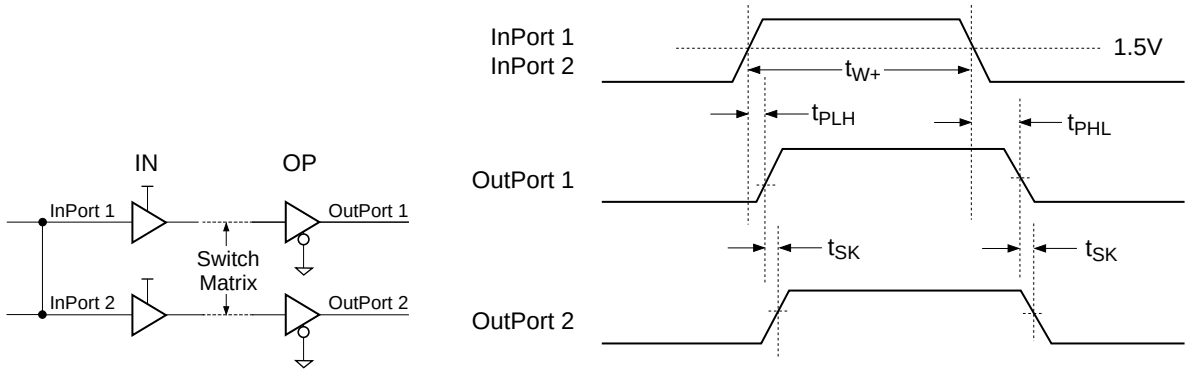


Figure 11 I/O Port Timing (Flow-through Mode)

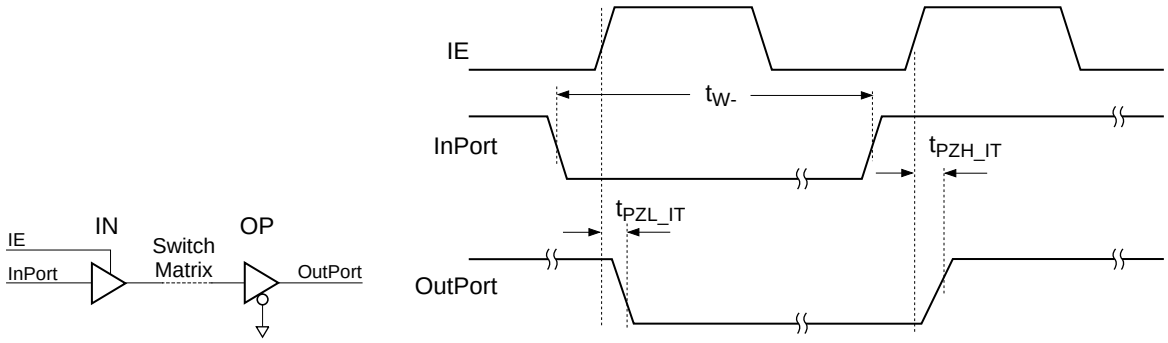


Figure 12 Input Enable Timing (Flow-through Mode)

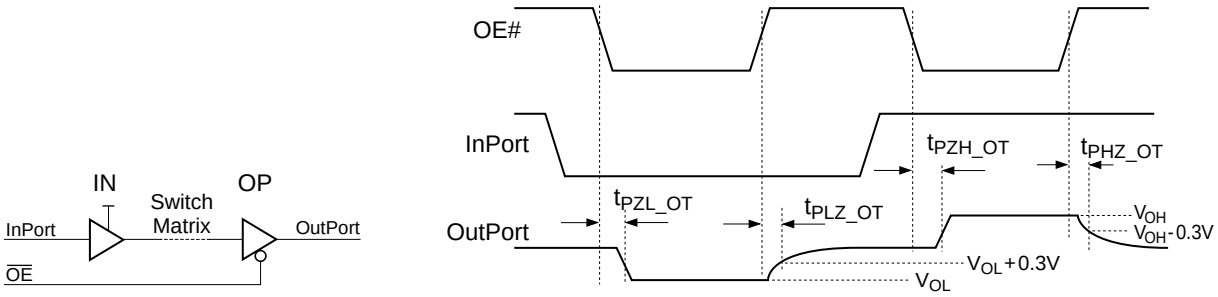


Figure 13 Output Enable Timing

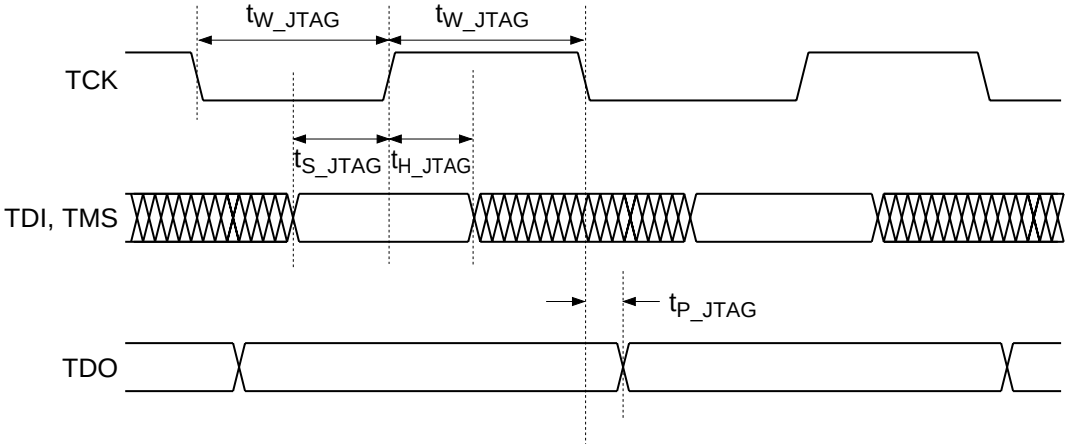


Figure 14 JTAG Timing

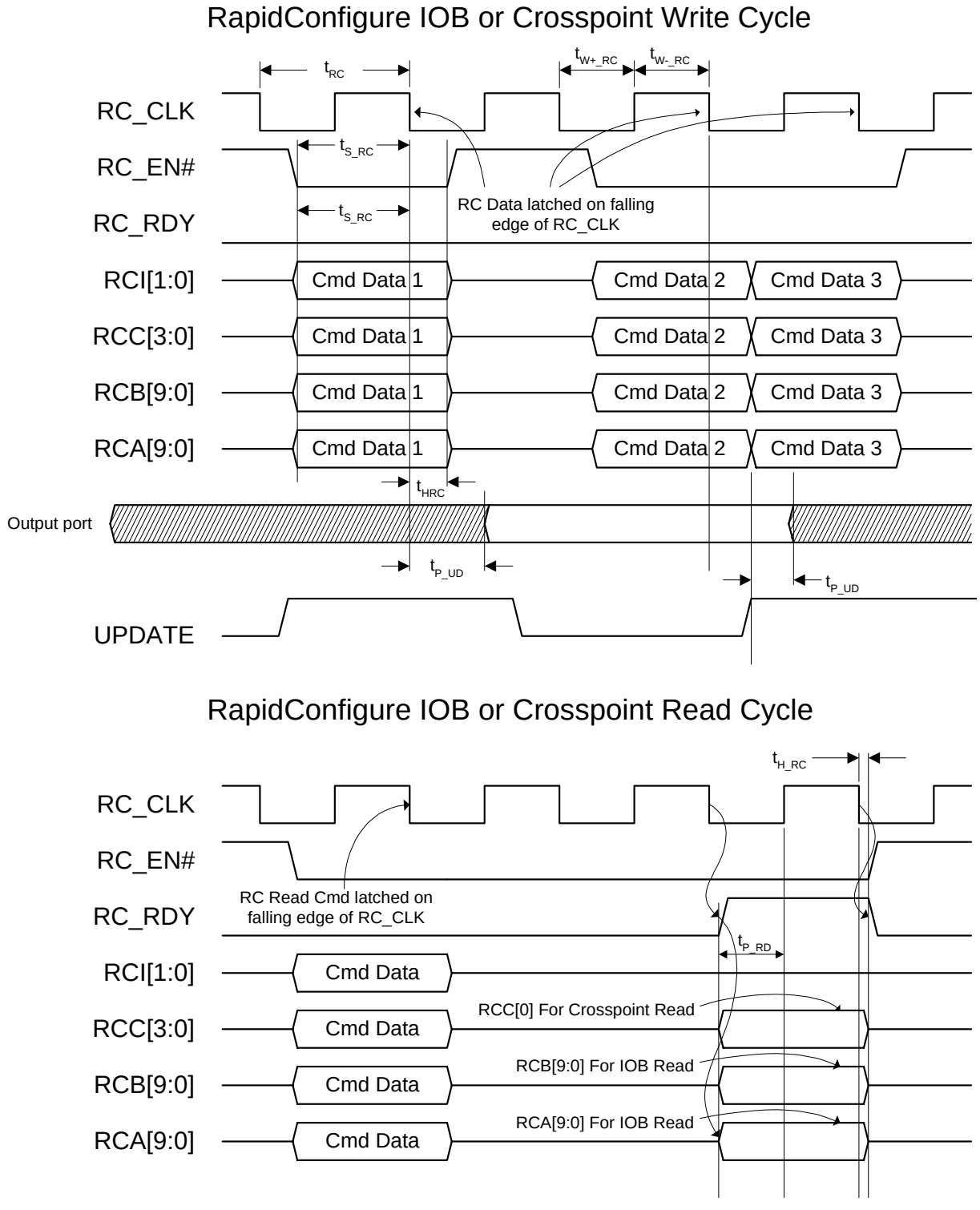


Figure 15 RapidConfigure IOB or Crosspoint Read and Write Cycles

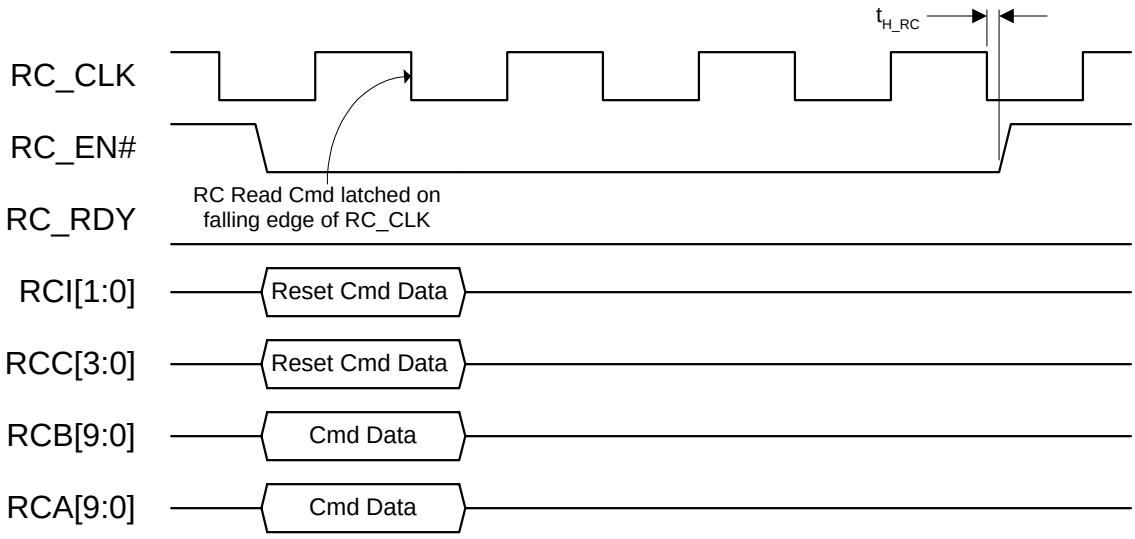
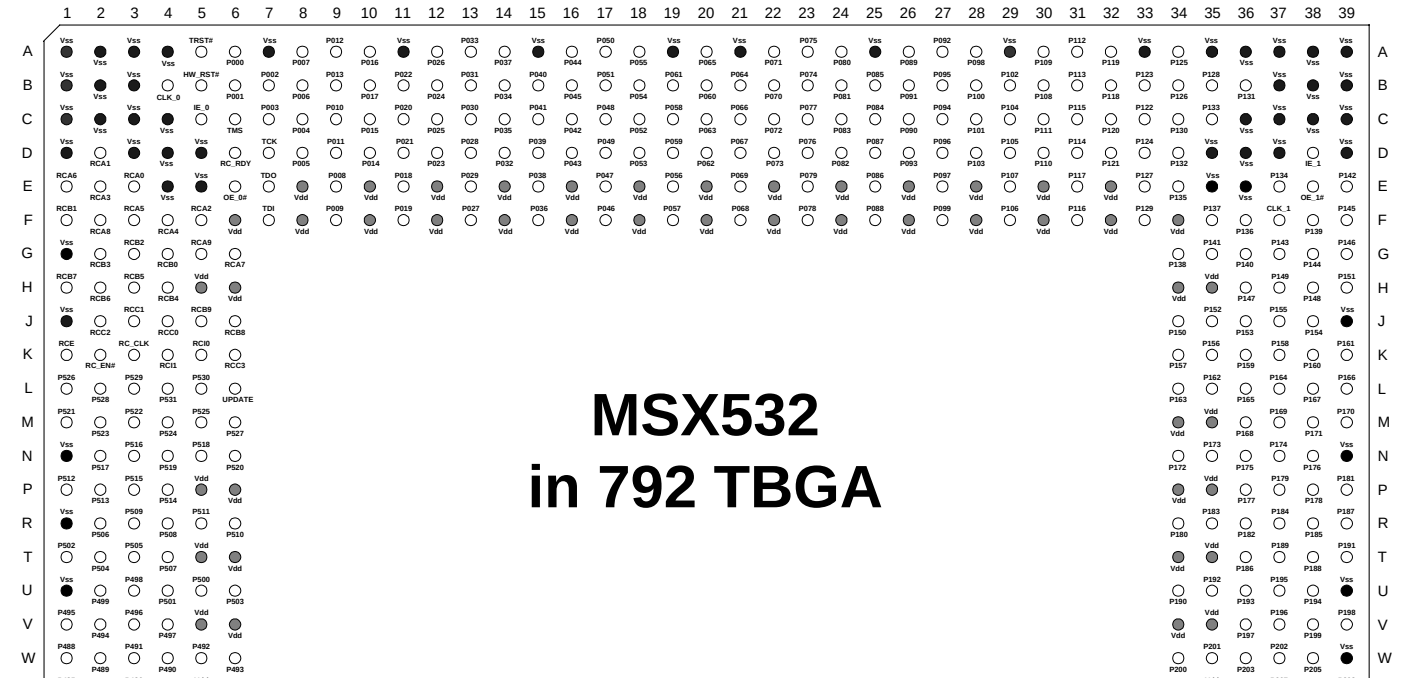


Figure 16 RapidConfigure Reset Command Cycle

4. Package and Pinout

4.1 MSX532 [792 TBGA Package] Pinout



4.2 MSX532 [792 TBGA Package] Pinout: By Ball Sequence

Table 15 MSX532 Pinout By Ball Sequence

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
A1	Vss	B1	Vss	C1	Vss	D1	Vss	E1	RCA6	F1	RCB1
A2	Vss	B2	Vss	C2	Vss	D2	RCA1	E2	RCA3	F2	RCA8
A3	Vss	B3	Vss	C3	Vss	D3	Vss	E3	RCA0	F3	RCA5
A4	Vss	B4	CLK_0	C4	Vss	D4	Vss	E4	Vss	F4	RCA4
A5	TRST#	B5	HW_RST#	C5	IE_0	D5	Vss	E5	Vss	F5	RCA2
A6	P000	B6	P001	C6	TMS	D6	RC_RDY	E6	OE_0#	F6	VDD
A7	Vss	B7	P002	C7	P003	D7	TCK	E7	TDO	F7	TDI
A8	P007	B8	P006	C8	P004	D8	P005	E8	V_{DD}	F8	V_{DD}
A9	P012	B9	P013	C9	P010	D9	P011	E9	P008	F9	P009
A10	P016	B10	P017	C10	P015	D10	P014	E10	V_{DD}	F10	V_{DD}
A11	Vss	B11	P022	C11	P020	D11	P021	E11	P018	F11	P019
A12	P026	B12	P024	C12	P025	D12	P023	E12	VDD	F12	V_{DD}
A13	P033	B13	P031	C13	P030	D13	P028	E13	P029	F13	P027
A14	P037	B14	P034	C14	P035	D14	P032	E14	V_{DD}	F14	V_{DD}
A15	Vss	B15	P040	C15	P041	D15	P039	E15	P038	F15	P036
A16	P044	B16	P045	C16	P042	D16	P043	E16	VDD	F16	V_{DD}
A17	P050	B17	P051	C17	P048	D17	P049	E17	P047	F17	P046
A18	P055	B18	P054	C18	P052	D18	P053	E18	V_{DD}	F18	V_{DD}
A19	Vss	B19	P061	C19	P058	D19	P059	E19	P056	F19	P057
A20	P065	B20	P060	C20	P063	D20	P062	E20	V_{DD}	F20	V_{DD}
A21	Vss	B21	P064	C21	P066	D21	P067	E21	P069	F21	P068
A22	P071	B22	P070	C22	P072	D22	P073	E22	V_{DD}	F22	V_{DD}
A23	P075	B23	P074	C23	P077	D23	P076	E23	P079	F23	P078
A24	P080	B24	P081	C24	P083	D24	P082	E24	V_{DD}	F24	V_{DD}
A25	Vss	B25	P085	C25	P084	D25	P087	E25	P086	F25	P088
A26	P089	B26	P091	C26	P090	D26	P093	E26	V_{DD}	F26	V_{DD}
A27	P092	B27	P095	C27	P094	D27	P096	E27	P097	F27	P099
A28	P098	B28	P100	C28	P101	D28	P103	E28	V_{DD}	F28	V_{DD}
A29	Vss	B29	P102	C29	P104	D29	P105	E29	P107	F29	P106
A30	P109	B30	P108	C30	P111	D30	P110	E30	V_{DD}	F30	V_{DD}
A31	P112	B31	P113	C31	P115	D31	P114	E31	P117	F31	P116
A32	P119	B32	P118	C32	P120	D32	P121	E32	V_{DD}	F32	V_{DD}
A33	Vss	B33	P123	C33	P122	D33	P124	E33	P127	F33	P129
A34	P125	B34	P126	C34	P130	D34	P132	E34	P135	F34	V_{DD}
A35	Vss	B35	P128	C35	P133	D35	Vss	E35	Vss	F35	P137
A36	Vss	B36	P131	C36	Vss	D36	Vss	E36	Vss	F36	P136
A37	Vss	B37	Vss	C37	Vss	D37	Vss	E37	P134	F37	CLK_1
A38	Vss	B38	Vss	C38	Vss	D38	IE_1	E38	OE_1#	F38	P139
A39	Vss	B39	Vss	C39	Vss	D39	Vss	E39	P142	F39	P145

Table 15 MSX532 Pinout By Ball Sequence *(Continued)*

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
G1	Vss	H1	RCB7	J1	Vss	K1	RCE	L1	P526	M1	P521
G2	RCB3	H2	RCB6	J2	RCC2	K2	RC_EN#	L2	P528	M2	P523
G3	RCB2	H3	RCB5	J3	RCC1	K3	RC_CLK	L3	P529	M3	P522
G4	RCB0	H4	RCB4	J4	RCC0	K4	RCI1	L4	P531	M4	P524
G5	RCA9	H5	V_{DD}	J5	RCB9	K5	RCI0	L5	P530	M5	P525
G6	RCA7	H6	V_{DD}	J6	RCB8	K6	RCC3	L6	UPDATE	M6	P527
G34	P138	H34	V_{DD}	J34	P150	K34	P157	L34	P163	M34	V_{DD}
G35	P141	H35	V_{DD}	J35	P152	K35	P156	L35	P162	M35	V_{DD}
G36	P140	H36	P147	J36	P153	K36	P159	L36	P165	M36	P168
G37	P143	H37	P149	J37	P155	K37	P158	L37	P164	M37	P169
G38	P144	H38	P148	J38	P154	K38	P160	L38	P167	M38	P171
G39	P146	H39	P151	J39	Vss	K39	P161	L39	P166	M39	P170

N1	Vss	P1	P512	R1	Vss	T1	P502	U1	Vss	V1	P495
N2	P517	P2	P513	R2	P506	T2	P504	U2	P499	V2	P494
N3	P516	P3	P515	R3	P509	T3	P505	U3	P498	V3	P496
N4	P519	P4	P514	R4	P508	T4	P507	U4	P501	V4	P497
N5	P518	P5	V_{DD}	R5	P511	T5	V_{DD}	U5	P500	V5	V_{DD}
N6	P520	P6	V_{DD}	R6	P510	T6	V_{DD}	U6	P503	V6	V_{DD}
N34	P172	P34	V_{DD}	R34	P180	T34	V_{DD}	U34	P190	V34	V_{DD}
N35	P173	P35	V_{DD}	R35	P183	T35	V_{DD}	U35	P192	V35	V_{DD}
N36	P175	P36	P177	R36	P182	T36	P186	U36	P193	V36	P197
N37	P174	P37	P179	R37	P184	T37	P189	U37	P195	V37	P196
N38	P176	P38	P178	R38	P185	T38	P188	U38	P194	V38	P199
N39	Vss	P39	P181	R39	P187	T39	P191	U39	Vss	V39	P198

W1	P488	Y1	P485	AA1	Vss	AB1	P479	AC1	P475	AD1	P468
W2	P489	Y2	P484	AA2	P482	AB2	P476	AC2	P473	AD2	P466
W3	P491	Y3	P486	AA3	P478	AB3	P477	AC3	P472	AD3	P467
W4	P490	Y4	P487	AA4	P483	AB4	P474	AC4	P470	AD4	P465
W5	P492	Y5	V_{DD}	AA5	P481	AB5	V_{DD}	AC5	P471	AD5	V_{DD}
W6	P493	Y6	V_{DD}	AA6	P480	AB6	V_{DD}	AC6	P469	AD6	V_{DD}
W34	P200	Y34	V_{DD}	AA34	P213	AB34	V_{DD}	AC34	P223	AD34	V_{DD}
W35	P201	Y35	V_{DD}	AA35	P212	AB35	V_{DD}	AC35	P220	AD35	V_{DD}
W36	P203	Y36	P206	AA36	P210	AB36	P217	AC36	P221	AD36	P227
W37	P202	Y37	P207	AA37	P211	AB37	P216	AC37	P218	AD37	P225
W38	P205	Y38	P204	AA38	P209	AB38	P214	AC38	P219	AD38	P224
W39	Vss	Y39	P208	AA39	Vss	AB39	P215	AC39	Vss	AD39	P222

Table 15 MSX532 Pinout By Ball Sequence *(Continued)*

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
AE1	Vss	AF1	P458	AG1	P450	AH1	P451	AJ1	P443	AK1	P441
AE2	P464	AF2	P459	AG2	P454	AH2	P449	AJ2	P447	AK2	P440
AE3	P462	AF3	P457	AG3	P455	AH3	P448	AJ3	P444	AK3	P438
AE4	P463	AF4	P456	AG4	P452	AH4	P446	AJ4	P445	AK4	P439
AE5	P460	AF5	V_{DD}	AG5	P453	AH5	V_{DD}	AJ5	P442	AK5	V_{DD}
AE6	P461	AF6	V_{DD}	AG6	Vss	AH6	V_{DD}	AJ6	Vss	AK6	V_{DD}
AE34	P230	AF34	V_{DD}	AG34	P240	AH34	V_{DD}	AJ34	P249	AK34	V_{DD}
AE35	P231	AF35	V_{DD}	AG35	P238	AH35	V_{DD}	AJ35	P248	AK35	V_{DD}
AE36	P228	AF36	P234	AG36	P239	AH36	P245	AJ36	P246	AK36	P253
AE37	P229	AF37	P235	AG37	P236	AH37	P242	AJ37	P247	AK37	P252
AE38	P226	AF38	P233	AG38	P237	AH38	P243	AJ38	P244	AK38	P250
AE39	Vss	AF39	P232	AG39	Vss	AH39	P241	AJ39	Vss	AK39	P251

AL1	P433	AM1	P432	AN1	Vss
AL2	P436	AM2	P430	AN2	P429
AL3	P437	AM3	P431	AN3	P426
AL4	P434	AM4	P428	AN4	P427
AL5	P435	AM5	V_{DD}	AN5	P425
AL6	Vss	AM6	V_{DD}	AN6	P423
AL34	P258	AM34	V_{DD}	AN34	P271
AL35	P259	AM35	V_{DD}	AN35	P268
AL36	P257	AM36	P262	AN36	P269
AL37	P256	AM37	P263	AN37	P267
AL38	P254	AM38	P260	AN38	P264
AL39	P255	AM39	P261	AN39	Vss

Table 15 MSX532 Pinout By Ball Sequence *(Continued)*

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
AP1	P424	AR1	Vss	AT1	Vss	AU1	Vss	AV1	Vss	AW1	Vss
AP2	P422	AR2	P421	AT2	OE_3#	AU2	Vss	AV2	Vss	AW2	Vss
AP3	P420	AR3	P418	AT3	Vss	AU3	Vss	AV3	Vss	AW3	Vss
AP4	P419	AR4	Vss	AT4	Vss	AU4	Vss	AV4	CLK_3	AW4	Vss
AP5	V_{DD}	AR5	Vss	AT5	Vss	AU5	P417	AV5	P415	AW5	P410
AP6	V_{DD}	AR6	IE_3	AT6	P416	AU6	P414	AV6	P412	AW6	P407
AP7	P413	AR7	P411	AT7	P409	AU7	P408	AV7	P406	AW7	Vss
AP8	P404	AR8	P405	AT8	P402	AU8	P403	AV8	P401	AW8	P400
AP9	P398	AR9	P399	AT9	P396	AU9	P397	AV9	P394	AW9	Vss
AP10	V_{DD}	AR10	V_{DD}	AT10	P395	AU10	P393	AV10	P392	AW10	P390
AP11	P391	AR11	P389	AT11	P388	AU11	P386	AV11	Vss	AW11	P387
AP12	V_{DD}	AR12	V_{DD}	AT12	P385	AU12	P384	AV12	P382	AW12	P383
AP13	P380	AR13	P381	AT13	P378	AU13	P379	AV13	P377	AW13	Vss
AP14	V_{DD}	AR14	V_{DD}	AT14	P376	AU14	P374	AV14	P375	AW14	P372
AP15	P373	AR15	P370	AT15	P371	AU15	P369	AV15	P368	AW15	P366
AP16	V_{DD}	AR16	V_{DD}	AT16	P367	AU16	P364	AV16	P365	AW16	P362
AP17	P363	AR17	P361	AT17	P360	AU17	P358	AV17	P359	AW17	Vss
AP18	V_{DD}	AR18	V_{DD}	AT18	P357	AU18	P356	AV18	P354	AW18	P355
AP19	P353	AR19	P352	AT19	P350	AU19	P351	AV19	P348	AW19	Vss
AP20	V_{DD}	AR20	V_{DD}	AT20	P346	AU20	P347	AV20	P349	AW20	P345
AP21	P341	AR21	P340	AT21	P343	AU21	P342	AV21	P344	AW21	Vss
AP22	V_{DD}	AR22	V_{DD}	AT22	P336	AU22	P337	AV22	P339	AW22	P338
AP23	P331	AR23	P330	AT23	P332	AU23	P333	AV23	P335	AW23	P334
AP24	V_{DD}	AR24	V_{DD}	AT24	P327	AU24	P326	AV24	P328	AW24	P329
AP25	P321	AR25	P323	AT25	P322	AU25	P325	AV25	P324	AW25	Vss
AP26	V_{DD}	AR26	V_{DD}	AT26	P316	AU26	P319	AV26	P318	AW26	P320
AP27	P310	AR27	P312	AT27	P313	AU27	P315	AV27	P314	AW27	P317
AP28	V_{DD}	AR28	V_{DD}	AT28	P306	AU28	P309	AV28	P308	AW28	P311
AP29	P303	AR29	P302	AT29	P304	AU29	P305	AV29	P307	AW29	Vss
AP30	P296	AR30	P297	AT30	P299	AU30	P298	AV30	P301	AW30	P300
AP31	P290	AR31	P293	AT31	P292	AU31	P295	AV31	P294	AW31	Vss
AP32	V_{DD}	AR32	V_{DD}	AT32	P286	AU32	P289	AV32	P288	AW32	P291
AP33	IE_2	AR33	P283	AT33	P282	AU33	P285	AV33	P287	AW33	Vss
AP34	V_{DD}	AR34	P279	AT34	P281	AU34	P280	AV34	OE_2#	AW34	P284
AP35	V_{DD}	AR35	Vss	AT35	Vss	AU35	P276	AV35	P278	AW35	CLK_2
AP36	P274	AR36	Vss	AT36	Vss	AU36	Vss	AV36	Vss	AW36	Vss
AP37	P272	AR37	P277	AT37	Vss	AU37	Vss	AV37	Vss	AW37	Vss
AP38	P270	AR38	P273	AT38	P275	AU38	Vss	AV38	Vss	AW38	Vss
AP39	P265	AR39	P266	AT39	Vss	AU39	Vss	AV39	Vss	AW39	Vss

4.3 MSX532 [792 TBGA Package] Pinout: By Ball Name (alphabetically)

Table 16 MSX532 Pinout By Ball Name

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
CLK_0	B4	P027	F13	P067	D21	P107	E29	P147	H36
CLK_1	F37	P028	D13	P068	F21	P108	B30	P148	H38
CLK_2	AW35	P029	E13	P069	E21	P109	A30	P149	H37
CLK_3	AV4	P030	C13	P070	B22	P110	D30	P150	J34
HW_RST#	B5	P031	B13	P071	A22	P111	C30	P151	H39
IE_0	C5	P032	D14	P072	C22	P112	A31	P152	J35
IE_1	D38	P033	A13	P073	D22	P113	B31	P153	J36
IE_2	AP33	P034	B14	P074	B23	P114	D31	P154	J38
IE_3	AR6	P035	C14	P075	A23	P115	C31	P155	J37
OE_0#	E6	P036	F15	P076	D23	P116	F31	P156	K35
OE_1#	E38	P037	A14	P077	C23	P117	E31	P157	K34
OE_2#	AV34	P038	E15	P078	F23	P118	B32	P158	K37
OE_3#	AT2	P039	D15	P079	E23	P119	A32	P159	K36
P000	A6	P040	B15	P080	A24	P120	C32	P160	K38
P001	B6	P041	C15	P081	B24	P121	D32	P161	K39
P002	B7	P042	C16	P082	D24	P122	C33	P162	L35
P003	C7	P043	D16	P083	C24	P123	B33	P163	L34
P004	C8	P044	A16	P084	C25	P124	D33	P164	L37
P005	D8	P045	B16	P085	B25	P125	A34	P165	L36
P006	B8	P046	F17	P086	E25	P126	B34	P166	L39
P007	A8	P047	E17	P087	D25	P127	E33	P167	L38
P008	E9	P048	C17	P088	F25	P128	B35	P168	M36
P009	F9	P049	D17	P089	A26	P129	F33	P169	M37
P010	C9	P050	A17	P090	C26	P130	C34	P170	M39
P011	D9	P051	B17	P091	B26	P131	B36	P171	M38
P012	A9	P052	C18	P092	A27	P132	D34	P172	N34
P013	B9	P053	D18	P093	D26	P133	C35	P173	N35
P014	D10	P054	B18	P094	C27	P134	E37	P174	N37
P015	C10	P055	A18	P095	B27	P135	E34	P175	N36
P016	A10	P056	E19	P096	D27	P136	F36	P176	N38
P017	B10	P057	F19	P097	E27	P137	F35	P177	P36
P018	E11	P058	C19	P098	A28	P138	G34	P178	P38
P019	F11	P059	D19	P099	F27	P139	F38	P179	P37
P020	C11	P060	B20	P100	B28	P140	G36	P180	R34
P021	D11	P061	B19	P101	C28	P141	G35	P181	P39
P022	B11	P062	D20	P102	B29	P142	E39	P182	R36
P023	D12	P063	C20	P103	D28	P143	G37	P183	R35
P024	B12	P064	B21	P104	C29	P144	G38	P184	R37
P025	C12	P065	A20	P105	D29	P145	F39	P185	R38
P026	A12	P066	C21	P106	F29	P146	G39	P186	T36

Table 16 MSX532 Pinout By Ball Name *(Continued)*

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
P187	R39	P227	AD36	P267	AN37	P307	AV29	P347	AU20
P188	T38	P228	AE36	P268	AN35	P308	AV28	P348	AV19
P189	T37	P229	AE37	P269	AN36	P309	AU28	P349	AV20
P190	U34	P230	AE34	P270	AP38	P310	AP27	P350	AT19
P191	T39	P231	AE35	P271	AN34	P311	AW28	P351	AU19
P192	U35	P232	AF39	P272	AP37	P312	AR27	P352	AR19
P193	U36	P233	AF38	P273	AR38	P313	AT27	P353	AP19
P194	U38	P234	AF36	P274	AP36	P314	AV27	P354	AV18
P195	U37	P235	AF37	P275	AT38	P315	AU27	P355	AW18
P196	V37	P236	AG37	P276	AU35	P316	AT26	P356	AU18
P197	V36	P237	AG38	P277	AR37	P317	AW27	P357	AT18
P198	V39	P238	AG35	P278	AV35	P318	AV26	P358	AU17
P199	V38	P239	AG36	P279	AR34	P319	AU26	P359	AV17
P200	W34	P240	AG34	P280	AU34	P320	AW26	P360	AT17
P201	W35	P241	AH39	P281	AT34	P321	AP25	P361	AR17
P202	W37	P242	AH37	P282	AT33	P322	AT25	P362	AW16
P203	W36	P243	AH38	P283	AR33	P323	AR25	P363	AP17
P204	Y38	P244	AJ38	P284	AW34	P324	AV25	P364	AU16
P205	W38	P245	AH36	P285	AU33	P325	AU25	P365	AV16
P206	Y36	P246	AJ36	P286	AT32	P326	AU24	P366	AW15
P207	Y37	P247	AJ37	P287	AV33	P327	AT24	P367	AT16
P208	Y39	P248	AJ35	P288	AV32	P328	AV24	P368	AV15
P209	AA38	P249	AJ34	P289	AU32	P329	AW24	P369	AU15
P210	AA36	P250	AK38	P290	AP31	P330	AR23	P370	AR15
P211	AA37	P251	AK39	P291	AW32	P331	AP23	P371	AT15
P212	AA35	P252	AK37	P292	AT31	P332	AT23	P372	AW14
P213	AA34	P253	AK36	P293	AR31	P333	AU23	P373	AP15
P214	AB38	P254	AL38	P294	AV31	P334	AW23	P374	AU14
P215	AB39	P255	AL39	P295	AU31	P335	AV23	P375	AV14
P216	AB37	P256	AL37	P296	AP30	P336	AT22	P376	AT14
P217	AB36	P257	AL36	P297	AR30	P337	AU22	P377	AV13
P218	AC37	P258	AL34	P298	AU30	P338	AW22	P378	AT13
P219	AC38	P259	AL35	P299	AT30	P339	AV22	P379	AU13
P220	AC35	P260	AM38	P300	AW30	P340	AR21	P380	AP13
P221	AC36	P261	AM39	P301	AV30	P341	AP21	P381	AR13
P222	AD39	P262	AM36	P302	AR29	P342	AU21	P382	AV12
P223	AC34	P263	AM37	P303	AP29	P343	AT21	P383	AW12
P224	AD38	P264	AN38	P304	AT29	P344	AV21	P384	AU12
P225	AD37	P265	AP39	P305	AU29	P345	AW20	P385	AT12
P226	AE38	P266	AR39	P306	AT28	P346	AT20	P386	AU11

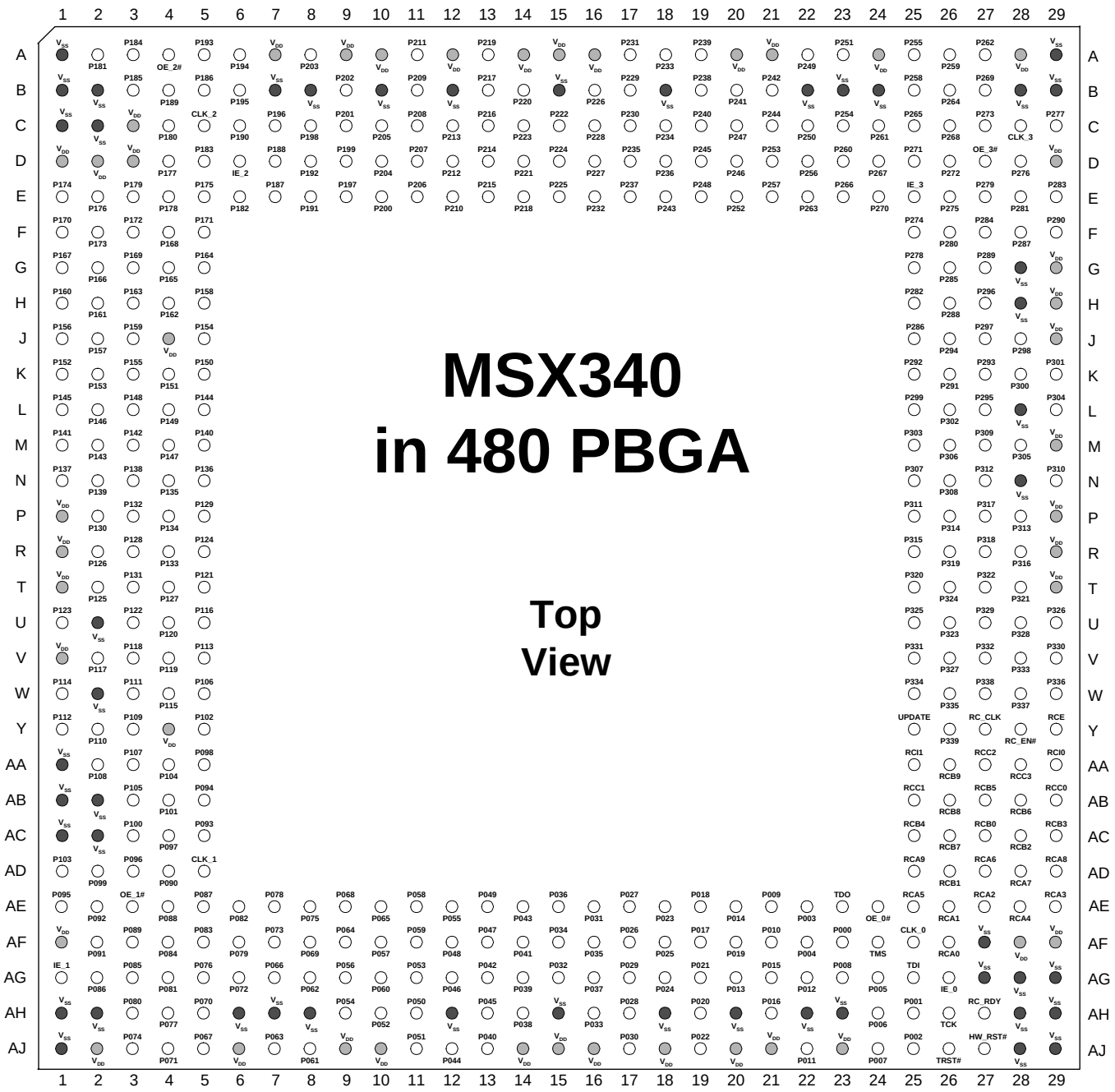
Table 16 MSX532 Pinout By Ball Name *(Continued)*

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
P387	AW11	P427	AN4	P467	AD3	P507	T4	RCB3	G2
P388	AT11	P428	AM4	P468	AD1	P508	R4	RCB4	H4
P389	AR11	P429	AN2	P469	AC6	P509	R3	RCB5	H3
P390	AW10	P430	AM2	P470	AC4	P510	R6	RCB6	H2
P391	AP11	P431	AM3	P471	AC5	P511	R5	RCB7	H1
P392	AV10	P432	AM1	P472	AC3	P512	P1	RCB8	J6
P393	AU10	P433	AL1	P473	AC2	P513	P2	RCB9	J5
P394	AV9	P434	AL4	P474	AB4	P514	P4	RCC0	J4
P395	AT10	P435	AL5	P475	AC1	P515	P3	RCC1	J3
P396	AT9	P436	AL2	P476	AB2	P516	N3	RCC2	J2
P397	AU9	P437	AL3	P477	AB3	P517	N2	RCC3	K6
P398	AP9	P438	AK3	P478	AA3	P518	N5	RCE	K1
P399	AR9	P439	AK4	P479	AB1	P519	N4	RCI0	K5
P400	AW8	P440	AK2	P480	AA6	P520	N6	RCI1	K4
P401	AV8	P441	AK1	P481	AA5	P521	M1	RC_RDY	D6
P402	AT8	P442	AJ5	P482	AA2	P522	M3	TCK	D7
P403	AU8	P443	AJ1	P483	AA4	P523	M2	TDI	F7
P404	AP8	P444	AJ3	P484	Y2	P524	M4	TDO	E7
P405	AR8	P445	AJ4	P485	Y1	P525	M5	TMS	C6
P406	AV7	P446	AH4	P486	Y3	P526	L1	TRST#	A5
P407	AW6	P447	AJ2	P487	Y4	P527	M6	UPDATE	L6
P408	AU7	P448	AH3	P488	W1	P528	L2	V_{DD}	E8
P409	AT7	P449	AH2	P489	W2	P529	L3	V_{DD}	E10
P410	AW5	P450	AG1	P490	W4	P530	L5	V_{DD}	E12
P411	AR7	P451	AH1	P491	W3	P531	L4	V_{DD}	E14
P412	AV6	P452	AG4	P492	W5	RC_CLK	K3	V_{DD}	E16
P413	AP7	P453	AG5	P493	W6	RC_EN#	K2	V_{DD}	E18
P414	AU6	P454	AG2	P494	V2	RCA0	E3	V_{DD}	E20
P415	AV5	P455	AG3	P495	V1	RCA1	D2	V_{DD}	E22
P416	AT6	P456	AF4	P496	V3	RCA2	F5	V_{DD}	E24
P417	AU5	P457	AF3	P497	V4	RCA3	E2	V_{DD}	E26
P418	AR3	P458	AF1	P498	U3	RCA4	F4	V_{DD}	E28
P419	AP4	P459	AF2	P499	U2	RCA5	F3	V_{DD}	E30
P420	AP3	P460	AE5	P500	U5	RCA6	E1	V_{DD}	E32
P421	AR2	P461	AE6	P501	U4	RCA7	G6	V_{DD}	F6
P422	AP2	P462	AE3	P502	T1	RCA8	F2	V_{DD}	F8
P423	AN6	P463	AE4	P503	U6	RCA9	G5	V_{DD}	F10
P424	AP1	P464	AE2	P504	T2	RCB0	G4	V_{DD}	F12
P425	AN5	P465	AD4	P505	T3	RCB1	F1	V_{DD}	F14
P426	AN3	P466	AD2	P506	R2	RCB2	G3	V_{DD}	F16

Table 16 MSX532 Pinout By Ball Name *(Continued)*

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
V_{DD}	F18	V_{DD}	AF6	V_{DD}	AR32	V_{SS}	E4	V_{SS}	AU3
V_{DD}	F20	V_{DD}	AF34	V_{SS}	A1	V_{SS}	E5	V_{SS}	AU4
V_{DD}	F22	V_{DD}	AF35	V_{SS}	A2	V_{SS}	E35	V_{SS}	AU36
V_{DD}	F24	V_{DD}	AH5	V_{SS}	A3	V_{SS}	E36	V_{SS}	AU37
V_{DD}	F26	V_{DD}	AH6	V_{SS}	A4	V_{SS}	G1	V_{SS}	AU38
V_{DD}	F28	V_{DD}	AH34	V_{SS}	A7	V_{SS}	J1	V_{SS}	AU39
V_{DD}	F30	V_{DD}	AH35	V_{SS}	A11	V_{SS}	J39	V_{SS}	AV1
V_{DD}	F32	V_{DD}	AK5	V_{SS}	A15	V_{SS}	N1	V_{SS}	AV2
V_{DD}	F34	V_{DD}	AK6	V_{SS}	A19	V_{SS}	N39	V_{SS}	AV3
V_{DD}	H5	V_{DD}	AK34	V_{SS}	A21	V_{SS}	R1	V_{SS}	AV11
V_{DD}	H6	V_{DD}	AK35	V_{SS}	A25	V_{SS}	U1	V_{SS}	AV36
V_{DD}	H34	V_{DD}	AM5	V_{SS}	A29	V_{SS}	U39	V_{SS}	AV37
V_{DD}	H35	V_{DD}	AM6	V_{SS}	A33	V_{SS}	W39	V_{SS}	AV38
V_{DD}	M34	V_{DD}	AM34	V_{SS}	A35	V_{SS}	AA1	V_{SS}	AV39
V_{DD}	M35	V_{DD}	AM35	V_{SS}	A36	V_{SS}	AA39	V_{SS}	AW1
V_{DD}	P5	V_{DD}	AP5	V_{SS}	A37	V_{SS}	AC39	V_{SS}	AW2
V_{DD}	P6	V_{DD}	AP6	V_{SS}	A38	V_{SS}	AE1	V_{SS}	AW3
V_{DD}	P34	V_{DD}	AP10	V_{SS}	A39	V_{SS}	AE39	V_{SS}	AW4
V_{DD}	P35	V_{DD}	AP12	V_{SS}	B1	V_{SS}	AG6	V_{SS}	AW7
V_{DD}	T5	V_{DD}	AP14	V_{SS}	B2	V_{SS}	AG39	V_{SS}	AW9
V_{DD}	T6	V_{DD}	AP16	V_{SS}	B3	V_{SS}	AJ6	V_{SS}	AW13
V_{DD}	T34	V_{DD}	AP18	V_{SS}	B37	V_{SS}	AJ39	V_{SS}	AW17
V_{DD}	T35	V_{DD}	AP20	V_{SS}	B38	V_{SS}	AL6	V_{SS}	AW19
V_{DD}	V5	V_{DD}	AP22	V_{SS}	B39	V_{SS}	AN1	V_{SS}	AW21
V_{DD}	V6	V_{DD}	AP24	V_{SS}	C1	V_{SS}	AN39	V_{SS}	AW25
V_{DD}	V34	V_{DD}	AP26	V_{SS}	C2	V_{SS}	AR1	V_{SS}	AW29
V_{DD}	V35	V_{DD}	AP28	V_{SS}	C3	V_{SS}	AR4	V_{SS}	AW31
V_{DD}	Y5	V_{DD}	AP32	V_{SS}	C4	V_{SS}	AR5	V_{SS}	AW33
V_{DD}	Y6	V_{DD}	AP34	V_{SS}	C36	V_{SS}	AR35	V_{SS}	AW36
V_{DD}	Y34	V_{DD}	AP35	V_{SS}	C37	V_{SS}	AR36	V_{SS}	AW37
V_{DD}	Y35	V_{DD}	AR10	V_{SS}	C38	V_{SS}	AT1	V_{SS}	AW38
V_{DD}	AB5	V_{DD}	AR12	V_{SS}	C39	V_{SS}	AT3	V_{SS}	AW39
V_{DD}	AB6	V_{DD}	AR14	V_{SS}	D1	V_{SS}	AT4		
V_{DD}	AB34	V_{DD}	AR16	V_{SS}	D3	V_{SS}	AT5		
V_{DD}	AB35	V_{DD}	AR18	V_{SS}	D4	V_{SS}	AT35		
V_{DD}	AD5	V_{DD}	AR20	V_{SS}	D5	V_{SS}	AT36		
V_{DD}	AD6	V_{DD}	AR22	V_{SS}	D35	V_{SS}	AT37		
V_{DD}	AD34	V_{DD}	AR24	V_{SS}	D36	V_{SS}	AT39		
V_{DD}	AD35	V_{DD}	AR26	V_{SS}	D37	V_{SS}	AU1		
V_{DD}	AF5	V_{DD}	AR28	V_{SS}	D39	V_{SS}	AU2		

4.4 MSX340 [480 PBGA Package] Pinout



4.5 MSX340 [480 PBGA Package] Pinout: By Ball Sequence

Table 17 MSX340 Pinout By Ball Sequence

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
A1	V_{SS}	B1	V_{SS}	C1	V_{SS}	D1	V_{DD}	E1	P174
A2	P181	B2	V_{SS}	C2	V_{SS}	D2	V_{DD}	E2	P176
A3	P184	B3	P185	C3	V_{DD}	D3	V_{DD}	E3	P179
A4	OE_2#	B4	P189	C4	P180	D4	P177	E4	P178
A5	P193	B5	P186	C5	CLK_2	D5	P183	E5	P175
A6	P194	B6	P195	C6	P190	D6	IE_2	E6	P182
A7	V_{DD}	B7	V_{SS}	C7	P196	D7	P188	E7	P187
A8	P203	B8	V_{SS}	C8	P198	D8	P192	E8	P191
A9	V_{DD}	B9	P202	C9	P201	D9	P199	E9	P197
A10	V_{DD}	B10	V_{SS}	C10	P205	D10	P204	E10	P200
A11	P211	B11	P209	C11	P208	D11	P207	E11	P206
A12	V_{DD}	B12	V_{SS}	C12	P213	D12	P212	E12	P210
A13	P219	B13	P217	C13	P216	D13	P214	E13	P215
A14	V_{DD}	B14	P220	C14	P223	D14	P221	E14	P218
A15	V_{DD}	B15	V_{SS}	C15	P222	D15	P224	E15	P225
A16	V_{DD}	B16	P226	C16	P228	D16	P227	E16	P232
A17	P231	B17	P229	C17	P230	D17	P235	E17	P237
A18	P233	B18	V_{SS}	C18	P234	D18	P236	E18	P243
A19	P239	B19	P238	C19	P240	D19	P245	E19	P248
A20	V_{DD}	B20	P241	C20	P247	D20	P246	E20	P252
A21	V_{DD}	B21	P242	C21	P244	D21	P253	E21	P257
A22	P249	B22	V_{SS}	C22	P250	D22	P256	E22	P263
A23	P251	B23	V_{SS}	C23	P254	D23	P260	E23	P266
A24	V_{DD}	B24	V_{SS}	C24	P261	D24	P267	E24	P270
A25	P255	B25	P258	C25	P265	D25	P271	E25	IE_3
A26	P259	B26	P264	C26	P268	D26	P272	E26	P275
A27	P262	B27	P269	C27	P273	D27	OE_3#	E27	P279
A28	V_{DD}	B28	V_{SS}	C28	CLK_3	D28	P276	E28	P281
A29	V_{SS}	B29	V_{SS}	C29	P277	D29	V_{DD}	E29	P283

Table 17 MSX340 Pinout By Ball Sequence *(Continued)*

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
F1	P170	G1	P167	H1	P160	J1	P156	K1	P152
F2	P173	G2	P166	H2	P161	J2	P157	K2	P153
F3	P172	G3	P169	H3	P163	J3	P159	K3	P155
F4	P168	G4	P165	H4	P162	J4	V_{DD}	K4	P151
F5	P171	G5	P164	H5	P158	J5	P154	K5	P150
F25	P274	G25	P278	H25	P282	J25	P286	K25	P292
F26	P280	G26	P285	H26	P288	J26	P294	K26	P291
F27	P284	G27	P289	H27	P296	J27	P297	K27	P293
F28	P287	G28	V_{SS}	H28	V_{SS}	J28	P298	K28	P300
F29	P290	G29	V_{DD}	H29	V_{DD}	J29	V_{DD}	K29	P301
L1	P145	M1	P141	N1	P137	P1	V_{DD}	R1	V_{DD}
L2	P146	M2	P143	N2	P139	P2	P130	R2	P126
L3	P148	M3	P142	N3	P138	P3	P132	R3	P128
L4	P149	M4	P147	N4	P135	P4	P134	R4	P133
L5	P144	M5	P140	N5	P136	P5	P129	R5	P124
L25	P299	M25	P303	N25	P307	P25	P311	R25	P315
L26	P302	M26	P306	N26	P308	P26	P314	R26	P319
L27	P295	M27	P309	N27	P312	P27	P317	R27	P318
L28	V_{SS}	M28	P305	N28	V_{SS}	P28	P313	R28	P316
L29	P304	M29	V_{DD}	N29	P310	P29	V_{DD}	R29	V_{DD}
T1	V_{DD}	U1	P123	V1	V_{DD}	W1	P114	Y1	P112
T2	P125	U2	V_{SS}	V2	P117	W2	V_{SS}	Y2	P110
T3	P131	U3	P122	V3	P118	W3	P111	Y3	P109
T4	P127	U4	P120	V4	P119	W4	P115	Y4	V_{DD}
T5	P121	U5	P116	V5	P113	W5	P106	Y5	P102
T25	P320	U25	P325	V25	P331	W25	P334	Y25	UPDATE
T26	P324	U26	P323	V26	P327	W26	P335	Y26	P339
T27	P322	U27	P329	V27	P332	W27	P338	Y27	RC_CLK
T28	P321	U28	P328	V28	P333	W28	P337	Y28	RC_EN#
T29	V_{DD}	U29	P326	V29	P330	W29	P336	Y29	RCE
AA1	V_{SS}	AB1	V_{SS}	AC1	V_{SS}	AD1	P103		
AA2	P108	AB2	V_{SS}	AC2	V_{SS}	AD2	P099		
AA3	P107	AB3	P105	AC3	P100	AD3	P096		
AA4	P104	AB4	P101	AC4	P097	AD4	P090		
AA5	P098	AB5	P094	AC5	P093	AD5	CLK1		
AA25	RCI1	AB25	RCC1	AC25	RCB4	AD25	RCA9		
AA26	RCB9	AB26	RCB8	AC26	RCB7	AD26	RCB1		
AA27	RCC2	AB27	RCB5	AC27	RCB0	AD27	RCA6		
AA28	RCC3	AB28	RCB6	AC28	RCB2	AD28	RCA7		
AA29	RCI0	AB29	RCC0	AC29	RCB3	AD29	RCA8		

Table 17 MSX340 Pinout By Ball Sequence *(Continued)*

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
AE1	P095	AF1	V_{DD}	AG1	IE_1	AH1	V_{SS}	AJ1	V_{SS}
AE2	P092	AF2	P091	AG2	P086	AH2	V_{SS}	AJ2	V_{DD}
AE3	OE_1#	AF3	P089	AG3	P085	AH3	P080	AJ3	P074
AE4	P088	AF4	P084	AG4	P081	AH4	P077	AJ4	P071
AE5	P087	AF5	P083	AG5	P076	AH5	P070	AJ5	P067
AE6	P082	AF6	P079	AG6	P072	AH6	V_{SS}	AJ6	V_{DD}
AE7	P078	AF7	P073	AG7	P066	AH7	V_{SS}	AJ7	P063
AE8	P075	AF8	P069	AG8	P062	AH8	V_{SS}	AJ8	P061
AE9	P068	AF9	P064	AG9	P056	AH9	P054	AJ9	V_{DD}
AE10	P065	AF10	P057	AG10	P060	AH10	P052	AJ10	V_{DD}
AE11	P058	AF11	P059	AG11	P053	AH11	P050	AJ11	P051
AE12	P055	AF12	P048	AG12	P046	AH12	V_{SS}	AJ12	P044
AE13	P049	AF13	P047	AG13	P042	AH13	P045	AJ13	P040
AE14	P043	AF14	P041	AG14	P039	AH14	P038	AJ14	V_{DD}
AE15	P036	AF15	P034	AG15	P032	AH15	V_{SS}	AJ15	V_{DD}
AE16	P031	AF16	P035	AG16	P037	AH16	P033	AJ16	V_{DD}
AE17	P027	AF17	P026	AG17	P029	AH17	P028	AJ17	P030
AE18	P023	AF18	P025	AG18	P024	AH18	V_{SS}	AJ18	V_{DD}
AE19	P018	AF19	P017	AG19	P021	AH19	P020	AJ19	P022
AE20	P014	AF20	P019	AG20	P013	AH20	V_{SS}	AJ20	V_{DD}
AE21	P009	AF21	P010	AG21	P015	AH21	P016	AJ21	V_{DD}
AE22	P003	AF22	P004	AG22	P012	AH22	V_{SS}	AJ22	P011
AE23	TDO	AF23	P000	AG23	P008	AH23	V_{SS}	AJ23	V_{DD}
AE24	OE_0#	AF24	TMS	AG24	P005	AH24	P006	AJ24	P007
AE25	RCA5	AF25	CLK_0	AG25	TDI	AH25	P001	AJ25	P002
AE26	RCA1	AF26	RCA0	AG26	IE_0	AH26	TCK	AJ26	TRST#
AE27	RCA2	AF27	V_{SS}	AG27	V_{SS}	AH27	RC_RDY	AJ27	HW_RST#
AE28	RCA4	AF28	V_{DD}	AG28	V_{SS}	AH28	V_{SS}	AJ28	V_{SS}
AE29	RCA3	AF29	V_{DD}	AG29	V_{SS}	AH29	V_{SS}	AJ29	V_{SS}

4.6 MSX340 [480 PBGA Package] Pinout: By Ball Name

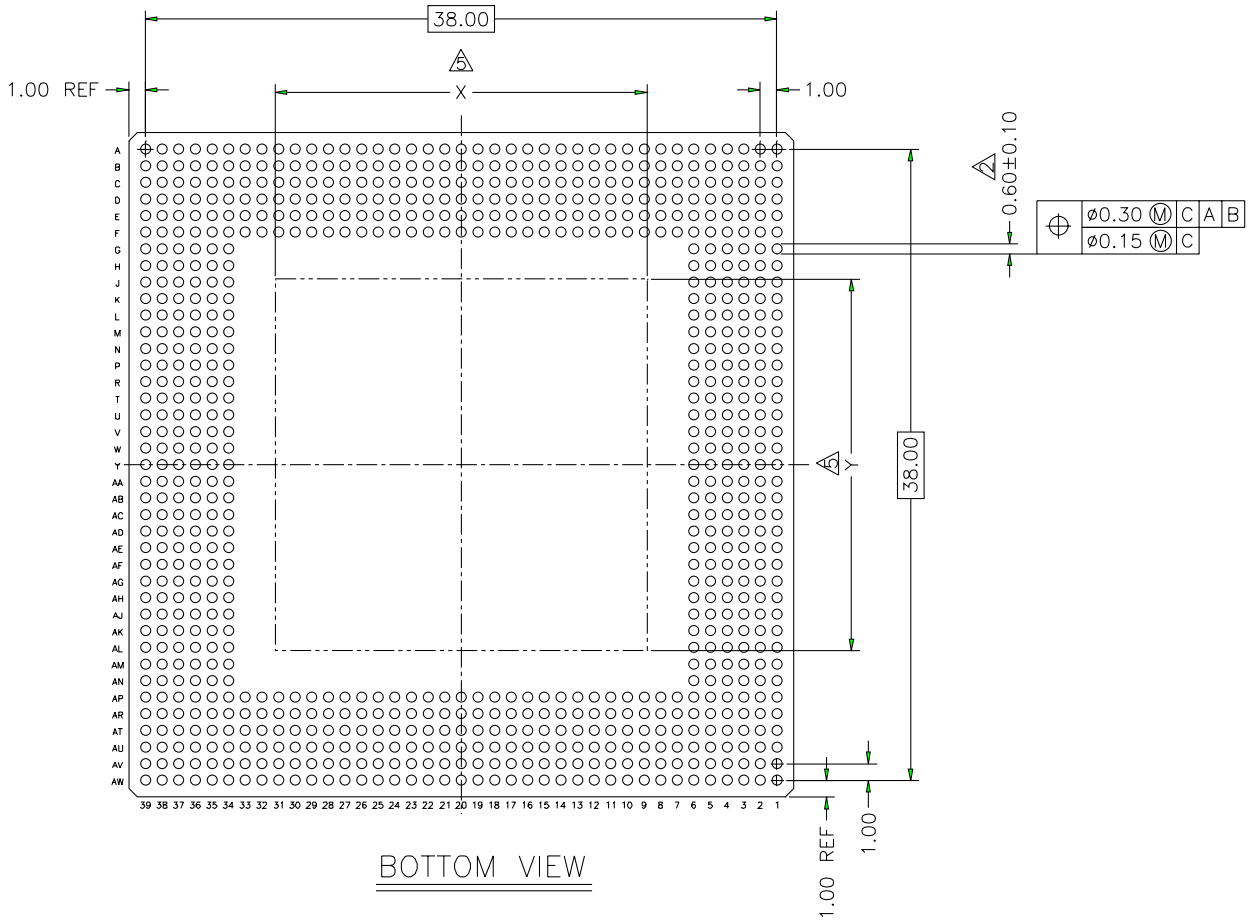
Table 18 MSX340 Pinout By Ball Name

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
CLK_0	AF25	P031	AE16	P075	AE8	P119	V4	P163	H3	P207	D11
CLK_1	AD5	P032	AG15	P076	AG5	P120	U4	P164	G5	P208	C11
CLK_2	C5	P033	AH16	P077	AH4	P121	T5	P165	G4	P209	B11
CLK_3	C28	P034	AF15	P078	AE7	P122	U3	P166	G2	P210	E12
HW_RST#	AJ27	P035	AF16	P079	AF6	P123	U1	P167	G1	P211	A11
IE_0	AG26	P036	AE15	P080	AH3	P124	R5	P168	F4	P212	D12
IE_1	AG1	P037	AG16	P081	AG4	P125	T2	P169	G3	P213	C12
IE_2	D6	P038	AH14	P082	AE6	P126	R2	P170	F1	P214	D13
IE_3	E25	P039	AG14	P083	AF5	P127	T4	P171	F5	P215	E13
OE_0#	AE24	P040	AJ13	P084	AF4	P128	R3	P172	F3	P216	C13
OE_1#	AE3	P041	AF14	P085	AG3	P129	P5	P173	F2	P217	B13
OE_2#	A4	P042	AG13	P086	AG2	P130	P2	P174	E1	P218	E14
OE_3#	D27	P043	AE14	P087	AE5	P131	T3	P175	E5	P219	A13
P000	AF23	P044	AJ12	P088	AE4	P132	P3	P176	E2	P220	B14
P001	AH25	P045	AH13	P089	AF3	P133	R4	P177	D4	P221	D14
P002	AJ25	P046	AG12	P090	AD4	P134	P4	P178	E4	P222	C15
P003	AE22	P047	AF13	P091	AF2	P135	N4	P179	E3	P223	C14
P004	AF22	P048	AF12	P092	AE2	P136	N5	P180	C4	P224	D15
P005	AG24	P049	AE13	P093	AC5	P137	N1	P181	A2	P225	E15
P006	AH24	P050	AH11	P094	AB5	P138	N3	P182	E6	P226	B16
P007	AJ24	P051	AJ11	P095	AE1	P139	N2	P183	D5	P227	D16
P008	AG23	P052	AH10	P096	AD3	P140	M5	P184	A3	P228	C16
P009	AE21	P053	AG11	P097	AC4	P141	M1	P185	B3	P229	B17
P010	AF21	P054	AH9	P098	AA5	P142	M3	P186	B5	P230	C17
P011	AJ22	P055	AE12	P099	AD2	P143	M2	P187	E7	P231	A17
P012	AG22	P056	AG9	P100	AC3	P144	L5	P188	D7	P232	E16
P013	AG20	P057	AF10	P101	AB4	P145	L1	P189	B4	P233	A18
P014	AE20	P058	AE11	P102	Y5	P146	L2	P190	C6	P234	C18
P015	AG21	P059	AF11	P103	AD1	P147	M4	P191	E8	P235	D17
P016	AH21	P060	AG10	P104	AA4	P148	L3	P192	D8	P236	D18
P017	AF19	P061	AJ8	P105	AB3	P149	L4	P193	A5	P237	E17
P018	AE19	P062	AG8	P106	W5	P150	K5	P194	A6	P238	B19
P019	AF20	P063	AJ7	P107	AA3	P151	K4	P195	B6	P239	A19
P020	AH19	P064	AF9	P108	AA2	P152	K1	P196	C7	P240	C19
P021	AG19	P065	AE10	P109	Y3	P153	K2	P197	E9	P241	B20
P022	AJ19	P066	AG7	P110	Y2	P154	J5	P198	C8	P242	B21
P023	AE18	P067	AJ5	P111	W3	P155	K3	P199	D9	P243	E18
P024	AG18	P068	AE9	P112	Y1	P156	J1	P200	E10	P244	C21
P025	AF18	P069	AF8	P113	V5	P157	J2	P201	C9	P245	D19
P026	AF17	P070	AH5	P114	W1	P158	H5	P202	B9	P246	D20
P027	AE17	P071	AJ4	P115	W4	P159	J3	P203	A8	P247	C20
P028	AH17	P072	AG6	P116	U5	P160	H1	P204	D10	P248	E19
P029	AG17	P073	AF7	P117	V2	P161	H2	P205	C10	P249	A22
P030	AJ17	P074	AJ3	P118	V3	P162	H4	P206	E11	P250	C22

Table 18 MSX340 Pinout By Ball Name *(Continued)*

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
P251	A23	P295	L27	P339	Y26	V_{DD}	A20	V_{SS}	AG27		
P252	E20	P296	H27	RC_EN#	Y28	V_{DD}	A21	V_{SS}	AG28		
P253	D21	P297	J27	RC_CLK	Y27	V_{DD}	A24	V_{SS}	AG29		
P254	C23	P298	J28	RCA0	AF26	V_{DD}	A28	V_{SS}	AH1		
P255	A25	P299	L25	RCA1	AE26	V_{DD}	AF1	V_{SS}	AH2		
P256	D22	P300	K28	RCA2	AE27	V_{DD}	AF28	V_{SS}	AH6		
P257	E21	P301	K29	RCA3	AE29	V_{DD}	AF29	V_{SS}	AH7		
P258	B25	P302	L26	RCA4	AE28	V_{DD}	AJ2	V_{SS}	AH8		
P259	A26	P303	M25	RCA5	AE25	V_{DD}	AJ6	V_{SS}	AH12		
P260	D23	P304	L29	RCA6	AD27	V_{DD}	AJ9	V_{SS}	AH15		
P261	C24	P305	M28	RCA7	AD28	V_{DD}	AJ10	V_{SS}	AH18		
P262	A27	P306	M26	RCA8	AD29	V_{DD}	AJ14	V_{SS}	AH20		
P263	E22	P307	N25	RCA9	AD25	V_{DD}	AJ15	V_{SS}	AH22		
P264	B26	P308	N26	RCB0	AC27	V_{DD}	AJ16	V_{SS}	AH23		
P265	C25	P309	M27	RCB1	AD26	V_{DD}	AJ18	V_{SS}	AH28		
P266	E23	P310	N29	RCB2	AC28	V_{DD}	AJ20	V_{SS}	AH29		
P267	D24	P311	P25	RCB3	AC29	V_{DD}	AJ21	V_{SS}	AJ1		
P268	C26	P312	N27	RCB4	AC25	V_{DD}	AJ23	V_{SS}	AJ28		
P269	B27	P313	P28	RCB5	AB27	V_{DD}	C3	V_{SS}	AJ29		
P270	E24	P314	P26	RCB6	AB28	V_{DD}	D1	V_{SS}	B1		
P271	D25	P315	R25	RCB7	AC26	V_{DD}	D2	V_{SS}	B2		
P272	D26	P316	R28	RCB8	AB26	V_{DD}	D3	V_{SS}	B7		
P273	C27	P317	P27	RCB9	AA26	V_{DD}	D29	V_{SS}	B8		
P274	F25	P318	R27	RCC0	AB29	V_{DD}	G29	V_{SS}	B10		
P275	E26	P319	R26	RCC1	AB25	V_{DD}	H29	V_{SS}	B12		
P276	D28	P320	T25	RCC2	AA27	V_{DD}	J4	V_{SS}	B15		
P277	C29	P321	T28	RCC3	AA28	V_{DD}	J29	V_{SS}	B18		
P278	G25	P322	T27	RCE	Y29	V_{DD}	M29	V_{SS}	B22		
P279	E27	P323	U26	RCI0	AA29	V_{DD}	P1	V_{SS}	B23		
P280	F26	P324	T26	RCI1	AA25	V_{DD}	P29	V_{SS}	B24		
P281	E28	P325	U25	RC_RDY	AH27	V_{DD}	R1	V_{SS}	B28		
P282	H25	P326	U29	TRST#	AJ26	V_{DD}	R29	V_{SS}	B29		
P283	E29	P327	V26	TCK	AH26	V_{DD}	T1	V_{SS}	C1		
P284	F27	P328	U28	TDI	AG25	V_{DD}	T29	V_{SS}	C2		
P285	G26	P329	U27	TDO	AE23	V_{DD}	V1	V_{SS}	G28		
P286	J25	P330	V29	TMS	AF24	V_{DD}	Y4	V_{SS}	H28		
P287	F28	P331	V25	UPDATE	Y25	V_{SS}	A1	V_{SS}	L28		
P288	H26	P332	V27	V_{DD}	A7	V_{SS}	A29	V_{SS}	N28		
P289	G27	P333	V28	V_{DD}	A9	V_{SS}	AA1	V_{SS}	U2		
P290	F29	P334	W25	V_{DD}	A10	V_{SS}	AB1	V_{SS}	W2		
P291	K26	P335	W26	V_{DD}	A12	V_{SS}	AB2				
P292	K25	P336	W29	V_{DD}	A14	V_{SS}	AC1				
P293	K27	P337	W28	V_{DD}	A15	V_{SS}	AC2				
P294	J26	P338	W27	V_{DD}	A16	V_{SS}	AF27				

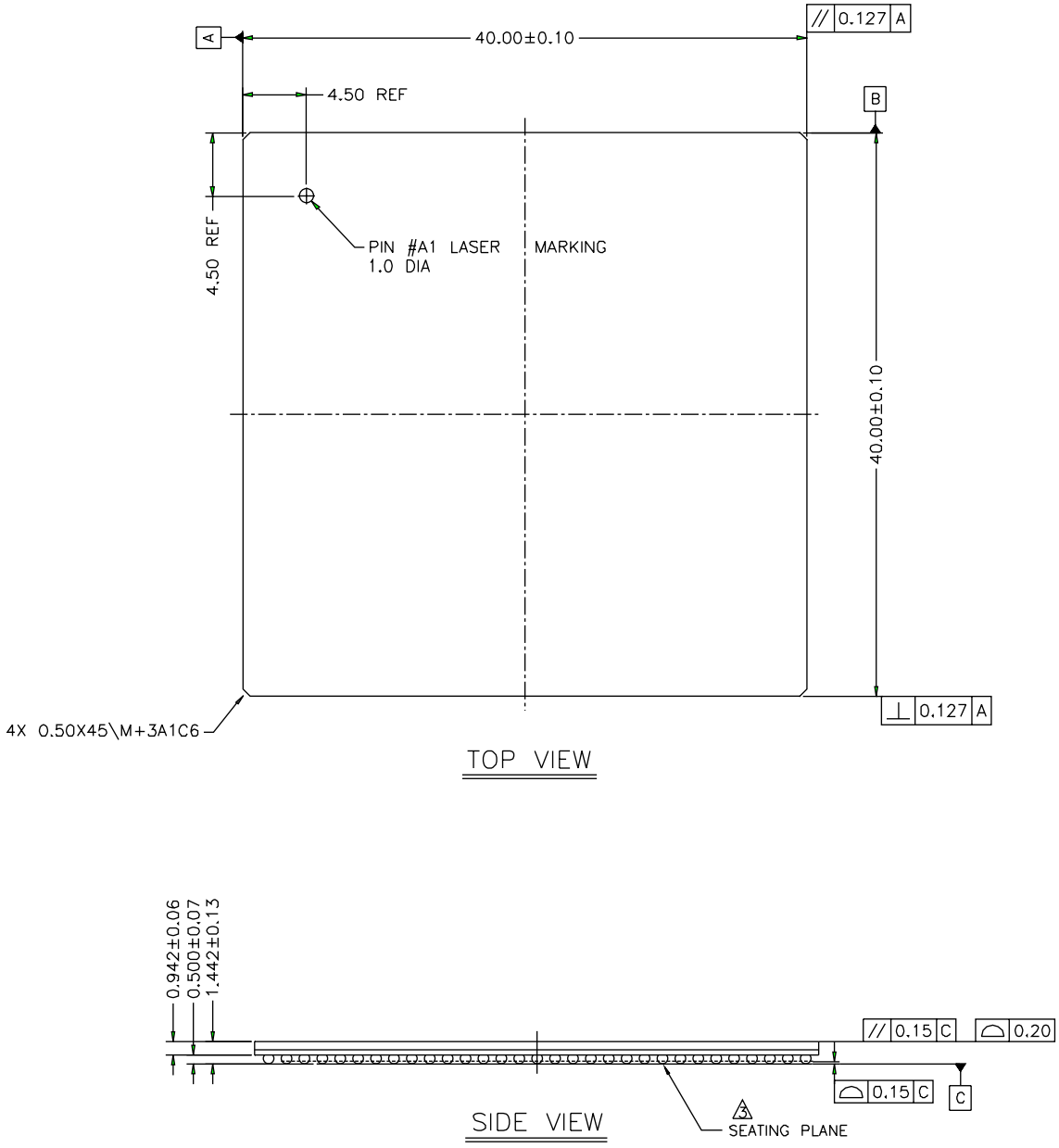
4.7 792 TBGA Package Dimensions (Bottom View)



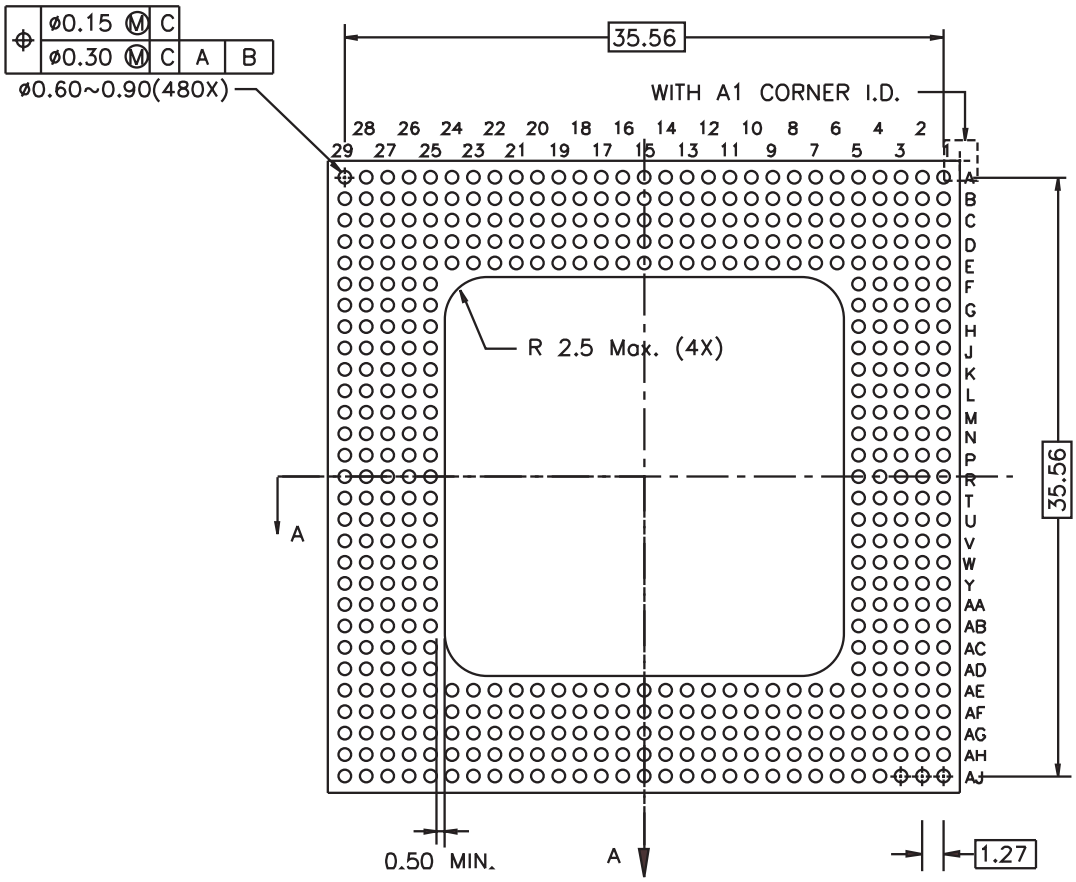
NOTE

1. DIMENSIONS AND TOLERANCE PER ASME Y 14.5M – 1994
2. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM C
3. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. SOLDER BALL POSITION DESINATION PER JESD 95-1.
5. THE ENCAPSULATION SIZE (X,Y) WILL VARY WITH CAVITY SIZE. THE DISTANCE FROM BOND FINGER EDGE TO ENCAPSULATION SHALL BE MIN. 0.50MM.
6. UNLESS OTHERWISE SPECIFIED TOLERANCE : DECIMAL ±0.05 ANGULAR ±2°.

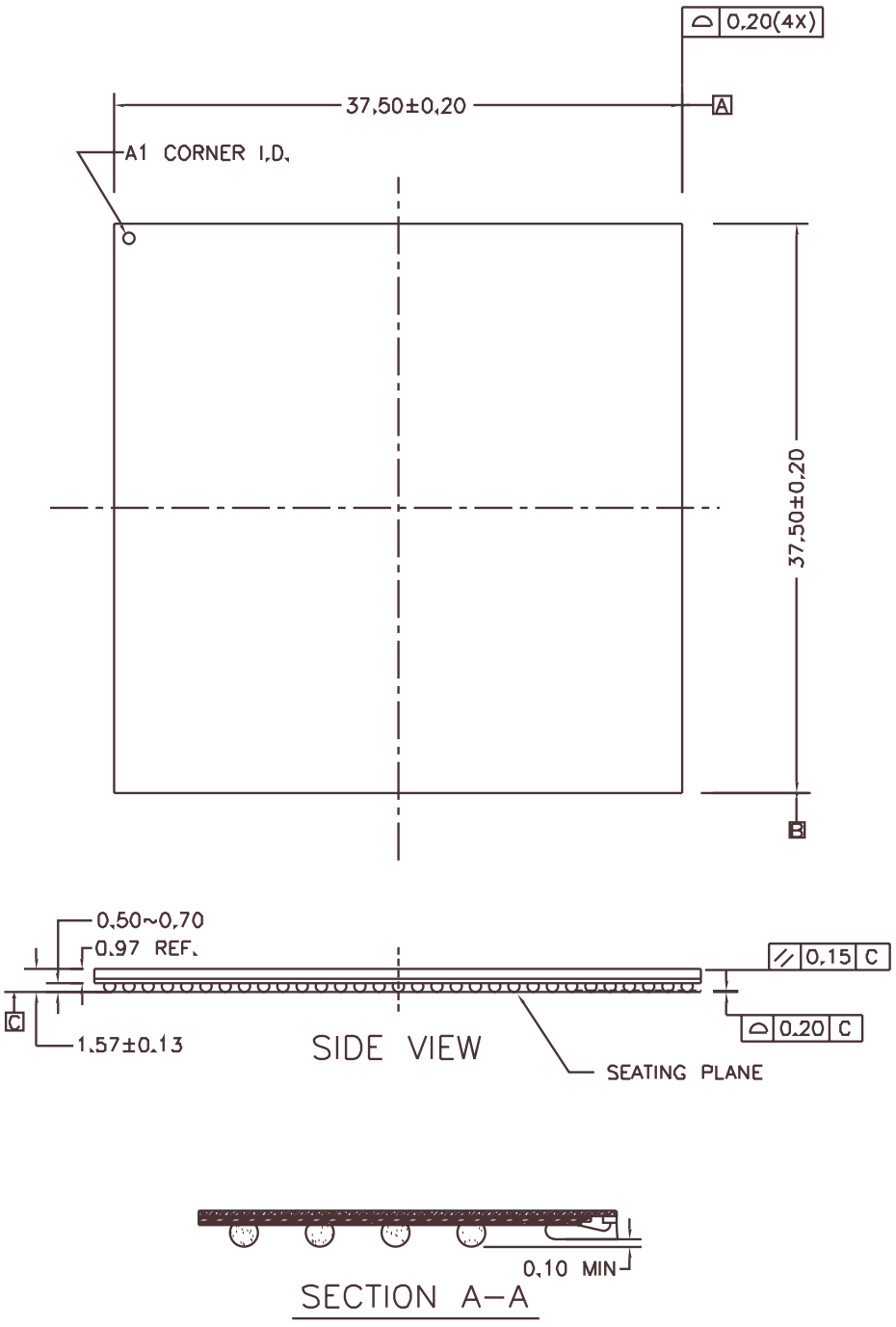
4.8 792 TBGA Package Dimensions (Top and Side View)



4.9 480 PBGA Package Dimensions (Bottom View)



4.10 480 PBGA Package Dimensions (Top and Side View)



4.11 Port Cross-Reference for the MSX532 and MSX340

Table 19 Port Cross-reference for MSX532 and MSX340

MSX532 Port #	MSX340 Port #	MSX532 Port #	MSX340 Port #	MSX532 Port #	MSX340 Port #	MSX532 Port #	MSX340 Port #	MSX532 Port #	MSX340 Port #
P000	P000	P040	P016	P080	P056	P120	P072	P160	—
P001	P001	P041	P017	P081	P057	P121	P073	P161	—
P002	P002	P042	P018	P082	P058	P122	P074	P162	—
P003	P003	P043	P019	P083	P059	P123	P075	P163	—
P004	P004	P044	P020	P084	P060	P124	P076	P164	—
P005	P005	P045	P021	P085	—	P125	P077	P165	—
P006	P006	P046	P022	P086	—	P126	P078	P166	—
P007	P007	P047	P023	P087	—	P127	P079	P167	—
P008	P008	P048	P024	P088	—	P128	P080	P168	—
P009	P009	P049	P025	P089	—	P129	P081	P169	—
P010	—	P050	P026	P090	—	P130	P082	P170	—
P011	—	P051	P027	P091	—	P131	P083	P171	—
P012	—	P052	P028	P092	—	P132	P084	P172	—
P013	—	P053	P029	P093	—	P133	P085	P173	—
P014	—	P054	P030	P094	—	P134	P086	P174	—
P015	—	P055	P031	P095	—	P135	P087	P175	—
P016	—	P056	P032	P096	—	P136	P088	P176	P104
P017	—	P057	P033	P097	—	P137	P089	P177	P105
P018	—	P058	P034	P098	—	P138	P090	P178	P106
P019	—	P059	P035	P099	—	P139	P091	P179	P107
P020	—	P060	P036	P100	—	P140	P092	P180	P108
P021	—	P061	P037	P101	—	P141	P093	P181	P109
P022	—	P062	P038	P102	—	P142	P094	P182	P110
P023	—	P063	P039	P103	—	P143	P095	P183	P111
P024	—	P064	P040	P104	—	P144	P096	P184	P112
P025	—	P065	P041	P105	—	P145	P097	P185	P113
P026	—	P066	P042	P106	—	P146	P098	P186	P114
P027	—	P067	P043	P107	—	P147	P099	P187	P115
P028	—	P068	P044	P108	—	P148	P100	P188	P116
P029	—	P069	P045	P109	P061	P149	P101	P189	P117
P030	—	P070	P046	P110	P062	P150	P102	P190	P118
P031	—	P071	P047	P111	P063	P151	P103	P191	P119
P032	—	P072	P048	P112	P064	P152	—	P192	P120
P033	—	P073	P049	P113	P065	P153	—	P193	P121
P034	P010	P074	P050	P114	P066	P154	—	P194	P122
P035	P011	P075	P051	P115	P067	P155	—	P195	P123
P036	P012	P076	P052	P116	P068	P156	—	P196	P124
P037	P013	P077	P053	P117	P069	P157	—	P197	P125
P038	P014	P078	P054	P118	P070	P158	—	P198	P126
P039	P015	P079	P055	P119	P071	P159	—	P199	P127

Table 19 Port Cross-reference for MSX532 and MSX340 *(Continued)*

MSX532 Port #	MSX340 Port #	MSX532 Port #	MSX340 Port #	MSX532 Port #	MSX340 Port #	MSX532 Port #	MSX340 Port #	MSX532 Port #	MSX340 Port #
P200	P128	P240	—	P280	P184	P320	P200	P360	P240
P201	P129	P241	—	P281	P185	P321	P201	P361	P241
P202	P130	P242	—	P282	P186	P322	P202	P362	P242
P203	P131	P243	—	P283	P187	P323	P203	P363	P243
P204	P132	P244	—	P284	P188	P324	P204	P364	P244
P205	P133	P245	—	P285	P189	P325	P205	P365	P245
P206	P134	P246	—	P286	P190	P326	P206	P366	P246
P207	P135	P247	—	P287	P191	P327	P207	P367	P247
P208	P136	P248	—	P288	P192	P328	P208	P368	P248
P209	P137	P249	—	P289	P193	P329	P209	P369	—
P210	P138	P250	—	P290	P194	P330	P210	P370	—
P211	P139	P251	—	P291	P195	P331	P211	P371	—
P212	P140	P252	P156	P292	P196	P332	P212	P372	—
P213	P141	P253	P157	P293	P197	P333	P213	P373	—
P214	P142	P254	P158	P294	—	P334	P214	P374	—
P215	P143	P255	P159	P295	—	P335	P215	P375	—
P216	P144	P256	P160	P296	—	P336	P216	P376	—
P217	P145	P257	P161	P297	—	P337	P217	P377	—
P218	P146	P258	P162	P298	—	P338	P218	P378	—
P219	P147	P259	P163	P299	—	P339	P219	P379	—
P220	P148	P260	P164	P300	—	P340	P220	P380	—
P221	P149	P261	P165	P301	—	P341	P221	P381	—
P222	P150	P262	P166	P302	—	P342	P222	P382	—
P223	P151	P263	P167	P303	—	P343	P223	P383	—
P224	P152	P264	P168	P304	—	P344	P224	P384	—
P225	P153	P265	P169	P305	—	P345	P225	P385	—
P226	P154	P266	P170	P306	—	P346	P226	P386	—
P227	P155	P267	P171	P307	—	P347	P227	P387	—
P228	—	P268	P172	P308	—	P348	P228	P388	—
P229	—	P269	P173	P309	—	P349	P229	P389	—
P230	—	P270	P174	P310	—	P350	P230	P390	—
P231	—	P271	P175	P311	—	P351	P231	P391	—
P232	—	P272	P176	P312	—	P352	P232	P392	—
P233	—	P273	P177	P313	—	P353	P233	P393	P249
P234	—	P274	P178	P314	—	P354	P234	P394	P250
P235	—	P275	P179	P315	—	P355	P235	P395	P251
P236	—	P276	P180	P316	—	P356	P236	P396	P252
P237	—	P277	P181	P317	—	P357	P237	P397	P253
P238	—	P278	P182	P318	P198	P358	P238	P398	P254
P239	—	P279	P183	P319	P199	P359	P239	P399	P255

Table 19 Port Cross-reference for MSX532 and MSX340 ***(Continued)***

MSX532 Port #	MSX340 Port #	MSX532 Port #	MSX340 Port #	MSX532 Port #	MSX340 Port #	MSX532 Port #	MSX340 Port #	MSX532 Port #	MSX340 Port #
P400	P256	P440	P296	P480	P312	P520	—		
P401	P257	P441	P297	P481	P313	P521	—		
P402	P258	P442	P298	P482	P314	P522	—		
P403	P259	P443	P299	P483	P315	P523	—		
P404	P260	P444	P300	P484	P316	P524	—		
P405	P261	P445	P301	P485	P317	P525	—		
P406	P262	P446	—	P486	P318	P526	—		
P407	P263	P447	—	P487	P319	P527	—		
P408	P264	P448	—	P488	P320	P528	—		
P409	P265	P449	—	P489	P321	P529	—		
P410	P266	P450	—	P490	P322	P530	—		
P411	P267	P451	—	P491	P323	P531	—		
P412	P268	P452	—	P492	P324				
P413	P269	P453	—	P493	P325				
P414	P270	P454	—	P494	P326				
P415	P271	P455	—	P495	P327				
P416	P272	P456	—	P496	P328				
P417	P273	P457	—	P497	P329				
P418	P274	P458	—	P498	P330				
P419	P275	P459	—	P499	P331				
P420	P276	P460	—	P500	P332				
P421	P277	P461	—	P501	P333				
P422	P278	P462	—	P502	P334				
P423	P279	P463	—	P503	P335				
P424	P280	P464	—	P504	P336				
P425	P281	P465	—	P505	P337				
P426	P282	P466	—	P506	P338				
P427	P283	P467	—	P507	P339				
P428	P284	P468	—	P508	—				
P429	P285	P469	—	P509	—				
P430	P286	P470	P302	P510	—				
P431	P287	P471	P303	P511	—				
P432	P288	P472	P304	P512	—				
P433	P289	P473	P305	P513	—				
P434	P290	P474	P306	P514	—				
P435	P291	P475	P307	P515	—				
P436	P292	P476	P308	P516	—				
P437	P293	P477	P309	P517	—				
P438	P294	P478	P310	P518	—				
P439	P295	P479	P311	P519	—				

4.12 Package Thermal Characteristics

Table 20 Package Thermal Characteristics

Package	Pin Count	θ_{JC}(°C/W)	θ_{JA}(°C/W) Still Air	θ_{JA}(°C/W) 200 lfpm	θ_{JA}(°C/W) 300 lfpm	θ_{JA}(°C/W) 500 lfpm
TBGA	792	0.4	7.58	6.00	5.66	5.26
PBGA	480	1.7	12.2	10.6	9.86	NA

Note – Thermal performance values are based on simulation data.

5. Power Consumption

There are three components to consider when calculating power for the MSX Family of devices:

1. **Steady State Component**—This element equals 252 milliwatts.
2. **Connection Component**—This element equals .006mW x Mb/s x connections.
3. **Output Drive Component**—This element equals .013mW x number of outputs x Mb/s x capacitive load (pF).

Power consumption = **Steady State Component + Connection Component + Output Drive Component**.
= 252mW + (0.006 x Mb/s x #connections) + (0.013 x Mb/s x #outputs x Cload)

The following examples shows the total power consumption as determined by the above formula:

Example 1

Using the MSX532 with 10 Mb/s into a 10pF load with 266 inputs connected to 266 outputs:

Power consumption = 252 mWatts + (0.006 x 10 x 266) + (0.013 x 266 x 10 x 10)
= 252mW + 16mW + 346mW = **0.614 Watts**

Example 2

Using the MSX532 with 150 Mb/s into a 10pF load with 266 inputs connected to 266 outputs:

Power consumption = 252 mWatts + (0.006 x 150 x 266) + (0.013 x 266 x 150 x 10)
= 252mW + 239.4mW + 5187mW = **5.68 Watts**

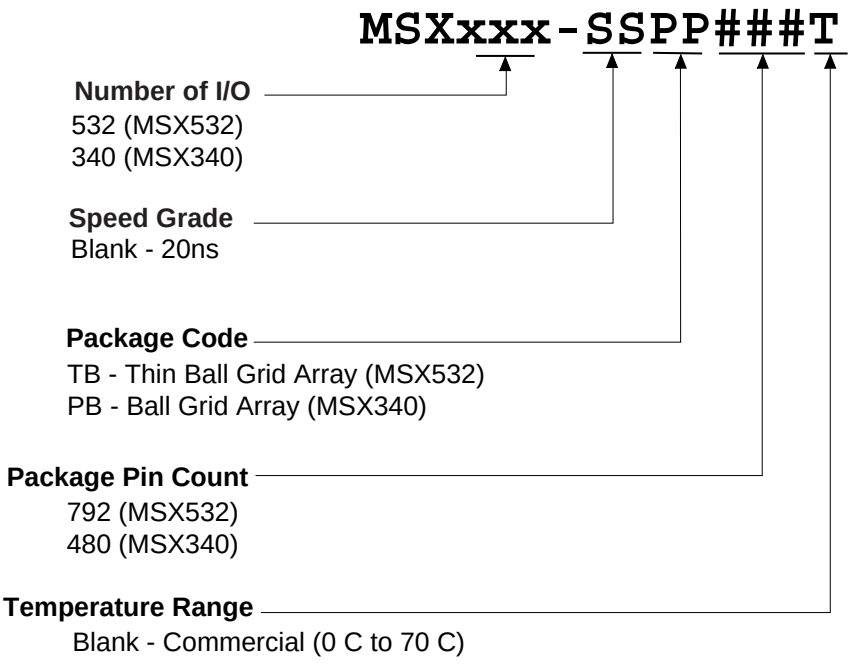
6. Component Availability and Ordering Information

The following table lists the MSX package options and operating temperature ranges that are currently available. Contact Fairchild Marketing for more up-to-date information.

Table 21 Component Availability

Device	Package Code	Package Pins	Temperature Range	Availability
MSX532-TB792	TB	792	Commercial	Now
MSX340-PB480	PB	480	Commercial	Now

Table 22 Order Information



7. Glossary

ARRAY SIDE: The signal and connections between the Crosspoint Array and the IO Buffer.

BUS REPEATER: A circuit operation of the IO Buffer that enables the MSX device to pass data in both directions on an IO device pin. The IO Buffer is placed in a disabled output state to the pin and to the Crosspoint array. A forced low on either side of the IO Buffer will be transmitted to the other side of the IO Buffer and held until the forced low is changed to a force high. At the change of the forcing input, the IO Buffer will force the other side to a following high state and drive a high level out for a period of time. After the period of time, the IO Buffer will return to the disabled state.

BYPASS: A JTAG instruction that connects the previous chip to the next chip through a one bit data register to speed up programming of other chips in a JTAG chain of devices.

CLOCK: Four device corner inputs used to gate data into registers in the IO Buffer. The Corner inputs serve two sides of the MSX. This provides two choices for each IO Buffer register in and register out. The neighbor input can also be used as register clock and the clocks can be inverted.

CONTROL REGISTER: A programmable register used to control various functions in programming and other circuit settings. All Bits programmed in the JTAG Mode. Rapid Configure Enable bit can be set with a high level on the RCE pin during a reset of the circuits.

CROSSPOINT: A single cell containing two N Channel transistors and two RAM bits. The RAM bits are connected in a master-slave configuration to provide an update for programming and changing program information all at once. Each cell contains both an X and Y reset to remove all ports connected to an addressed port in a single program cycle.

CROSSPOINT ARRAY: An array of Crosspoint used to connect any port to any other port or any combination of other ports. The array has all redundant cell removed; there is a single Crosspoint cell for each port to port connection. The reduced cell count is folded to provide a square array. The array has a diagonal line where the cells are rotated.

DATA BIT LINES: A pair of signal lines used to write into and read out of Crosspoint Cells. The lines are pre-charged before a read and one is pulled low for a write.

DEVICE ID: A 32-bit register in the MSX device with a wired identification. The ID consists of a given number for the device and a revision history field. The identification is shifted out during JTAG reset and the DEVICE ID instruction in JTAG mode. The ID for the MSX devices is 0x0000A89F.

EXTEST: A JTAG instruction that samples I/O pin states and loads new I/O buffer states for testing device pin connections. The MSX devices use a special test mode in EXTEXT to observe the buffer data on the pin side and the array side. A bit in the CONTROL REGISTER controls this mode.

IO BUFFER: The circuit that controls the driving of its associated pin and its port into and out of the Crosspoint Array. The buffer contains all the circuits to make it independent of the other IO Buffers. Each Buffer contains registers for input and output, driving circuits for input and output, sense for Crosspoint Array input, and RAM bits to hold programmed data controlling the function of the buffer.

INPUT OR OUTPUT PATH: The signal flow from pin to array and array to pin. Each path has a register with selectable clocks, drivers for the loaded outputs with selectable enables, and sense circuits to detect changes on either side of the IO Buffer.

JTAG: The Joint Test Action group is a committee to standardize scan testing of devices. The JTAG interface is referred to as IEEE 1149.1. This is a five bit serial programming and testing method.

JTAG SEQUENCE: The ordering of all the pins in a serial chain for driving and sensing signals on pins during EXTEST and SAMPLE/PRELOAD. All pins except power and ground and the five JTAG pins are in the serial string.

NEXT NEIGHBOR: Input can be selected as the clock for the IOB registers for data and clock pairing. The next higher port is the selected neighbor except for Port 531, which uses Port 0.

PIN SIDE DRIVER: The IO Buffer circuit that drives the device pin associated with that buffer.

PORT: A name followed by a number to identify a pin on the device. Ports are numbered from 531 to 0 on the MSX device. In shifting sequence, Port P000 is shifted in first and shifted out first.

RapidConfigure: A parallel programming method for the MSX devices. The RC mode uses 29 dedicated pins to program the Crosspoint Array and the IO Buffers. The 29 pins consist of an enable, a strobe, two instruction bits, four variable bits, and two ten-bit address fields.

RCE: A control pin of the MSX device that is sampled during reset to determine if the device becomes active in the JTAG or the Rapid Configure mode. This pin places the CONTROL REGISTER bit in the state to allow RC operations or not based on the voltage level of the RCE pin. The JTAG mode is always enabled and can set or clear the RC bit in the CONTROL REGISTER.

TRICKLE CURRENT: A very low current (~15 microamperes) used to pull unused or non-driven circuits to a stable high level. Prevents signals from drifting between CMOS thresholds and drawing currents from the power supply. In the case of BUS REPEATER, the small trickle current provides a known high level on the pin and array side inputs.

Revision History

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Table 23 Revision History

Date/	Version No.	Description
5/1/2000	Revision 1.3	Initial release of “Preliminary” datasheet
6/30/2000	Revision 1.4	Converted datasheet from a Word document to a FrameMaker document. Corrected RCC[1] statement in 1.4.3 “Crosspoint Programming”.
10/16/00	Revision 1.5	Added MSX340 pinout tables, package pinout drawing, package dimension drawings. Changed verbiage throughout document to reflect MSX Family. Added the -10 and the -15 device specifications to the AC Electrical tables. Updated ordering information.
12/1/00	Revision 1.6	Changed the -15 device to a -20 device in the AC Electrical specifications table and modified the parameters for Additional Multicast Mode, JTAG Clock Frequency, and One Way Signal Propagation Delay. Modified the RapidConfigure IOB Read and Write Cycles timing diagram. Changed the UPDATE signal and relative descriptions from low (UPDATE#) to high (UPDATE) throughout entire document.Corrected pinout drawings for the MSX532 and MSX340 to reflect the change to the UPDATE pin. Modified Component Availability and Ordering Information tables.
2/20/2001	Revision 1.7	Changed Ball Name for AJ26 from RST to TRST# on MSX340 pinout drawing and MSX340 “Pinout By Ball Name” table; added “...output data inversion mode...” to OP I/O port function in Table 1.
2/26/01	Revision 1.8	Table 14—changed Max parameters for NRZ Data Rate from 200Mb/s to 150Mb/s, and Registered Input/Output Clock Frequency from 100MHz to 75MHz; made specific references to product/package size on front page.
5/11/01	Revision 1.9	Changes to Table 10 - Absolute Maximum Ratings; Pmax limits from TBD to 10.5, ESD limits from 2000 to 1500; removed -10 part from AC Electrical Specs Table 14; changed power consumption examples from 100 Mb/s to 10Mb/s in Example 1, and 300 Mb/s to 150Mb/s in Example 2; updated Component Availability information by removing -10 part.
9/5/01	Revision 1.10	Changed speed ratings on cover sheet from 300Mb/s and 150MHz to 150Mb/s and 75MHz; changed propagation delay on cover sheet from 10ns to 20ns; added a minimum value of 6 to Positive and Negative Pulse widths (tw+ and tw-) in Table 14, AC Electrical specs.

8. Product Status Definition

Datasheet Identification	Product Status	Definition
Advanced	Formative or In Design	This datasheet contains the design specifications for product development. Specification may change in any manner without notice.
Preliminary	Preproduction Product	This datasheet contains the preliminary data, and supplementary data will be published at a later date. Fairchild reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification	Full Production	This datasheet contains final specifications. Fairchild reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	No longer in Production	This datasheet contains specifications for a product that has been discontinued by Fairchild. The datasheet is provided for reference information only.