PI2125
Cool-ORing™ Series

30 Volt, 12 Amp Full-Function Active ORing Solution

Description

The *Cool-ORing™* PI2125 is a complete full-function Active ORing solution with a high-speed ORing MOSFET controller and a very low on-state resistance MOSFET designed for use in redundant power system architectures. The PI2125 *Cool-ORing* solution is offered in an extremely small, thermally enhanced 5mm x 7mm LGA package and can be used in high side Active ORing applications on bus voltages up to 12V. The PI2125 enables extremely low power loss with fast dynamic response to fault conditions, critical for high availability systems. A master/slave feature allows the paralleling of PI2125 solutions for high current Active ORing requirements.

The PI2125, with its 5.5mΩ internal MOSFET provides very high efficiency and low power loss during steady state operation, while achieving high-speed turn-off of the internal MOSFET during input power source fault conditions that cause reverse current flow. The PI2125 provides an active low fault flag output to the system during excessive forward current, light load, reverse current, over-voltage, under-voltage and over-temperature fault conditions. A temperature sensing function indicates a fault if the maximum junction temperature exceeds 160°C. The under-voltage and over-voltage thresholds are programmable via an external resistor divider.

Features

- Integrated High Performance 12A, 5.5mΩ MOSFET
- Very-small, high density fully-optimized solution providing simple PCB layout.
- Fast Dynamic Response to Power Source failures, with 160ns reverse current turn-off delay time
- Accurate sensing capability to indicate system fault conditions
- Programmable under & over-voltage functions
- Over temperature fault detection
- Adjustable reverse current blanking timer
- Master/Slave I/O for paralleling
- Active low fault flag output

Applications

- N+1 Redundant Power Systems
- Servers & High End Computing
- Telecom Systems
- High-side Active ORing
- High current Active ORing (≤ 12Vbus)

Package Information

- 17-pin 5mm x 7mm Thermally Enhanced LGA Package

Typical Application:

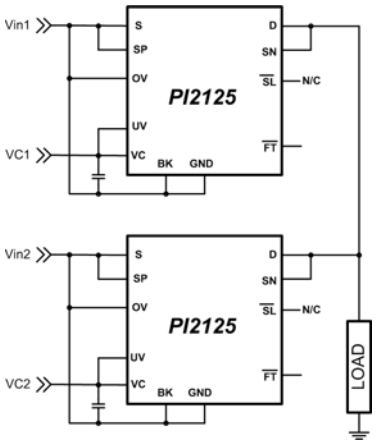


Figure 1: PI2125 High Side Active ORing

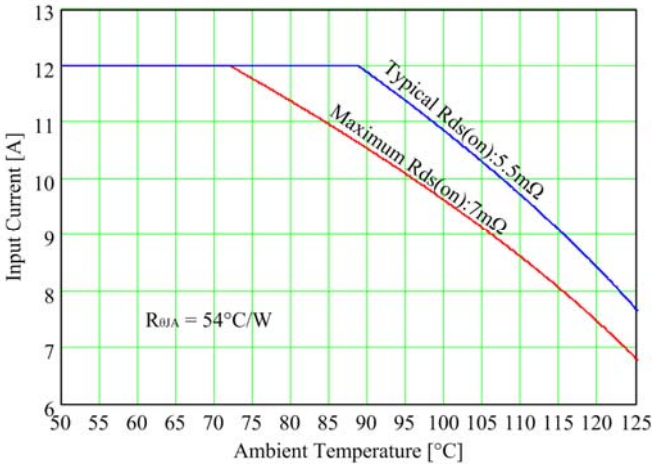
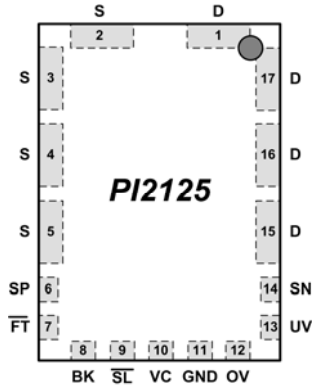


Figure 2: PI2125 input current de-rating based on maximum T_J=150°C vs. ambient temperature.

Pin Description

Pin Name	Pin Number	Description
D	1, 15, 16, 17	**Drain-** The Drain of the internal N-channel MOSFET, connect to the output load.
S	2, 3, 4, 5	**Source-**The source of the internal N-channel MOSFET, connect to the input power source bus voltage.
SP	6	**Positive Sense Input & Clamp:** Connect SP pin to the S pin. The polarity of the voltage difference between SP and SN provides an indication of current flow direction through the MOSFET.
$\overline{FT}$	7	**Fault State Output:** This open collector pin pulls low when a fault occurs. Fault logic inputs are VC Under-Voltage, Input Under-Voltage, Input Over-Voltage, Forward Over-Current, light load, reverse current, and Over-Temperature. Leave this pin open if unused.
BK	8	**Blanking timer Input-Output:** Connect a resistor from BK to GND to set the blanking time for the Reverse Comparator function. To configure in slave mode, connect BK to VC. To configure in master mode with the fastest turn-off response connect BK directly to GND.
$\overline{SL}$	9	**Slave Input-Output:** This pin is used for paralleling multiple PI2125 solutions in high power applications. When the PI2125 is configured as the Master, this pin functions as an output capable of driving up to 10 $\overline{SL}$ pins of slaved PI2125 devices. It serves as an input when the PI2125 is configured in slave mode.
VC	10	**Input Supply Pin:** This pin is the supply pin for the control circuitry and gate driver. Connect a 1µF capacitor between VC pin and the GND pin. Voltage on this pin is limited to 15.5V by an internal shunt regulator in high auxiliary voltage applications. For high voltage auxiliary supply applications connect a shunt resistor between VC and the auxiliary supply.
GND	11	**Ground:** This pin is ground for the gate driver and control circuitry.
OV	12	**Input Over Voltage Input:** The OV pin is used to detect an input source over-voltage condition in ground referenced applications. When the OV pin voltage crosses the OV threshold, the $\overline{FT}$ pin pulls low indicating a fault condition. The input voltage OV threshold is programmable through an external resistor divider. Connect OV to GND to disable this function.
UV	13	**Input Under-Voltage Input:** The UV pin is used to detect an input source under-voltage condition in ground referenced applications. When the UV pin voltage drops below the UV threshold, the $\overline{FT}$ pin pulls low indicating a fault condition. The input voltage UV threshold is programmable through an external resistor divider. Connect UV to VC to disable this function.
SN	14	**Negative Sense Input & Clamp-** Connect SN to D pin. The polarity of the voltage difference between SP and SN provides an indication of current flow direction through the MOSFET.

Package Pin-out



17 Pin LGA (5mm x 7mm)
Top view

Absolute Maximum Ratings

Drain-to-Source Voltage (V_{DS})	30V @ 25°C
Source Current (I_S) Continuous	12A
Source Current (I_S) Pulsed (10µs)	60A
Thermal Resistance $R_{\theta JA}$ (3)	54°C/W
VC	-0.3V to 17.3V / 40mA
SN	-0.3V to 30V / 10mA
SP, OV, $\overline{SL}$	-0.3V to 8.0V / 10mA
UV,BK, $\overline{FT}$	-0.3V to 17.3V / 10mA
GND	-0.3V / 5A peak
Storage Temperature	-65°C to 150°C
Operating Junction Temperature	-40°C to Over Temperature Fault (T_{FT})
Lead Temperature (Soldering, 20 sec)	250°C
ESD Rating	2kV HBM

Electrical Specifications

Unless otherwise specified: -40°C < T_J < 125°C, VC =12V, C_{Vc} = 1uF, C_{SL} = 10pF

Parameter	Symbol	Min	Typ	Max	Units	Conditions
VC Supply						
Operating Supply Range(4)	V_{VC-GND}	4.5		13.2	V	No VC limiting resistors
Quiescent Current	I_{VC}		3.7	4.2	mA	Normal Operating Condition, No Faults
VC Clamp Voltage	V_{VC-CLM}	15	15.5	16	V	I_{VC}=10mA
VC Clamp Shunt Resistance	R_{VC}			7.5	Ω	Delta I_{VC}=10mA
VC Under-voltage Rising Threshold	V_{VCUVR}		4.3	4.5	V	
VC Under-voltage Falling Threshold	V_{VCUVF}	4.0	4.15		V	
VC Under-voltage Hysteresis	$V_{VCUV-HS}$		150		mV	
Internal N-Channel MOSFET						
Drain-to-Source Breakdown Voltage	BV_{DSS}	30			V	In OFF state, I_D=250µA , Tj=25°C, Figure 10, Page 11
Source Current Continuous	I_S			12	A	In ON state, Tj=25°C
Drain Leakage Current	I_{DLK}			10	µA	In OFF state, V_{DS}=30V, Tj=25°C
Drain-to-Source On Resistance	R_{DSon}		5.5	7.0	mΩ	In ON state, I_S=8A, Tj=25°C VC-V(S) ≥ 5V
Body Diode Forward Voltage	V_{f-BD}		0.7	1.0	V	In ON state, I_S=4A, Tj=25°C
FAULT						
Under-Voltage Rising Threshold	V_{UVR}		500	540	mV	
Under-Voltage Falling Threshold	V_{UVF}	440	475		mV	
Under-Voltage Threshold Hysteresis	V_{UV-HS}		25		mV	
Under-Voltage Bias Current	I_{UV}	-1		1	µA	
Over-Voltage Rising Threshold	V_{OVR}		500	540	mV	
Over-Voltage Falling Threshold	V_{OVF}	440	475		mV	

Electrical Specifications

Unless otherwise specified: -40°C < T_J < 125°C, VC =12V, C_{Vc} = 1uF, C_{SL} = 10pF

Parameter	Symbol	Min	Typ	Max	Units	Conditions
FAULT (Continued)						
Over-Voltage Threshold Hysteresis	V_{OV-HS}		25		mV	
Over-Voltage Bias Current	I_{OV}	-1		1	µA	
Fault Output Low Voltage	V_{FTL}		0.2	0.5	V	I_{FT}=2mA, VC>3.5V
Fault Output High Leakage Current	I_{FT-LC}			10	µA	V_{FT}=14V
Fault Delay Time	t_{FT-DEL}	20	40	60	µs	Includes output glitch filter
Over Temperature Fault (1)	T_{FT}		160		°C	
Over Temperature Fault Hysteresis(1)	T_{FT-HS}		-10		°C	
DIFFERENTIAL AMPLIFIER AND COMPARATORS						
Common Mode Input Voltage	V_{CM}	-0.1		5.5	V	SP to GND & SN to GND
VC to SP differential(1)	V_{VC-SP}	3.5			V	
Differential Operating Input Voltage	V_{SP-SN}	-50		125	mV	SP-SN
SP Input Bias Current	I_{SP}	-50	-37		µA	SP=SN=1.25V
SN Input Bias Current	I_{SN}		3.5	8	µA	SP=SN=1.25V
SN Voltage	V_{SN}			26.4	V	SP=0V
Reverse Comparator Threshold	V_{RVS-TH}	-10	-6	-2	mV	V_{CM} = 3.3V
Reverse Comparator Hysteresis	V_{RVS-HS}	2		5	mV	V_{CM} = 3.3V
Reverse Fault to Slave Low Delay Time	t_{RVS-MS}		160	200	ns	V_{SP-SN} = -50mV step, V_{BK}=0 (minimum blanking)
Reverse Fault to Slave Low Delay Time	t_{RVS-SL}		430	600	ns	V_{SP-SN} = -50mV step, V_{BK}= V_{VC} (maximum blanking)
Forward Comparator Threshold	V_{FWD-TH}	2	6	9	mV	V_{CM} = 3.3V
Forward Comparator Hysteresis	V_{FWD-HS}	-5		-2	mV	V_{CM} = 3.3V
Forward Over Current Comparator Threshold	V_{OC-TH}	60	66	70	mV	V_{CM} = 3.3V
Forward Over Current Comparator Hysteresis	V_{OC-HS}	-8		-4	mV	V_{CM} = 3.3V
SLAVE						
Slave Source Current	I_{SL}		-60	-25	µA	V_{SL} = 1V, Normal Operating Conditions, No Faults
Slave Output Voltage High	V_{SL-Hi}		4.3	5.5	V	Normal Operating Conditions, No Faults
Slave Output Voltage Low	V_{SL-Lo}		0.2	0.5	V	I_{SL}=4mA
Slave Hold-off Voltage at VC UVLO	V_{SL-UV}		0.7	1	V	I_{SL}=5µA,1.5V<VC<3.5V
SLAVE Threshold	V_{SL-TH}		1.75	2	V	
Slave Fall Time	t_{SL-FL}		15	25	ns	VBK=0
Slave Low to FET Turn Off Delay (1) Time ***Master Mode***	t_{G-SL}		20	30	ns	VBK=0
Slave Low to FET Turn Off Delay (1) Time ***Slave Mode***	t_{G-SL}		100	130	ns	VBK=VC

Electrical Specifications

Unless otherwise specified: -40°C < T_J < 125°C, VC =12V, C_{Vc} = 1uF, C_{SL} = 10pF

Parameter	Symbol	Min	Typ	Max	Units	Conditions
BLANK						
Blank Source Current	I_{BK}	-60	-45	-30	µA	V_{BK}=0V
Blank Output Voltage	V_{BK}		0.77	0.9	V	I_{BK}=5µA Connected to GND
Blank Slave Mode Threshold	V_{BK-TH}	1.2	1.45	1.7	V	

Note 1*:* These parameters are not production tested but are guaranteed by design, characterization and correlation with statistical process control.

Note 2: Current sourced by a pin is reported with a negative sign.

Note 3: Thermal resistance characterized on PI2125-EVAL2 evaluation board with 0 LFM airflow.

Note 4: Refer to the *Auxiliary Power Supply* section in the *Application Information* for details on the VC requirement to fully enhance the internal MOSFET.

Functional Description:

The PI2125 integrated *Cool-ORing* product takes advantage of two different technologies combining a 5.5mΩ on-state resistance (Rds(on)) single N-channel MOSFET with high density control circuitry. This combination provides superior density, minimizing PCB space to achieve an ideal ORing diode function, significantly reducing power dissipation and eliminating the need for heat sinking, while minimizing design complexity.

The PI2125's 5.5mΩ on-state resistance MOSFET used in the conduction path enables a dramatic reduction in power dissipation versus the performance of a diode used in conventional ORing applications due to its high forward voltage drop. This can allow for the elimination of complex heat sinking and other thermal management requirements. Due to the inherent characteristics of the integrated MOSFET, while the gate remains enhanced above the gate threshold voltage it will allow current to flow in the forward and reverse direction. Ideal ORing applications do not allow for reverse current flow, so the integrated controller has to be capable of very fast and accurate detection of reverse current caused by input power source failures, and turn off the gate of the MOSFET as quickly as possible. Once the gate voltage falls below the gate threshold, the MOSFET is off and the body diode will be reverse biased preventing reverse current flow and subsequent excessive voltage droop on the redundant bus. During forward over-current conditions caused by load faults, the controller maintains gate drive to the MOSFET to keep power dissipation as low as possible, otherwise the inherent body diode of the MOSFET would conduct, which has higher effective forward drop. Conventional ORing solutions using diodes offer no protection against forward over-current conditions. During the forward over-current condition, the PI2125 will provide an active-low fault flag to the system via the fault pin. The fault flag is also issued during the reverse current condition, light load conditions, VC under-voltage, Input Under-Voltage and Over-Voltage and Over-Temperature conditions.

Differential Amplifier:
The PI2125 integrates a high-speed, low offset voltage differential amplifier to sense the difference between the Sense Positive (SP) pin voltage and Sense Negative (SN) pin voltage with high accuracy. The amplifier output is connected to three comparators: Reverse comparator, Forward comparator, and Forward over-current comparator.

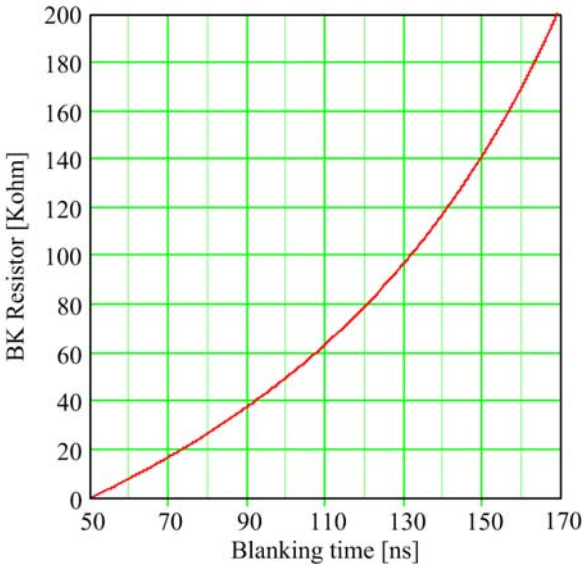
Reverse Comparator: RVS
The reverse comparator is the most critical comparator. It looks for negative voltage caused by reverse current. When the SN pin is 6mV higher than the SP pin, the reverse comparator will enable the BK current source to charge an internal 2pF capacitor. The blanking timer provides noise filtering for typical switching power conversion that might cause premature reverse current detection. Once the voltage across the capacitor reaches the timer threshold voltage (1.25V) the MOSFET will be turned off. The shortest blanking time is 50ns when BK is connected to ground. The Blanking time will be added to the controller delay time. The Electrical Specifications in the *DIFFERENTIAL AMPLIFIER AND COMPARATOR* section for Reverse Fault to Slave Low Delay Time "t_{RVS-MS} or t_{RVS-SL}" is the controller delay time plus the blanking time.

Reverse Blanking Timer: BK
Connecting an external resistor (R_{BK}) between the BK pin and ground will increase the blanking time as shown in the following chart.

Where: $R_{BK} \leq 200K\Omega$

If BK is connected to VC for slave mode operation, then the blanking time will be about 320ns typically, and total delay time will be 430ns.

The reverse comparator has 3mV of hysteresis referenced to SP-SN.
If the conditions are met for a reverse current fault, then the active-low fault flag output will also indicate a fault to the system after the 40µs fault delay time.



Forward Voltage Comparator: FWD

The FWD comparator detects when a forward current condition exists and SP is 6mV positive with respect to SN. When SP-SN is less than 6mV, the FWD comparator will assert the Fault flag to report a fault condition indicative of a light load or "load not present" condition or possible shorted MOSFET.

Forward Over Current Comparator: FOC

The FOC comparator indicates an excessive forward current condition when SP is 66mV (typical) higher than SN. When the FET is in the on-state and SP-SN is higher than 66mV (typical) the PI2125 will initiate a fault condition via the $\overline{FT}$ pin.

Slave:
In high current applications that exceed the single PI2125 current handling capability, multiple PI2125's can be paralleled and synchronized by using the slave function.

The Slave function synchronizes multiple PI2125's together and allows for localized control of each paralleled MOSFET. One PI2125 will be designated as the master and it will control the response of the slaved PI2125's.

When the PI2125 is configured in the "Master Mode" by connecting the BK to ground, the $\overline{SL}$ will be an output having the same signal characteristics as the internal Gate Driver. In this configuration, the $\overline{SL}$ output is capable of driving up to ten PI2125's, configured in "Slave Mode", through their corresponding $\overline{SL}$ pins. Logic high for the $\overline{SL}$ pin is limited to 5.5V (max).

When the BK pin is tied to VC, the PI2125 becomes a slave and the $\overline{SL}$ pin will be an input. The internal Gate driver section and reverse current section are the only active circuits in the slaved PI2125 while the master performs the diagnostics and gate drive control.

VC and Internal Voltage Regulator:
The PI2125 has a separate input (VC) that provides power to the control circuitry and the internal gate driver. An internal regulator clamps the VC voltage to 15.5V.

For high side applications, the VC input should be at least 6V above the bus voltage (Vin) to properly enhance the internal N-channel MOSFET. For bus voltages higher than 10V (15.5V – 5.5V), the PI2125 should be floated to Vin as shown in Figure 23, and a resister has to be added in series between Vaux and VC. The required resister value calculation is shown in the application section of this document.

The internal regulator circuit has a comparator to monitor the VC voltage and initiates a FAULT condition when VC is lower than the VC Under-Voltage Threshold

UV:
The Under-Voltage (UV) input trip point can be programmed through an external resistor divider to monitor the input voltage, when the PI2125 is used in ground referenced applications. The UV comparator initiates a fault condition and pulls the $\overline{FT}$ pin low, when UV falls below the Under-Voltage Falling Threshold. If the PI2125 is configured in a floating application, where the GND pin is connected to the input voltage, as shown in Fig 23, the UV pin cannot detect the input voltage. In this case, the UV pin should be disabled by connecting it to the VC pin.

OV:
The Over-Voltage (OV) input trip point can be programmed through an external resistor divider to monitor the input voltage, when the PI2125 is used in ground referenced applications. The OV comparator initiates a fault condition and pulls the $\overline{FT}$ pin low when OV rises above the Over-Voltage Rising Threshold. If the PI2125 is configured in a floating application, where the GND pin is connected to the input voltage, as shown in Fig 23, the OV pin cannot detect the input voltage. In this case, the OV pin should be disabled by connecting it to controller ground pin.

Over-Temperature Detection:
The internal Over-Temperature block monitors the junction temperature of the controller. The over-temperature threshold is set to 160°C with -10°C of hysteresis. When the controller temperature exceeds this threshold, the over-temperature circuit initiates a fault condition and pulls the $\overline{FT}$ pin low.

Fault:
The fault circuit output is an open collector with 40µs delay to prevent any false triggering. The $\overline{FT}$ pin will be pulled low when any of the following faults occurs:

- Reverse Current
- Forward Over-Current
- Forward Low Current
- Over-Temperature
- Input Under-Voltage
- Input Over-Voltage
- VC pin Under-Voltage

A gate voltage detector prevents FOC or FWD from initiating a fault when the MOSFET is in an OFF condition.

The only fault condition that initiates gate turn-off of the MOSFET (as well as a fault flag signal) is when the reverse current fault conditions are met. All other fault conditions issue only a fault flag signal via the $\overline{FT}$ pin, but do not affect the gate of the MOSFET. The $\overline{FT}$ pin serves as an indicator that a fault condition may be present. This information can be reported to a Host to signal that some system level maintenance may be required.

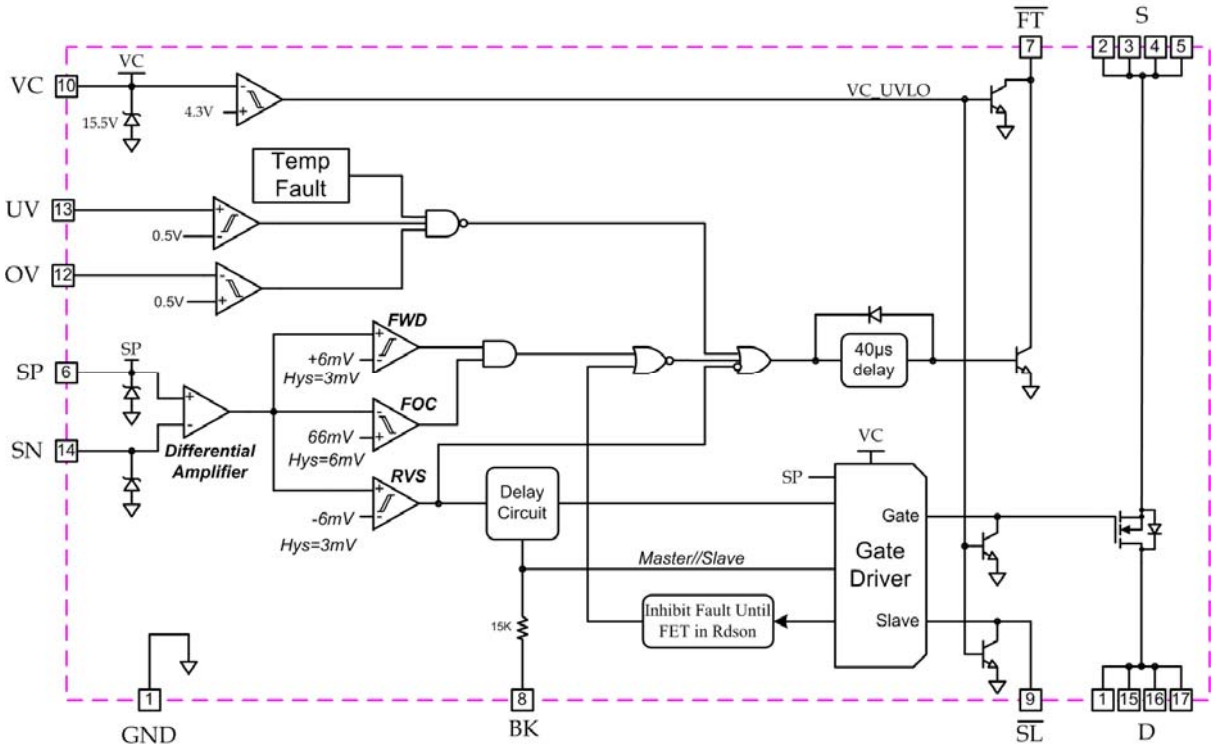


Figure 3: **PI2125** Internal Block Diagram

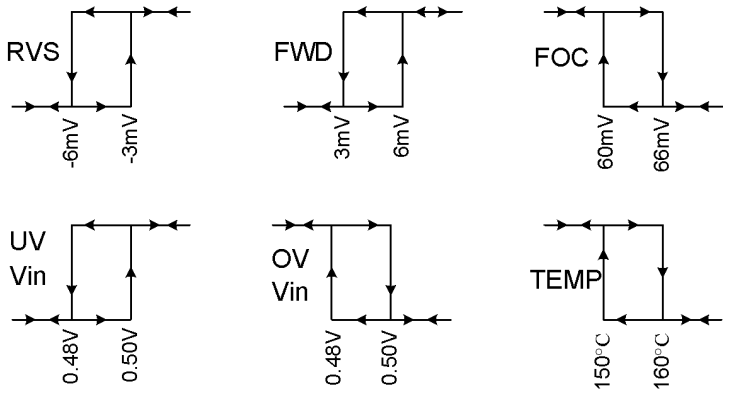


Figure 4: Comparator hysteresis, values are for reference only. Please refer to the electrical specifications.

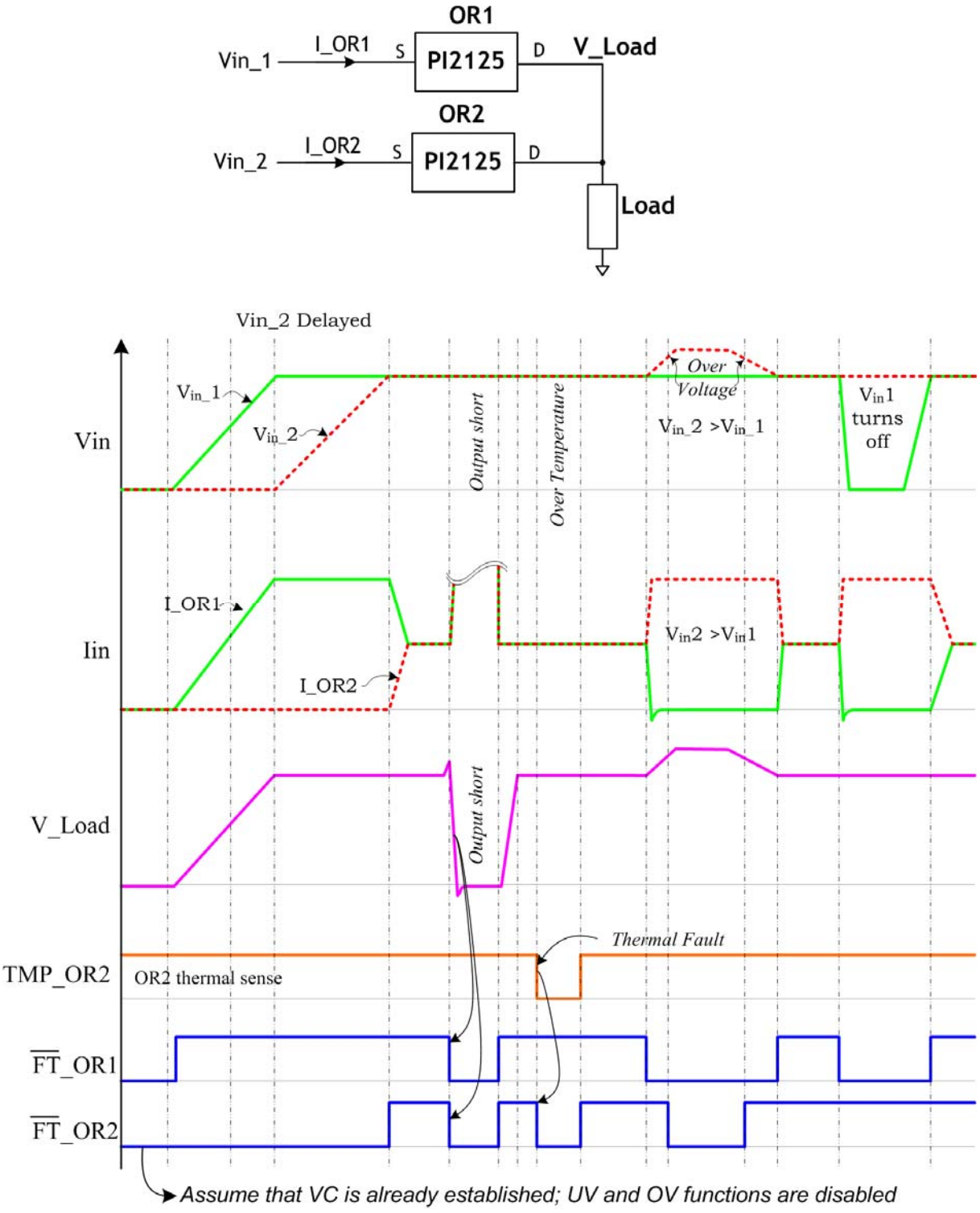


Figure 5: Timing diagram for two PI2125 solutions in an Active ORing application

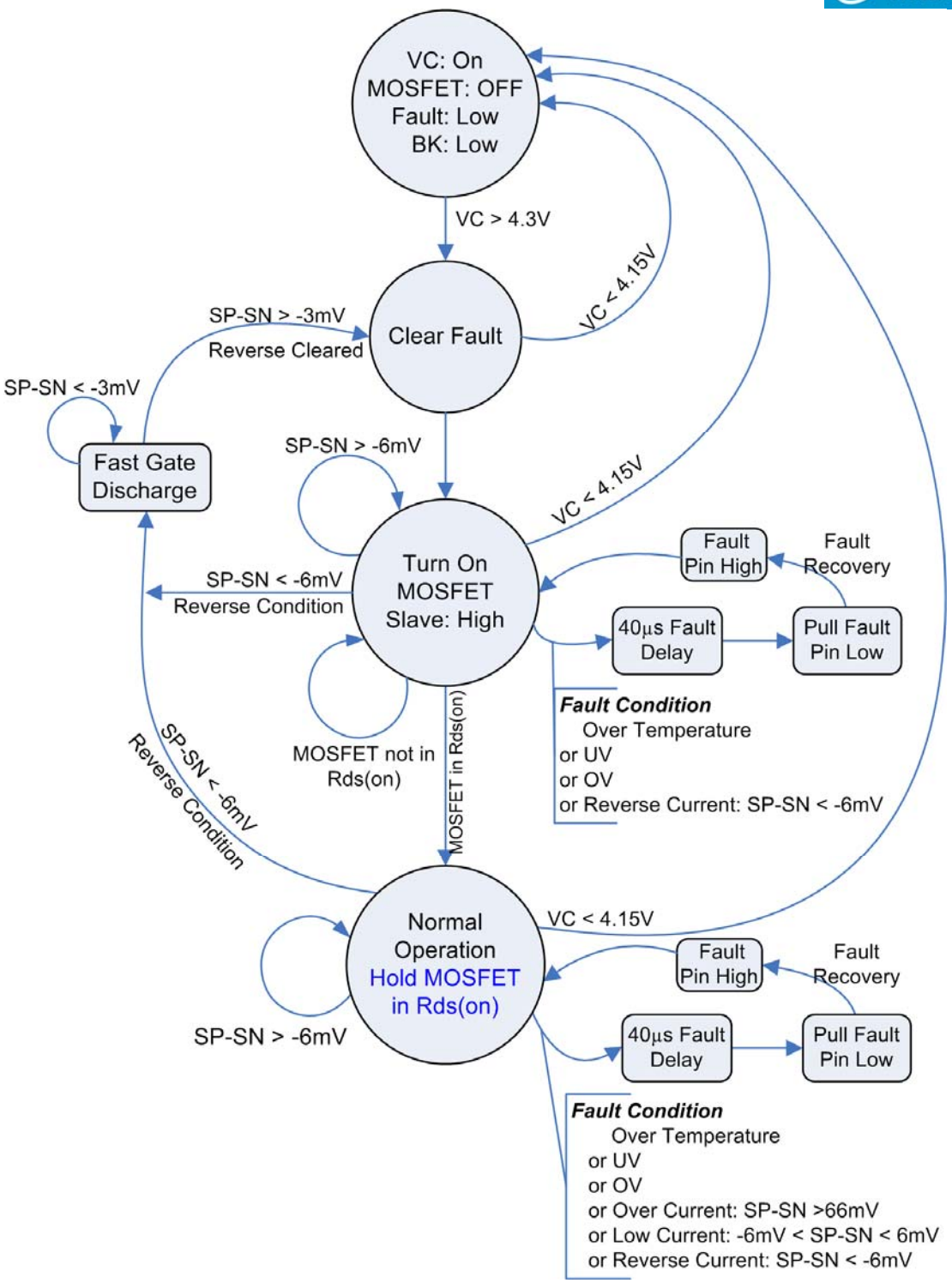


Figure 6: PI2125 State diagram, Master Mode

Typical Characteristics:

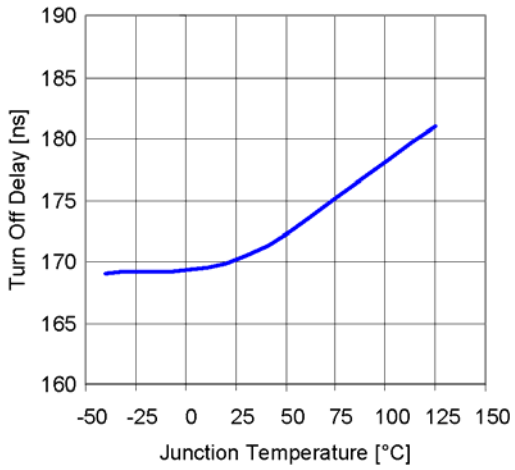


Figure 7: Reverse Condition internal MOSFET Turn off delay time vs. temperature.

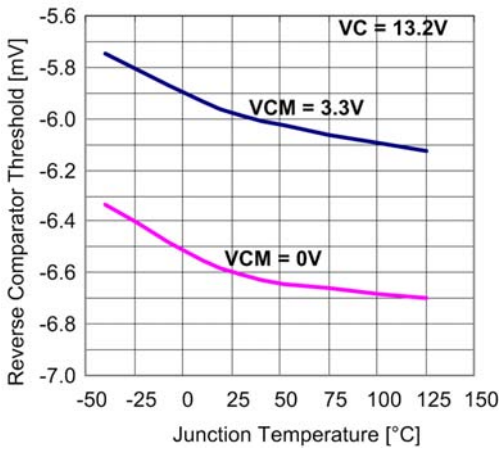


Figure 8: Reverse comparator threshold vs. temperature.
V*CM:* *Common Mode Voltage*

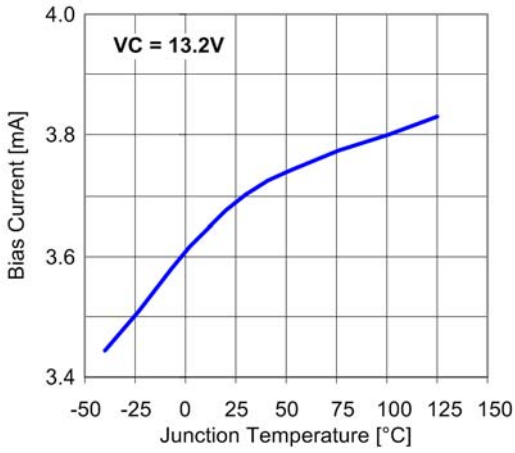


Figure 9: Controller bias current vs. temperature

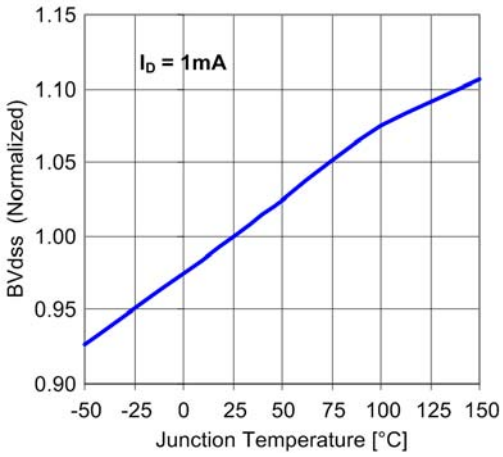


Figure 10: Internal MOSFET drain to source breakdown voltage vs. temperature

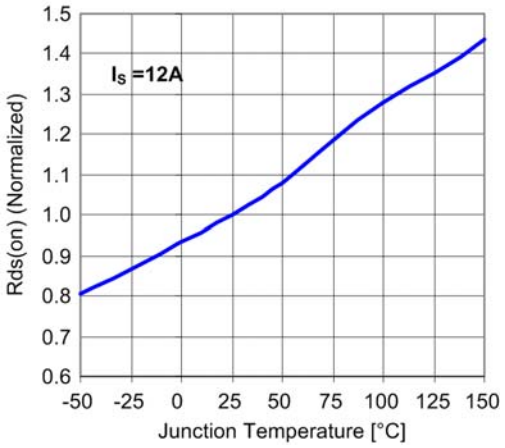


Figure 11: Internal MOSFET on-state resistance vs. temperature

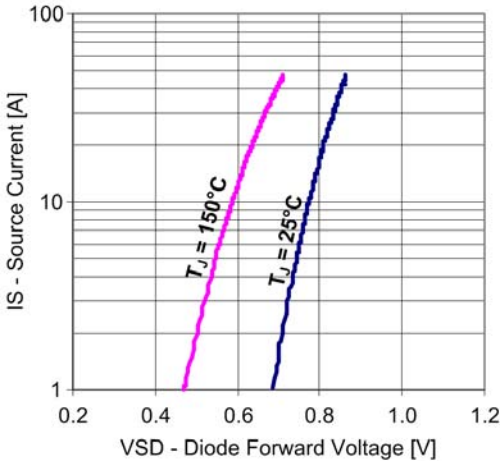


Figure 12: Internal MOSFET source to drain diode forward voltage (pulsed ≤ 300μs)

Thermal Characteristics:

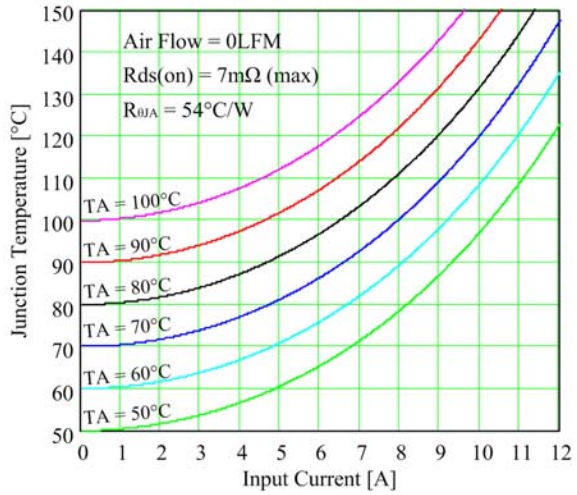


Figure 13: Junction Temperature vs. Input Current (0LFM)

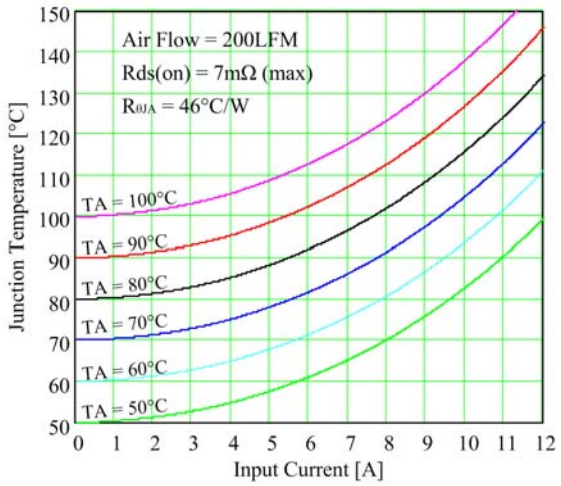


Figure 14: Junction Temperature vs. Input Current (200LFM)

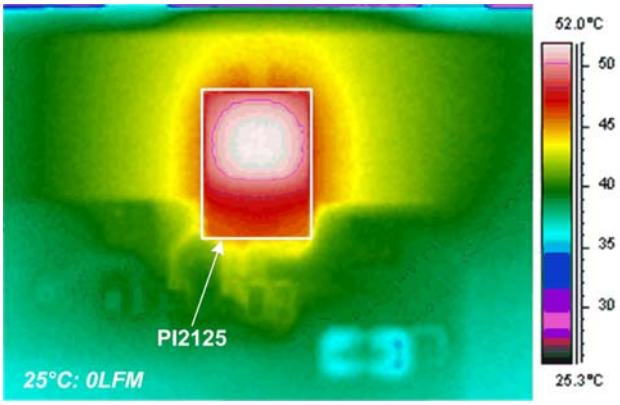


Figure 15: PI2125 mounted on PI2125-EVAL Thermal Image picture, Iout=12A, T_A=25°C, Air Flow=0LFM

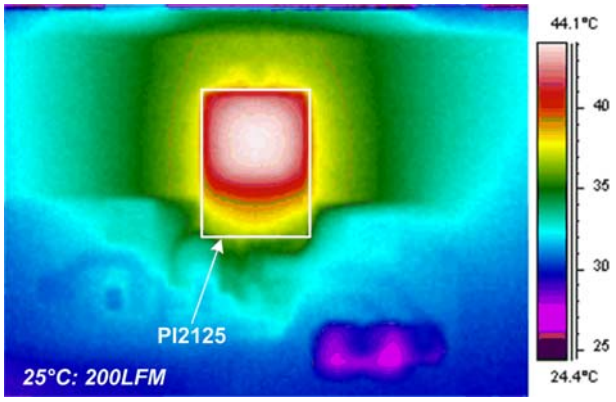


Figure 16: PI2125 mounted on PI2125-EVAL Thermal Image picture, Iout=12A, T_A=25°C, Air Flow=200LFM

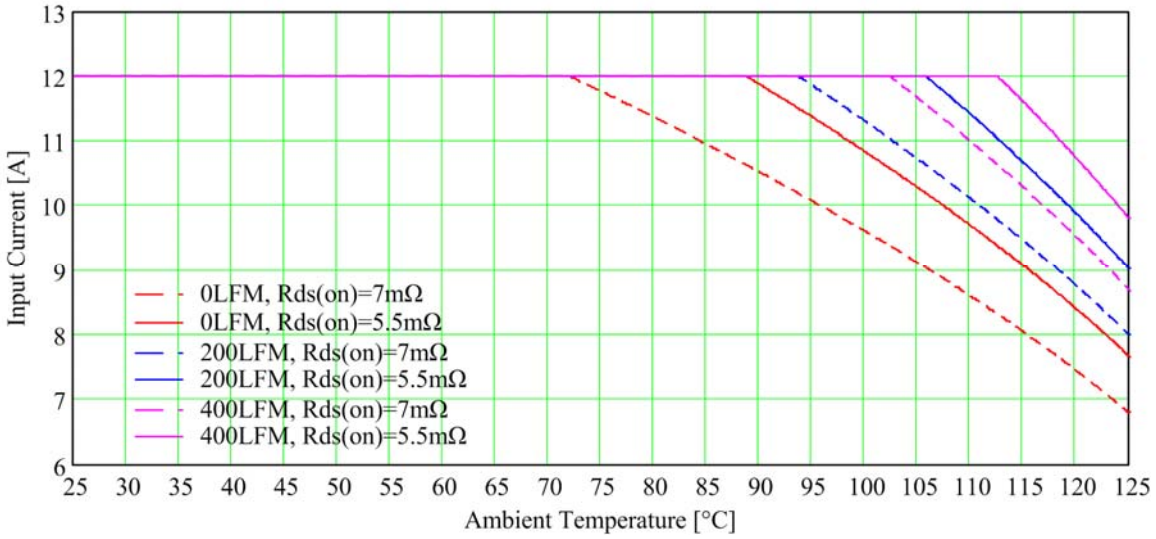


Figure 17: PI2125 input current de-rating based on maximum T_J=150°C vs. ambient temperature

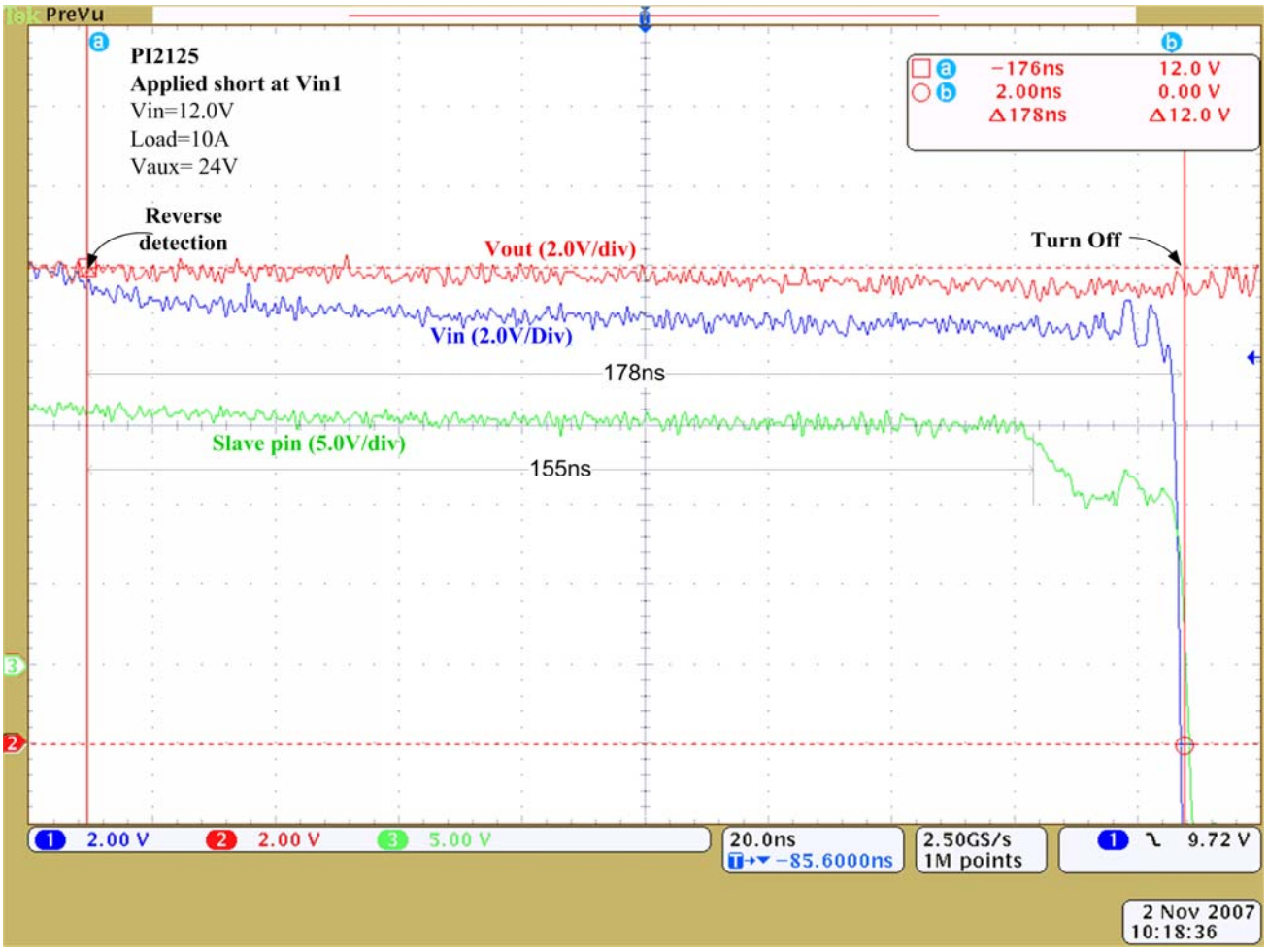


Figure 18: Plot of PI2125 response time to reverse current detection (Example 1, Figure 23)

Application Information

The PI2125 is designed to replace ORing diodes in high current, low voltage redundant power architectures. Replacing a traditional diode with a PI2125 will result in significant power dissipation reduction as well as board space reduction, efficiency improvement and additional protection features. This section describes in detail the procedure to follow when designing with the PI2125 Active ORing solution.

Fault Indication:

The $\overline{FT}$ output pin is an open collector and should be pulled up to the logic voltage or to the controller VC via a resistor (10KΩ).

In a floating configuration, the $\overline{FT}$ pin is referenced to the PI2125 GND pin which is referenced to the input voltage, Vin. The $\overline{FT}$ output status can be reference to the system ground by adding a level shifting circuit, as shown in figure 19. The level shift circuit can be designed with one small and inexpensive off-the-shelf device, a Dual Bias Resistor Transistor, containing NPN and PNP transistors with their bias resistors, NSBC114EPDXV6T1.

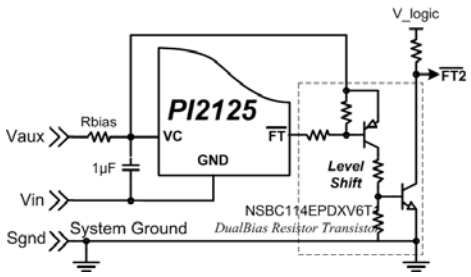


Figure 19: $\overline{FT}$ Level shift circuit

Blanking Timer:
Connect the blanking timer pin (BK) to GND to program the device for the fastest reverse comparator response time of 160ns typical. To increase the blanking time, connect the BK pin to GND via a resistor to avoid the fault response to short reverse current pulses. Refer to the plot in the reverse comparator functional description for resistor values versus the reverse blanking time.

Auxiliary Power Supply (Vaux):
Vaux is an independent power source required to supply power to the VC input. The Vaux voltage should be 6V higher than Vin (redundant power source output voltage) to fully enhance the internal MOSFET.

A bias resistor (Rbias) is required if Vaux is higher than 15V. Rbias should be connected between the VC pin and Vaux.

Minimize the resistor value for low Vaux voltage levels to avoid a voltage drop that may reduce the VC voltage lower than required to drive the gate of the internal MOSFET.

Select the value of Rbias using the following equations:

$$Rbias = \frac{Vaux_{\min} - VC_{clamp}}{IC_{\max}}$$

Rbias maximum power dissipation:

$$Pd_{Rbias} = \frac{(Vaux_{\max} - VC_{clamp})^2}{Rbias}$$

Where:

$Vaux_{\min}$: Vaux minimum voltage

$Vaux_{\max}$: Vaux maximum voltage

VC_{Clamp} : Controller clamp voltage, 15.5V

$IC_{\max}$: Controller maximum bias current, use 4.2mA

Example: Vaux 20V to 30V

$$Rbias = \frac{Vaux_{\min} - VC_{clamp}}{IC_{\max}} = \frac{20V - 15.5V}{4.2mA} = 1.07K\Omega$$

$$Pd_{Rbias} = \frac{(Vaux_{\max} - VC_{clamp})^2}{Rbias} = \frac{(30V - 15.5V)^2}{1.07K\Omega} = 196mW$$

Internal N-Channel MOSFET BVdss:
The PI2125's internal N-Channel MOSFET breakdown voltage (BVdss) is rated for 30V at 25°C and will degrade at -40°C to 28V, refer to Figure 10. In an application when the MOSFET is turned off due to a reverse fault, the series parasitic elements in the circuit may contribute to the MOSFET being exposed to a voltage higher than its voltage rating.

In Active ORing applications when one of the input power sources is shorted, a large reverse current is sourced from the circuit output through the MOSFET. Depending on the output impedance of the system, the reverse current may reach over 60A in some conditions before the MOSFET is turned off. Such high current conditions will store energy even in a small parasitic element. For example: a 1nH parasitic inductance with 60A reverse current will generate 1.8µJ (½LI^2). When the MOSFET is turned off, the stored energy will be released and produce a high negative voltage ringing at the MOSFET source. At the same time the energy stored at the drain side of the internal MOSFET will be released and produce a voltage higher than the load voltage. This event will create a high voltage difference between the drain and source of the MOSFET. To reduce the magnitude of the ringing voltage, add a ceramic capacitor very close to the source that can react to the voltage ringing frequency and another capacitor close to the drain. Recommended values for the ceramic capacitors are 1µF, refer to C4 and C6 in Figure 24.

Slave:
For a high current application where one PI2125 can not handle the total load current, multiple PI2125's can be paralleled in a master / slave configuration to support the total current per input. In the Master / Slave mode, one PI2125 is configured as the master and the rest are configured as slaves. The slave ($\overline{SL}$) pin of the master unit will act as an output driving the units configured in slave mode. The $\overline{SL}$ pins of the slave units will act as inputs under the control of the master.

Tie the BK pin to VC to configure the unit in slave mode.

Power dissipation:
In active ORing circuits the MOSFET is always on in steady state operation mode and the power dissipation is derived from the total source current and the on-state resistance of the internal MOSFET.

The PI2125 internal MOSFET power dissipation can be calculated with the following equation:

$$Pd_{MOSFET} = Is^2 * Rds(on)$$

Where:
Is : Source Current
Rds(on) : MOSFET on-state resistance

Note:
Calculate with Rds(on) at maximum MOSFET temperature because Rds(on) is temperature dependent, Refer to figure 11 for normalized Rds(on) values over temperature. PI2125 nominal Rds(on) at 25°C is 3mΩ and will increase by 35% at 125°C junction temperature.

The junction temperature rise is a function of power dissipation and thermal resistance.

$$Trise = Rth_{JA} * Pd_{MOSFET} = Rth_{JA} * Is^2 * Rds(on),$$

Where: Rth_{JA}: Junction-to-Ambient thermal resistance (54°C/Watt)(3)

This may require iteration to get to the final junction temperature. Figures 13, 14, and 17 show the PI2125 internal MOSFET final junction temperature curves versus conducted current at given ambient temperatures and air flow.

OV/UV resistor selection:
The UV and OV comparators inputs are used to monitor the input voltage and will indicate a fault condition when this voltage is out of range. It can be used to monitor the input voltage (Vin) level if the PI2125 is referenced to the same ground as Vin. If the PI2125 is floating on Vin then OV and UV can not monitor Vin and should be disabled by connecting UV to the VC pin and OV to the GND pin of the same PI2125.

The Fault pin ($\overline{FT}$) will indicate a fault (active low) when the UV pin is below the threshold or when the OV pin is above the threshold. The threshold is 0.50V typical with 25mV hysteresis and the input current is less than ±1µA. It is important to consider the maximum current that will flow in the resistor divider and maximum error due to UV and OV input current. Set the resistor current to 100µA or higher to maintain better than 1% accuracy for UV and OV due to the bias current.

The three-resistor voltage divider configuration for both UV and OV to monitor the same voltage node is shown in Figure 20:

$$Ra = \frac{V(OV_{TH})}{I_{Ra}}$$

Set Ra value based on system allowable current I_{Ra}

$$Rb = Ra\left(\frac{V(OV)}{V(UV)} - 1\right)$$

$$Rc = (Ra + Rb)\left(\frac{V(UV)}{V(UV_{TH})} - 1\right)$$

Where:
$V(UV_{TH})$: UV threshold voltage at Vin.
$V(OV_{TH})$: OV threshold voltage at Vin.
$V(UV)$: UV voltage set
I_{Ra} : Ra current.

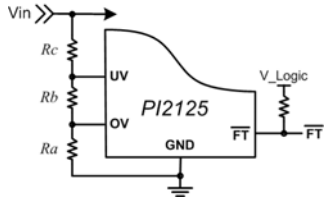


Figure 20: UV & OV three-resistor divider configuration

Alternatively, a two-resistor voltage divider configuration can be used and is shown in Figure 21.

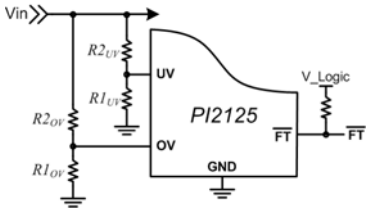


Figure 21: UV & OV two-resistor divider configuration

UV resistor voltage divider from the following equations:

$$R1_{UV} = \frac{V(UV_{TH})}{I_{RUV}}$$

Set $R1_{UV}$ value based on system allowable current $I_{RUV} \geq 100\mu A$

$$R2_{UV} = R1_{UV}\left(\frac{V(UV)}{V(UV_{TH})} - 1\right)$$

Where:

$V(UV_{TH})$: UV Threshold Voltage

I_{RUV} : $R1_{UV}$ current

$$R1_{UV} = \frac{V(UV_{TH})}{I_{RUV}}$$

Set $R1_{OV}$ value based on system allowable current $I_{RUV} \geq 100\mu A$

$$R2_{OV} = R1_{OV}\left(\frac{V(OV)}{V(OV_{TH})} - 1\right)$$

Where:
$V(OV_{TH})$: OV threshold voltage
I_{ROV} : $R1_{OV}$ current.

Typical Application Example 1:

Requirement:
Redundant Bus Voltage = 12V
Load Current = 10A (assume through each redundant path)
Maximum Ambient Temperature = 70°C; no air flow
Auxiliary Voltage = 24V±10% (21.6V to 26.4V).

Solution:

A single PI2125 for each redundant 12V power source should be used. Vin is 12V which is higher than the SP pin maximum voltage rating of 8V, so the PI2125 should be configured in the floating configuration as shown in Figure 23. PI2125 is floated on Vin by connecting it's GND pin and the low side of the VC coupling capacitor to Vin.

Vaux: Make sure that the Vaux voltage is always higher than Vin (dc-dc converter output) by 6.0V to ensure that the internal MOSFET is fully enhanced.

Since the auxiliary voltage is higher than the PI2125 VC clamp voltage a bias resistor (Rbias) is needed in series with the VC pin.

Rbias value:

$$Rbias = \frac{21.6V - 15.5V}{4.2mA} = 1.45K\Omega$$ or 1.43KΩ

Rbias Power dissipation rating

$$Pd_{Rbias} = \frac{(26.4V - 15.5)^2}{1.43K\Omega} = 83mW$$

Based on the resultant power dissipation on the bias resistor, use a ¼W rated resistor.

SP and SN pins: Since the PI2125 is floating, the GND pin and S pin are connected to Vin, so connect the SP pin directly to the PI2125 GND pin to reduce the effect of parasitics between the SP pin and the GND pin. This will avoid negative voltages on the SP pin with respect to the GND pin. Connect SN to the D pin.

BK pin: Connect the BK pin to the GND pin to achieve the minimum reverse current response time

$\overline{SL}$ **pin:** Not required, so leave floating

Fault pin: The $\overline{FT}$ pin output is referenced to the PI2125 GND pin which is connected to Vin. A level shift circuit can be added to make $\overline{FT}$ output referenced to the system ground. The recommended level shift circuit is shown in Figure 23. The level shift circuit uses a Dual Bias Resistor

Transistor circuit which is available as a small device that contains two transistors and their bias resistors.

UV and OV inputs: In floating applications these pins can not be used to monitor Vin. Connect UV to the VC pin and OV to the GND pin to disable their function.

Power Dissipation and Junction Temperature:
First use Figure 13 (Junction Temperature vs. Input Current) to find the final junction temperature at 10A load current and 70°C ambient temperature. In Figure 13 (illustrated in Figure 22) draw a vertical line from 10A to intersect the TA=70°C line. At the 10A and TA=70°C line intersection draw a horizontal line towards the Y-axis (Junction Temperature). The Junction Temperature at full load current (10A) and 70°C ambient is 120°C.

Rds(on) is 7.0mΩ maximum at 25°C and will increase as the Junction temperature increases. From Figure 11, at 120°C Rds(on) will increase by ~35%, then

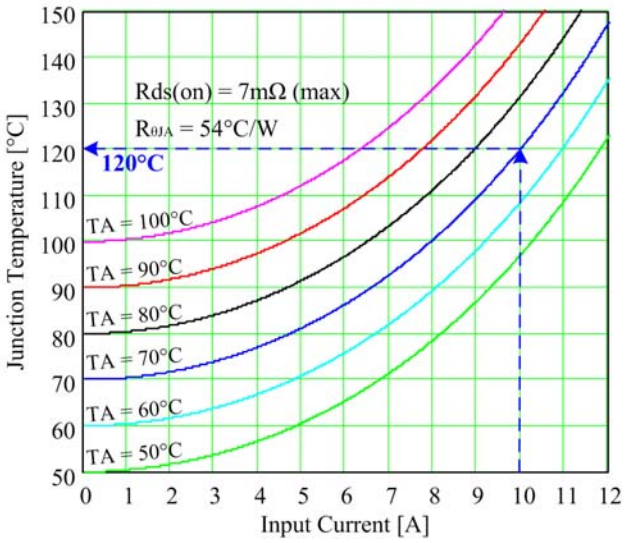


Figure 22: Example 1 final junction temperature at 10A/70°C T_A

$Rds(on) = 7.0m\Omega \bullet 1.35 = 9.45m\Omega$ maximum at 120°C

Rth_{JA} : 54°C/W

$$T_J = T_A + Rth_{JA} * Is^2 * Rds(on)$$

Recalculate T_J:

$$T_J = 70°C + \left(\frac{54°C}{W} * (10A)^2 * 9.45m\Omega\right) = 121°C$$

Maximum power dissipation at 121°C:

$$Pd_{max} = Iin^2 * Rds(on) = (10A)^2 * 9.45m\Omega = 945mW$$

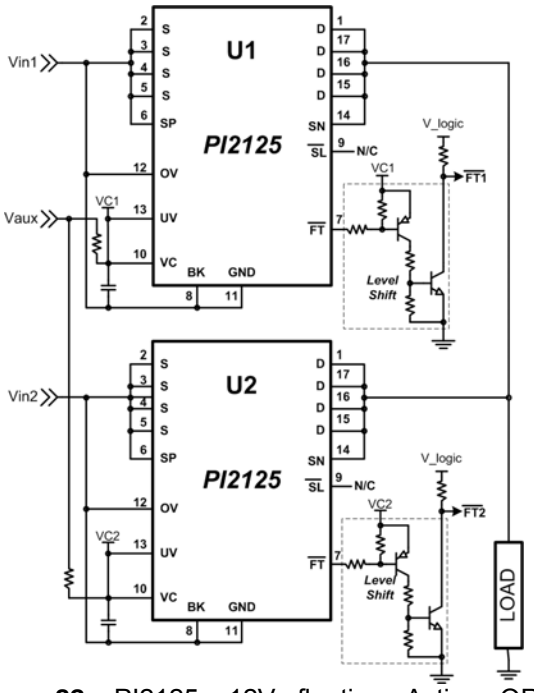


Figure 23: PI2125, 12V floating Active ORing application

Reverse current threshold:
The following procedure demonstrates how to calculate the minimum required reverse current in the internal MOSFET to generate a reverse fault condition and turn off the internal MOSFET.

At room temperature (25°C) typical Rds(on):

$$Is.reverse = \frac{Vth.reverse}{Rds(on)} = \frac{-6mV}{5.5m\Omega} = -1.1A$$

At maximum junction temperature (121°C) and maximum Rds(on):

$$Is.reverse = \frac{Vth.reverse}{Rds(on)} = \frac{-6mV}{9.45m\Omega} = -635mA$$

Layout Recommendation:

Use the following general guidelines when designing printed circuit boards. An example of the typical land pattern for the PI2125 in floating configuration is shown in Figure 24:

- Make sure to have a sold ground (return) plane to reduce circuit parasitics.
- In floating configuration, connect the GND pin to the S pins with a solid plane. In the event it can not be done on the top plane, create a plane on the second layer and use multiple vias from the S pins to the second layer to reduce parasitics. Connect the SP pin directly to the PI2125 GND pin to reduce parasitics between the SP pin and the GND pin to avoid negative voltages on the SP pin with respect to the GND pin.
- Connect all S pads together with a wide trace to reduce trace parasitics to accommodate the high input current, and also connect all D pads together with a wide trace to accommodate the high output current.
- Use 1oz of copper or thicker if possible to reduce trace resistance and reduce power dissipation.
- The VC bypass capacitor should be located as close as possible to the VC and GND pins. Place the PI2125 and bypass capacitor on the same layer of the board. The VC pin and C_{VC} PCB trace should not contain any vias.
- Keep the power source very close to S input pins, since any parasitic in the trace connecting the power source and S pins will have inductive kick back when there is high current flow in the trace and the MOSFET turns off due to reverse current fault conditions. The inductive kick back will produce a high voltage across the MOSFET. If it is not possible to connect the power source and S pins with a very short trace or common point, connect the capacitor (shown as C4 in figure 24) close to the S pins and return (ground). Also for the same reason use C6, in figure 24 at the output.

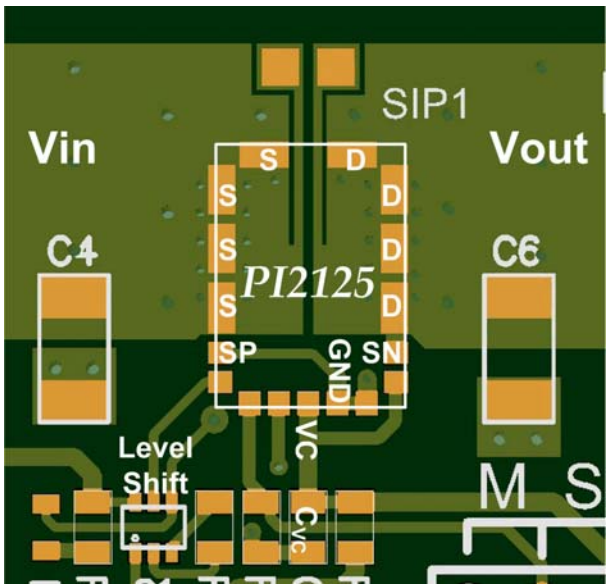


Figure 24: PI2125 layout recommendation

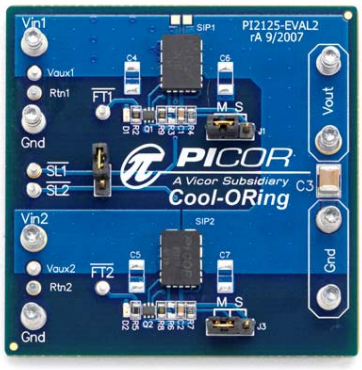
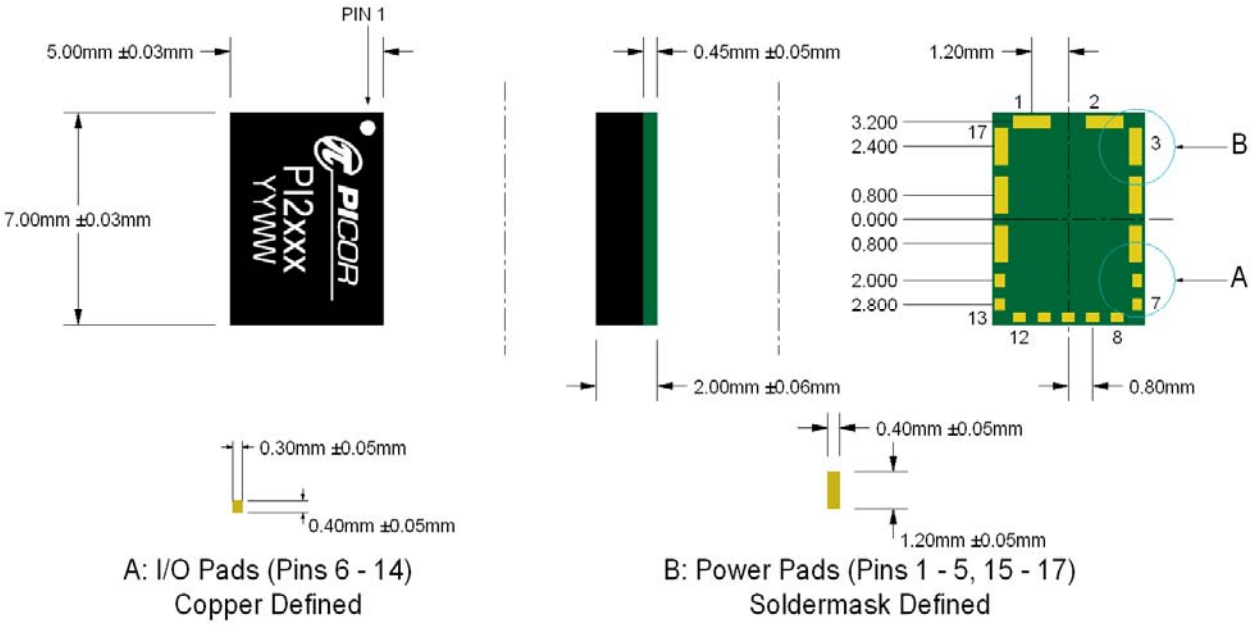


Figure 25: PI2125 Mounted on PI2125-EVAL2

Please visit www.picorpower.com for information on PI2125-EVAL2

Package Drawing



Thermal Resistance Ratings

Parameter	Symbol	Typical	Max	Unit
Junction-to-Ambient [3]	θ_{JA}	-	54	°C/W
Junction-to-PCB	θ_{JC}	14	-	°C/W

Note 3: Thermal resistance characterized on PI2125-EVAL2 evaluation board with 0 LFM airflow.

Ordering Information

Part Number	Package	Transport Media
PI2125-00-LGIZ	5x7mm 17-pin LGA	Tape & Reel

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