ANALOG DEVICES

Circuit Note
CN-0283

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Devices Connected/Referenced	
ADL5375	400 MHz to 6 GHz Broadband Quadrature Modulator
ADL5320	400 MHz to 2700 MHz ¼ Watt RF Driver Amplifier

Providing Fixed Power Gain at the Output of an IQ Modulator

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

ADL5375 Evaluation Board (ADL5375-05-EVALZ)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

Whether an IQ modulator is used in a direct conversion application or as an upconverter to a first intermediate frequency (IF), some gain is generally applied directly after the IQ modulator. How to choose an appropriate driver amplifier to provide the first stage of gain at the output of an IQ modulator will be described. The devices shown in Figure 1 are the ADL5375 IQ modulator and the ADL5320 driver amplifier. They are well matched from a system performance level; that is, they have equivalent performance so neither device contributes to degradation in the overall performance. Because these devices are well matched in terms of their dynamic ranges, a simple direct connection between the IQ modulator and the RF driver amplifier is recommended without any need for attenuation between the devices.

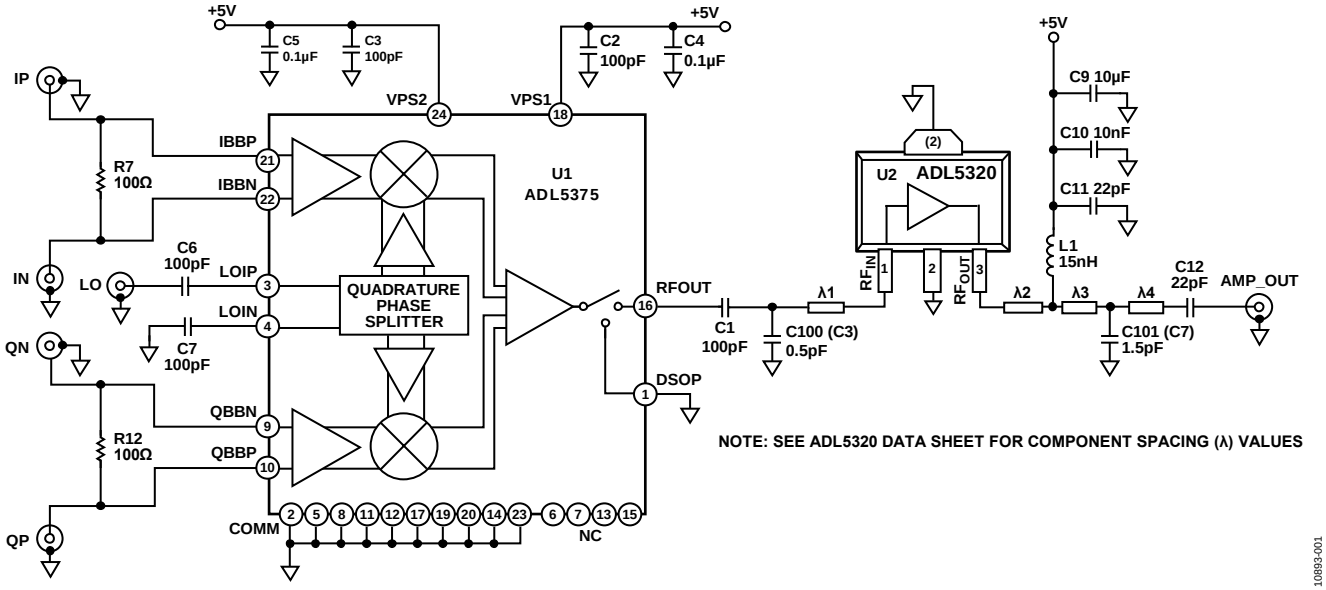

Figure 1. Circuit Schematic for IQ Modulator with Output Power Gain

Rev. 0

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CIRCUIT DESCRIPTION

The ADL5375 is a general-purpose, high performance IQ modulator. It operates at output frequencies from 400 MHz to 6 GHz. Because of its low noise and wide input baseband bandwidth (3 dB) of 750 MHz, it can be driven by signals with a wide variety of modulations and bandwidths. These input signals can be centered at dc or at a complex IF.

The LO interface to the ADL5375 is a 1XLO type, that is, the output frequency and LO frequency is equal (when the baseband signal is centered at dc). Circuit Note CN-0134 describes how the ADL5375 can be driven by the ADF4350.

System Level Calculations and RF Amplifier Choice

In the 1 GHz to 2 GHz frequency range, the ADL5375 has an output compression point (OP1dB) and a third-order compression point (OIP3) of approximately 10 dBm and 25 dBm, respectively. In choosing an RF amplifier to provide gain after the IQ modulator, it is important to choose a device whose input P1dB and input IP3 are equal or a little bit higher than these numbers. Choosing a device with lower specifications results in degraded performance for the cascade while choosing a device whose input P1dB and input IP3 are significantly higher than those of the ADL5375, has little benefit and is likely to needlessly increase the overall supply current of the signal chain.

The ADL5320 is a driver amplifier (RF amplifier that requires external tuning components) that is specified for operation from 400 MHz to 2700 MHz. It consumes 104 mA when operating from a 5 V supply (operation down to 3.3 V is possible with reduced power consumption and performance).

Table 1 shows the output-referred IP3 (OIP3) and P1dB (OP1dB) of the ADL5375 IQ modulator along with the input-referred specifications of the ADL5320 driver amplifier at 1900 MHz. In both cases, there is approximately a 3 dB difference between the output-referred specifications of the IQ modulator and the input-referred specifications of the amplifier.

Table 1. IP3 and P1dB Specifications for the ADL5375 IQ Modulator and the ADL5320 Driver Amplifier at 1900 MHz

Parameter	ADL5375 (Output Referred)	ADL5320 (Input Referred)
IP3	24.2 dBm	28.3 dBm
P1dB	10 dBm	13 dBm

Figure 2 shows the simulated cascaded performance of the IQ modulator and drive amplifier at 2140 MHz. This simulation was done using the ADIsimRF Design Tool. It is notable that the 12.3 dB difference between the OIP3 of the modulator (24.2 dBm) and the composite OIP3 (36.5 dBm) is just slightly less than the gain of the ADL5320 driver amplifier, 13.7 dB. This indicates that the driver amplifier has only a very slight effect on the overall OIP3.

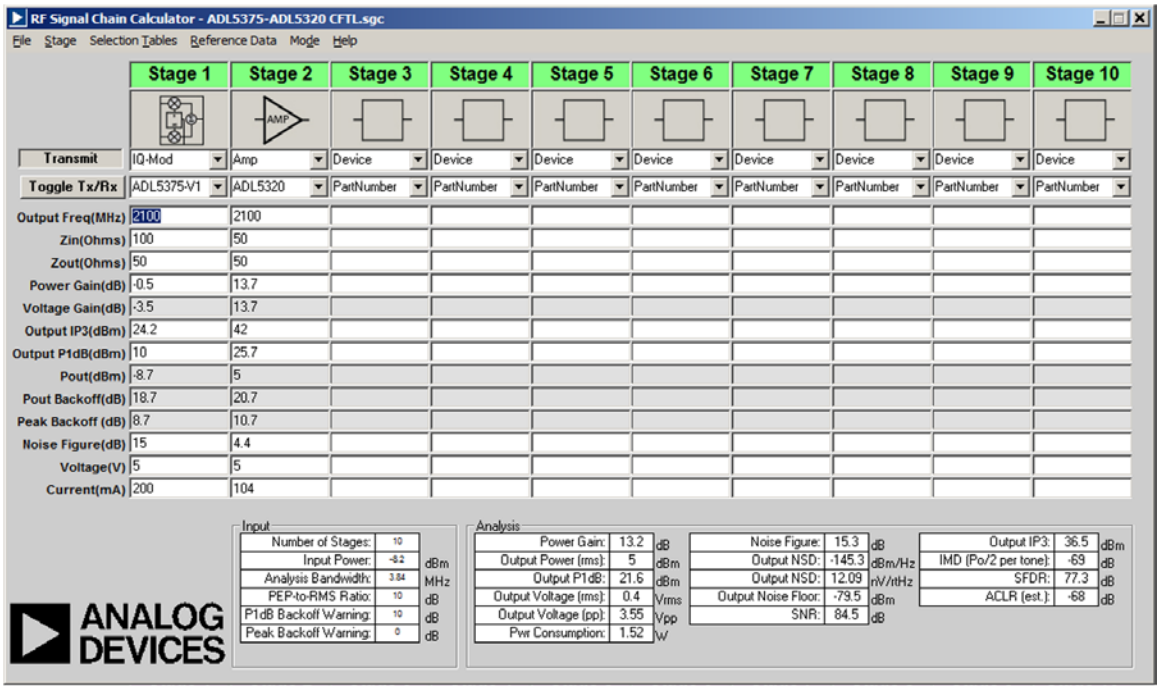

Figure 2. ADIsimRF Design Tool Screenshot Showing Cascaded Performance of ADL5375 and ADL5320

Figure 3 shows a plot of OIP3 vs. output power (P_{OUT}) measured at the IQ modulator output and at the output of the composite circuit. The shape of the two OIP3 profiles are quite similar, just shifted in terms of output power and OIP3. This reinforces the idea that the IP3 is only slightly degraded as the signal passes through the RF amplifier

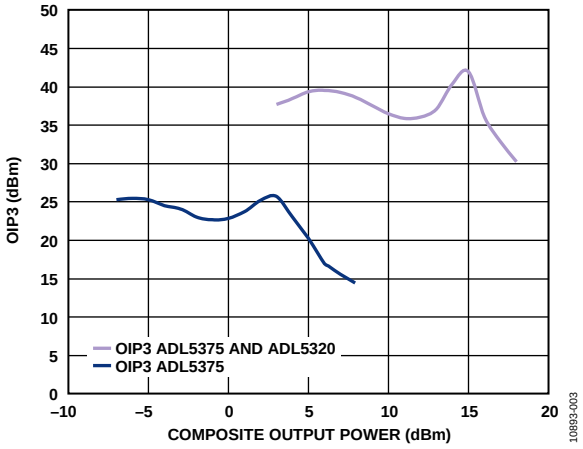

Figure 3. OIP3 vs. P_{OUT} at 2100 MHz for ADL5375 IQ Modulator and for the Composite Circuit (ADL5375 and ADL5320 Driver Amplifier)

Choosing an Output Power Level

While the circuit achieves OIP3 levels in the 35 dBm to 40 dBm range for output power levels up to 15 dBm, operation is not practical up to these levels, particularly with nonconstant envelope modulation schemes that tend to have relatively high peak-to-average ratios. To understand why, look at the volts-in to power-out transfer function of the circuit and consider the typical drive levels that are available at the input to the IQ modulator.

Figure 4 shows the transfer function of the circuit in terms of output power (in dBm) and input voltage (in V p-p) with a CW sine wave, drive signal. An IQ modulator, such as the ADL5375, is driven typically by a dual, current-out, digital-to-analog converter (DAC). Normally, the two current outputs (0 mA to 20 mA nominal) of the DAC are terminated to ground with two 50 Ω resistors and two 100 Ω shunt resistors are placed across each of the IQ inputs (for more information on this interface, see Circuit Note CN-0205). With the DAC running at 0 dBFS, this corresponds to a drive level at the IQ modulator of 1 V p-p or 0.353 V rms (this is neglecting the insertion loss of the low-pass filter that is generally placed between the DAC and the IQ modulator). This results in an output power of approximately 13 dBm.

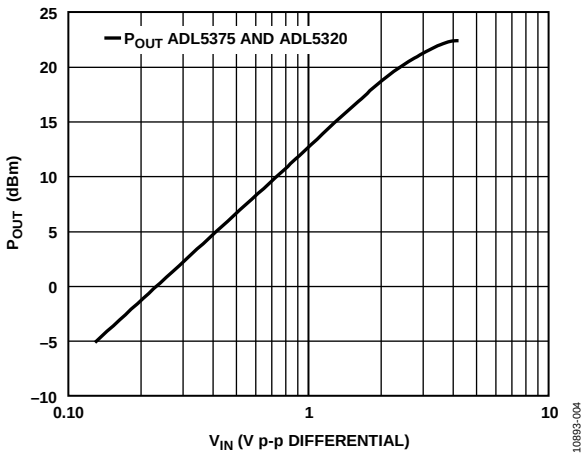

Figure 4. Transfer Function of Circuit in Terms of Output Power in dBm and Input Level in V p-p Differential

If it is assumed that the I and Q inputs of the IQ modulator are terminated with 100 Ω as previously discussed, the output power relative to the dBFS drive level of a typical Analog Devices, Inc., DAC can be plotted (see Figure 5). Therefore, a drive level of 0 dBFS corresponds to 1 V p-p, resulting in the same 13 dBm output power previously discussed.

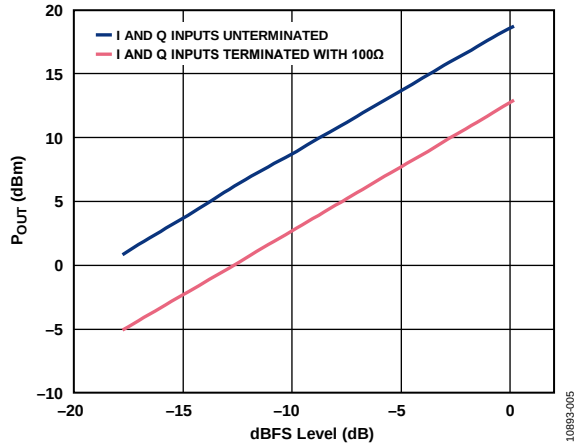

Figure 5. Transfer Function of Circuit in Terms of Output Power vs. DAC Drive Level with IQ Modulator I and Q Inputs Terminated with 100 Ω and with I and Q Inputs Unterminated

Figure 5 also shows the transfer function of the circuit when the I and Q inputs are not terminated with 100 Ω resistors. Because the resulting DAC voltage drive level is doubled (2 V p-p maximum), the resulting output power is higher by 6 dB for the same DAC drive level.

While operation of the circuit without I and Q termination resistors is possible, it does pose some problems for the filter that is usually placed between the DAC and IQ modulator. Because this filter is generally terminated at both ends, it is desirable to have some resistance across the I and Q inputs of the IQ modulator (the unterminated input resistance of these inputs is approximately 60 kΩ). A value that is in the 100 Ω to 1000 Ω range can be used to increase the resulting DAC voltage drive level and corresponding output power. However, take care to design

the filter between the DAC and IQ modulator so that it can support different source and load impedances.

As already noted, from Figure 4 and Figure 5, it can be seen that a 1 V p-p sine wave (0 dBFS) is provided an output power of approximately 13 dBm (the I and Q inputs terminated with 100 Ω). In practice, the DAC drive level must be reduced slightly from 0 dBFS to reduce distortion (typically 1 dB to 2 dB). In addition to this, the rms drive level should be lower again by an amount equal to the peak-to-average ratio of the modulation of the carrier. The ratio of peak envelope power (PEP) to rms power is typically in a range from 5 dB for QPSK-like modulation schemes (0 dB in the special case where the modulation is constant envelope) to around 10 dB for higher order QAM-based modulation. Referring to Figure 6, this suggests that output power levels in the 0 dBm to 10 dBm range are feasible.

The adjacent channel power ratio (ACPR) of a single carrier, wideband code division multiple access (WCDMA) signal has become a popular metric for assessing the system level distortion of a circuit (that is, as opposed to an assessment that is solely based on IP3 and IMD levels). Figure 6 shows the measured ACPR of the circuit vs. the output power level. In the case of a WCDMA signal, ACPR is defined as the ratio of the power in the carrier (in a bandwidth of 3.84 MHz) to the power in an adjacent channel (channel spacing = 5 MHz), also measured in a 3.84 MHz bandwidth. The plot also shows an alternate channel power ratio that is the same type of measurement; however, at a carrier offset of 10 MHz.

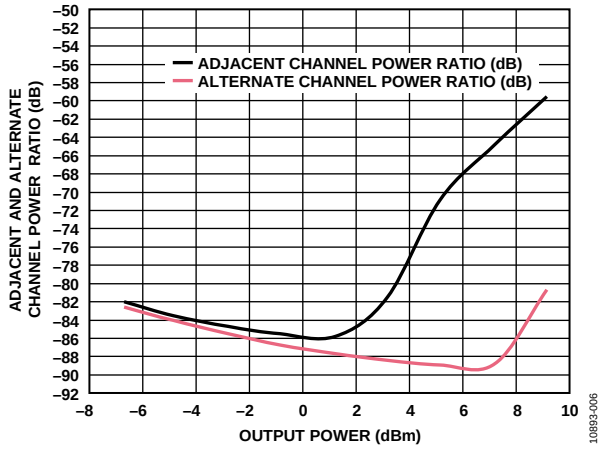

Figure 6. Plot of OIP3 and WDCMA ACPR vs. Output Power

In this case, the signal has a PEP-to-rms ratio of approximately 10 dB (the peak-to-average ratio of a WCDMA signal can vary based on how the carrier is configured and loaded). Based on this plot and the desired level of ACPR, select an output power level in the 0 dBm to 10 dBm range. At power levels less than 0 dBm, the ACPR becomes dominated by the degrading signal-to-noise ratio of the circuit.

COMMON VARIATIONS

The ADL5320 driver amplifier is specified to operate from 400 MHz to 2.7 GHz. This conveniently covers the lower end of the specified frequency range of the ADL5375 IQ modulator. For operation at frequencies in the 2.3 GHz to 4 GHz range, the ADL5321 driver amplifier is recommended. Both the ADL5320 and ADL5321 must be tuned to the frequency at which they will be operating. The data sheets of both devices contain tables that provide recommended values for tuning components at popular operating frequencies.

A broadband internally matched gain block, such as the ADL5601 or the ADL5602, can also be used to provide gain at the output of the IQ modulator. However, because these devices have lower OIP3 (than ADL5320 and ADL5321), they tend to dominate and reduce the overall IP3 of the circuit.

A number of narrow-band IQ modulators are available that provide higher performance over their operating frequency ranges. Examples are ADL5370/ADL5371/ADL5372/ADL5373/ADL5374. These narrow-band devices provide higher gain and OIP3 compared to ADL5375. When paired with the ADL5320 and ADL5321 driver amplifiers, the net result is overall higher output power with similar composite OIP3.

The ADRF6701/ADRF6702/ADRF6703/ADRF6704 families of narrow-band IQ modulators include an integrated phase-locked loop (PLL) and voltage controlled oscillator (VCO). These devices provide similar performance to the ADL5370/ADL5371/ADL5372/ADL5373/ADL5374 family; however, with a higher level of integration.

A number of options exist to drive the I and Q inputs of the IQ modulator. The AD9125 and AD9122 are 16-bit dual DACs that operate at 1 GSPS or 1.2 GSPS, respectively. These devices can be used to generate either a baseband spectrum (centered at 0 Hz) or a complex IF spectrum typically in the 100 MHz to 200 MHz range.

CIRCUIT EVALUATION AND TEST

The circuit was implemented using the ADL5375 evaluation board (ADL5375-05-EVALZ) that includes the ADL5320 driver amplifier. This board can be configured to provide the IQ modulator output signal, or the composite modulator and amplifier signal. The default configuration for this board is the modulator and amplifier composite output with the amplifier tuned for operation in the 1800 MHz to 2200 MHz range. As already noted, the ADL5320 data sheet provides the values and placement locations for tuning capacitors that support other frequencies.

Equipment Needed

The following equipment is needed:

- The ADL5375 evaluation board (ADL5375-05-EVALZ)
- Two RF signal generators: Agilent 8648C or equivalent operating at 25 MHz and 26 MHz
- A RF signal generator: Agilent 8648C or equivalent operating at approximately 2 GHz
- A RF spectrum analyzer: Rohde & Schwarz FSIQ, Rohde & Schwarz FSQ, Agilent PSA, or equivalent
- A ZFSC-2-2-S+ 180° power splitter/combiner, Mini-Circuits
- A ZMSCQ-2-50+ 90° power splitter, Mini-Circuits
- Two ADT2-1T 1:2 baluns, Mini-Circuits
- Four ZFBT-6GW-FT+ bias tees, Mini-Circuits

Setup and Test

Figure 7 shows the test setup that was used for the IP3 testing and for the power sweep testing. The signals from two RF signal generators running at 25 MHz and 26 MHz are passively combined using a 180° phase splitter/combiner that provides good input-to-input isolation. The 2-tone signal is then applied to a 90° phase splitter that is specified to operate from 25 MHz to 50 MHz. These phase splitter outputs are then applied to two 1:2 transformers to create differential output signals (the 0° output of the phase splitter should go towards the IP and IN inputs of the IQ modulator). The differential signals are applied to four bias tees that bias the signals to 0.5 V. The network is terminated by two 100 Ω resistors (pads for these resistors are provided on the ADL5375 evaluation board).

The local oscillator (LO) for the ADL5375 is provided by a third signal generator, generating 0 dBm. The final output frequency is equal to the difference between the input RF signal frequencies and the LO frequency. Therefore, if the 2-tone signals are at 25 MHz and 26 MHz, and the LO is at 2150 MHz, the output spectrum appears at 2124 MHz and 2125 MHz.

The circuit can also be implemented using the AD9122 dual DAC evaluation board (AD9122-M5375-EBZ) that includes the ADL5375 IQ modulator. In this case, connect the output of the ADL5375 IQ modulator to a standalone ADL5320 evaluation board (ADL5320-EVALZ). The advantage of this approach is that the DAC generates appropriately biased differential signals without the need for bias tees, phase splitters, and transformers.

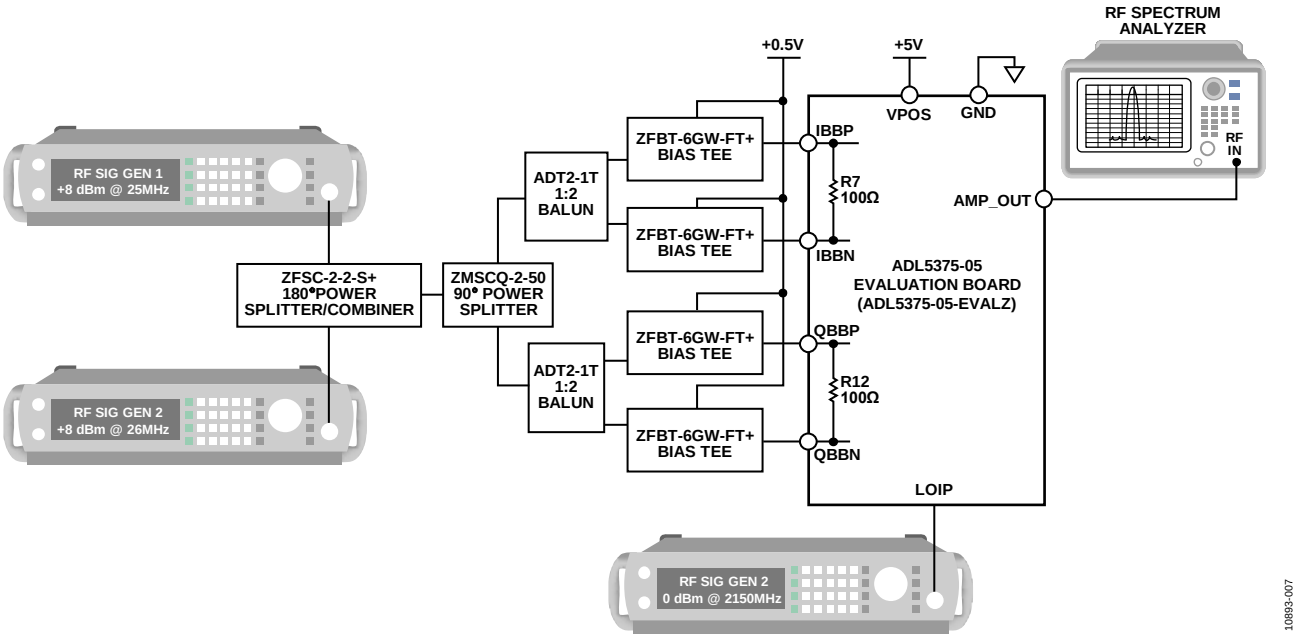

Figure 7. Measurement Setup for IP3 Testing and Power Sweep

LEARN MORE

CN0283 Design Support Package:
http://www.analog.com/CN0283-DesignSupport

Nash, Eamon, *Correcting Imperfections in IQ Modulators to Improve RF Signal Fidelity*, Application Note AN-1039, Analog Devices

ADIsimRF Design Tool

Circuit Note CN-0016, *Interfacing the ADL5370 I/Q Modulator to the AD9779A Dual-Channel, 1 GSPS High Speed DAC*, Analog Devices.

Circuit Note CN-0017, *Interfacing the ADL5371 I/Q Modulator to the AD9779A Dual-Channel, 1 GSPS High Speed DAC*, Analog Devices.

Circuit Note CN-0018, *Interfacing the ADL5372 I/Q Modulator to the AD9779A Dual-Channel, 1 GSPS High Speed DAC*, Analog Devices.

Circuit Note CN-0019, *Interfacing the ADL5373 I/Q Modulator to the AD9779A Dual-Channel, 1 GSPS High Speed DAC*, Analog Devices.

Circuit Note CN-0020, *Interfacing the ADL5374 I/Q Modulator to the AD9779A Dual-Channel, 1 GSPS High Speed DAC*, Analog Devices.

Circuit Note CN-0021, *Interfacing the ADL5375 I/Q Modulator to the AD9779A Dual-Channel, 1 GSPS High Speed DAC*, Analog Devices.

Circuit Note CN-0070, *Precise Control of I/Q Modulator Output Power Using the ADL5386 Quadrature Modulator and the AD5621 12-Bit DAC*, Analog Devices.

Circuit Note CN-0134, *Broadband Low Error Vector Magnitude (EVM) Direct Conversion Transmitter*, Analog Devices.

Circuit Note CN-0140, *High Performance, Dual Channel IF Sampling Receiver*, Analog Devices.

Circuit Note CN-0144, *Broadband Low Error Vector Magnitude (EVM) Direct Conversion Transmitter Using LO Divide-by-2 Modulator*, Analog Devices.

Circuit Note CN-0205, *Interfacing the ADL5375 I/Q Modulator to the AD9122 Dual Channel, 1.2 GSPS High Speed DAC*, Analog Devices.

Circuit Note CN-0243, *High Dynamic Range RF Transmitter Signal Chain using Single External Frequency Reference for DAC Sample Clock and IQ Modulator LO Generation*, Analog Devices.

Circuit Note CN-0245, *Wideband LO PLL Synthesizer with Simple Interface to Quadrature Demodulators*, Analog Devices.

Data Sheets and Evaluation Boards

ADL5375 Evaluation Board, ADL5375-05-EVALZ

ADL5320 Evaluation Board, ADL5320-EVALZ

AD9122 Evaluation Board, AD9122-M5375-EBZ

ADL5375 Data Sheet

ADL5320 Data Sheet

REVISION HISTORY

9/12—Revision 0: Initial Version