HM23C1000P,HM23C1000AP,HM23C1000M,HM23C1000AM
128K X 8 CMOS ROM

General Description

The HM23C1000 serial high performance Read Only Memories are organized as 131,072 words by 8 bits with access times from 150 ns to 200 ns. The ROMs are designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations.

The HM23C1000P/M offers the simplest operation (no power down). Its programmable chip selects allow up to two 1,024 K ROMs to be Wired-OR without external decoding.

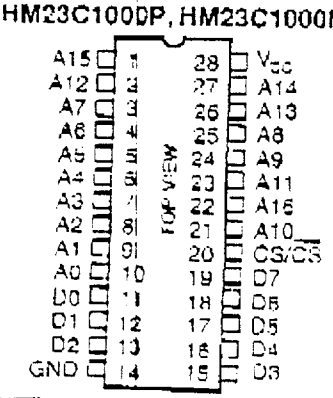
The HM23C1000AP/AM has the automatic power down feature. Power down is controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes high, the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$ remains high. This unique feature provides system level power savings as much as 90 %.

Features

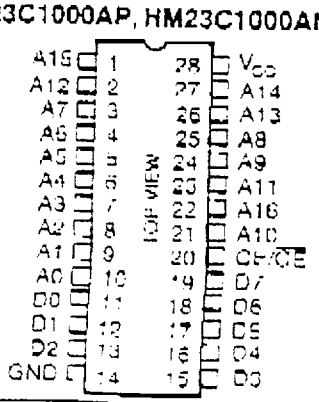
* 131,072 X 8 bit organization.
* Single +5 Volt Supply.
* Access Time - 150/200ns (Max.)
* Totally static operation.
* Completely TTL compatible.
* Low power consumption.
* Three-state outputs.
* HM23C1000P/M
  -Non powerdown version.
  -Programmable chip selects ($\overline{CS}$).
* HM23C1000AP/AM
  -Automatic power down ($\overline{CE}$).
* Package HM23C1000P/AP - 28 pin 600 mil plastic DIP.
  HM23C1000M/AM - 28 pin 300 mil plastic SOP.

Pin Assignment

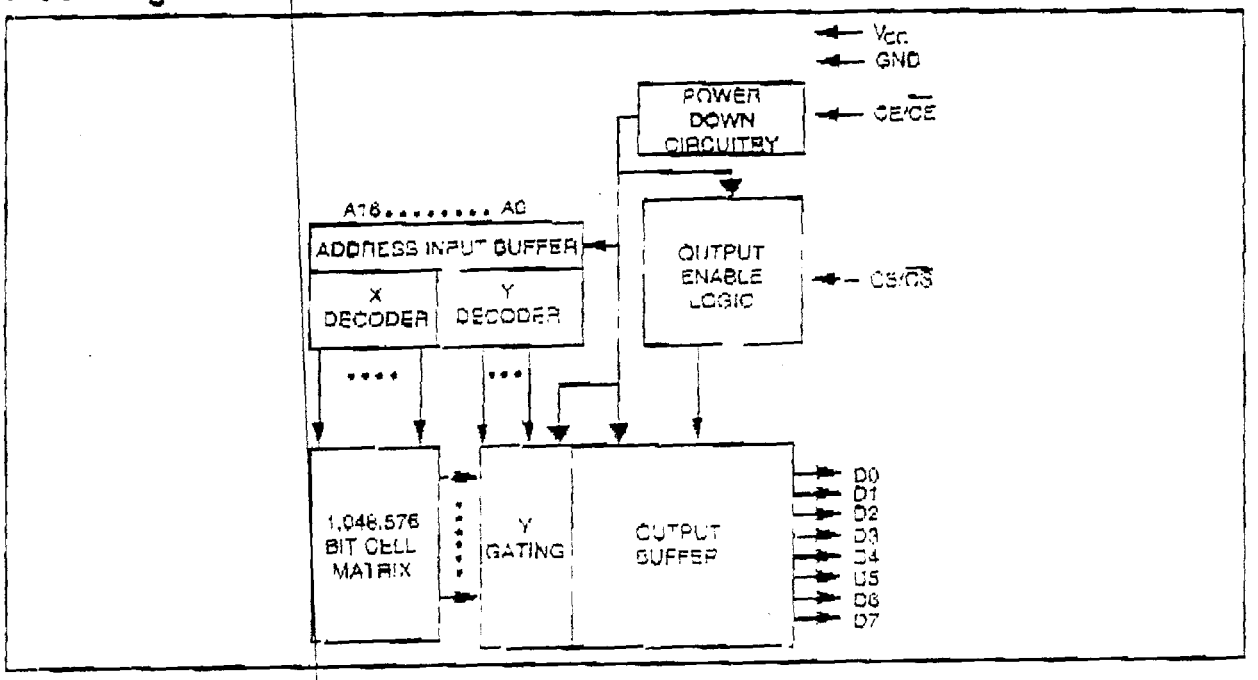
HM23C1000P, HM23C1000M



HM23C1000AP, HM23C1000AM



Block Diagram



Function Descriptions

HM23C1000AP/AM

Mode	CE	A0 - A16	D0 - D7	Power
Read	Active	Valid	Data Out	I_{cc}
Standby	Inactive	*	High -z	I_{sb}

HM23C100P//M

Mode	CS	A0 - A16	D0 - D7	Power
Read	Active	Valid	Data Out	I_{cc}
Output Disable	Inactive	*	High -z	I_{cc}

Note : "* " means "Active (Valid) " or " Inactive (Invalid) ".

Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Ambient temperature under bias	T_A	- 10 to +80	°C
Storage temperature	T_{stg}	- 65 to +150	°C
Power supply voltage	V_{cc}	- 0.5 to +7	V
Input voltage	V_{IN}	-0.5 to V_{cc}	V
Output voltage	V_{OUT}	0 to V_{cc}	V
Power dissipation	P_D	1.0	W

* Stresses above those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Electrical Characteristics

(T_A=0 to +70°C , V_{CC}=5V±10%)

Parameter	Sym.	Limits Min.	Typ.	Max.	Unit	Conditions
Output High Level	V_{OH}	2.4	-	V_{CC}	V	I_{OH}=-400μA
Output Low Level	V_{OL}	-	-	0.4	V	I_{OL}=4.0mA
Input High Level	V_{IH}	2.2	-	V_{CC}+0.2	V	
Input Low Level	V_{IL}	-0.3	-	0.8	V	
Input Leakage Current	I_{LI}	-	-	10	μA	V_{IN}=0V to V_{CC}
Output Leakage Current	I_{LO}	-	-	10	μA	V_{OUT}=0V to V_{CC}
Operating Supply Current	I_{CC1}	-	-	40	mA	Note 1.
Operating Supply Current	I_{CC2}	-	-	30	mA	Note 2.
Standby Supply Current	I_{SB1}	-	-	4	mA	Note 3.
Standby supply Current	I_{SB2}	-	-	10	μA	Note 4.

A.C. Electrical Characteristics

(T_A=0 to 70°C, V_{CC}=+5V±10%) (Note 7.)

Parameter	Sym.	23C1000-15 23C1000A-15 Min.	Max.	23C1000-20 23C1000A-20 Min.	Max.	Unit	Condition
Cycle Time	t_{CYC}	150	-	200	-	ns	
Address Access Time	t_{ACC}	-	150	-	200	ns	
Output hold after address change	t_{OH}	10	-	10	-	ns	
Chip Enable Access Time	t_{CE}	-	150	-	200	ns	Note 5
Chip Select Access Time	t_{CS}	-	70	-	100	ns	
Output disable Delay	t_{DF}	-	50	-	50	ns	Note 6

Notes:

1. Measured with device selected and output unloaded V_{IH}=V_{CC}, V_{IL}, T_{CYC}=150/200ns.
2. Measured with device selected and output unloaded V_{IH}=V_{CC}-0.2V/0.2V, T_{CYC}=150/200ns
3. Applies to "A" versions only and measured with $\overline{CE}$=2.2V or CE=0.8V
4. Applies to "A" versions only and measured with CE=V_{CC} - 0.2V or CE=0.2V, V_{IN} =GND or V_{CC}.
5. Applies to "A" versions (power down) only.
6. Outputs high impedance delay (t_{DF}) is measured from either CE/$\overline{CE}$ going disabled or CS/$\overline{CS}$ going inactive.
7. A minimum 0.5 ms time delay is required after application of V_{CC} (+5V) before proper device operation is achieved.

Capacitance*

(T_A=25°C, f=1.0MHz)

Parameter	Symbol	Limits Typ.	Max.	Unit	Conditions
Input capacitance	C_{IN}	-	9	pF	All pins except pin under test are
Output capacitance	C_{OUT}	-	10	pF	tied to AC ground.

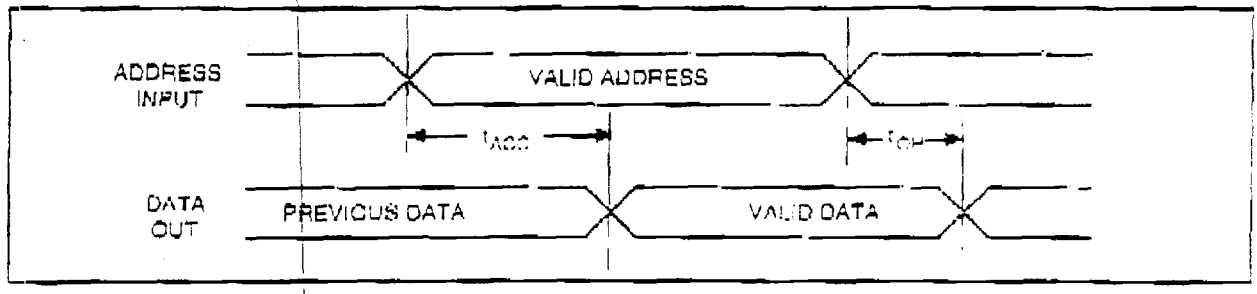
* This parameter is periodically sampled and is not 100% tested.

Test Conditions

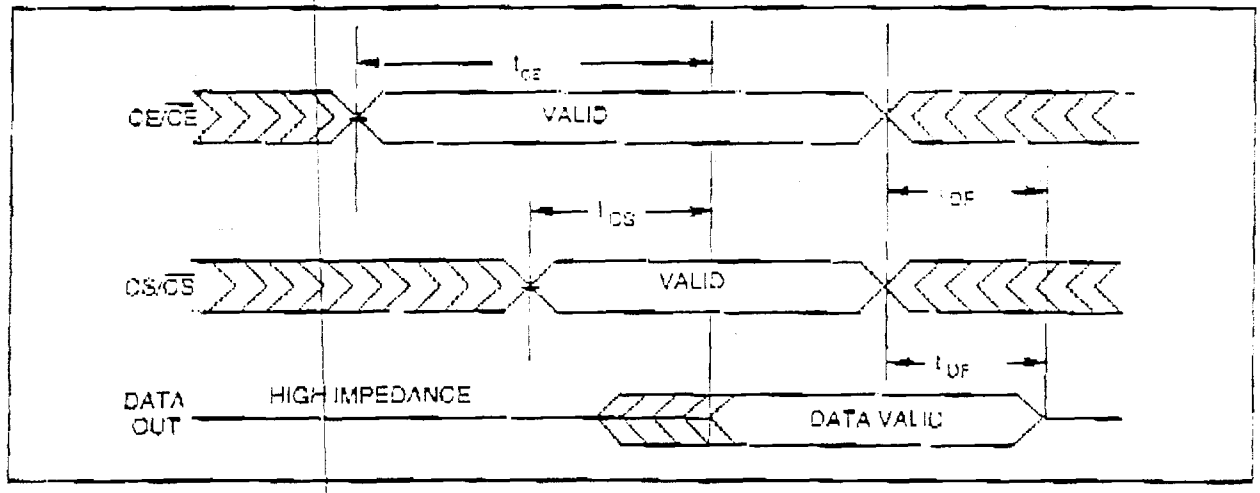
Output load	1 TTL load and 100pF
Input transition time	10 ns
Timing reference levels	Input = 1.5V, Output = 0.8V and 2.0V
Input levels	0.4V, 2.4V

Timing Diagram

Propagation delay from Address (CE/$\overline{CE}$- Enable or CS/$\overline{CS}$=Active)



Propagation delay from Chip Enable or Chip Select (Address Valid)



Programming Instructions

All HMC Read Only Memories (ROM) utilize computer aided techniques to manufacture and test custom bit patterns. The customer's bit pattern and address information can be supplied to HMC in a number of different ways. HMC can process customer inputs in EPROM, ROM, PROM, paper tape, and computer punched cards. Contact HMC sales representative for complete details on each of the various data input formats.

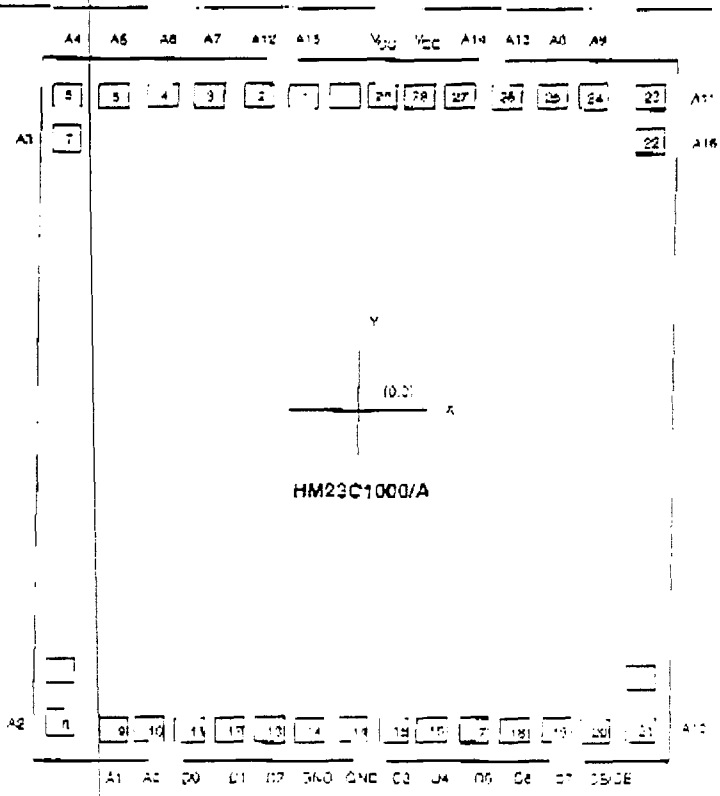
Ordering Information

HM 23C1000 A M –20

- HM: HMC prefix code
- 23C1000: Product number, 128K x 8 Mask ROM
- A: None : Non power down version; A : Automatic down version
- M: Package : P : Plastic DIP; M : SOP
- -20: Speed : -15 : 150 ns (max.); -20 : 200 ns (max.)

Order Number	Access Time	Operation Current	Standby Current	Package Ty
HM23C1000P-15	150 ns	40 mA	N.A	28L DIP
HM23C1000P-20	200 ns	40 mA		
HM23C1000AP-15	150 ns	40 mA	4 mA	28L DIP
HM23C1000AP-20	200 ns	40 mA		
HM23C1000M-15	150 ns	40 mA	N.A.	28L SOP
HM23C1000M-20	200 ns	40 mA		
HM23C1000AM-15	150 ns	40 mA	4 mA	28L SOP
HM23C1000AM-20	200 ns	40 mA		

Pad Diagram



Pad No.	Name	X	Y
1	A15	-269.2	1679.1
2	A12	-437.2	1679.1
3	A7	-607.4	1679.1
4	A6	-775.4	1679.1
5	A5	960.5	1679.1
6	A4	-1283.2	1679.1
7	A3	-1277.8	1519.1
	NC	-1252.7	-1473.2
8	A2	-1263.8	-1667.1
9	A1	-1016.3	-1688.3
10	A0	-844.1	-1688.3
11	D0	-670.1	-1693.2
12	D1	-498.5	-1693.2
13	D2	-334.5	-1693.2
14	GND	-156.7	-1735.6
14	GND	0.2	-1735.6
15	D3	168.0	-1693.2
16	D4	332.0	-1693.2
17	D5	503.6	-1693.2
18	D6	667.6	-1693.2
19	D7	839.2	-1693.2
20	CS/CE	1011.6	-1697.3
21	A10	1260.8	-1688.2
	NC	1229.0	-1515.7
22	A16	1276.7	1519.1

Pad No.	Name	X	Y
23	A11	1240.2	1679.1
24	A9	952.4	1679.1
25	A8	782.2	1679.1
26	A13	614.2	1679.1
27	A14	444.0	1679.1
28	V_{cc}	280.0	1671.9
28	V_{cc}	115.0	1649.0
	NC	-99.0	1679.1

Chip Size: 2980 x 3870 µm

Note : The substrate must be connected to V_{ss} in PCB layout artwork.