256Mb A-die Page NOR Specification

Document Title

256M Bit (16M x16) Page Mode / Multi-Bank NOR Flash Memory

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial draft	October 02, 2006	Target Information
0.1	Change Vih Min. from 2.0 to Vcc x0.8 Change Vil Max. from 0.8V to Vcc x 0.2 Change Isb Max from 40uA to 55uA	October 25, 2006	Target Information
0.2	MCP Product Voltage Information is added	November 06, 2006	Target Information
0.3	TSOP1 description is added in Ordering Information	November 13,2006	Target Information
0.4	Package Demension Information is added	November 19, 2006	Target Information
0.5	Change Isb2 Max. from 40uA to 55uA Change Isb3 Max. from 40uA to 55uA	January 11, 2007	Target Information
1.0	Specification is finalized	May 08, 2007	
1.1	Change Isb1 Max. from 55uA to 60uA Change Isb2 Max. from 55uA to 60uA Change Isb3 Max. from 55uA to 60uA	July 27, 2007	

256M Bit (16M x16) Page Mode / Multi-Bank NOR Flash Memory

FEATURES

- Single Voltage, 2.7V to 3.6V for Read and Write operations
  Voltage range of 2.7V to 3.1V valid for MCP product
- Organization
  16M x16 bit (Word mode Only)
- Fast Read Access Time : 70ns
- Page Mode Operation
  8 Words Page access allows fast asychronous read
  Page Read Access Time : 30ns
- Read While Program/Erase Operation
- Multiple Bank architectures (4 banks)
  Bank 0: 32Mbit (32Kw x 4 and 128Kw x 15)
  Bank 1: 96Mbit (128Kw x 48)
  Bank 2: 96Mbit (128Kw x 48)
  Bank 3: 32Mbit (32Kw x 4 and 128Kw x 15)
- OTP Block : Extra 256 word
  - 128word for factory and 128word for customer OTP
- Power Consumption (typical value)
  - Active Read Current : 30mA (@5MHz)
  - Program/Erase Current : 25mA
  - Read While Program or Read While Erase Current : 65mA
  - Standby Mode/Auto Sleep Mode : 20uA
- Support Single & 32word Buffer Program
- $\overline{WP}$/ACC input pin
  - Allows special protection of two outermost boot blocks on both ends of flash array at V_{IL}, regardless of block protect status
  - Removes special protection at V_{IH}, the two outermost blocks on both ends of flash array return to normal block protect status
  - Reduce program time at V_{HH} : 6us/word at Write Buffer
- Erase Suspend/Resume
- Program Suspend/Resume
- Unlock Bypass Program
- Hardware $\overline{RESET}$ Pin
- Command Register Operation
- Supports Common Flash Memory Interface
- Industrial Temperature : -40°C to 85°C
- Extended Temperature : -25°C to 85°C
- Endurance : 100,000 Program/Erase Cycles Minimum
- Data Retention : 10 years
- Package options
  - 84 Ball Fine-pitch BGA (11.6x8mm)
  - 56 Pin TSOP (20x14mm)

GENERAL DESCRIPTION

The K8P5615UQA featuring single 3.0V power supply, is an 256Mbit NOR-type Flash Memory organized as 16M x16. The memory architecture of the device is designed to divide its memory arrays into 134 blocks with independent hardware protection. This block architecture provides highly flexible erase and program capability. The K8P5615UQA NOR Flash consists of four banks. This device is capable of reading data from one bank while programming or erasing in the other banks.

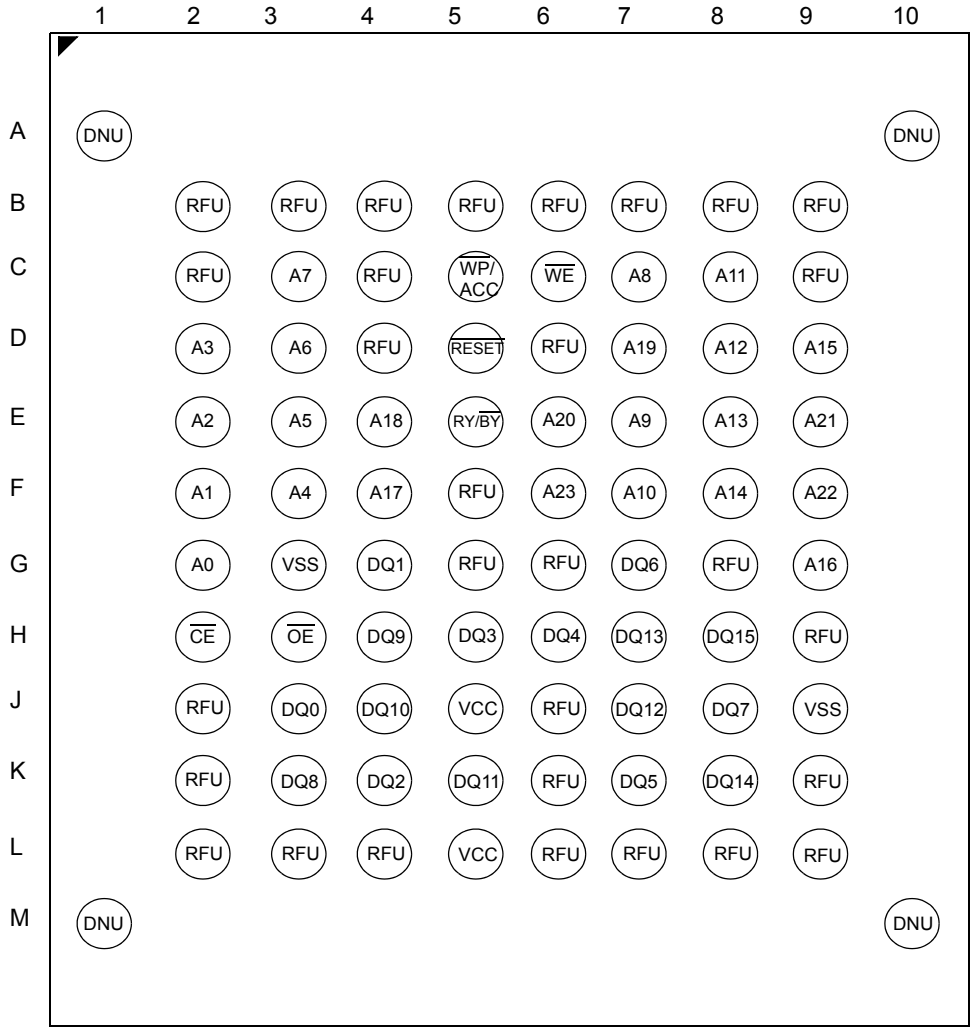
The K8P5615UQA offers fast page access time of 30ns with random access time of 70ns. The device's fast access times allow high speed microprocessors to operate without wait states. The device performs a program operation in unit of 16 bits (Word) and erases in units of a block. Single or multiple blocks can be erased. The block erase operation is completed within typically 1.6 sec. The device requires 15mA as program/erase current in the commercial and extended temperature ranges.

The K8P5615UQA NOR Flash Memory is created by using Samsung's advanced CMOS process technology. This device is available in 84 Ball FBGA and 56 Pin TSOP. The device is compatible with EPROM applications to require high-density and cost-effective nonvolatile read/write storage solutions.

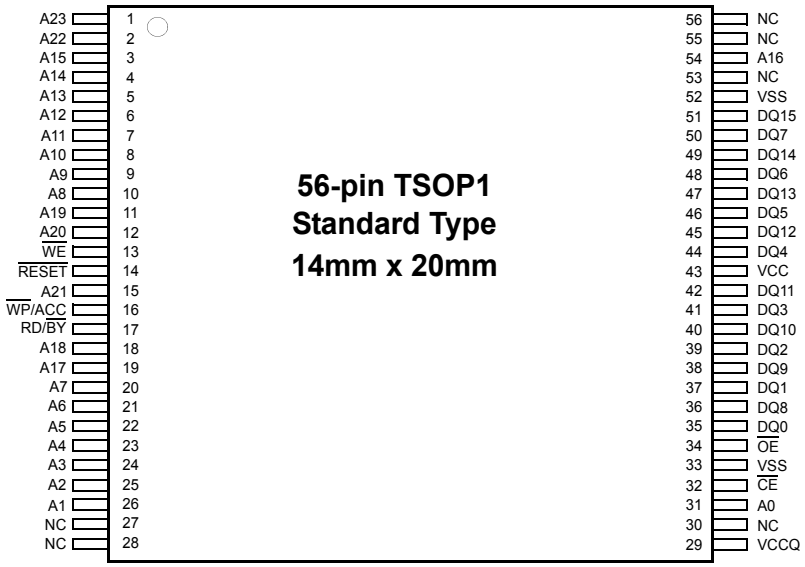
PIN DESCRIPTION

Pin Name	Pin Function
A0 - A23	Address Inputs
DQ0 - DQ15	Data Inputs / Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{RESET}$	Hardware Reset Pin
RY/$\overline{BY}$	Ready/Busy Output
$\overline{WE}$	Write Enable
$\overline{WP}$/ACC	Hardware Write Protection/Program Acceleration
Vcc	Power Supply
Vss	Ground
NC	No Connection

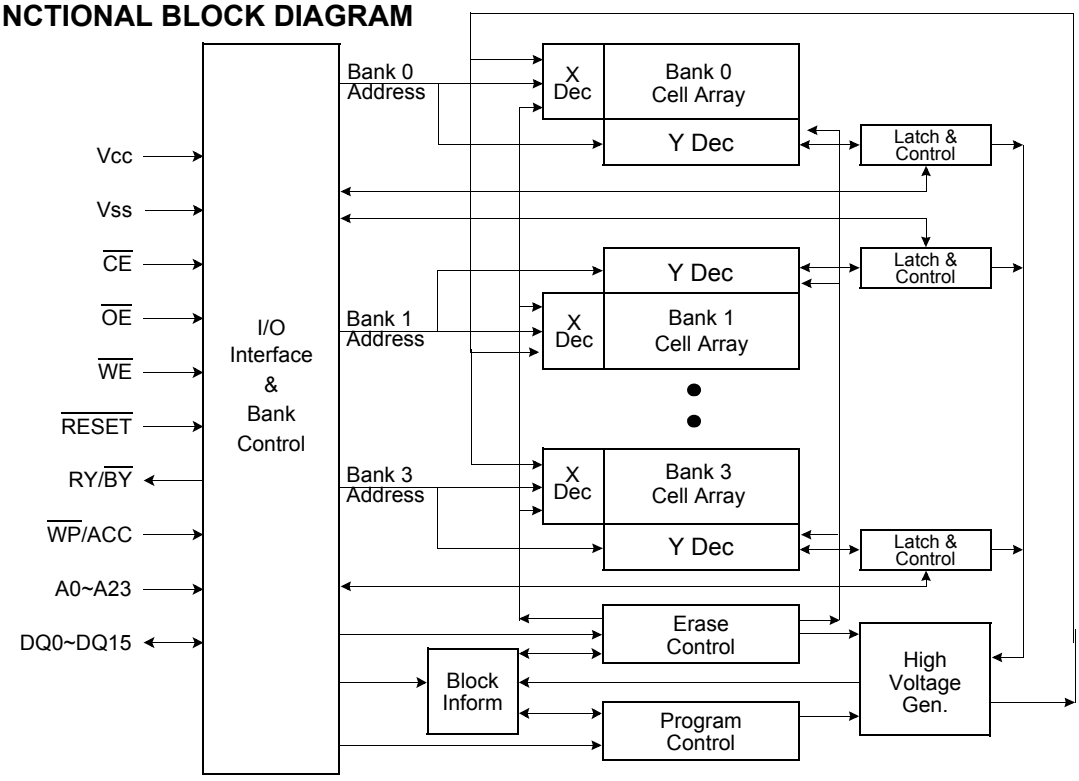
84 Ball FBGA TOP VIEW (BALL DOWN)



TSOP PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

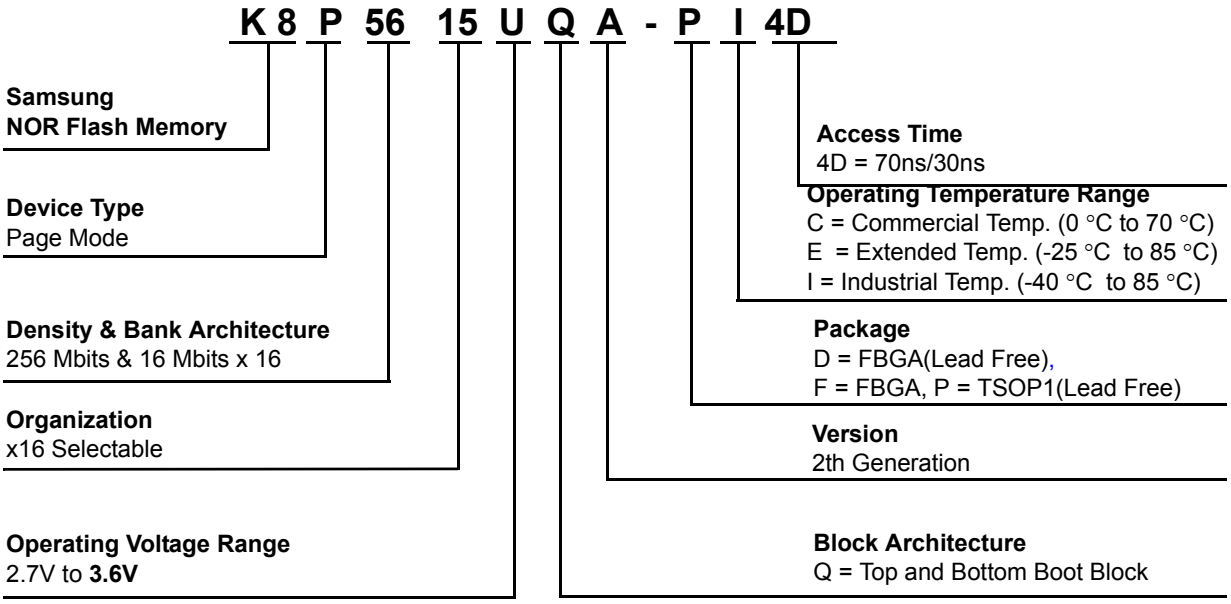


Table 1. PRODUCT LINE-UP

	4D
Vcc	2.7V~3.6V
VIO	2.7V~3.6V
Max. Address Access Time (ns)	70ns
Max. $\overline{CE}$ Access Time (ns)	70ns
Max. $\overline{OE}$ Access Time (ns)	30ns
Max. Page Access Time (ns)	30ns

Table 2. K8P5615UQA DEVICE BANK DIVISIONS

Bank 0, Bank 3		Bank 1, Bank 2	
Mbit	**Block Sizes**	**Mbit**	**Block Sizes**
32 Mbit	32 Kw x 4 and 128 Kw x 15	96 Mbit	128 Kw x 48

Table 3. OTP BLOCK

	Block Address A23~A8	Area	Block Size	Address Range
OTP	0000h	Factory-Locked Area	128 words	000000h-00007Fh
		Customer-Locked Area	128 words	000080h-0000FFh

After entering OTP block, any issued addresses should be in the range of OTP block address

PRODUCT INTRODUCTION

The K8P5615UQA is an 256Mbit NOR-type Flash memory. The device features single voltage power supply operating within the range of 2.7V to 3.6V. The device is programmed by using the Channel Hot Electron (CHE) injection mechanism which is used to program EPROMs. The device is erased electrically by using Fowler-Nordheim tunneling mechanism. To provide highly flexible erase and program capability, the device adapts a block memory architecture that divides its memory array into 134 blocks (32 Kw x 8, 128 Kw x 126). Programming is done in units of 16 bits (Word). All bits of data in one or multiple blocks can be erased simultaneously when the device executes the erase operation. The device offers fast page access time of 30ns with random access time of 70ns supporting high speed microprocessors to operate without any wait states.
The command set of K8P5615UQA is fully compatible with standard Flash devices. The device is controlled by chip enable ($\overline{CE}$), output enable ($\overline{OE}$) and write enable ($\overline{WE}$). Device operations are executed by selective command codes. The command codes to be combined with addresses and data are sequentially written to the command registers using microprocessor write timing. The command codes serve as inputs to an internal state machine which controls the program/erase circuitry. Register contents also internally latch addresses and data necessary to execute the program and erase operations. The K8P5615UQA is implemented with Internal Program/Erase Algorithms to execute the program/erase operations. The Internal Program/Erase Algorithms are invoked by program/erase command sequences. The Internal Program Algorithm automatically programs and verifies data at specified addresses. The Internal Erase Algorithm automatically pre-programs the memory cell which is not programmed and then executes the erase operation. The K8P5615UQA has means to indicate the status of completion of program/erase operations. The status can be indicated via the RY/$\overline{BY}$ pin, $\overline{Data}$ polling of DQ7, or the Toggle bit (DQ6). Once the operations have been completed, the device automatically resets itself to the read mode.

Table 4. Operations Table

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{WP}$/ACC	A0 ~ 23	DQ0 ~ DQ15	$\overline{RESET}$
Read	L	L	H	X	A_{IN}	D_{OUT}	H
Stand-by	H	X	X	X	A_{IN}	High-Z	H
Output Disable	L	H	H	X	A_{IN}	High-Z	H
Reset	X	X	X	X	A_{IN}	High-Z	L
Write	L	H	L	X (Note 1)	A_{IN}	D_{IN}	H

Notes :
L = V_{IL} (Low), H = V_{IH} (High), D_{IN} = Data in, D_{OUT} = Data out, X = Don't care.
1. $\overline{WP}$/ACC must be V_{IH} when writing to upper two and lower two blocks (BA0, BA1, BA132, and BA133)

COMMAND DEFINITIONS

The K8P5615UQA operates by selecting and executing its operational modes. Each operational mode has its own command set. In order to select a certain mode, a proper command with specific address and data sequences must be written into the command register. Writing incorrect information which include address and data or writing an improper command will reset the device to the read mode. The defined valid register command sequences are stated in Table 5.

Table 5. Command Sequences

Command Sequence		Cycle	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
Read	Addr	1	RA					
	Data		RD					
Reset	Addr	1	XXXH					
	Data		F0H					
Autoselect Manufacturer ID (Note 1, 2)	Addr	4	555H	2AAH	DA/555H	DA/X00H		
	Data		AAH	55H	90H	ECH		
Autoselect Device ID (Note 1, 2, 3)	Addr	6	555H	2AAH	DA/555H	DA/X01H	DA/X0EH	DA/X0FH
	Data		AAH	55H	90H	227EH	2263H	2260H
Autoselect Block Protect Verify (Note 1, 2)	Addr	4	555H	2AAH	DA/555H	BA / X02H		
	Data		AAH	55H	90H	(See Table 6)		
Autoselect Indicator Bit (Note 1, 2)	Addr	4	555H	2AAH	DA/555H	X03H		
	Data		AAH	55H	90H	(See Table 6)		
Program	Addr	4	555H	2AAH	555H	PA		
	Data		AAH	55H	A0H	PD		
Write to Buffer (Note 4)	Addr	6	555H	2AAH	BA	BA	PA	WBL
	Data		AAH	55H	25H	WC	PD	PD
Program Buffer to Flash	Addr	1	BA					
	Data		29H					
Write to Buffer Abort Reset (Note 4)	Addr	3	555H	2AAH	555H			
	Data		AAH	55H	F0H			
Unlock Bypass	Addr	3	555H	2AAH	555H			
	Data		AAH	55H	20H			
Unlock Bypass Program	Addr	2	XXXH	PA				
	Data		A0H	PD				
Unlock Bypass Block Erase	Addr	2	XXXH	BA				
	Data		80H	30H				
Unlock Bypass Chip Erase	Addr	2	XXXH	XXXH				
	Data		80H	10H				
Unlock Bypass Reset	Addr	2	XXXH	XXXH				
	Data		90H	00H				
Unlock Bypass CFI	Addr	1	DAH					
	Data		98H					
Chip Erase	Addr	6	555H	2AAH	555H	555H	2AAH	555H
	Data		AAH	55H	80H	AAH	55H	10H
Block Erase	Addr	6	555H	2AAH	555H	555H	2AAH	BA
	Data		AAH	55H	80H	AAH	55H	30H
Block Erase Suspend (Note 5, 6)	Addr	1	XXXH					
	Data		B0H					
Block Erase Resume	Addr	1	XXXH					
	Data		30H					

Table 5. Command Sequences (Continued)

Command Definitions		Cycle	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
Program Suspend (Note 7 ,8)	Addr	1	XXXH					
	Data		B0H					
Program Resume	Addr	1	XXXH					
	Data		30H					
CFI Query (Note 9)	Addr	1	DA/X55H					
	Data		98H					
Enter OTP Block Region	Addr	3	555H	2AAH	555H			
	Data		AAH	55H	88H			
OTP Block Program	Addr	4	555H	2AAH	555H	PA		
	Data		AAH	55H	A0H	PD		
OTP Block Read	Addr	1	RA					
	Data		RD					
Exit OTP Block Region	Addr	4	555H	2AAH	555H	XXXH		
	Data		AAH	55H	90H	00H		
Enter OTP Block Lock Register Region	Addr	3	555H	2AAH	555H			
	Data		AAH	55H	40H			
OTP Block Lock Register Bit Program	Addr	2	XXXH	00H				
	Data		A0H	(Note 10)				
Exit OTP Block Lock Register Region	Addr	2	XXXH	XXXH				
	Data		90H	00H				

Notes :
- RA : Read Address, PA : Program Address, RD : Read Data, PD : Program Data, WBL : Write Buffer Location
- DA : Bank Address (A21 - A23), BA : Block Address (A15 - A23), ABP : Address of the block to be protected or unprotected, X = Don't care .
- DQ8 - DQ15 are don't care in command sequence, except for RD and PD
- A14 - A23 are also don't care, except for the case of special notice.

1. To terminate the Autoselect Mode, it is necessary to write Reset command to the register.
2. The 4th cycle data of Autoselect mode is output data.
   The 3rd and 4th cycle bank addresses of Autoselect mode must be same.
3. Device ID must be read across cycles 4, 5 and 6.
   Device ID data : X0EH = "2263H", X0FH = "2260H" for 256Mb Top and Boot Block Device
4. Command sequence resets device for next command after write-to-buffer operation.
5. The Read / Program operations at non-erasing blocks and the autoselect mode are allowed in the Erase Suspend mode.
6. The Erase Suspend command is applicable only to the Block Erase operation.
7. The Read Operation is allowed in the Program Suspend mode.
8. The Program Suspend command is applicable to Program and Erase Suspend - Program operation.
9. Command is valid when the device is in read mode or Autoselect mode.
10. Programming DQ0 (setting to zero), non-volatile bit locks the OTP Block region permanently.

Table 6. K8P5615UQA Autoselect Codes

Description		$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A22 - A12	A10 - A4	A3	A2	A1	A0	DQ15 - DQ8	DQ7 - DQ0
Manufacturer ID		L	L	H	DA	X	L	L	L	L	X	ECH
Device ID	Read Cycle1	L	L	H	DA	X	L	L	L	H	22H	7EH
	Read Cycle2	L	L	H	DA	X	H	H	H	L	22H	63H
	Read Cycle3	L	L	H	DA	X	H	H	H	H	22H	60H
Block Protection Verification		L	L	H	BA	X	L	L	H	L	X	01H : (Proected) 00H : (Unproteced)
Indicator Bit		L	L	H	DA	X	L	L	H	H	X	DQ15~8 : V_{IL} DQ7 : Factory Lock Bit DQ6 : Customer Lock Bit DQ5 : Handshake Bit DQ4~3 : WP Protection Code DQ2~0 : V_{IL}

Notes : 1. L=Logic Low=V_{IL}, H=Logic High=V_{IH}, DA= Bank Address, BA=Block Address, X=Don't care.

DEVICE OPERATION

Read Mode

The K8P5615UQA is controlled by Chip Enable ($\overline{CE}$), Output Enable ($\overline{OE}$) and Write Enable ($\overline{WE}$). When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the specified address location,will be the output of the device. The outputs are in high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high.
The K8P5615UQA is available for 8-Word Page mode. Page mode provides fast access time for high performance system.
After address access time(tAA), eight data words are loaded into an internal page buffer. A0~A2 bits determine which page word is output during a read operation. A3~A23 bits must be stable throughout the page read access. Figure 11 shows the asynchronous page read more timing.

Standby Mode

The K8P5615UQA features Stand-by Mode to reduce power consumption. This mode puts the device on hold when the device is deselected by making $\overline{CE}$ high ($\overline{CE}$ = V_{IH}). Refer to the DC characteristics for more details on stand-by modes.

Output Disable

The device outputs are disabled when $\overline{OE}$ is High ($\overline{OE}$ = V_{IH}). The output pins are in high impedance state.

Automatic Sleep Mode

The K8P5615UQA features Automatic Sleep Mode to minimize the device power consumption. When addresses remain steady for t_{AA}+30ns, the device automatically activates the Automatic Sleep Mode. In the sleep mode, output data is latched and always available to the system. When addresses are changed, the device provides new data without wait time.

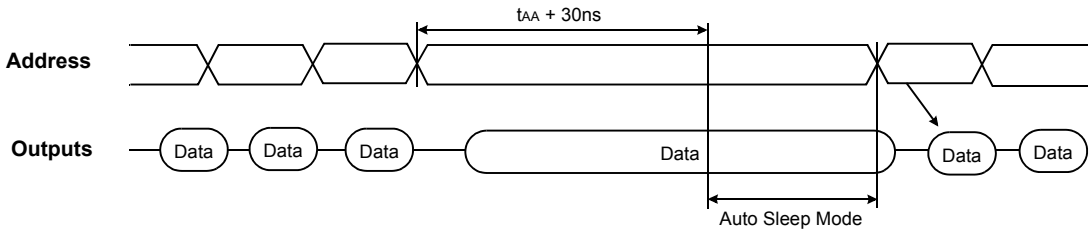


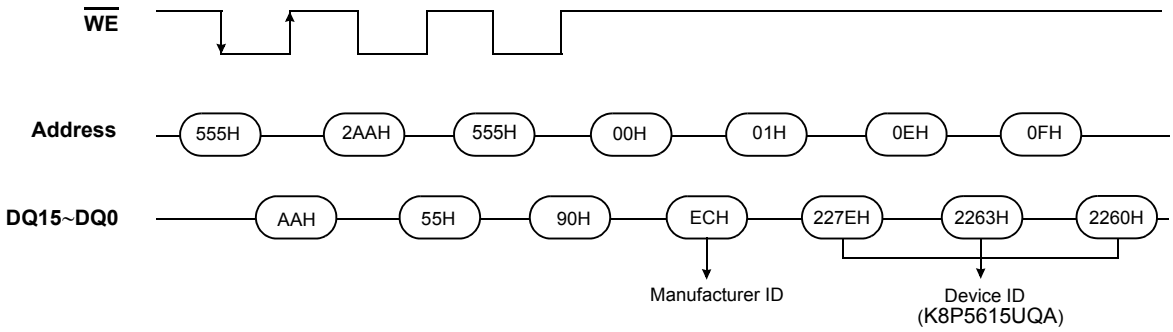
Figure 1. Auto Sleep Mode Operation

Autoselect Mode

The K8P5615UQA offers the Autoselect Mode to identify manufacturer, device type and block protection verification by reading a binary code. The Autoselect Mode allows programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. The manufacturer, device code ,block protection verification and indicator bit can be read via the command register. The Command Sequence is shown in Table 6 and Figure 2. In addition, below Table 7 shows indicator bit in detail. The autoselect operation of block protection verification is initiated by first writing two unlock cycle. The third cycle must contain the bank address and autoselect command (90H). If Block address while (A6, A1, A0) = (0,1,0) is finally asserted on the address pin, it will produce a logical "1" at the device output DQ0 to indicate a write protected block or a logical "0" at the device output DQ0 to indicate a write unprotected block. To terminate the autoselect operation, write Reset command (F0H) into the command register.

Table 7. Indicator Bit Codes.

Description	DQ15 to DQ8	DQ7	DQ6	DQ5	DQ4 to DQ3	DQ2 to DQ0
Indicator Bit	L	1=Factory-Locked 0=Not Locked	1=Customer-Locked 0=Not Locked	1=Reserved 0=Standard Handshake	00=$\overline{WP}$ Protects both Top & Bottom Boot Sector 11=No $\overline{WP}$ Protection	L



Note : The 3rd Cycle and 4th Cycle address must include the same bank address. Please refer to Table 6 for device code.

Figure 2. Autoselect Operation (by Command Sequence Method)

Write (Program/Erase) Mode

The K8P5615UQA executes its program/erase operations by writing commands into the command register. In order to write the commands to the register, $\overline{CE}$ and $\overline{WE}$ must be low and $\overline{OE}$ must be high. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$ (whichever occurs last) and the data are latched on the rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever occurs first). The device uses standard microprocessor write timing.

Program

The K8P5615UQA can be programmed in units of a word. Programming is writing 0's into the memory array by executing the Internal Program Routine. In order to perform the Internal Program Routine, a four-cycle command sequence is necessary. The first two cycles are unlock cycles. The third cycle is assigned for the program setup command. In the last cycle, the address of the memory location and the data to be programmed at that location are written. The device automatically generates adequate program pulses and verifies the programmed cell margin by the Internal Program Routine. During the execution of the Routine, the system is not required to provide further controls or timings.
During the Internal Program Routine, commands written to the device will be ignored. Note that a hardware reset during a program operation will cause data corruption at the corresponding location.

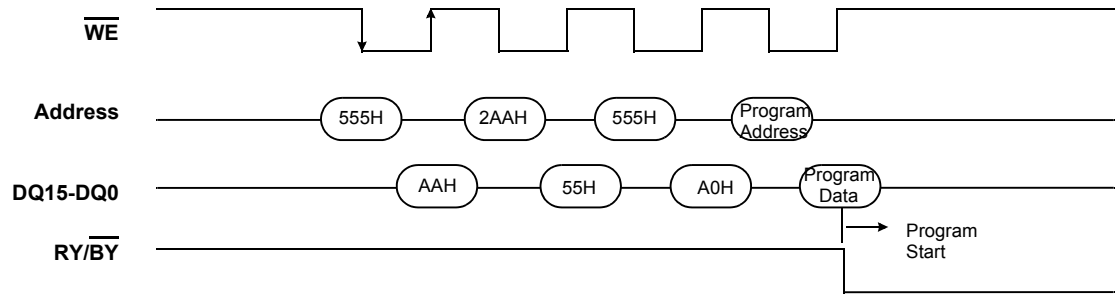


Figure 3. Program Command Sequence

In accross block boundaries and any sequence programming is allowed. A bit cannot be programmed from '0' back to '1'. If attempting to do, it may cause that bank to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still '0'. Only erase operations can convert a '0' to a '1'.

Writer Buffer Programming

Write Buffer Programming allows the system write to a maximum of 32 words in one programming operation. This results in faster effective programming time than the standard programming algorithms. The Write Buffer Programming command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the Write Buffer Load command written at the block address in which programming will occur. The fourth cycle writes the block address and the number of word locations, minus one, to be programmed. For example, if the system will program 19 unique address locations, then 12h should be written to the device. This tells the device how many write buffer addresses will be loaded with data. The number of locations to program cannot exceed the size of the write buffer or the operation will abort. The fifth cycle writes the first address location and data to be programmed. **The write-buffer-page is selected by address bits A23(max.) ~ A5 entered at fifth cycle**. **All subsequent address/ data pairs must fall within the selected write-buffer-page, so that all subsequent addresses must have the same address bit A23(max.) ~ A5 as those entered at fifth cycle. Write buffer locations may be loaded in any order.**
Once the specified number of write buffer locations have been loaded, the system must then write the "Program Buffer to Flash" com mand at the block address. Any other command address/data combination aborts the Write Buffer Programming operation. The device then begins programming. Data polling should be used while monitoring the last address location loaded into the write buffer. DQ7, DQ6, DQ5, and DQ1 can be monitored to determine the device status during Write Buffer Programming. The write-buffer programming operation can be suspended using the standard program suspend/resume commands. Upon successful completion of the Write Buffer Programming operation, the device is ready to execute the next command.
Note also that an address loaction cannot be loaded more than once into the write-buffer-page.

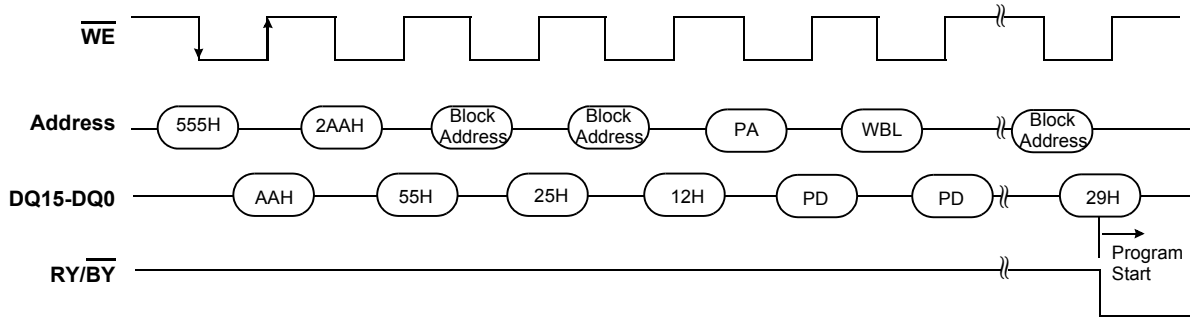


Figure 4. Write Buffer Program Command Sequence

Accelerated Program Operation

Accelerated program operation reduces the program time through the ACC function. This is one of two functions provided by the $\overline{WP}$/ACC pin. When the $\overline{WP}$/ACC pin is asserted as V_{HH}, the device automatically enters the Unlock Bypass mode, temporarily unprotecting any protected blocks, and reduces the program operation time. Removing V_{HH} from the $\overline{WP}$/ACC pin returns the device to normal operation.
Recommend that the $\overline{WP}$/ACC pin must not be asserted at V_{HH} except on accelerated program operation, or the device may be damaged. In addition, the $\overline{WP}$/ACC pin must not be in the state of floating or unconnected, otherwise the device may be led to malfunction.

Single word accelerated program operation

The system would use two-cycle program sequence (One-cycle (XXX - A0H) is for single word program command, and Next one-cycle (PA - PD) is for program address and data).

Accelerated Write Buffer Programming

In accelerated Write Buffer Program mode, the system must enter "Write to Buffer" and "Program Buffer to Flash" command sequence to be same as them of normal Write Buffer Programming and only can reduce the program time. Note that the third cycle of "Write to Buffer Abort Reset" command sequence is required in an Accelerated mode.
Note that Read While Accelerated Write Buffer Program and Program suspend mode are not guaranteed.

- Program/Erase cycling must be limited below 100cycles for optimum performance.
- Ambient temperature requirements : T_A = 30°C±10°C
- The device automatically generates adequate program pulses and ignores other command after program command
- Program/Erase cycling must be limited below 100cycles for optimum performance

Unlock Bypass

The K8P5615UQA provides the unlock bypass mode to save its operation time. This mode is possible for program, CFI, block erase and chip erase operation. There are two methods to enter the unlock bypass mode. The mode is invoked by the unlock bypass command sequence. Unlike the standard program/erase command sequence that contains four to six bus cycles, the unlock bypass program/erase command sequence comprises only two bus cycles. The unlock bypass mode is engaged by issuing the unlock bypass command sequence which is comprised of three bus cycles. Writing first two unlock cycles is followed by a third cycle containing the unlock bypass command (20H). Once the device is in the unlock bypass mode, the unlock bypass program/erase command sequence is necessary. The unlock bypass program command sequence is comprised of only two bus cycles; writing the unlock bypass program command (A0H) is followed by the program address and data. This command sequence is the only valid one for programming the device in the unlock bypass mode. The unlock bypass CFI command sequence is comprised of only one bus cycle; writing the unlock bypass program command (98H). This command sequence is the only valid one for programming the device in the unlock bypass mode. Also, The unlock bypass erase command sequence is comprised of two bus cycles; writing the unlock bypass block erase command(80H-30H) or writing the unlock bypass chip erase command(80H-10H). This command sequences are the only valid ones for erasing the device in the unlock bypass mode. The unlock bypass reset command sequence is the only valid command sequence to exit the unlock bypass mode. The unlock bypass reset command sequence consists of two bus cycles. The first cycle must contain the data (90H). The second cycle contains only the data (00H). Then, the device returns to the read mode.

Chip Erase

To erase a chip is to write 1′s into the entire memory array by executing the Internal Erase Routine. The Chip Erase requires six bus cycles to write the command sequence. The erase set-up command is written after first two "unlock" cycles. Then, there are two more write cycles prior to writing the chip erase command. The Internal Erase Routine automatically pre-programs and verifies the entire memory for an all zero data pattern prior to erasing. The automatic erase begins on the rising edge of the last $\overline{WE}$ or $\overline{CE}$ pulse in the command sequence and terminates when DQ7 is "1". After that the device returns to the read mode.

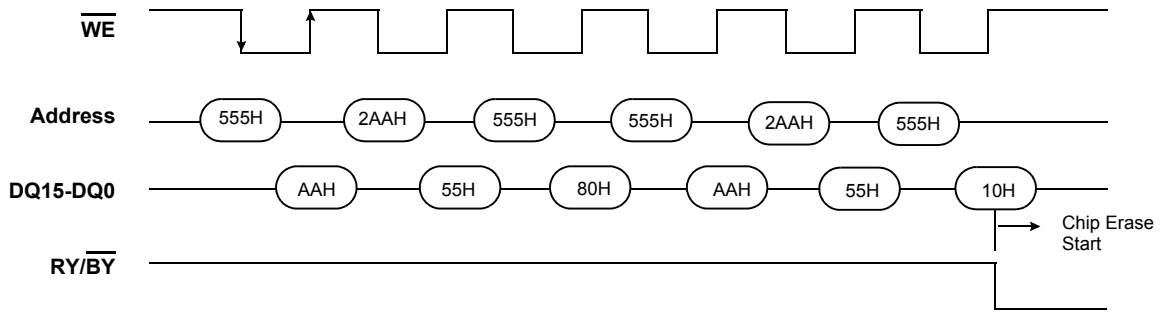


Figure 5. Chip Erase Command Sequence

Block Erase

To erase a block is to write 1′s into the desired memory block by executing the Internal Erase Routine. The Block Erase requires six bus cycles to write the command sequence shown in Table 5. After the first two "unlock" cycles, the erase setup command (80H) is written at the third cycle. Then there are two more "unlock" cycles followed by the Block Erase command. The Internal Erase Routine automatically pre-programs and verifies the entire memory prior to erasing it. The block address is latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, while the Block Erase command is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$.

Multiple blocks can be erased sequentially by writing the six bus-cycle. Upon completion of the last cycle for the Block Erase, additional block address and the Block Erase command (30H) can be written to perform the Multi-Block Erase. An 50us (typical) "time window" is required between the Block Erase command writes. The Block Erase command must be written within the 50us "time window", otherwise the Block Erase command will be ignored. The 50us "time window" is reset when the falling edge of the $\overline{WE}$ occurs within the 50us of "time window" to latch the Block Erase command. During the 50us of "time window", any command other than the Block Erase or the Erase Suspend command written to the device will reset the device to read mode. After the 50 us of "time window", the Block Erase command will initiate the Internal Erase Routine to erase the selected blocks. Any Block Erase address and command following the exceeded "time window" may or may not be accepted. No other commands will be recognized except the Erase Suspend command.

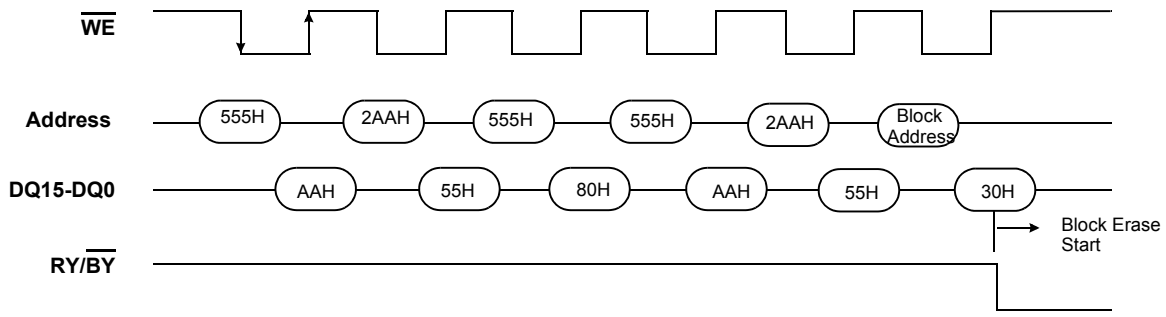


Figure 6. Block Erase Command Sequence

Erase Suspend / Resume

The Erase Suspend command interrupts the Block Erase to read or program data in a block that is not being erased. The Erase Suspend command is only valid during the Block Erase operation including the time window of 50us. The Erase Suspend command is not valid while the Chip Erase or the Internal Program Routine sequence is running.
When the Erase Suspend command is written during a Block Erase operation, the device requires a maximum of 20us to suspend the erase operation. But, when the Erase Suspend command is written during the block erase time window (50us) , the device immediately terminates the block erase time window and suspends the erase operation.
After the erase operation has been suspended, the device is availble for reading or programming data in a block that is not being erased. The system may also write the autoselect command sequence when the device is in the Erase Suspend mode.
When the Erase Resume command is executed, the Block Erase operation will resume. When the Erase Suspend or Erase Resume command is executed, the addresses are in don't care state.

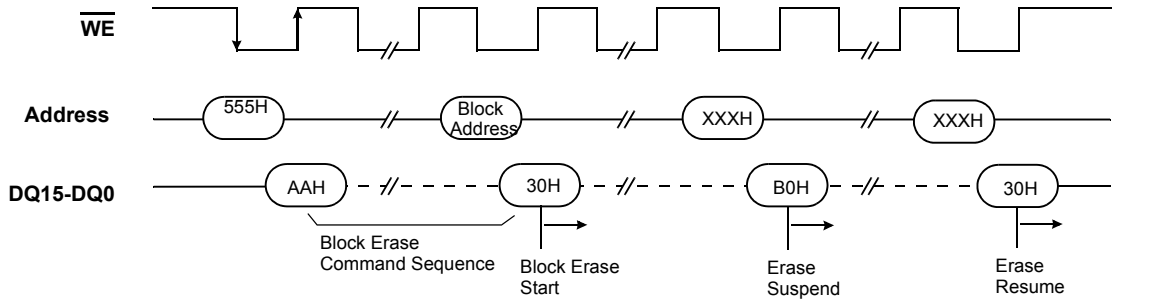


Figure 7. Erase Suspend/Resume Command Sequence

Program Suspend / Resume

The Program Suspend command interrupts the Program operation. Also the Program Suspend command interrupts the Program operation during Erase Suspend Mode. The Read operation is available only during Program Suspend. When the Program Suspend command is written during a Program operation, the device requires a maximum of 10us to suspend the Program operation. The system may also write the autoselect command sequence when the device is in the Program Suspend mode. When the Program Resume command is executed, the Program operation will resume. When the Program Suspend or Program Resume command is executed, the addresses are in don't care state.

Read While Write

The K8P5615UQA provides multi-bank memory architecture that divides the memory array into four banks. The device is capable of reading data from one bank and writing data to the other bank simultaneously. This is so called the Read While Write operation with multi-bank architecture; this feature provides the capability of executing the read operation during Program/Erase or Erase-Suspend-Program operation. The Read While Write operation is prohibited during the chip erase operation. It is also allowed during erase operation when either single block or multiple blocks from same bank are loaded to be erased. It means that the Read While Write operation is prohibited when blocks from one Bank and another blocks from the other Bank are loaded all together for the multi-block erase operation.

Write Protect ($\overline{WP}$)

The $\overline{WP}$/ACC pin has two useful functions. The one is that certain boot block is protected by the hardware method not to use V_{ID}. The other is that program operation is accelerated to reduce the program time (Refer to Accelerated program Operation Paragraph).
When the $\overline{WP}$/ACC pin is asserted at V_{IL}, the device can not perform program and erase operation in the two "outermost" 32 Kword boot blocks on both ends of the flash array independently of whether those blocks were protected or unprotected. (BA133, BA132, BA1 and BA0)
The write protected blocks can only be read. This is useful method to preserve an important program data.
When the $\overline{WP}$/ACC pin is asserted at V_{IH}, the device reverts the two outermost 32Kword boot blocks on both ends to default protection state. Note that the $\overline{WP}$/ACC pin must not be at VHH for operations other than accelerated programming, or device damage may result.

Software Reset

The reset command provides that the bank is reseted to read mode or erase-suspend-read mode. The addresses are in don't Care state. The reset command is vaild between the sequence cycles in an erase command sequence before erasing begins, or in a program command sequence before programming begins. This resets the bank in which was operating to read mode. if the device is be erasing or programming, the reset command is invalid until the operation is completed. Also, the reset command is valid between the sequence cycles in an autoselect command sequence. In the autoselect mode, the reset command returns the bank to read mode. If a bank entered the autoselect mode in the Erase Suspend mode, the reset command returns the bank to erase-suspend-read mode. If DQ5 is high on erase or program operation, the reset command return the bank to read mode or erase-suspend-read mode if the bank was in the Erase Suspend state.

Hardware Reset

The K8P5615UQA offers a reset feature by driving the $\overline{RESET}$ pin to V_{IL}. When the $\overline{RESET}$ pin is held low(V_{IL}) for at least a period of t_{RP}, the device immediatley terminates any operation in progress, tristates all outputs, and ignores all read/write commands for duration of the $\overline{RESET}$ pulse. The device also resets the internal state machine to asynchronous read mode. If a hardware reset occurs during a program operation, the data at that particular location will be lost. Once the $\overline{RESET}$ pin is taken high, the device requires 200ns of wake-up time until outputs are valid for read access. Also, note that all the data output pins are tri-stated for the duration of the $\overline{RESET}$ pulse. The $\overline{RESET}$ pin may be tied to the system reset pin. If a system reset occurs during the Internal Program and Erase Routine, the device will be automatically reset to the read mode ; this will enable the systems microprocessor to read the boot-up firmware from the Flash memory.

Power-up Protection

To avoid initiation of a write cycle during Vcc Power-up, $\overline{RESET}$ low must be asserted during power-up. After $\overline{RESET}$ goes high, the device is reset to the read mode.

Low Vcc Write Inhibit

To avoid initiation of a write cycle during Vcc power-up and power-down, a write cycle is locked out for Vcc less than 2.3V. If Vcc < V_{LKO} (Lock-Out Voltage), the command register and all internal program/erase circuits are disabled. Under this condition the device will reset itself to the read mode. Subsequent writes will be ignored until the Vcc level is greater than V_{LKO}. It is the user′s responsibility to ensure that the control pins are logically correct to prevent unintentional writes when Vcc is above 2.3V.

Write Pulse Glitch Protection

Noise pulses of less than 5ns(typical) on $\overline{CE}$, $\overline{OE}$, or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited under any one of the following conditions : $\overline{OE}$ = V_{IL}, $\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IH}. To initiate a write, $\overline{CE}$ and $\overline{WE}$ must be "0", while $\overline{OE}$ is "1".

Commom Flash Memory Interface

Common Flash Momory Interface is contrived to increase the compatibility of host system software. It provides the specific information of the device, such as memory size, word configuration, and electrical features. Once this information has been obtained, the system software will know which command sets to use to enable flash writes, block erases, and control the flash component.
When the system writes the CFI command(98H) to address 55H in word mode, the device enters the CFI mode. And then if the system writes the address shown in Table 8, the system can read the CFI data. Query data are always presented on the lowest-order data outputs(DQ0-7) only. In word(x16) mode, the upper data outputs(DQ8-15) is 00h. To terminate this operation, the system must write the reset command.

OTP Block Region

The OTP Block feature provides a 256-word Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The OTP Block is customer lockable and shipped with itself unlocked, allowing customers to untilize the that block in any manner they choose. Indicator bits DQ6 and DQ7 are used to indicate the factory-locked and customer locked status of the part. The data is DQ6 = "1" for customer locked and DQ7 = "1" for factory locked.
The system accesses the OTP Block through a command sequence (see "Enter OTP Block / Exit OTP Block Command sequence" at Table 5). After the system has written the "Enter OTP Block" Command sequence, it may read the OTP Block by using the addresses (000000h~0000FFh) normally and may check the Protection Verify Bit (DQ7,DQ6) by using the "Autoselect Indicator Bit" Command sequence with OTP Block address. This mode of operation continues until the system issues the "Exit OTP Block" Command suquence, a hardware reset or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to main blocks. Note that the Accelerated function and unlock bypass modes are not available when the OTP Block is enabled.

• After Enter OTP Block command sequence is written, read while write operation are disabled until exiting this mode and any issued addresses should be in the range of OTP block address.

OTP Block Protection

In a Customer lockable device, The OTP Block is one-time programmable and can be locked only once. Locking operation to the OTP Block is started by writing the "Enter OTP Block Lock Register Region" Command sequence, and then the "OTP Block Lock Register Bit Program" Command sqeunce (Table 5) with data that have zero(setting to 0) in DQ0. Note that the other DQs except DQ0 will be ignored. The Locking operation has to be above 100us. After that timing, "Exit OTP Block Lock Register Region" command sequence or Hardware reset must be issued in order to exit OTP block mode and revert the device to read mode in main array.

• The OTP Block Lock operation must be used with caution since, once locked, there is no procedure available for unlocking and none of the bits in the OTP Block space can be modified in any way.

• Suspend and resume operation are not supported during OTP protect, nor is OTP protect supported during any suspend operation.

• After Enter OTP Block Lock Register Region command sequence is written, read while write operation are disabled until exiting this mode.

Table 8. Common Flash Memory Interface Code

Description	Addresses (Word Mode)	Data
Query Unique ASCII string "QRY"	10H 11H 12H	0051H 0052H 0059H
Primary OEM Command Set	13H 14H	0002H 0000H
Address for Primary Extended Table	15H 16H	0040H 0000H
Alternate OEM Command Set (00h = none exists)	17H 18H	0000H 0000H
Address for Alternate OEM Extended Table (00h = none exists)	19H 1AH	0000H 0000H
Vcc Min. (write/erase) D7-D4: volt, D3-D0: 100 millivolt	1BH	0027H
Vcc Max. (write/erase) D7-D4: volt, D3-D0: 100 millivolt	1CH	0031H
Vpp Min. voltage(00H = no Vpp pin present)	1DH	0000H
Vpp Max. voltage(00H = no Vpp pin present)	1EH	0000H
Typical timeout per single word write 2^N us	1FH	0006H
Typical timeout for Min. size buffer write 2^N us(00H = not supported)	20H	0009H
Typical timeout per individual block erase 2^N ms	21H	000BH
Typical timeout for full chip erase 2^N ms(00H = not supported)	22H	00CCH
Max. timeout for word write 2^N times typical	23H	0003H
Max. timeout for buffer write 2^N times typical	24H	0003H
Max. timeout per individual block erase 2^N times typical	25H	0002H
Max. timeout for full chip erase 2^N times typical(00H = not supported)	26H	0002H
Device Size = 2^N byte	27H	0019H
Flash Device Interface description	28H 29H	0001H 0000H
Max. number of byte in multi-byte write = 2^N	2AH 2BH	0006H 0000H
Number of Erase Block Regions within device	2CH	0003H
Erase Block Region 1 Information	2DH 2EH 2FH 30H	0003H 0000H 0000H 0001H
Erase Block Region 2 Information	31H 32H 33H 34H	007DH 0000H 0000H 0004H
Erase Block Region 3 Information	35H 36H 37H 38H	0003H 0000H 0000H 0001H
Erase Block Region 4 Information	39H 3AH 3BH 3CH	0000H 0000H 0000H 0000H

Table 8. Common Flash Memory Interface Code

Description	Addresses (Word Mode)	Data
Query-unique ASCII string "PRI"	40H 41H 42H	0050H 0052H 0049H
Major version number, ASCII	43H	0031H
Minor version number, ASCII	44H	0030H
Address Sensitive Unlock(Bits 1-0) 0 = Required, 1= Not Required Silcon Revision Number(Bits 7-2)	45H	0000H
Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write	46H	0002H
Block Protect 00 = Not Supported, 01 = Supported	47H	0001H
Block Temporary Unprotect 00 = Not Supported, 01 = Supported	48H	0000H
Block Protect/Unprotect scheme, 00 = Not Supported, 01 = Supported	49H	0001H
Simultaneous Operation 00 = Not Supported, XX = Number of Blocks except Bank 0	4AH	0073H
Burst Mode Type 00 = Not Supported, 01 = Supported	4BH	0000H
Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page	4CH	0002H
ACC(Acceleration) Supply Minimum 00 = Not Supported, D7 - D4 : Volt, D3 - D0 : 100mV	4DH	0085H
ACC(Acceleration) Supply Maximum 00 = Not Supported, D7 - D4 : Volt, D3 - D0 : 100mV	4EH	0095H
Top/Bottom Boot Block Flag 00H = No Boot, 01H = Dual Boot Device 02H = Bottom Boot Device, 03H = Top Boot Device	4FH	0001H

DEVICE STATUS FLAGS

The K8P5615UQA has means to indicate its status of operation in the bank where a program or erase operation is in processes. Address must include bank address being excuted internal routine operation. The status is indicated by raising the device status flag via corresponding DQ pins or the RY/ BY pin. The corresponding DQ pins are DQ7, DQ6, DQ5, DQ3 and DQ2. The statuses are as follows :

Table 9. Hardware Sequence Flags

	Status		DQ7	DQ6	DQ5	DQ3	DQ2	DQ1
In Progress	Programming		$\overline{DQ7}$	Toggle	0	0	1	0
	Block Erase or Chip Erase		0	Toggle	0	1	Toggle	0
	Erase Suspend Read	Erase Suspended Block	1	1	0	0	Toggle (Note 1)	0
	Erase Suspend Read	Non-Erase Suspended Block	Data	Data	Data	Data	Data	Data
	Erase Suspend Program	Non-Erase Suspended Block	$\overline{DQ7}$	Toggle	0	0	1	0
	Program Suspend Read	Program Suspended Block	DQ7	1	0	0	Toggle (Note 1)	0
	Program Suspend Read	Non-Program Suspended Block	Data	Data	Data	Data	Data	Data
Exceeded Time Limits	Programming		$\overline{DQ7}$	Toggle	1	0	No Toggle	0
	Block Erase or Chip Erase		0	Toggle	1	1	(Note 2)	0
	Erase Suspend Program		$\overline{DQ7}$	Toggle	1	0	No Toggle	0
Write to Buffer (Note 3)	BUSY State		$\overline{DQ7}$	Toggle	0	0	No Toggle	0
	Exceeded Timing Limits		$\overline{DQ7}$	Toggle	1	0	No Toggle	0
	ABORT State		$\overline{DQ7}$	Toggle	0	0	No Toggle	1

Notes :
1. DQ2 will toggle when the device performs successive read operations from the erase/program suspended block.
2. If DQ5 is High (exceeded timing limits), successive reads from a problem block will cause DQ2 to toggle.
3. Note that $\overline{DQ7}$ during Write-to-Buffer-Programming indicates the data-bar for DQ7 for the last loaded write-buffer address location.

DQ7 : $\overline{\text{Data}}$ Polling

When an attempt to read the device is made while executing the Internal Program, the complement of the data is written to DQ7 as an indication of the Routine in progress. When the Routine is completed an attempt to access to the device will produce the true data written to DQ7. When a user attempts to read the block being erased, DQ7 will be low. If the device is placed in the Erase/Program Suspend Mode, the status can be detected via the DQ7 pin. If the system tries to read an address which belongs to a block that is being erase suspended, DQ7 will be high. And, if the system tries to read an address which belongs to a block that is being program suspended, the output will be the true data of DQ7 itself. If a non-erase-suspended or non-program-suspended block address is read, the device will produce the true data to DQ7. If an attempt is made to program a protected block, DQ7 outputs complements the data for approximately 1μs and the device then returns to the Read Mode without changing data in the block. If an attempt is made to erase a protected block, DQ7 outputs complement data in approximately 100us and the device then returns to the Read Mode without erasing the data in the block.

DQ6 : Toggle Bit

Toggle bit is another option to detect whether an Internal Routine is in progress or completed. Once the device is at a busy state, DQ6 will toggle. Toggling DQ6 will stop after the device completes its Internal Routine. If the device is in the Erase/Program Suspend Mode, an attempt to read an address that belongs to a block that is being erased or programmed will produce a high output of DQ6. If an address belongs to a block that is not being erased or programmed, toggling is halted and valid data is produced at DQ6. If an attempt is made to program a protected block, DQ6 toggles for approximately 1us and the device then returns to the Read Mode without changing the data in the block. If an attempt is made to erase a protected block, DQ6 toggles for approximately 100μs and the device then returns to the Read Mode without erasing the data in the block.

DQ5 : Exceed Timing Limits

If the Internal Program/Erase Routine extends beyond the timing limits, DQ5 will go High, indicating program/erase failure.

DQ3 : Block Erase Timer

The status of the multi-block erase operation can be detected via the DQ3 pin. DQ3 will go High if 50μs of the block erase time window expires. In this case, the Internal Erase Routine will initiate the erase operation.Therefore, the device will not accept further write commands until the erase operation is completed. DQ3 is Low if the block erase time window is not expired. Within the block erase time window, an additional block erase command (30H) can be accepted. To confirm that the block erase command has been accepted, the software may check the status of DQ3 following each block erase command.

DQ2 : Toggle Bit 2

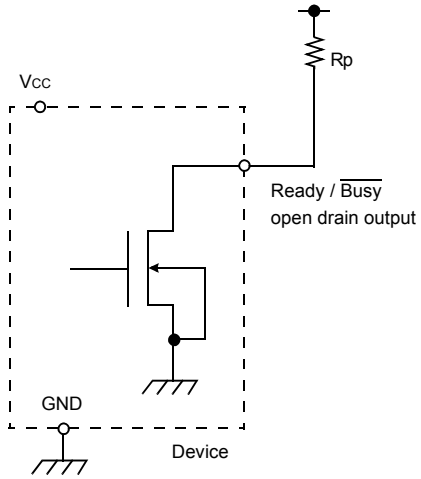
The device generates a toggling pulse in DQ2 only if an Internal Erase Routine or an Erase/Program Suspend is in progress. When the device executes the Internal Erase Routine, DQ2 toggles only if an erasing bank is read. Although the Internal Erase Routine is in the Exceeded Time Limits, DQ2 toggles only if an erasing block in the Exceeded Time Limits is read. When the device is in the Erase/Program Suspend mode, DQ2 toggles only if an address in the erasing or programming block is read. If a non-erasing or non-programmed block address is read during the Erase/Program Suspend mode, then DQ2 will produce valid data. DQ2 will go High if the user tries to program a non-erase suspend block while the device is in the Erase Suspend mode.

DQ1 : Buffer Program Abort Indicator

DQ1 indicates whether a Write-to-Buffer operation was aborted. Under these conditions DQ1 produces a "1". The system must issue the Write-to-Buffer-Abort-Reset command sequence to return the device to reading array data.

RY/$\overline{BY}$: Ready/$\overline{Busy}$

The K8P5615UQA has a Ready / $\overline{Busy}$ output that indicates either the completion of an operation or the status of Internal Algorithms. If the output is Low, the device is busy with either a program or an erase operation. If the output is High, the device is ready to accept any read/write or erase operation. When the RY/ $\overline{BY}$ pin is low, the device will not accept any additional program or erase commands with the exception of the Erase Suspend command. If the K8P5615UQA is placed in an Erase Suspend mode, the RY/ $\overline{BY}$ output will be High. For programming, the RY/ $\overline{BY}$ is valid (RY/ $\overline{BY}$ = 0) after the rising edge of the fourth $\overline{WE}$ pulse in the four write pulse sequence. For Chip Erase, RY/ $\overline{BY}$ is also valid after the rising edge of $\overline{WE}$ pulse in the six write pulse sequence. For Block Erase, RY/ $\overline{BY}$ is also valid after the rising edge of the sixth $\overline{WE}$ pulse.
The pin is an open drain output, allowing two or more Ready/ $\overline{Busy}$ outputs to be OR-tied. An appropriate pull-up resistor is required for proper operation.



$$Rp = \frac{Vcc\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \Sigma I_L} = \frac{3.5\ V}{2.1mA + \Sigma I_L}$$

where ΣI_L is the sum of the input currents of all devices tied to the Ready / $\overline{Busy}$ pin.

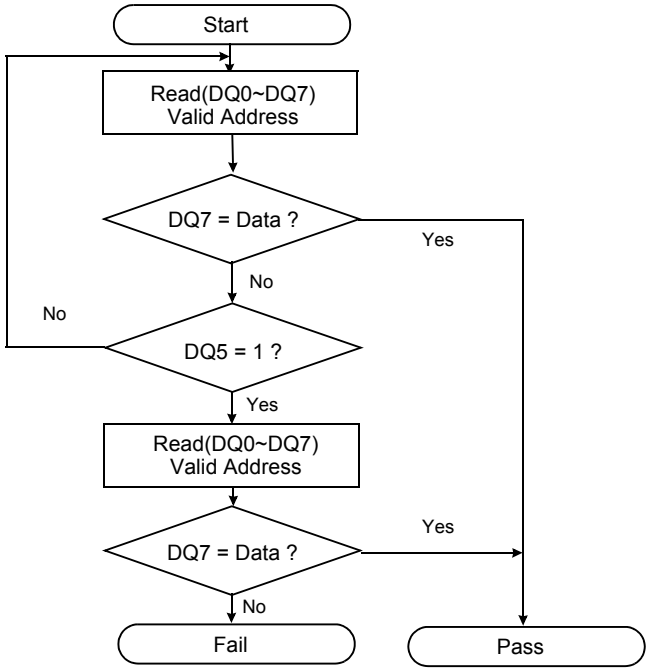


Figure 8. Data Polling Algorithms

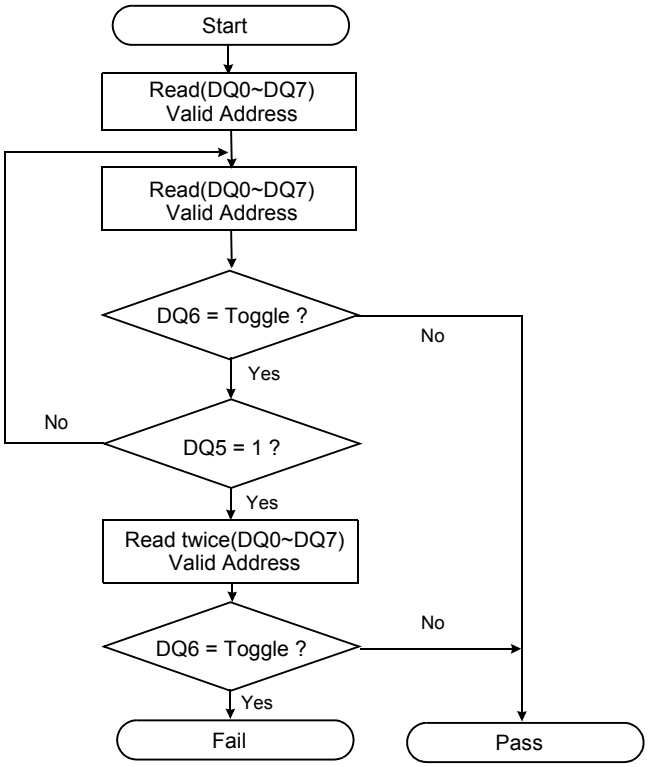


Figure 9. Toggle Bit Algorithms

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{CC}	V_{CC}	-0.5 to +4.0	V
	$\overline{WP}$/ACC	V_{IN}	-0.5 to +9.5	
	All Other Pins		-0.5 to Vcc+0.5	
Temperature Under Bias	Commercial	T_{bias}	-10 to +125	°C
	Extended		-25 to +125	
Storage Temperature		T_{stg}	-65 to +150	°C
Short Circuit Output Current		I_{OS}	5	mA
Operating Temperature		T_A (Industrial Temp.)	-40 to +85	°C
		T_A (Extended Temp.)	-25 to + 85	°C

Notes :
1. Minimum DC voltage is -0.5V on Input/ Output pins. During transitions, this level may fall to -2.0V for periods <20ns. Maximum DC voltage on input / output pins is Vcc+0.5V which, during transitions, may overshoot to Vcc+2.0V for periods <20ns.
2. Minimum DC voltage is -0.5V on $\overline{WP}$/ACC pins. During transitions, this level may fall to -2.0V for periods <20ns. Maximum DC voltage on $\overline{WP}$/ACC pins is 9.5V which, during transitions, may overshoot to 10.5V for periods <20ns.
3. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to GND)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC}	2.7	3.0	3.6	V
Supply Voltage	V_{SS}	0	0	0	V

DC CHARACTERISTICS

Parameter	Sym-bol	Test Conditions		Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}, V_{CC}=V_{CCmax}		– 1.0	-	+ 1.0	µA
$\overline{WP}$/ACC Input Leakage Current	I_{LIW}	V_{CC}=V_{CCmax}, $\overline{WP}$/ACC=9.5V		-	-	35	µA
Output Leakage Current	I_{LO}	V_{OUT}=V_{SS} to V_{CC},V_{CC}=V_{CCmax},$\overline{OE}$=V_{IH}		– 1.0	-	+ 1.0	µA
Active Read Current (1)	I_{CC1}	$\overline{OE}$=V_{IH}, V_{CC}=V_{CCmax}	5MHz	-	30	45	mA
Active Write Current (2)	I_{CC2}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}, $\overline{WE}$=V_{IL}		-	25	50	mA
Read While Program Current (3)	I_{CC3}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH} (@5Mhz)		-	35	50	mA
Read While Erase Current (3)	I_{CC4}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH} (@10Mhz)		-	35	50	mA
Program While Erase Suspend Current	I_{CC5}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}		-	27	55	mA
Page Read Current	I_{CC6}	$\overline{OE}$=VIH, 8-word Page Read	40MHz	-	10	15	mA
ACC Accelerated Program Current	I_{ACC}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}		-	15	30	mA
Standby Current	I_{SB1}	$\overline{CE}$, $\overline{RESET}$, $\overline{WP}$/ACC= V_{cc}± 0.3		-	20	60	µA
Standby Current During Reset	I_{SB2}	$\overline{RESET}$= Vss± 0.3		-	20	60	µA
Automatic Sleep Mode	I_{SB3}	V_{IH}=Vcc ± 0.3V, V_{IL}=V_{SS} ±0.2V		-	20	60	µA
Input Low Level	V_{IL}	Vcc=2.7~3.6V		-0.5	-	Vcc x 0.2	V
Input High Level	V_{IH}	Vcc=2.7~3.6V		Vcc x 0.8	-	Vcc+0.3	V
Voltage for $\overline{WP}$/ACC Block Temporarily Unprotect and Program Acceleration (4)	V_{HH}	Vcc = 2.7~3.6V		8.5	-	9.5	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Low Level	V_{OL}	IOL =100uA,Vcc=VCCmin	-	-	0.1	V
Output High Level	V_{OH}	IOH = -100uA, Vcc=VCCmin	Vcc - 0.2	-	-	V
Low VCC Lock-out Voltage (5)	V_{LKO}		2.3	-	2.5	V

Notes :
1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component(at 5 MHz).
2. I_{CC} active during Internal Routine(program or erase) is in progress.
3. I_{CC} active during Read while Write is in progress.
4. The high voltage (V_{HH}) must be used in the range of Vcc = 2.7V ~ 3.6V
5. Not 100% tested.

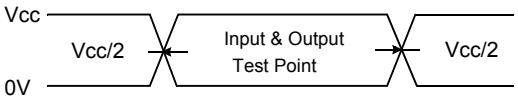
CAPACITANCE(T_A = 25 °C, V_{CC} = 3.0V, f = 1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	10	pF
Control Pin Capacitance	C_{IN2}	V_{IN}=0V	-	10	pF

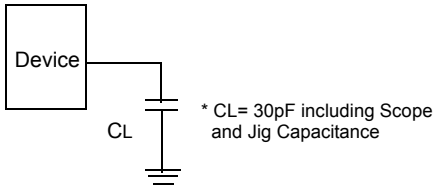
Note : Capacitance is periodically sampled and not 100% tested.

AC TEST CONDITION

Parameter	Value
Input Pulse Levels	0V to Vcc
Input Rise and Fall Times(Vio=1.8,3.0V)	5ns
Input and Output Timing Levels	Vcc/2
Output Load	C_L = 30pF



Input Pulse and Test Point



Output Load

AC CHARACTERISTICS
Read Operations

Parameter	Symbol	Vcc = 2.7V~3.6V		Unit
		4D		
		Min	Max	
Read Cycle Time (1)	t_{RC}	70	-	ns
Address Access Time	t_{AA}	-	70	ns
Chip Enable Access Time	t_{CE}	-	70	ns
Output Enable Time	t_{OE}	-	30	ns
Page Address Access Time	t_{PA}	-	30	ns
$\overline{CE}$ & $\overline{OE}$ Disable Time (1)	t_{DF}	-	16	ns
Output Hold Time from Address, $\overline{CE}$ or $\overline{OE}$ (1)	t_{OH}	5	-	ns

Note : 1. Not 100% tested.

SWITCHING WAVEFORMS

Conventional Read Operations

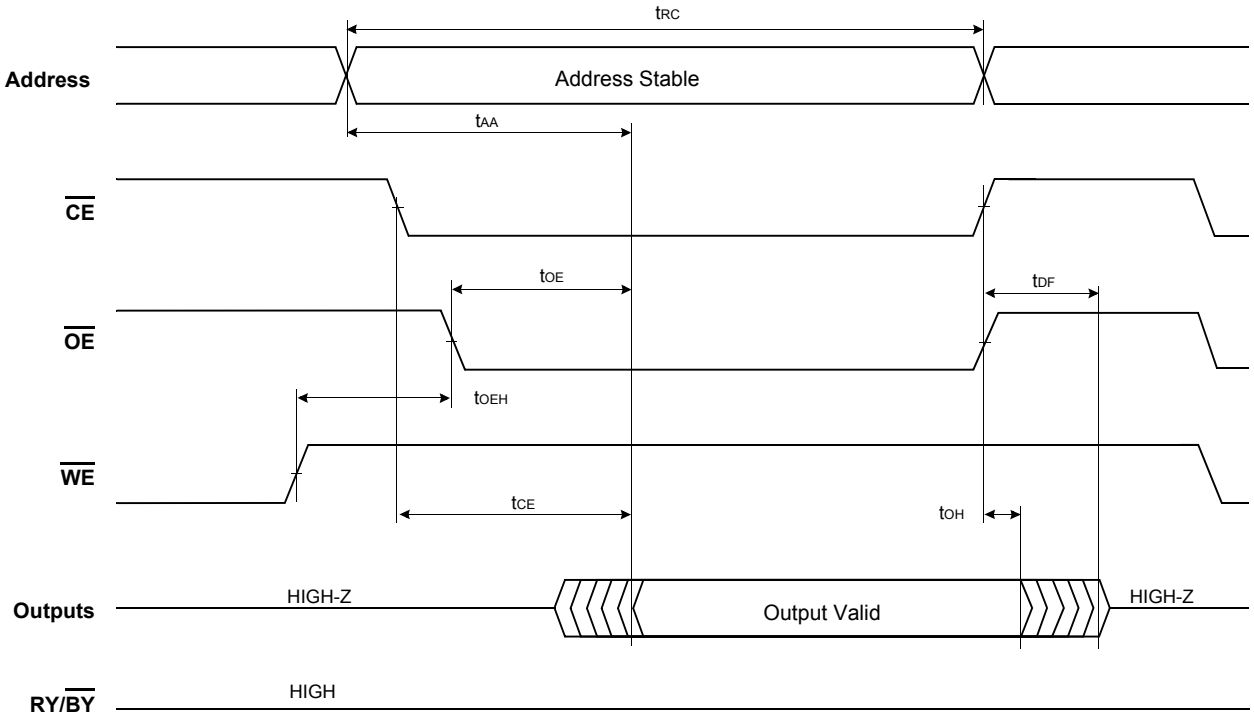


Figure 10. Conventional Read Operation Timings

Page Read Operations

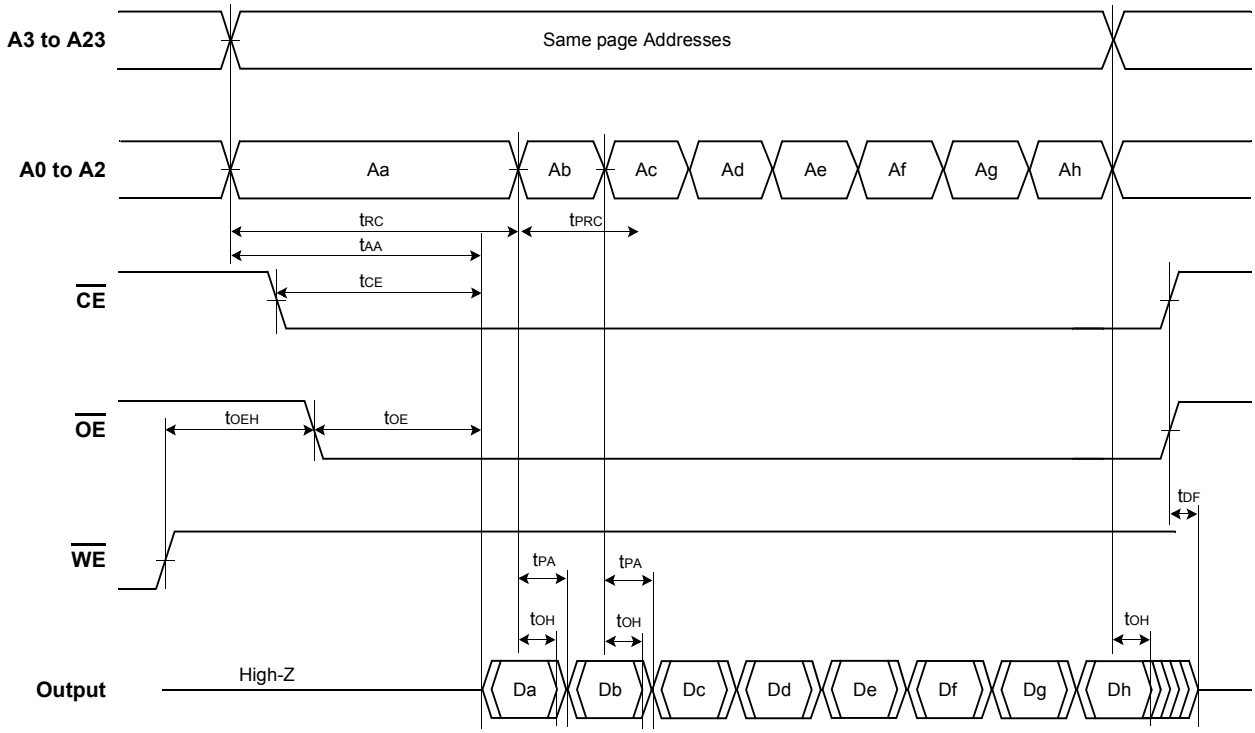


Figure 11. Page Read Operation Timings

SWITCHING WAVEFORMS

Hardware Reset/Read Operations

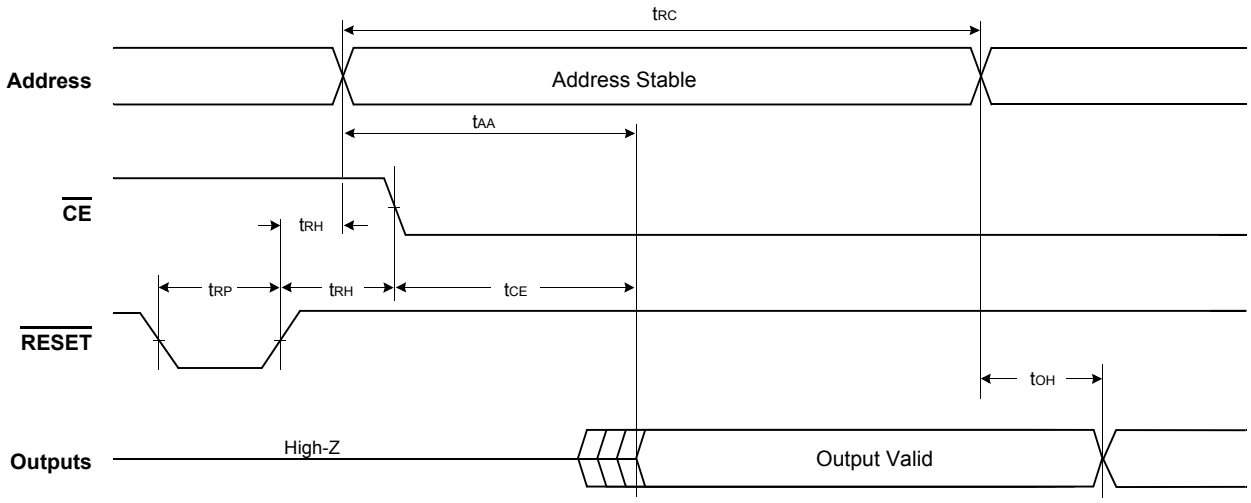


Figure 12. Hardware Reset/Read Operation Timings

Parameter	Symbol	4D		Unit
		Min	Max	
Read Cycle Time	t_{RC}	70	-	ns
Address Access Time	t_{AA}	-	70	ns
Chip Enable Access Time	t_{CE}	-	70	ns
Output Hold Time from Address, $\overline{CE}$ or $\overline{OE}$	t_{OH}	5	-	ns
$\overline{RESET}$ Pulse Width	t_{RP}	30	-	μs
$\overline{RESET}$ High Time Before Read	t_{RH}	200	-	ns

AC CHARACTERISTICS
Write(Erase/Program)Operations

Parameter		Symbol	Vcc = 2.7V ~ 3.6V		Unit
			4D		
			Min	Max	
Write Cycle Time (1)		t_{WC}	70	-	ns
Address Setup Time		t_{AS}	0	-	ns
Address Hold Time		t_{AH}	35	-	ns
		t_{AHT}	0	-	ns
Data Setup Time		t_{DS}	30	-	ns
Data Hold Time		t_{DH}	0	-	ns
Output Enable Setup Time (1)		t_{OES}	0	-	ns
Output Enable Hold	Read (1)	t_{OEH1}	0	-	ns
	Toggle and $\overline{\text{Data}}$ Polling (1)	t_{OEH2}	10	-	ns
$\overline{\text{CE}}$ Setup Time		t_{CS}	0	-	ns
$\overline{\text{CE}}$ Hold Time		t_{CH}	0	-	ns
Write Pulse Width		t_{WP}	40	-	ns
Write Pulse Width High		t_{WPH}	25	-	ns
Programming Operation (2)		t_{PGM}	40(typ.)		µs
Accelerated Programming Operation (2)		t_{ACCPGM}	24(typ.)		µs
Sector Erase Operation (2)		t_{BERS}	1.6(typ)		sec
V_{CC} Set Up Time		t_{VCS}	250	-	µs
V_{HH} Set Up Time		t_{VHH}	250		ns
Write Recovery Time from RY/$\overline{\text{BY}}$		t_{RB}	0	-	ns
Program/Erase Valid to RY/$\overline{\text{BY}}$ Delay		t_{BUSY}	-	90	ns
Read Recovery Time Before Write		t_{GHWL}	0	-	ns
$\overline{\text{CE}}$ High during toggling bit polling		t_{CEPH}	20	-	ns
$\overline{\text{OE}}$ High during toggling bit polling		t_{OEPH}	10	-	ns

Notes : 1. Not 100% tested.
2. The duration of the Program or Erase operation varies and is calculated in the internal algorithms.

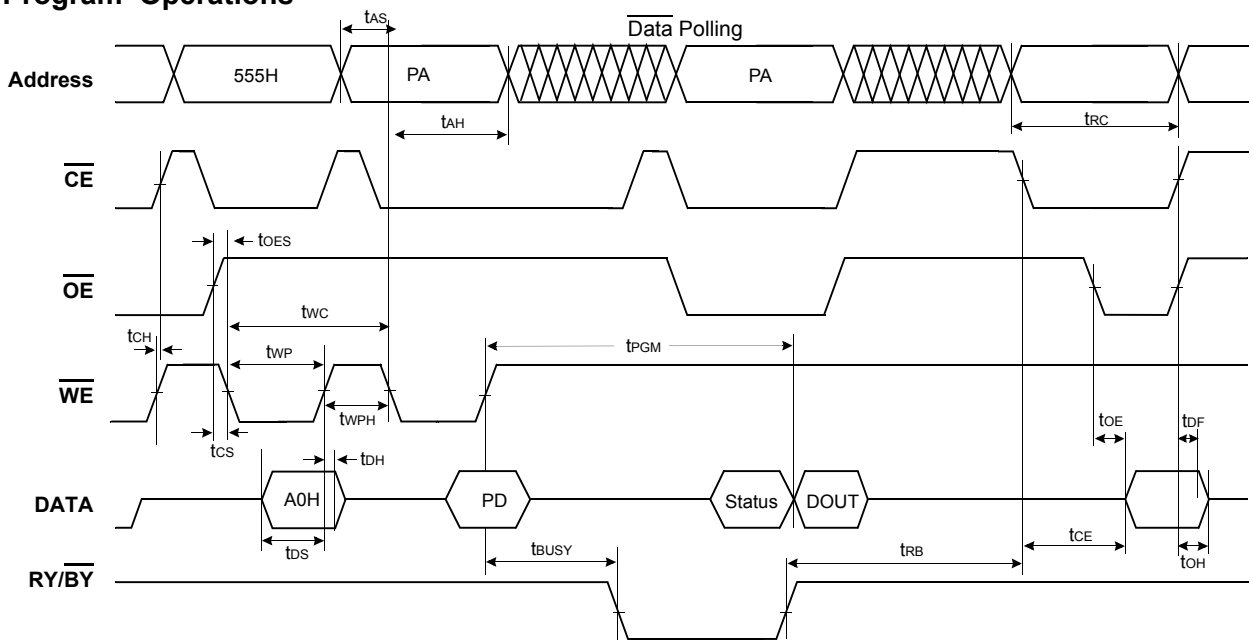
ERASE AND PROGRAM PERFORMANCE

Parameter		Condition	Limits			Unit	Comments
			Min	Typ	Max		
Block Erase Time	128 Kword	V_{CC}	-	1.6	7	sec	Excludes 00H programming prior to erasure
		ACC		1.6	7		
	32 Kword	V_{CC}		0.5	4		
		ACC	-	0.5	4		
Chip Erase Time		V_{CC}	-	206	900	sec	
		ACC		130	512		
Word Programming Time		V_{CC}	-	40	400	µs	Excludes system-level overhead
		ACC		24	240		
Word Programming time with 32-words Buffer		V_{CC}	-	9.4	94	µs	
		ACC		6	60		
Total 32-words Buffer Programming Time		V_{CC}	-	300	3000	µs	Excludes system-level overhead
		ACC		192	1920		
Chip Programming Time with 32-word Buffer		V_{CC}	-	157.3	315	sec	Excludes system-level overhead
		ACC		100	200		
Erase/Program Endurance			100,000	-	-	cycles	Minimum 100,000 cycles guaranteed

Notes : 1. 25 °C, V_{CC} = 3.0V 100,000 cycles, typical pattern.
2. System-level overhead is defined as the time required to execute the four bus cycle command necessary to program each word. In the preprogramming step of the Internal Erase Routine, all words are programmed to 00H before erasure.

SWITCHING WAVEFORMS

Program Operations



Notes : 1. $\overline{DQ7}$ is the output of the complement of the data written to the device.
2. D_{OUT} is the output of the data written to the device.
3. PA : Program Address, PD : Program Data
4. The illustration shows the last two cycles of the program command sequence.

Figure 13. Program Operation Timings

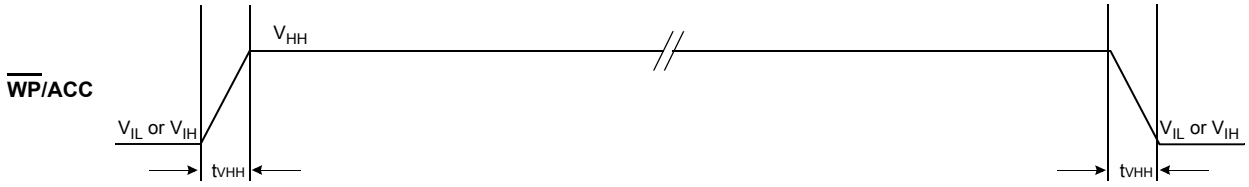


Figure 14. Accelerated Program Timings

SWITCHING WAVEFORMS

Chip/Block Erase Operations

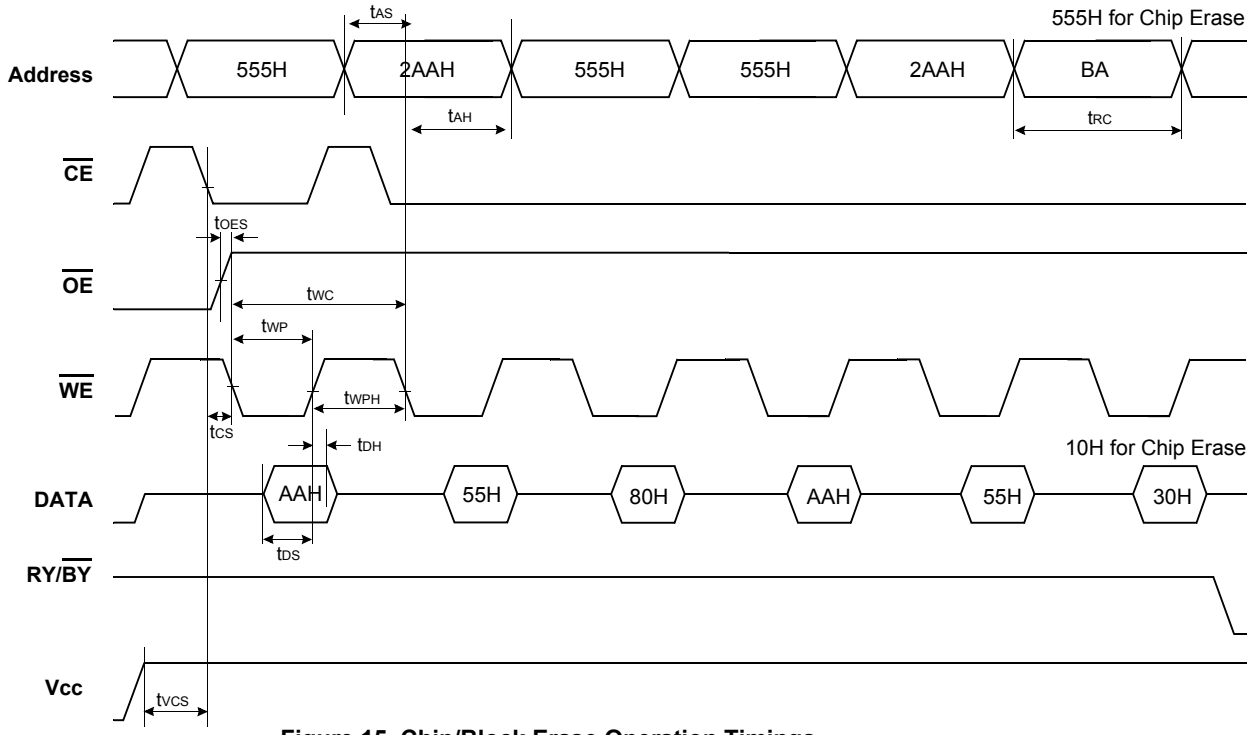


Figure 15. Chip/Block Erase Operation Timings

Note : BA : Block Address

Read While Write Operations

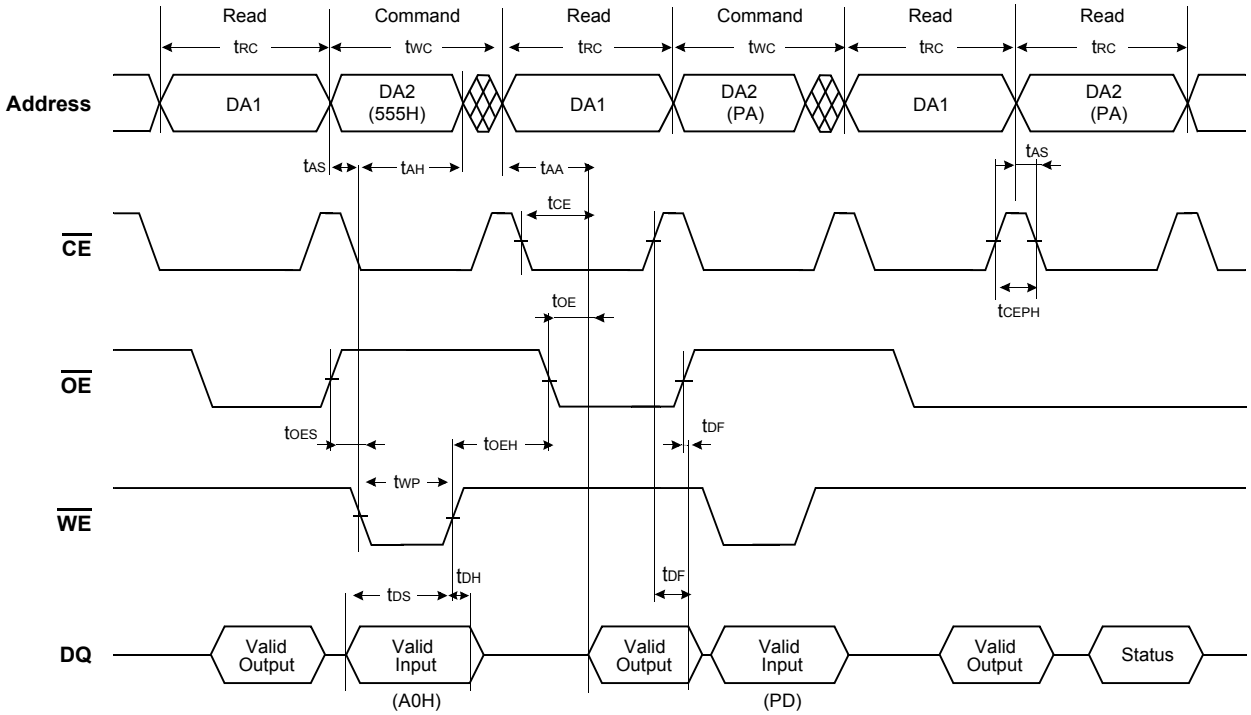
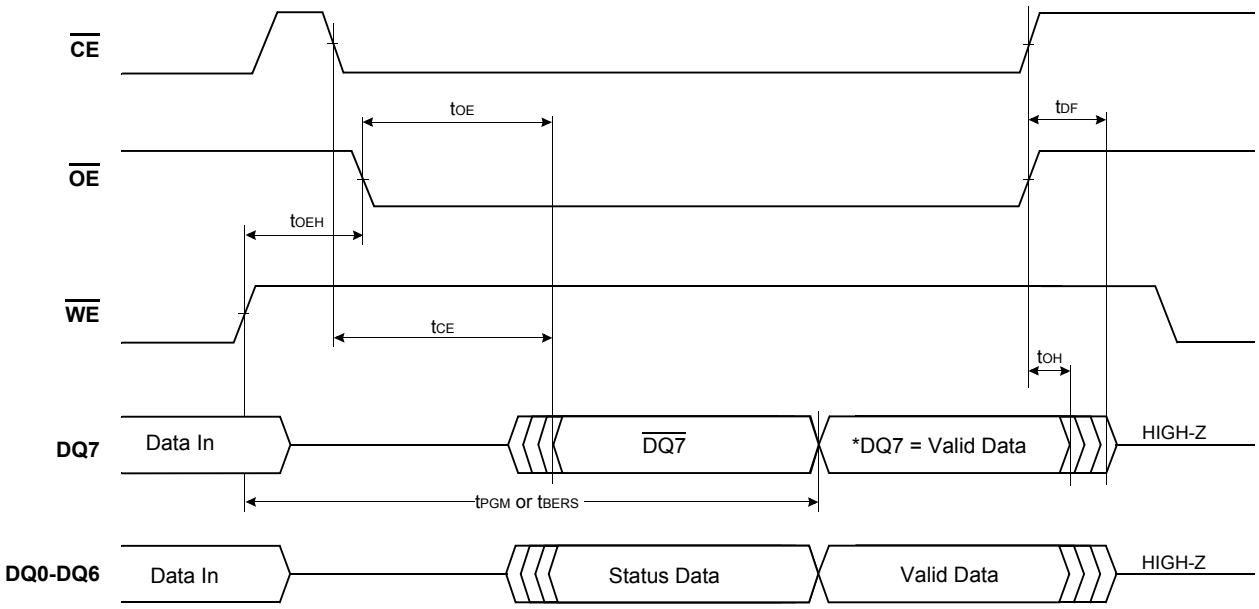


Figure 16. Read While Write Operation Timings

Note : This is an example in the program-case of the Read While Write function.
DA1 : Address of Bank1, DA2 : Address of Bank 2, PA = Program Address at one bank , RA = Read Address at the other bank,
PD = Program Data In , RD = Read Data Out

SWITCHING WAVEFORMS

$\overline{\text{Data}}$ Polling During Internal Routine Operation



Note : *DQ7=Vaild Data (The device has completed the internal operation).

Figure 17. $\overline{\text{Data}}$ Polling During Internal Routine Operation Timings

RY/$\overline{\text{BY}}$ Timing Diagram During Program/Erase Operation

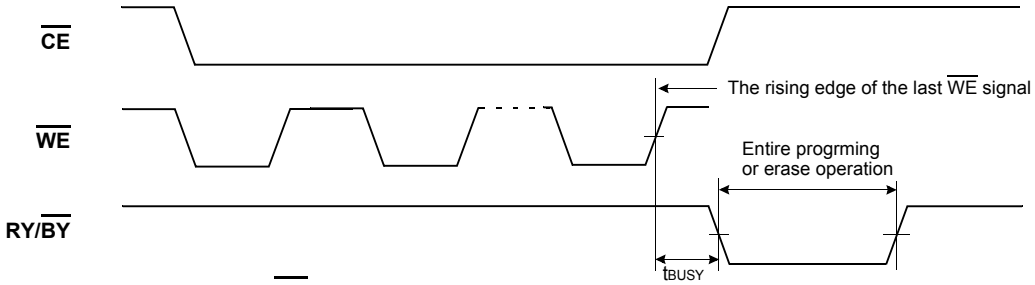
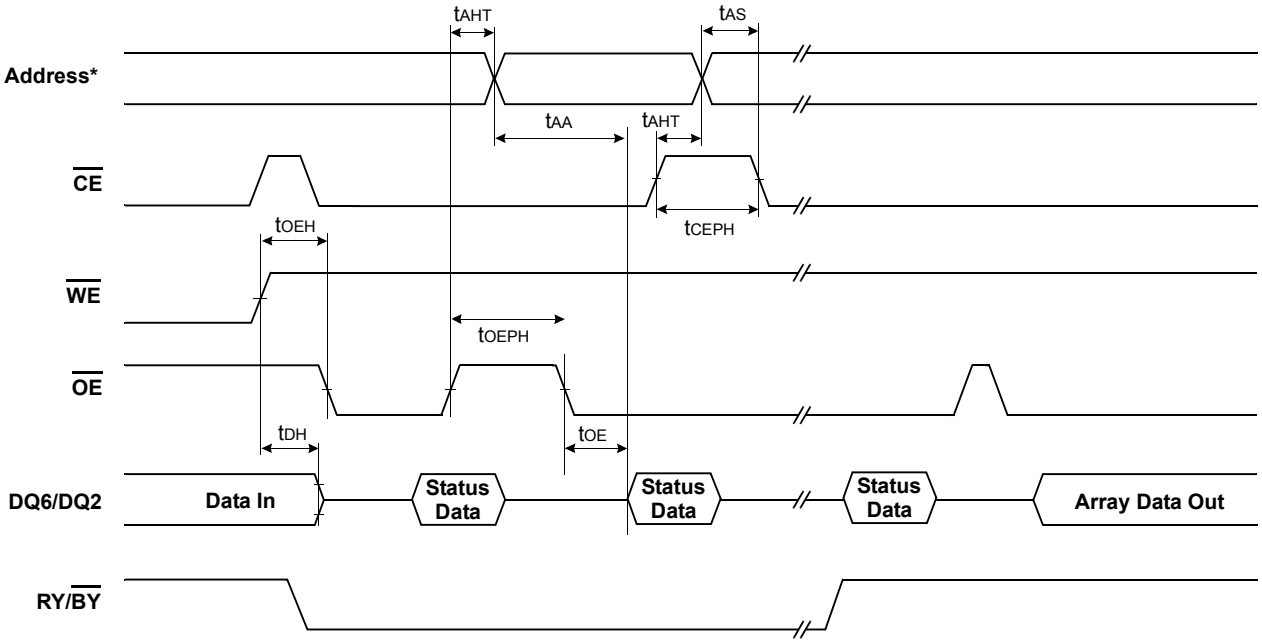


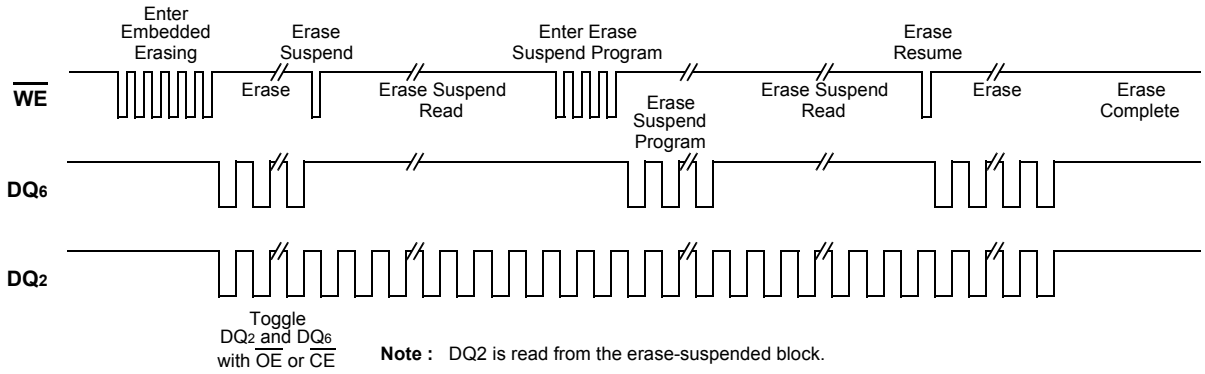
Figure 18. RY/$\overline{\text{BY}}$ Timing Diagram During Program/Erase Operation Timings

Parameter	Symbol	4D		Unit
		Min	Max	
Program/Erase Valid to RY/$\overline{\text{BY}}$ Delay	tBUSY	-	90	ns
Chip Enable Access Time	tCE	-	70	ns
Output Enable Time	tOE	-	20	ns
$\overline{\text{CE}}$ & $\overline{\text{OE}}$ Disable Time	tDF	-	16	ns
Output Hold Time from Address, $\overline{\text{CE}}$ or $\overline{\text{OE}}$	tOH	5	-	ns
$\overline{\text{OE}}$ Hold Time	tOEH	10	-	ns

SWITCHING WAVEFORMS
Toggle Bit During Internal Routine Operation



Note : Address for the write operation must include a bank address (A19~A22) where the data is written.

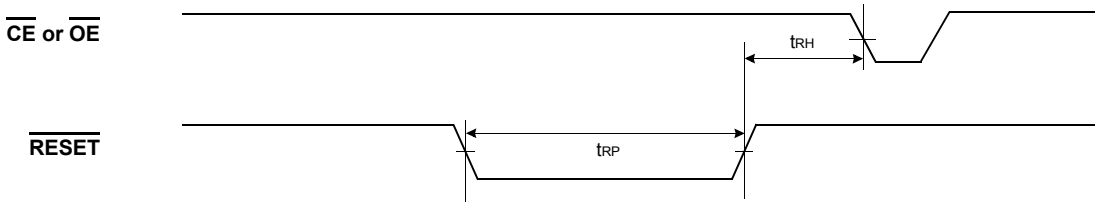


Note : DQ2 is read from the erase-suspended block.

Figure 19. Toggle Bit During Internal Routine Operation Timings

SWITCHING WAVEFORMS

$\overline{\text{RESET}}$ Timing Diagram



Power-up and $\overline{\text{RESET}}$ Timing Diagram

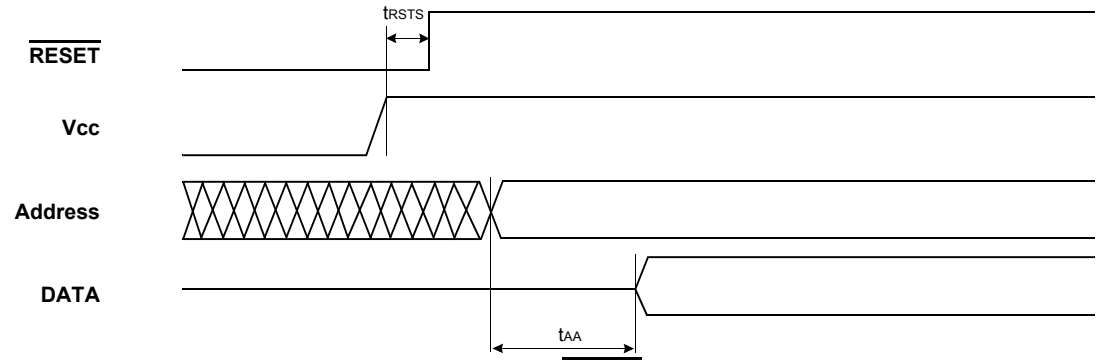
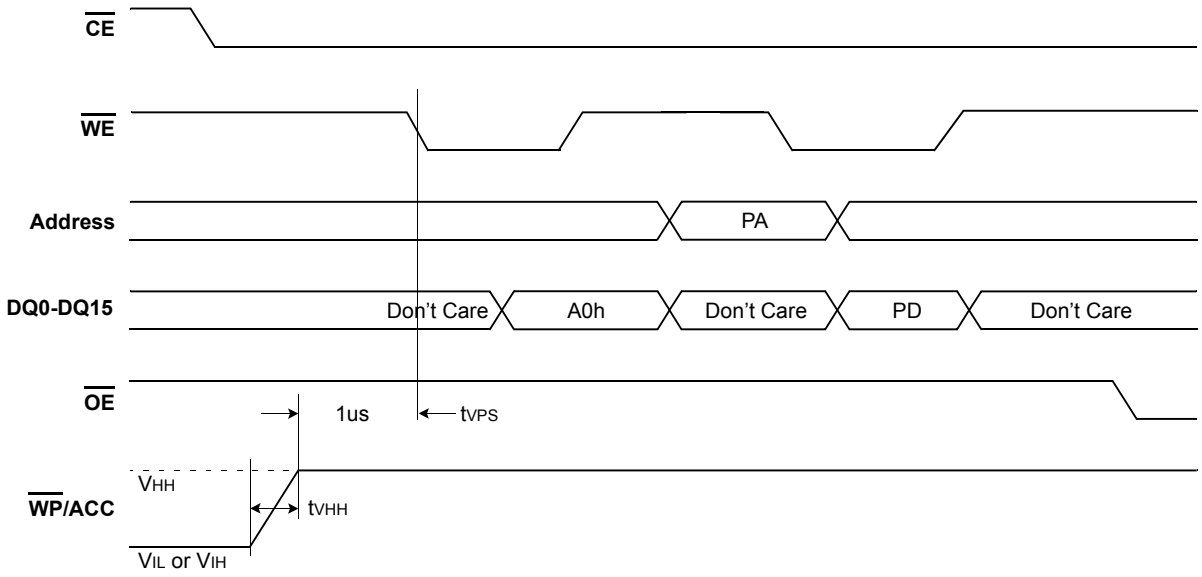


Figure 20. Power-up and $\overline{\text{RESET}}$ Timing Diagram

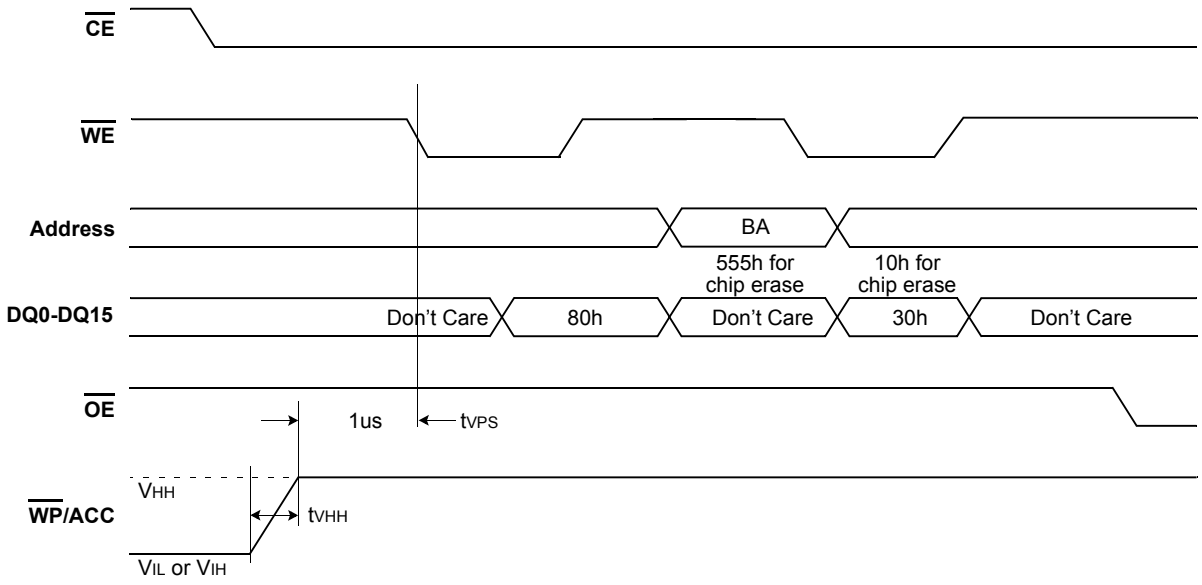
Parameter	Sym-bol	4D		Unit
		Min	Max	
$\overline{\text{RESET}}$ Pulse Width	t_{RP}	30	-	μs
$\overline{\text{RESET}}$ High Time Before Read	t_{RH}	200	-	ns
$\overline{\text{RESET}}$ Low Set-up Time	t_{RSTS}	250	-	μs

SWITCHING WAVEFORMS

Unlock Bypass Program Operations(Accelerated Program)



Unlock Bypass Block Erase Operations(Accelerated Program)



Notes:

1. V_{HH} can be left high for subsequent programming pulses.
2. Use setup and hold times from conventional program operations.
3. Unlock Bypass Program/Erase commands can be used when the V_{HH} is applied to $\overline{WP}$/ACC

Figure 22. Unlock Bypass Operation Timings

Table 10. Block Architecture (K8P5615UQA)

Bank	Block	Block Size	(x16) Address Range
Bank 3	BA133	32 Kwords	FF8000h-FFFFFFh
	BA132	32 Kwords	FF0000h-FF7FFFh
	BA131	32 Kwords	FE8000h-FEFFFFh
	BA130	32 Kwords	FE0000h-FE7FFFh
	BA129	128 Kwords	FC0000h-FDFFFFh
	BA128	128 Kwords	FA0000h-FBFFFFh
	BA127	128 Kwords	F80000h-F9FFFFh
	BA126	128 Kwords	F60000h-F7FFFFh
	BA125	128 Kwords	F40000h-F5FFFFh
	BA124	128 Kwords	F20000h-F3FFFFh
	BA123	128 Kwords	F00000h-F1FFFFh
	BA122	128 Kwords	EE0000h-EFFFFFh
	BA121	128 Kwords	EC0000h-EDFFFFh
	BA120	128 Kwords	EA0000h-EBFFFFh
	BA119	128 Kwords	E80000h-E9FFFFh
	BA118	128 Kwords	E60000h-E7FFFFh
	BA117	128 Kwords	E40000h-E5FFFFh
	BA116	128 Kwords	E20000h-E3FFFFh
	BA115	128 Kwords	E00000h-E1FFFFh
Bank 2	BA114	128 Kwords	DE0000h-DFFFFFh
	BA113	128 Kwords	DC0000h-DDFFFFh
	BA112	128 Kwords	DA0000h-DBFFFFh
	BA111	128 Kwords	D80000h-D9FFFFh
	BA110	128 Kwords	D60000h-D7FFFFh
	BA109	128 Kwords	D40000h-D5FFFFh
	BA108	128 Kwords	D20000h-D3FFFFh
	BA107	128 Kwords	D00000h-D1FFFFh
	BA106	128 Kwords	CE0000h-CFFFFFh
	BA105	128 Kwords	CC0000h-CDFFFFh
	BA104	128 Kwords	CA0000h-CBFFFFh
	BA103	128 Kwords	C80000h-C9FFFFh
	BA102	128 Kwords	C60000h-C7FFFFh
	BA101	128 Kwords	C40000h-C5FFFFh
	BA100	128 Kwords	C20000h-C3FFFFh
	BA99	128 Kwords	C00000h-C1FFFFh
	BA98	128 Kwords	BE0000h-BFFFFFh
	BA97	128 Kwords	BC0000h-BDFFFFh
	BA96	128 Kwords	BA0000h-BBFFFFh
	BA95	128 Kwords	B80000h-B9FFFFh
	BA94	128 Kwords	B60000h-B7FFFFh
	BA93	128 Kwords	B40000h-B5FFFFh
	BA92	128 Kwords	B20000h-B3FFFFh

Table 10. Block Architecture (K8P5615UQA)

Bank	Block	Block Size	(x16) Address Range
Bank 2	BA91	128 Kwords	B00000h-B1FFFFh
	BA90	128 Kwords	AE0000h-AFFFFFh
	BA89	128 Kwords	AC0000h-ADFFFFh
	BA88	128 Kwords	AA0000h-ABFFFFh
	BA87	128 Kwords	A80000h-A9FFFFh
	BA86	128 Kwords	A60000h-A7FFFFh
	BA85	128 Kwords	A40000h-A5FFFFh
	BA84	128 Kwords	A20000h-A3FFFFh
	BA83	128 Kwords	A00000h-A1FFFFh
	BA82	128 Kwords	9E0000h-9FFFFFh
	BA81	128 Kwords	9C0000h-9DFFFFh
	BA80	128 Kwords	9A0000h-9BFFFFh
	BA79	128 Kwords	980000h-99FFFFh
	BA78	128 Kwords	960000h-97FFFFh
	BA77	128 Kwords	940000h-95FFFFh
	BA76	128 Kwords	920000h-93FFFFh
	BA75	128 Kwords	900000h-91FFFFh
	BA74	128 Kwords	8E0000h-8FFFFFh
	BA73	128 Kwords	8C0000h-8DFFFFh
	BA72	128 Kwords	8A0000h-8BFFFFh
	BA71	128 Kwords	880000h-89FFFFh
	BA70	128 Kwords	860000h-87FFFFh
	BA69	128 Kwords	840000h-85FFFFh
	BA68	128 Kwords	820000h-83FFFFh
	BA67	128 Kwords	800000h-81FFFFh
Bank 1	BA66	128 Kwords	7E0000h-7FFFFFh
	BA65	128 Kwords	7C0000h-7DFFFFh
	BA64	128 Kwords	7A0000h-7BFFFFh
	BA63	128 Kwords	780000h-79FFFFh
	BA62	128 Kwords	760000h-77FFFFh
	BA61	128 Kwords	740000h-75FFFFh
	BA60	128 Kwords	720000h-73FFFFh
	BA59	128 Kwords	700000h-71FFFFh
	BA58	128 Kwords	6E0000h-6FFFFFh
	BA57	128 Kwords	6C0000h-6DFFFFh
	BA56	128 Kwords	6A0000h-6BFFFFh
	BA55	128 Kwords	680000h-69FFFFh
	BA54	128 Kwords	660000h-67FFFFh
	BA53	128 Kwords	640000h-65FFFFh
	BA52	128 Kwords	620000h-63FFFFh
	BA51	128 Kwords	600000h-61FFFFh
	BA50	128 Kwords	5E0000h-5FFFFFh
	BA49	128 Kwords	5C0000h-5DFFFFh
	BA48	128 Kwords	5A0000h-5BFFFFh
	BA47	128 Kwords	580000h-59FFFFh

Table 10. Block Architecture (K8P5615UQA)

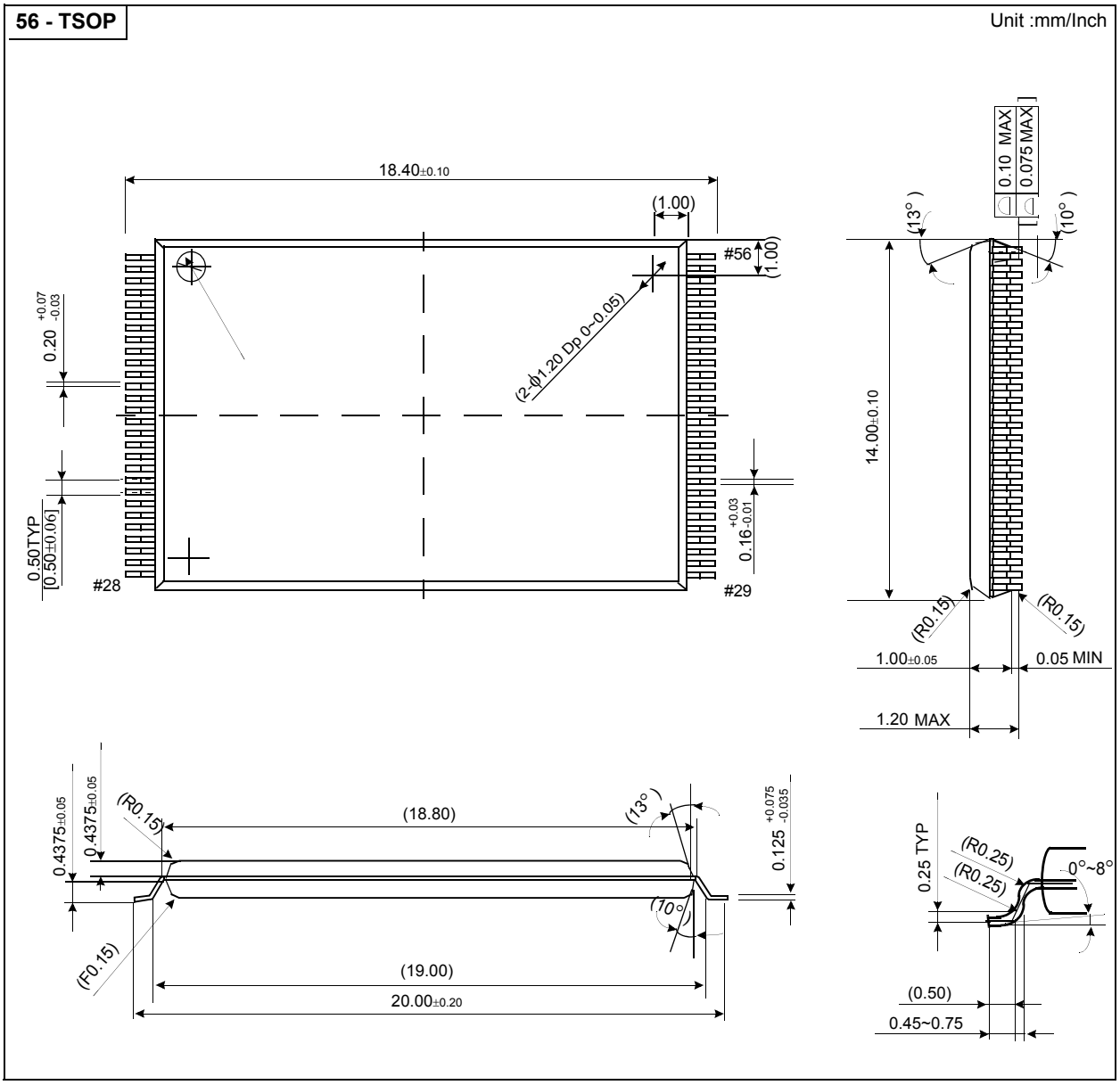
Bank	Block	Block Size	(x16) Address Range
Bank 1	BA46	128 Kwords	560000h-57FFFFh
	BA45	128 Kwords	540000h-55FFFFh
	BA44	128 Kwords	520000h-53FFFFh
	BA43	128 Kwords	500000h-51FFFFh
	BA42	128 Kwords	4E0000h-4FFFFFh
	BA41	128 Kwords	4C0000h-4DFFFFh
	BA40	128 Kwords	4A0000h-4BFFFFh
	BA39	128 Kwords	480000h-49FFFFh
	BA38	128 Kwords	460000h-47FFFFh
	BA37	128 Kwords	440000h-45FFFFh
	BA36	128 Kwords	420000h-43FFFFh
	BA35	128 Kwords	400000h-41FFFFh
	BA34	128 Kwords	3E0000h-3FFFFFh
	BA33	128 Kwords	3C0000h-3DFFFFh
	BA32	128 Kwords	3A0000h-3BFFFFh
	BA31	128 Kwords	380000h-39FFFFh
	BA30	128 Kwords	360000h-37FFFFh
	BA29	128 Kwords	340000h-35FFFFh
	BA28	128 Kwords	320000h-33FFFFh
	BA27	128 Kwords	300000h-31FFFFh
	BA26	128 Kwords	2E0000h-2FFFFFh
	BA25	128 Kwords	2C0000h-2DFFFFh
	BA24	128 Kwords	2A0000h-2BFFFFh
	BA23	128 Kwords	280000h-29FFFFh
	BA22	128 Kwords	260000h-27FFFFh
	BA21	128 Kwords	240000h-25FFFFh
	BA20	128 Kwords	220000h-23FFFFh
	BA19	128 Kwords	200000h-21FFFFh
Bank 0	BA18	128 Kwords	1E0000h-1FFFFFh
	BA17	128 Kwords	1C0000h-1DFFFFh
	BA16	128 Kwords	1A0000h-1BFFFFh
	BA15	128 Kwords	180000h-19FFFFh
	BA14	128 Kwords	160000h-17FFFFh
	BA13	128 Kwords	140000h-15FFFFh
	BA12	128 Kwords	120000h-13FFFFh
	BA11	128 Kwords	100000h-11FFFFh
	BA10	128 Kwords	0E0000h-0FFFFFh
	BA9	128 Kwords	0C0000h-0DFFFFh
	BA8	128 Kwords	0A0000h-0BFFFFh
	BA7	128 Kwords	080000h-09FFFFh
	BA6	128 Kwords	060000h-07FFFFh
	BA5	128 Kwords	040000h-05FFFFh
	BA4	128 Kwords	020000h-03FFFFh
	BA3	32 Kwords	018000h-01FFFFh
	BA2	32 Kwords	010000h-017FFFh
	BA1	32 Kwords	008000h-00FFFFh
	BA0	32 Kwords	000000h-007FFFh

PACKAGE DIMENSIONS

56-PIN LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE

56 - TSOP

Unit :mm/Inch



NOTE
( ) is reference.
[ ] is Assambly Out Quality.

SAMSUNG ELECTRONICS