ML117, ML117R

2, 4, or 6-Channel Read/Write Circuits

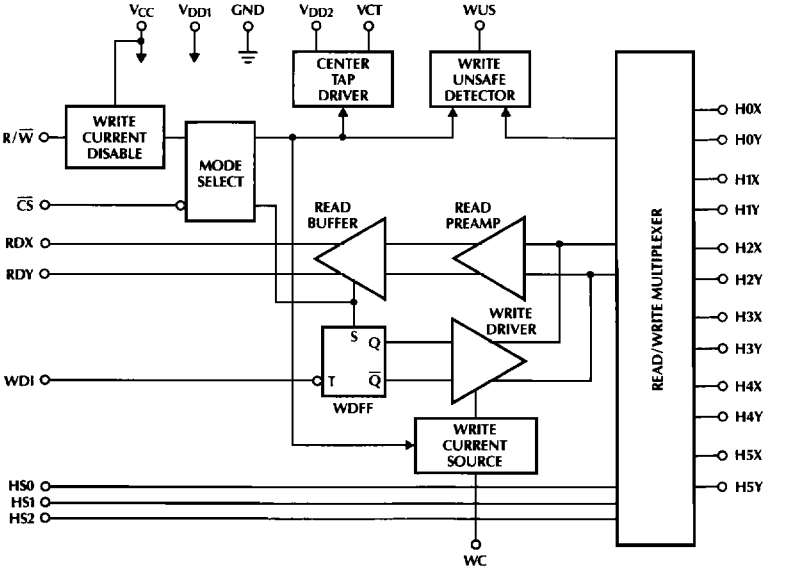
GENERAL DESCRIPTION

The ML117 devices are bipolar monolithic integrated circuits designed for use with center-tapped ferrite recording heads. They provide a low noise read path, write current control, and data protection circuitry for as many as six channels. The ML117 requires +5V and +12V power supplies and is available in 2, 4, or 6-channel versions with a variety of packages. The ML117 contains exclusive circuitry that inhibits write current during device power-up, thereby eliminating power-up "glitches" common to similar read/write circuits. The ML117R differs from the ML117 by having internal damping resistors.

FEATURES

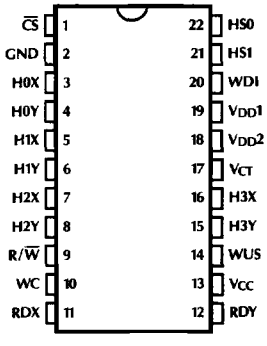
- Exclusive write current disable during power-up
- Replacement for SSI 32R117/117R
- +5V, +12V power supplies
- Single or multi-platter Winchester drives
- Designed for center-tapped ferrite heads
- Programmable write current source
- Available in 2, 4, or 6 channels
- Easily multiplexed for larger systems
- Includes write unsafe detection
- TTL compatible control signals

BLOCK DIAGRAM



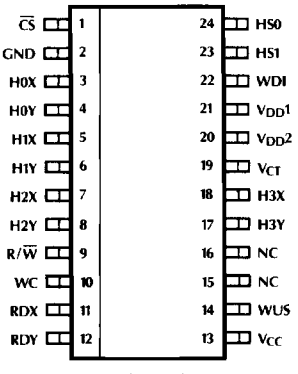
PIN CONNECTIONS

ML117-4 OR ML117R-4
4 Channels
22-PIN DIP



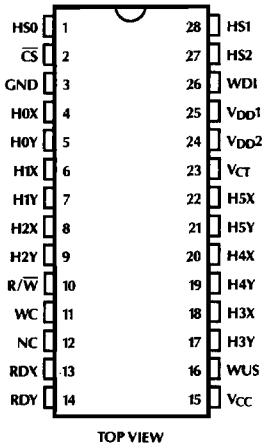
TOP VIEW

ML117-4 OR ML117R-4
4 Channels
24-PIN SOIC



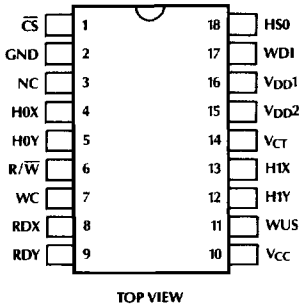
TOP VIEW

ML117-6 OR ML117R-6
6 Channels
28-PIN DIP



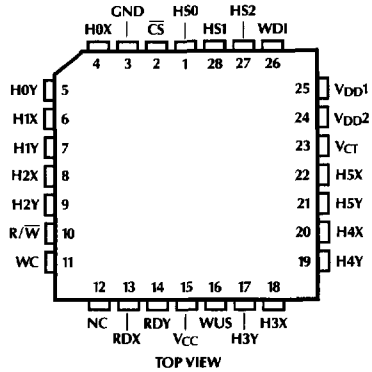
TOP VIEW

ML117-2 OR ML117R-2
2 Channels
18-PIN SOIC AND DIP



TOP VIEW

ML117-6 OR ML117R-6
6 Channels
28-PIN PCC



TOP VIEW

PIN DESCRIPTION

NAME	FUNCTION
HS0–HS2	Head Select (six heads)
$\overline{CS}$	Chip Select (low level enables chip)
R/$\overline{W}$	Read/Write (high level selects Read mode)
WUS	Write Unsafe, open collecter output (high level indicates alarm)
WDI	Write Data In (negative transition toggles head current direction)
H0X–H5X	X head connections
H0Y–H5Y	Y head connections

NAME	FUNCTION
RDX, RDY	X, Y Read Data (differential read signal out)
WC	Write Current (used to set the write current magnitude)
V_{CT}	Voltage Center Tap (center tap voltage source)
V_{CC}	+5 volts
$V_{DD}1$	+12 volts
$V_{DD}2$	Positive supply for center tap
GND	Ground

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Power Supply Voltage Range
- $V_{DD}1$ ..... −0.3 to 14 V_{DC}
- $V_{DD}2$ ..... −0.3 to 14 V_{DC}
- V_{CC} ..... −0.3 to 6 V_{DC}

Input Voltage Range
- Digital Inputs ($\overline{CS}$, R/$\overline{W}$, HS, WDI) ..... −0.3 to V_{CC} +0.3 V_{DC}
- Head Ports (H0X–H5X, H0Y–H5Y) .... −0.3 to $V_{DD}1$ +0.3 V_{DC}
- Write Unsafe (WUS) ..... −0.3 to 14 V_{DC}

Write Current (I_W) ..... 60 mA

Output Current
- Read Data (RDX, RDY) ..... −10 mA
- Center Tap Current (I_{CT}) ..... −60 mA
- Write Unsafe (WUS) ..... 12 mA

Storage Temperature ..... −65°C to 150°C

Junction Temperature (T_J) ..... 125°C

Lead Temperature (Soldering 10 sec.) ..... 300°C

OPERATING CONDITIONS

Supply Voltage
- $V_{DD}1$ ..... 12 V ± 10%
- V_{CC} ..... 5 V ± 10%
- $V_{DD}2$ ..... 6.5 to $V_{DD}1$

Head Inductance (L_H) ..... 5 to 15 µH

Damping Resistor (R_D, ML117 only) ..... 500 to 2000 Ω

RCT Resistor (1/2 Watt) ..... 130 Ω ± 5%

Write Current (I_W) ..... 25 to 50 mA

ELECTRICAL CHARACTERISTICS

Unless otherwise specified $V_{DD}1 = 12\,V \pm 10\%$, $V_{CC} = 5\,V \pm 10\%$, $0°C \leq T_A \leq 70°C$ (Notes 2 and 3).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC OPERATING CHARACTERISTICS						
POWER SUPPLY						
I_{CC}	V_{CC} Supply Current	Read or Idle Mode			25	mA
		Write Mode			30	mA
I_{DD}	V_{DD} Supply Current	Read Mode			50	mA
		Write Mode			30 + I_W	mA
		Idle Mode			25	mA
P_D	Power Dissipation	Read Mode			600	mW
		Write Mode $I_W = 50\,mA$, $R_{CT} = 130\,\Omega$			700	mW
		Write Mode $I_W = 50\,mA$, $R_{CT} = 0\,\Omega$			1050	mW
		Idle Mode			400	mW
DIGITAL INPUTS ($\overline{CS}$, R/$\overline{W}$, HS, WDI)						
V_{IH}	High Voltage		2		V_{CC}+0.3	V_{DC}
V_{IL}	Low Voltage		−0.3		0.8	V_{DC}
I_{IH}	High Current	$V_{IH} = 2.0\,V$			100	µA
I_{IL}	Low Current	$V_{IL} = 0.8\,V$	−0.4			mA
WUS OUTPUT						
V_{OL}	Output Low Voltage	$I_{OL} = 8\,mA$ (Safe)			0.5	V_{DC}
I_{OH}	Output High Current	$V_{OH} = 5\,V$ (Unsafe)			100	µA
CENTER TAP VOLTAGES						
V_{CT}	Read Mode	Read Mode		4		V_{DC}
V_{CT}	Write Mode	Write Mode		6		V_{DC}

5

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $V_{DD}1 = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $I_W = 45mA$, $L_H = 10\mu H$, $R_D = 750\Omega$, $f_{DATA} = 5MHz$, C_L (RDX, RDY) $\leq 20pF$, $0°C \leq T_A \leq 70°C$ (Notes 2 and 3) (V_{IN} is referenced to V_{CT} for Read Mode Characteristics).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WRITE MODE CHARACTERISTICS						
I_{WR}	Write Current Range	$I_W = K/R_{WC}$	10		50	mA
K	Write Current Constant		133		147	V
V_{HD}	Differential Head Voltage Swing		8			V_{PK}
I_{HU}	Unselected Head Transient Current				2	mA_{PK}
C_{OD}	Differential Output Capacitance				15	pF
R_{OD}	Differential Output Resistance	ML117	10k			Ω
		ML117R	562		938	Ω
f_{WDI}	WDI Transition Frequency	WUS = Low	250			kHz
A_I	I_{WS} to Head Current Gain			20		A/A
I_L	Unselected Head Leakage	Sum of X & Y Side Leakage Current			85	μA
READ MODE CHARACTERISTICS						
A_V	Differential Voltage Gain	$V_{IN} = 1mV_{P-P}$ @ 300kHz, R_L (RDX, RDY) = 1kΩ	80		120	V/V
DR	Dynamic Range	DC Input Voltage (V_i) Where Gain Falls 10%, $V_{IN} = V_i + 0.5mV_{P-P}$ @ 300kHz	−3		+3	mV
BW	Bandwidth (−3dB)	$\|Z_S\| < 5\Omega$, $V_{IN} = 1mV_{RMS}$	30			MHz
e_{IN}	Input Noise Voltage	BW = 15MHz, $L_H = 0$, $R_H = 0$			2.1	$nV/\sqrt{Hz}$
C_{IN}	Differential Input Capacitance				20	pF
R_{IN}	Differential Input Resistance	ML117	2k			Ω
		ML117R	390		810	Ω
I_{IN}	Input Bias Current				45	μA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = V_{CT} + 100mV_{P-P}$ @ f = 5MHz	50			dB
PSRR	Power Supply Rejection Ratio	$100mV_{P-P}$ @ 5MHz on $V_{DD}1$, $V_{DD}2$, or V_{CC}	45			dB
CS	Channel Separation	Unselected Channels: $V_{IN} = 100mV_{P-P}$ @ 5MHz and Selected Channel: $V_{IN} = 0mV_{P-P}$	45			dB
V_{OS}	Output Offset Voltage		−480		+480	mV
V_{OCM}	Common-Mode Output Voltage	Read Mode	5		7	V
		Write or Idle Mode		4.3		V
R_{OUT}	Single-Ended Output Resistance	f = 5MHz			30	Ω
I_L	Leakage Current, RDX, RDY	RDX, RDY = 6V Write or Idle Mode	−100		+100	μA
I_O	Output Current	AC Coupled Load, RDX to RDY	2			mA

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified $V_{DD1} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $I_W = 45mA$, $L_H = 10\mu H$, $R_D = 750\Omega$, $f_{DATA} = 5MHz$, $0°C \leq T_A \leq 70°C$ (Notes 2 and 3).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS						
t_{RW}	R/$\overline{W}$ to Write Switching Delay	To 90% of Write Current Output			1	µS
t_{WR}	R/$\overline{W}$ to Read Switching Delay	To 90% of 100mV, 10MHz Read Signal Envelope or to 90% Decay of Write Current			1	µS
t_{IW} or t_{IR}	$\overline{CS}$ to Select Switching Delay	To 90% of Write Current or to 90% of 100mV, 10MHz Read Signal Envelope			1	µS
t_{WI} or t_{RI}	$\overline{CS}$ to Select Switching Delay	To 90% Decay of 100mV, 10MHz Read Signal Envelope or to 90% Decay of Write Current			1	µS
t_{HS}	Head Select Switching Delay	To 90% of 100mV, 10MHz Read Signal Envelope			1	µS
tD1	Safe to Unsafe Write Unsafe Delay	$I_W = 50mA$	1.6		8	µS
tD2	Unsafe to Safe Write Unsafe Delay	$I_W = 50mA$			1	µS
tD3	Head Current Prop. Delay	$L_H = 0$, $R_H = 0$ From 50% points			25	nS
tD3	Head Current Asymmetry	WDI has 50% Duty Cycle and 1nS Rise/Fall Time			2	nS
	Time Head Current Rise/Fall	10% and 90% Points			20	nS

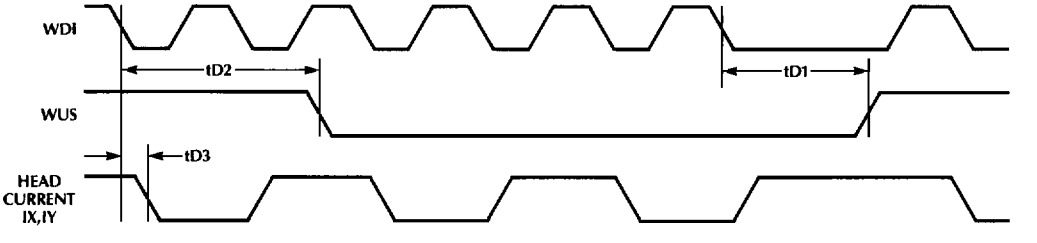
Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 3: Maximum junction temperature (T_J) should not exceed 125°C.

5

TIMING DIAGRAMS



Write Mode Timing Diagram

FUNCTIONAL DESCRIPTION

CIRCUIT OPERATION

The ML117, ML117R functions as a write driver or as a read amplifier for the selected head. Head selection and mode control are described in *Tables 1 & 2*. Both R/$\overline{W}$ and $\overline{CS}$ have internal pull-up resistors for the prevention of an accidential write condition.

READ MODE

In the Read Mode the ML117, ML117R is configured as a low noise differential amplifier, the write current source and the write unsafe detector are deactivated, and the write data flip-flop is set. The RDX and RDY outputs are driven by emitter followers and are in phase with the "X" and "Y" head ports.

The internal write current source is deactivated for both the Read and the Chip Deselect modes which eliminates the need for external gating of the write current source.

WRITE MODE

The Write mode configures the ML117, ML117R as a current switch and activates the Write Unsafe Detector. The head current is toggled between the X- and Y-side of the recording head on the falling edges of WDI, Write Data Input. A preceding read operation initializes the Write Data Flip-Flop, WDFF, to pass current through the X-side of the head. The magnitude of the write current, given by:

$I_W = K/R_{WC}$, where K = Write Current Constant

is set by the external resistor, R_{WC}, connected from pin WC to GND.

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- Head open
- Head center tap open
- WDI frequency too low
- Device in Read mode
- Device not selected
- No write current

Two negative transitions on WDI are required to clear WUS after the fault condition is removed.

Table 1.

Head Select

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	X	NONE

0 = Logic Level Low
1 = Logic Level High
X = Don't Care

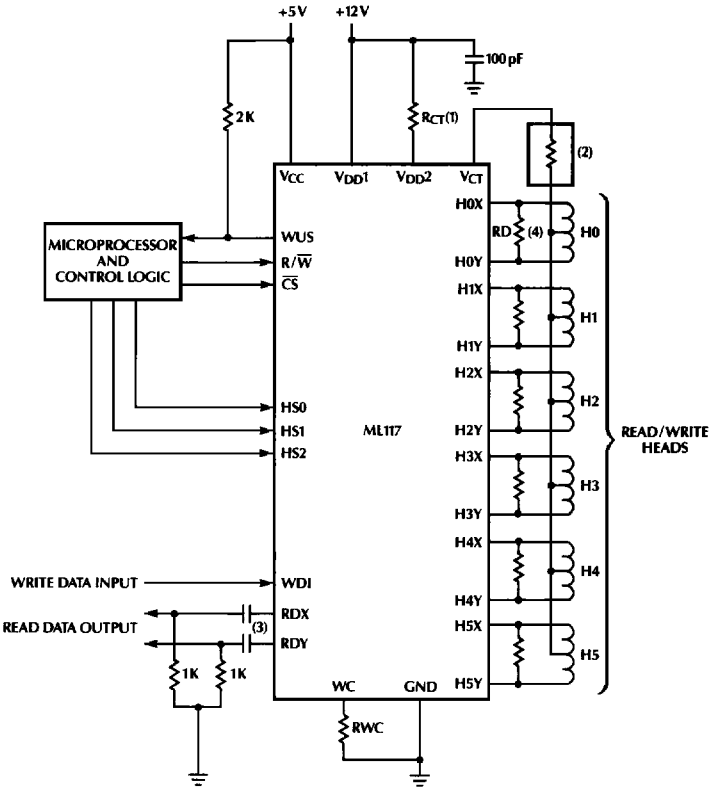
Table 2.

Mode Select

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

0 = Logic Level Low
1 = Logic Level High
X = Don't Care

TYPICAL APPLICATION



NOTES:

1. RCT is optional and is used to limit internal power dissipation (Otherwise connect $V_{DD}1$ to $V_{DD}2$).
   RCT (1/2 Watt) = 130 (55/I_W) ohms
   where I_W = Write Current, in mA
2. Ferrite bead optional: used to suppress write current overshoot and ringing. Recommend Ferroxcube 3659065/4A6.
3. RDX and RDY load capacitance 20 pF maximum. RDX and RDY output current must be limited to 100 µA.
4. Damping resistors not required on ML117R.

THERMAL CHARACTERISTICS

28-Lead	
PDIP	80°C/W
PCC	60°C/W
24-Lead	
SOIC	60°C/W
22-Lead	
PDIP	100°C/W
18-Lead	
PDIP	115°C/W
SOIC	85°C/W

5

ORDERING INFORMATION

PART NUMBER	PACKAGE	NUMBER OF CHANNELS
ML117-2CP	18-Lead Molded DIP (P18)	2
ML117R-2CP	18-Lead Molded DIP (P18)	2
ML117-2CS	18-Lead Molded SOIC (S18)	2
ML117R-2CS	18-Lead Molded SOIC (S18)	2
ML117-4CP	22-Lead Molded DIP (P22)	4
ML117R-4CP	22-Lead Molded DIP (P22)	4
ML117-4CS	24-Lead Molded SOIC (S24)	4
ML117R-4CS	24-Lead Molded SOIC (S24)	4
ML117-6CP	28-Lead Molded DIP (P28)	6
ML117R-6CP	28-Lead Molded DIP (P28)	6
ML117-6CQ	28-Lead PCC (Q28)	6
ML117R-6CQ	28-Lead PCC (Q28)	6