

# **MP02TT200**

## **Dual Thyristor Water Cooled Module**

Advance Information DS5434-1.1 April 2001

#### FEATURES

- Dual Device Module
- Electrically Isolated Package
- Pressure Contact Construction
- International Standard Footprint
- Alumina (Non Toxic) Isolation Medium
- Integral Water Cooled Heatsink

#### APPLICATIONS

- Motor Control
- Controlled Rectifier Bridges
- Heater Control
- AC Phase Control

#### **VOLTAGE RATINGS**

Type Number	Repetitive Peak Voltages V <sub>DRM</sub> V <sub>RRM</sub> V	Conditions
MP02TT200-16 MP02TT200-15 MP02TT200-14 MP02TT200-13 MP02TT200-12	1600 1500 1400 1300 1200	$\begin{split} T_{vj} &= 0^{\circ} \text{ to } 125^{\circ}\text{C}, \\ I_{\text{DRM}} &= I_{\text{RRM}} = 30\text{mA} \\ V_{\text{DSM}} &= V_{\text{RSM}} = \\ V_{\text{DRM}} &= V_{\text{RRM}} + 100\text{V} \\ \text{respectively} \end{split}$

Lower voltage grades available

#### **ORDERING INFORMATION**

Order As:

MP02TT200-XX-W12	1/4 - 18 NPT connection
MP02TT200-XX-W13	1/4 BSP connection

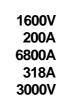
XX shown in the part number about represents  $V_{_{\rm DRM}}/100$  selection required, e.g. MP02TT200-14-W12

Note: When ordering, please use the whole part number.

Auxiliary gate and cathode leads can be ordered separately.

### KEY PARAMETERS

 $\begin{array}{c} V_{\text{DRM}} \\ I_{\text{T(AV)}} \\ I_{\text{TSM(per arm)}} \\ I_{\text{T(RMS)}} \\ V_{\text{isol}} \end{array}$ 



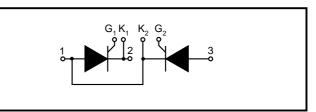
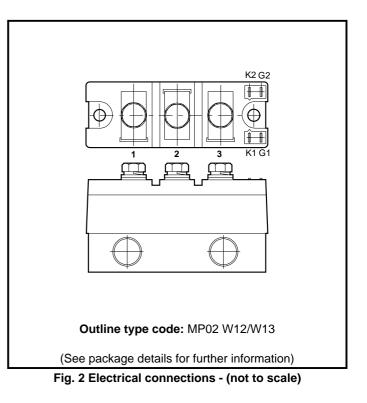


Fig. 1 Circuit diagram





#### **ABSOLUTE MAXIMUM RATINGS - PER ARM**

Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture of the package. Appropriate safety precautions should always be followed. Exposure to Absolute Maximum Ratings may affect device reliability.

Symbol	Parameter	Test Conditions		Max.	Units
I <sub>T(AV)</sub>	Mean on-state current	Half wave resistive load,	$T_{water (in)} = 25^{\circ}C$	230	А
		4.5 Ltr/min	$T_{water (in)} = 40^{\circ}C$	200	А
			T <sub>water (in)</sub> = 50°C	180	А
I <sub>T(RMS</sub>	RMS value	T <sub>water (in)</sub> = 25°C @ 4.5 Ltr/min		360	А
		T <sub>water (in)</sub> = 40°C @ 4.5 Ltr/min		318	А
I <sub>TSM</sub>	Surge (non-repetitive) on-current	10ms half sine, $T_j = 125^{\circ}C$		6.8	kA
l²t	I <sup>2</sup> t for fusing	V <sub>R</sub> = 0		0.231 x 10 <sup>6</sup>	A²s
I <sub>TSM</sub>	Surge (non-repetitive) on-current	10ms half sine, T <sub>j</sub> = 125°C		5.5	kA
l²t	I <sup>2</sup> t for fusing	$V_{R} = 50\% V_{DRM}$		0.15 x 10 <sup>6</sup>	A²s
V <sub>isol</sub>	Isolation voltage	Commoned terminals to base plate. AC RMS, 1 min, 50Hz		3000	V

### THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions	Min.	Max.	Units
R <sub>th(j-w)</sub>	Thermal resistance - junction to water	dc, 4.5 Ltr/min	-	0.3	°C/kW
	(per thyristor)	Half wave, 4.5 Ltr/min	-	0.32	°C/kW
		3 Phase, 4.5 Ltr/min	-	0.33	°C/kW
T <sub>vj</sub>	Virtual junction temperature	Reverse (blocking)	-	125	°C
T <sub>stg</sub>	Storage temperature range	-	-40	125	°C
-	Screw torque	Mounting - M6	5 (44)	-	Nm (lb.ins)
		Electrical connections - M6	-	5 (44)	Nm (lb.ins)
-	Weight (nominal)	-	-	1200	g



## **DYNAMIC CHARACTERISTICS**

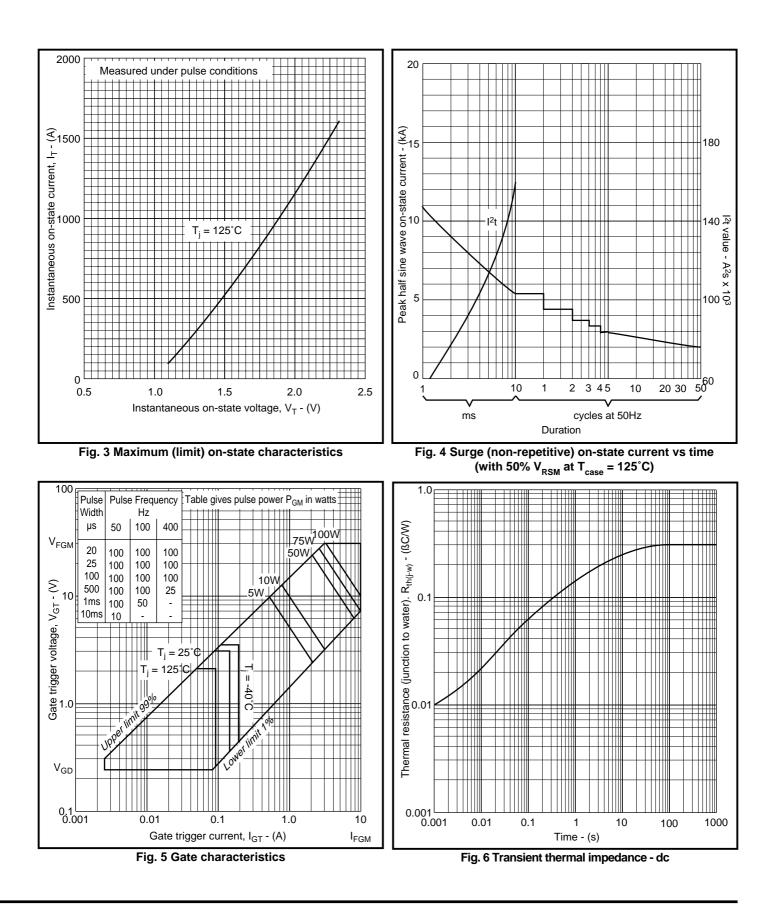
Symbol	Parameter	Test Conditions	Min.	Max.	Units
I <sub>RRM</sub> /I <sub>DRM</sub>	Peak reverse and off-state current	At $V_{RRM}/V_{DRM}$ , $T_j = 125^{\circ}C$	-	30	mA
dV/dt	Linear rate of rise of off-state voltage	To 67% V <sub>DRM</sub> , T <sub>j</sub> = 125°C	-	1000	V/µs
dl/dt	Rate of rise of on-state current	From 67% V $_{\rm DRM}$ to 200A, gate source 10V, 5 $\Omega$	-	500	A/μs
		t <sub>r</sub> = 0.5μs, T <sub>j</sub> = 125°C			
V <sub>T(TO)</sub>	Threshold voltage	At $T_{vj} = 125^{\circ}C$	-	0.98	V
r <sub>T</sub>	On-state slope resistance	At $T_{v_j} = 125^{\circ}C$	-	0.75	mΩ

**Note 1:** The data given in this datasheet with regard to forward voltage drop is for calculation of the power dissipation in the semiconductor elements only. Forward voltage drops measured at the power terminals of the module will be in excess of these figures due to the impedance of the busbar from the terminal to the semiconductor.

#### GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V <sub>GT</sub>	Gate trigger voltage	$V_{\text{DRM}} = 5V, T_{\text{case}} = 25^{\circ}\text{C}$	3	V
Ι <sub>gτ</sub>	Gate trigger current	$V_{\text{DRM}} = 5V, T_{\text{case}} = 25^{\circ}\text{C}$	150	mA
V <sub>GD</sub>	Gate non-trigger voltage	At $V_{\text{DRM}} T_{\text{case}} = 125^{\circ}\text{C}$	0.25	V
V <sub>FGM</sub>	Peak forward gate voltage	Anode positive with respect to cathode	30	V
V <sub>FGN</sub>	Peak forward gate voltage	Anode negative with respect to cathode	0.25	V
V <sub>RGM</sub>	Peak reverse gate voltage	-	5	V
I <sub>FGM</sub>	Peak forward gate current	Anode positive with respect to cathode	10	А
Р <sub>бм</sub>	Peak gate power	See table fig. 5	100	W
P <sub>G(AV)</sub>	Mean gate power	-	5	W







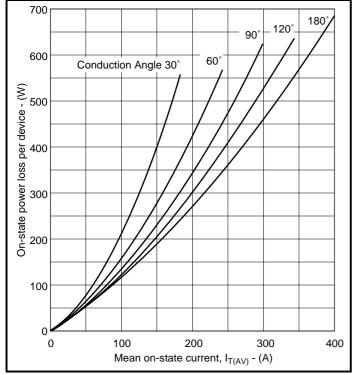


Fig. 7 On-state power loss per arm vs on-state current at specified conduction angles, sine wave 50/60Hz

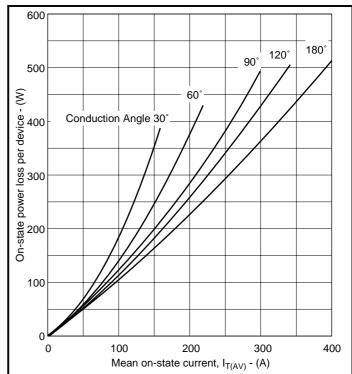
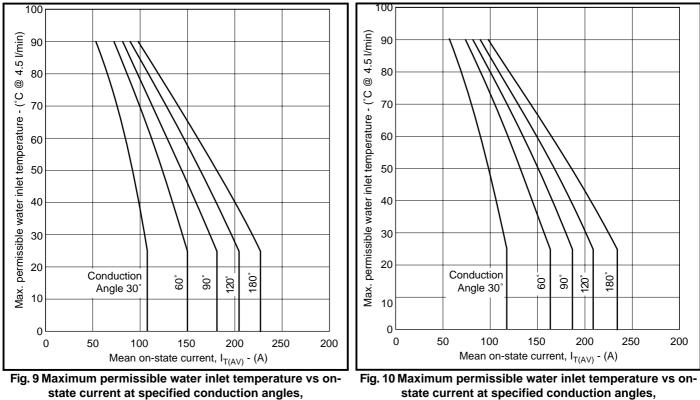


Fig. 8 On-state power loss per arm vs on-state current at specified conduction angles, square wave 50/60Hz



sine wave 50/60Hz

square wave 50/60Hz



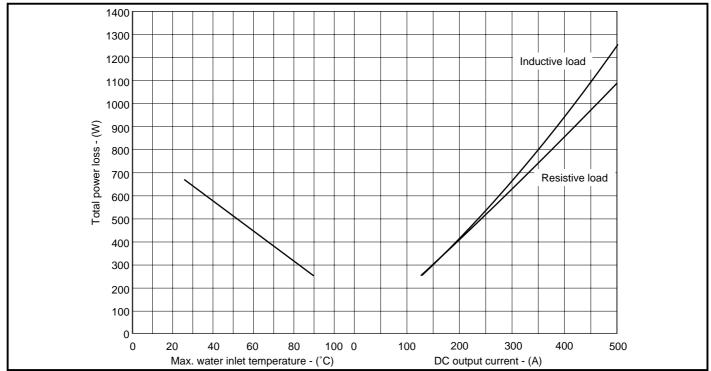


Fig. 11 50/60Hz single phase bridge DC output current vs power loss and maximum permissible water inlet temperature for specified values of heatsink thermal resistance

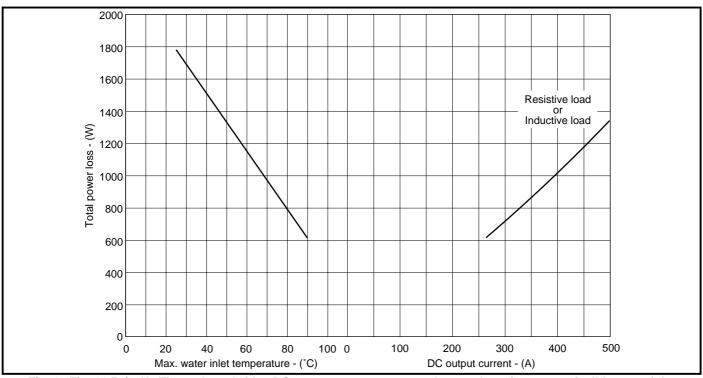
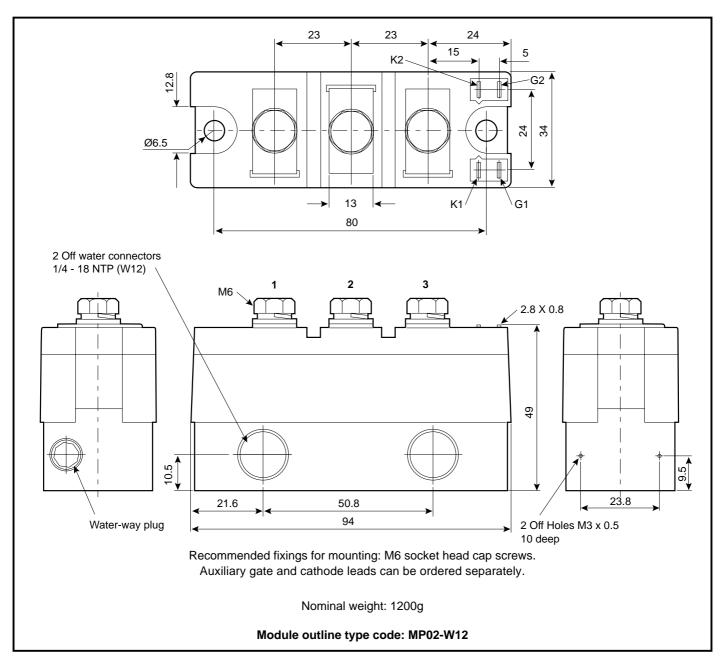


Fig. 12 Fig. 11 50/60Hz Three phase bridge DC output current vs power loss and maximum permissible water inlet temperature for specified values of heatsink thermal resistance



#### **PACKAGE DETAILS**

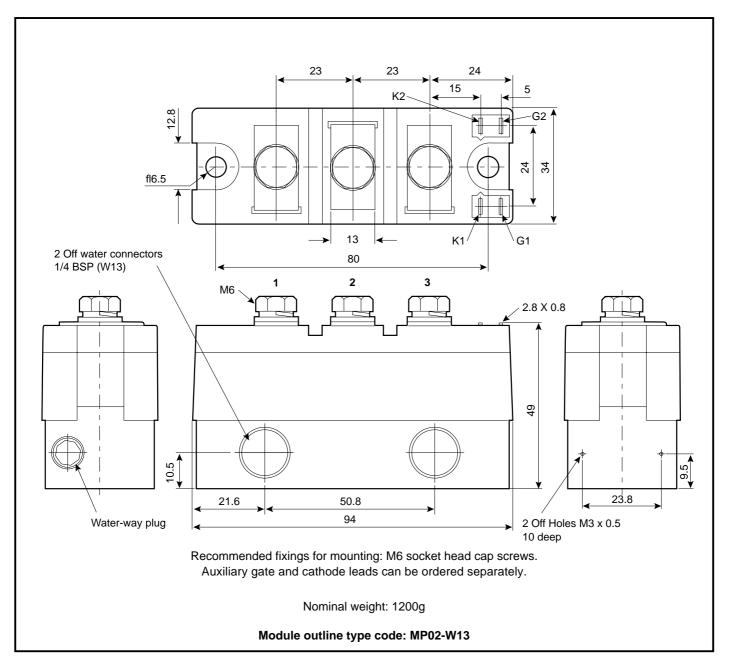
For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.





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#### POWER ASSEMBLY CAPABILITY

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink and clamping systems in line with advances in device voltages and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group offers high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the latest CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete Solution (PACs).

#### HEATSINKS

The Power Assembly group has its own proprietary range of extruded aluminium heatsinks which have been designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or Customer Services.



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Preliminary Information: The product is in design and development. The datasheet represents the product as it is understood but details may change.

Advance Information: The product design is complete and final characterisation for volume production is well in hand

No Annotation: The product parameters are fixed and the product is available to datasheet specification.

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