

RJK03P9DPA

MOS1 30 V, 20 A, 7.0 mΩ max.

MOS2 30 V, 50 A, 2.2 mΩ max.

Built in SBD Dual N-channel Power MOS FET

High Speed Power Switching

R07DS0907EJ0110

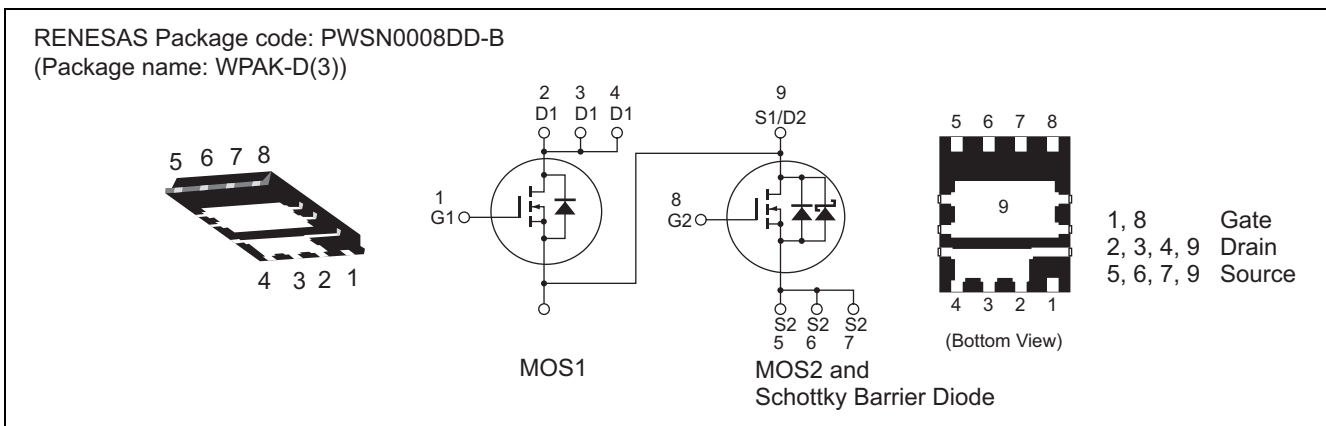
Rev.1.10

Nov 01, 2012

Features

- Low on-resistance
- Capable of 4.5 V gate drive
- High density mounting
- Pb-free
- Halogen-free

Outline



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings		Unit
		MOS1	MOS2	
Drain to source voltage	V _{DSS}	30	30	V
Gate to source voltage	V _{GSS}	±20	±20	V
Drain current	I _D	20	50	A
Drain peak current	I _{D(pulse)} ^{Note1}	80	200	A
Reverse drain current	I _{DR}	20	50	A
Avalanche current	I _{AP} ^{Note 2}	12	22	A
Avalanche energy	E _{AS} ^{Note 2}	14.4	48	mJ
Channel dissipation	P _{ch} ^{Note3}	15	35	W
Channel temperature	T _{ch}	150	150	°C
Storage temperature	T _{stg}	-55 to +150	-55 to +150	°C

- Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
 2. Value at T_{ch} = 25°C, R_g ≥ 50 Ω
 3. T_c=25°C

Electrical Characteristics

• MOS1

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 30 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.5	V	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	5.8	7.0	$\text{m}\Omega$	$I_D = 10 \text{ A}, V_{GS} = 10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	8.4	10.9	$\text{m}\Omega$	$I_D = 10 \text{ A}, V_{GS} = 4.5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	—	35	—	S	$I_D = 10 \text{ A}, V_{DS} = 5 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	1180	1660	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	252	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	90	—	pF	$f = 1 \text{ MHz}$
Gate Resistance	R_g	—	1.0	2.2	Ω	
Total gate charge	Q_g	—	7.7	—	nC	$V_{DD} = 10 \text{ V}$
Gate to source charge	Q_{gs}	—	3.3	—	nC	$V_{GS} = 4.5 \text{ V}$
Gate to drain charge	Q_{gd}	—	2.0	—	nC	$I_D = 20 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	3.8	—	ns	$V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$
Rise time	t_r	—	3.4	—	ns	$V_{DD} \approx 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	13.2	—	ns	$R_L = 1.0 \Omega$
Fall time	t_f	—	3.8	—	ns	$R_g = 4.7 \Omega$
Body-drain diode forward voltage	V_{DF}	—	0.83	1.08	V	$I_F = 20 \text{ A}, V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	9.0	—	ns	$I_F = 20 \text{ A}, V_{GS} = 0$ $di_F/dt = 500 \text{ A}/\mu\text{s}$

Notes: 4. Pulse test

• MOS2

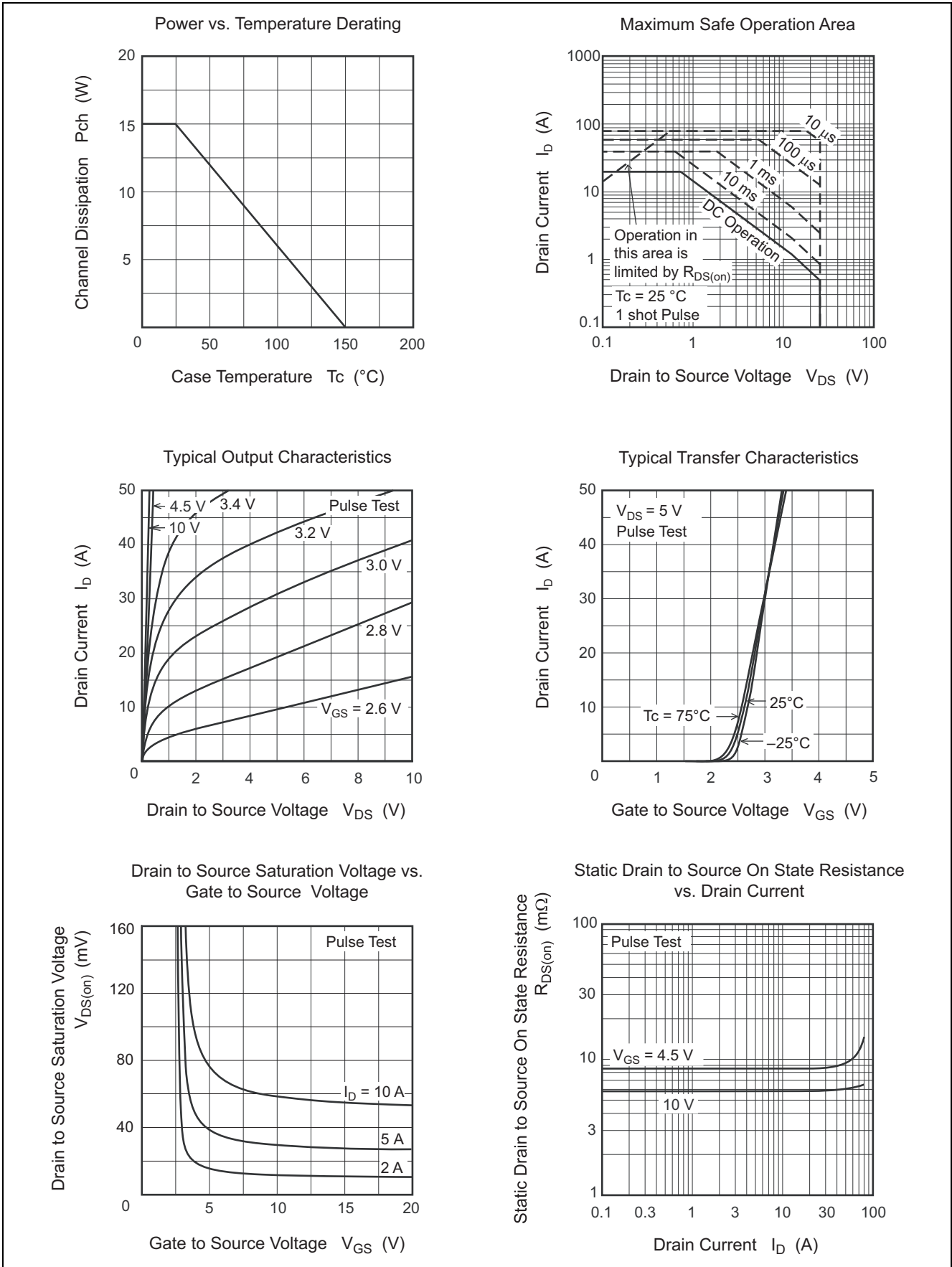
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.5	μA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	mA	$V_{DS} = 24 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.5	V	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	1.8	2.2	m Ω	$I_D = 25 \text{ A}, V_{GS} = 10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	2.1	2.7	m Ω	$I_D = 25 \text{ A}, V_{GS} = 4.5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	—	115	—	S	$I_D = 25 \text{ A}, V_{DS} = 5 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	4680	6560	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	780	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	450	—	pF	$f = 1 \text{ MHz}$
Gate Resistance	R_g	—	1.3	2.6	Ω	
Total gate charge	Q_g	—	36.7	—	nC	$V_{DD} = 10 \text{ V}$
Gate to source charge	Q_{gs}	—	12.1	—	nC	$V_{GS} = 4.5 \text{ V}$
Gate to drain charge	Q_{gd}	—	12.1	—	nC	$I_D = 50 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	8.0	—	ns	$V_{GS} = 10 \text{ V}, I_D = 25 \text{ A}$
Rise time	t_r	—	6.0	—	ns	$V_{DD} \approx 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	76.4	—	ns	$R_L = 0.4 \Omega$
Fall time	t_f	—	24.8	—	ns	$R_g = 4.7 \Omega$
Schottky Barrier diode forward voltage	V_F	—	0.40	—	V	$I_F = 2 \text{ A}, V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	10.0	—	ns	$I_F = 50 \text{ A}, V_{GS} = 0$ $di_F/dt = 500 \text{ A}/\mu\text{s}$

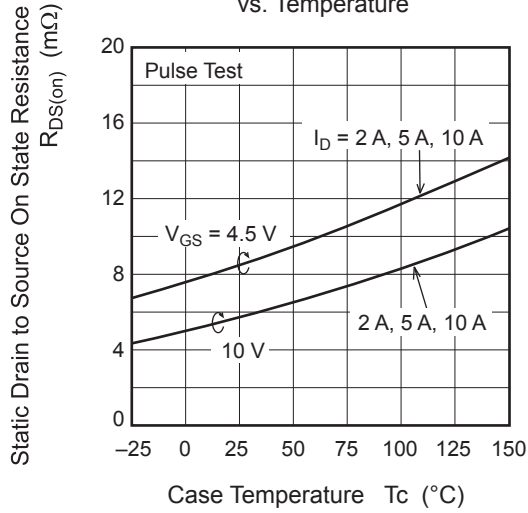
Notes: 4. Pulse

Main Characteristics

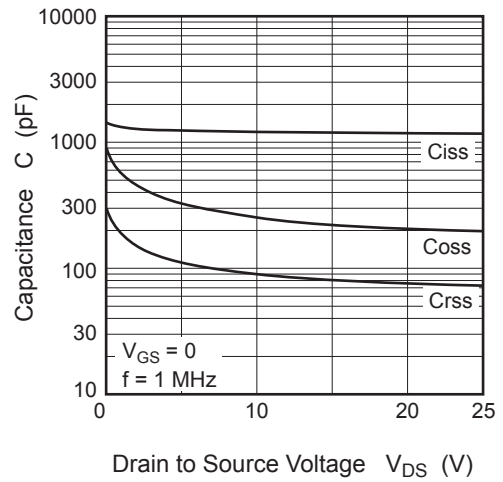
• MOS1



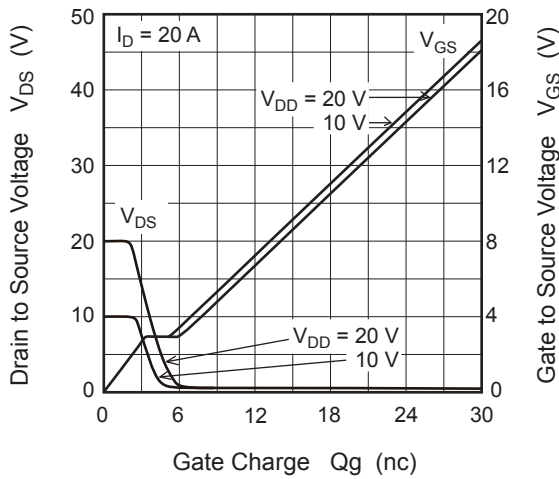
Static Drain to Source On State Resistance vs. Temperature



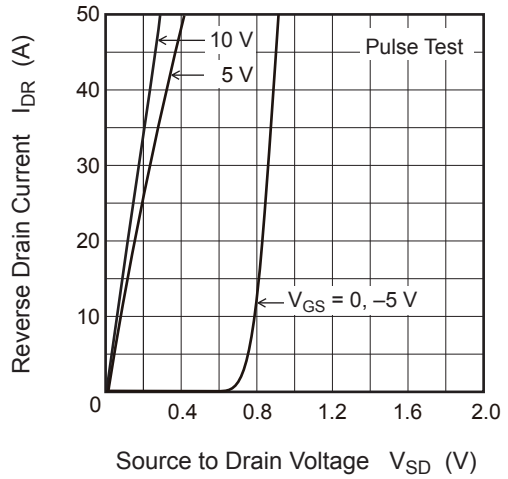
Typical Capacitance vs. Drain to Source Voltage



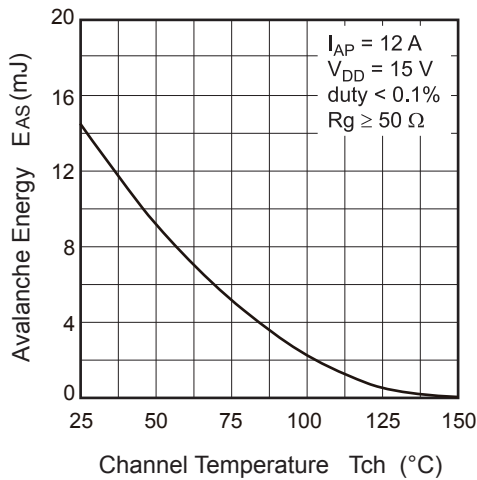
Dynamic Input Characteristics



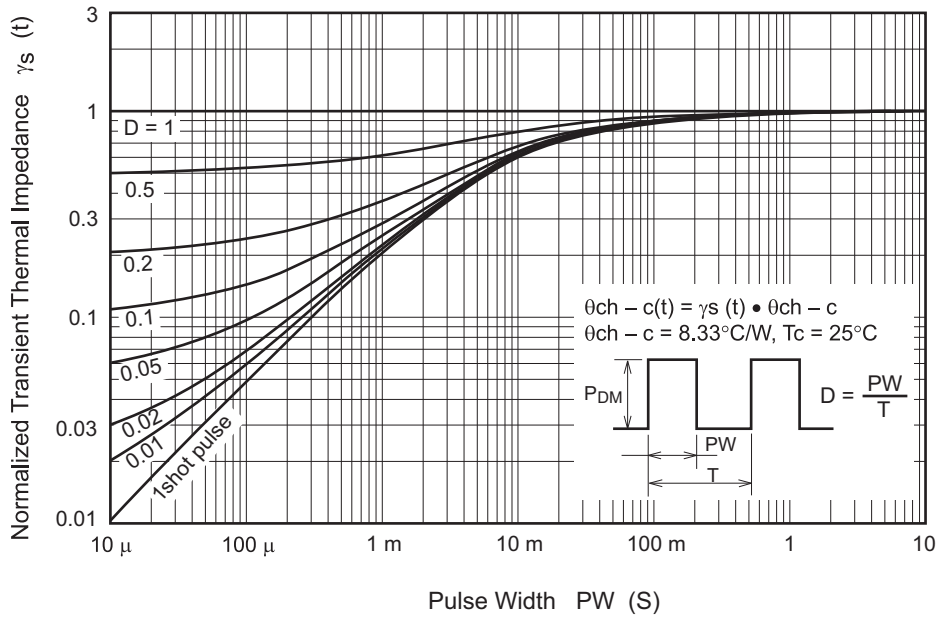
Reverse Drain Current vs. Source to Drain Voltage



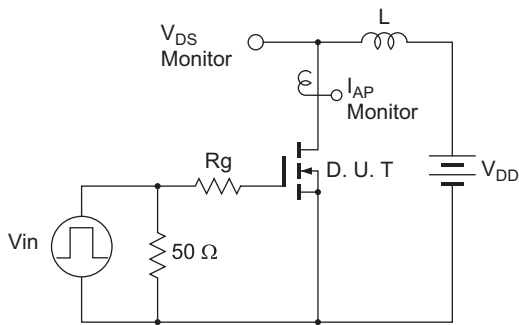
Maximum Avalanche Energy vs. Channel Temperature Derating



Normalized Transient Thermal Impedance vs. Pulse Width

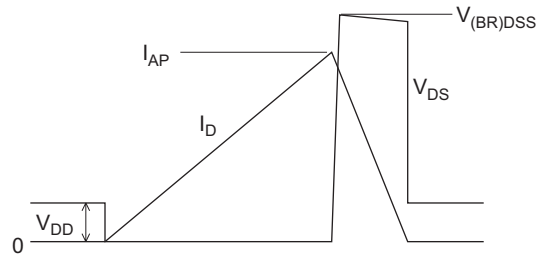


Avalanche Test Circuit

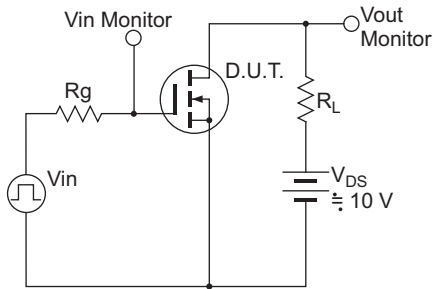


Avalanche Waveform

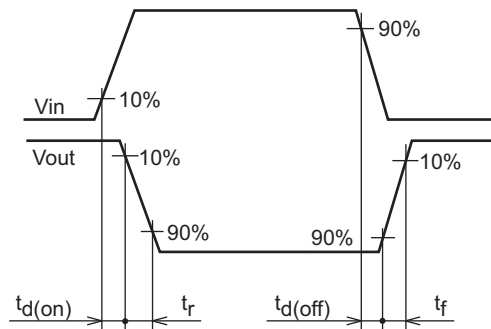
$$E_{AS} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



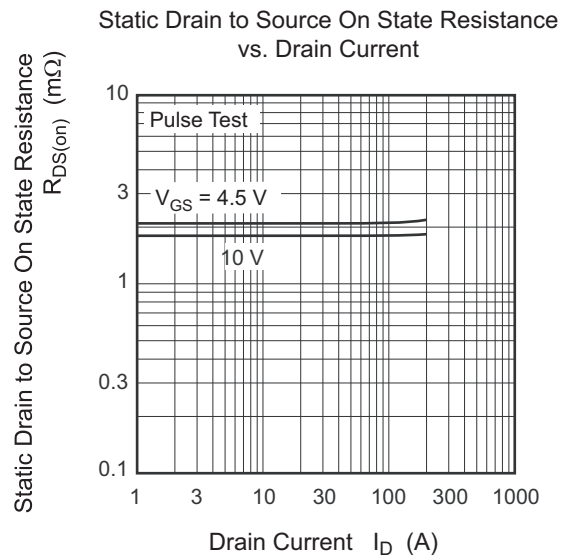
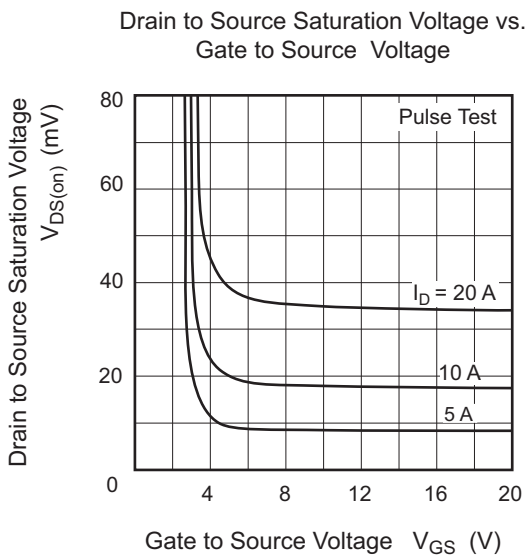
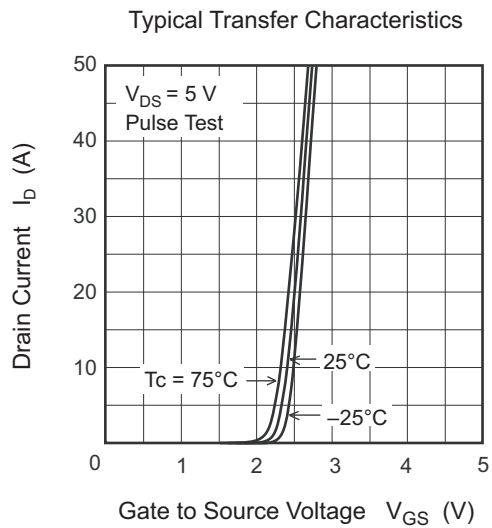
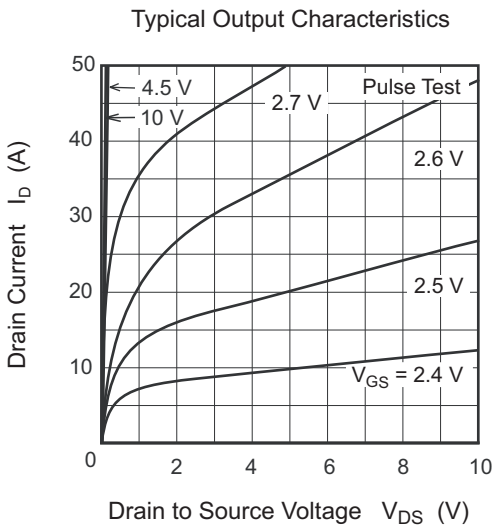
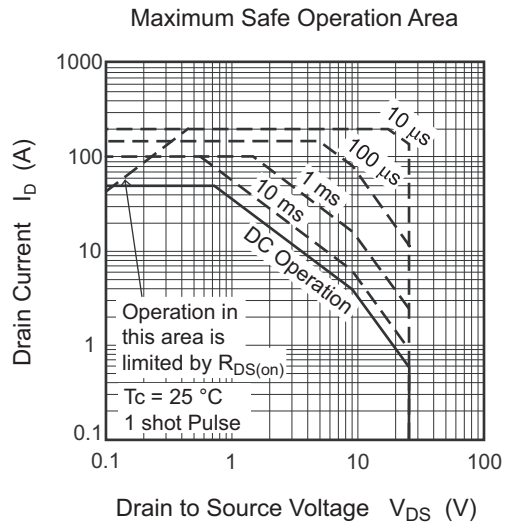
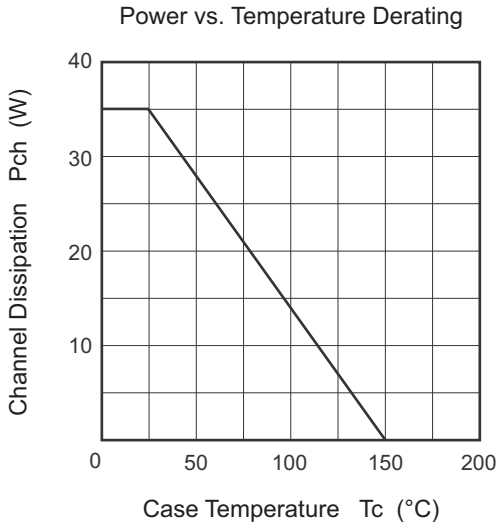
Switching Time Test Circuit



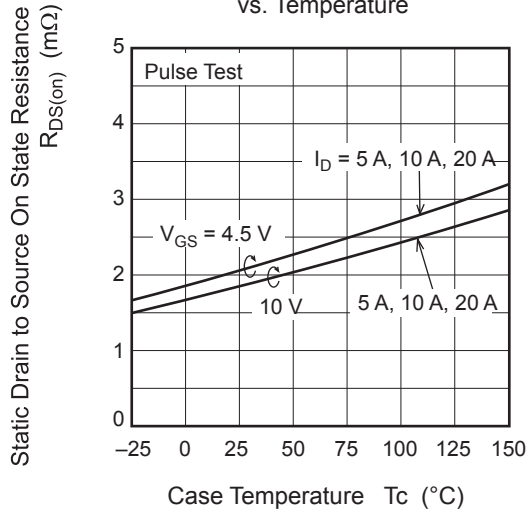
Switching Time Waveform



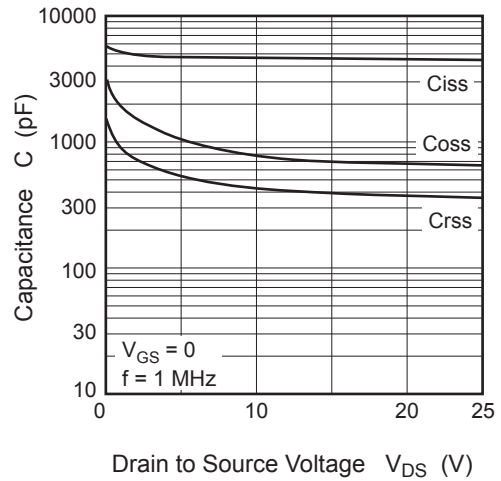
• MOS2 and Schottky Barrier Diode



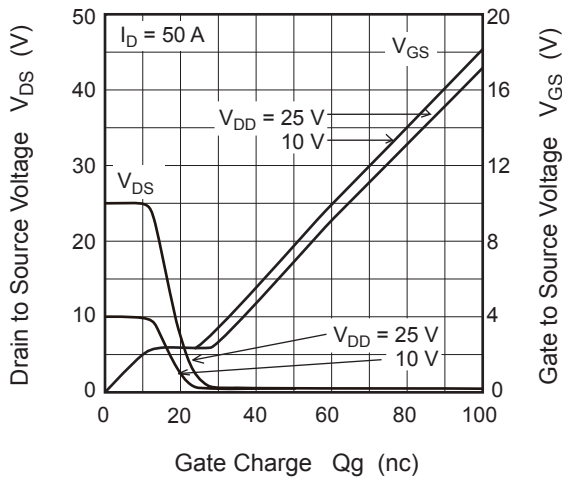
Static Drain to Source On State Resistance vs. Temperature



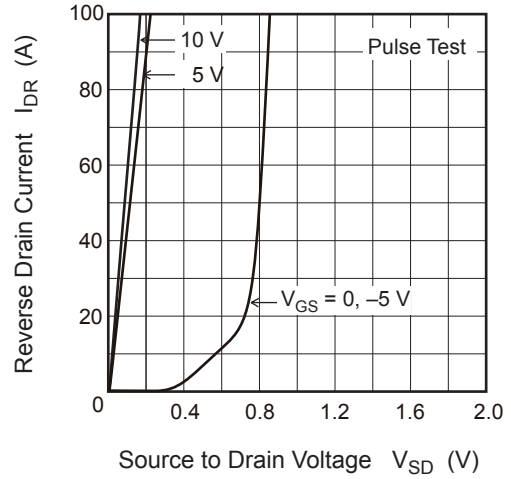
Typical Capacitance vs. Drain to Source Voltage



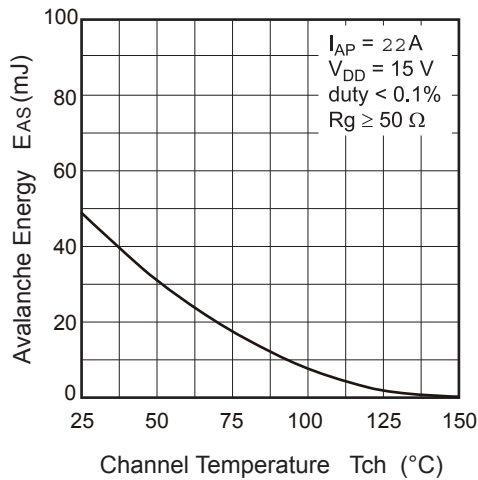
Dynamic Input Characteristics



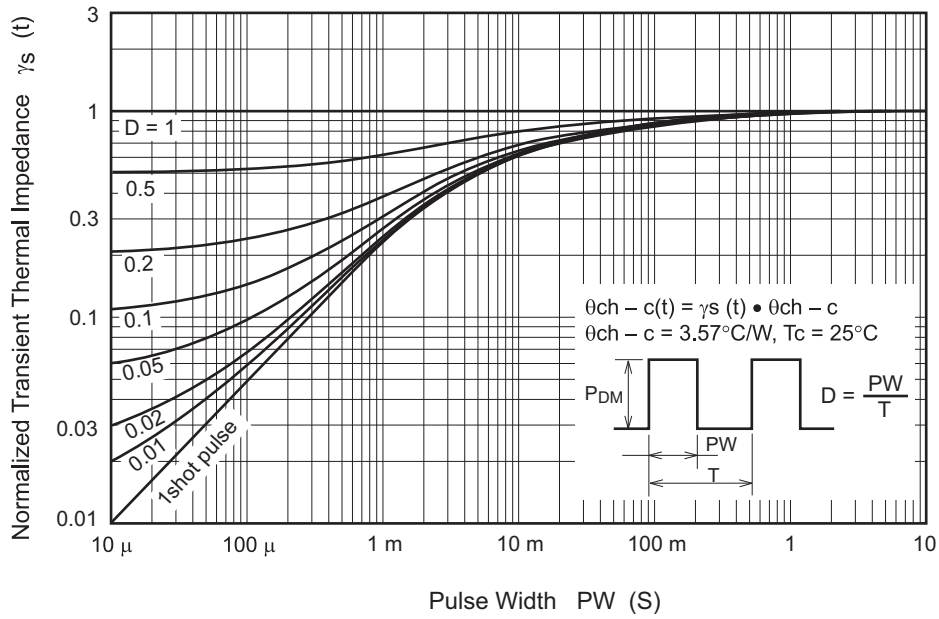
Reverse Drain Current vs. Source to Drain Voltage



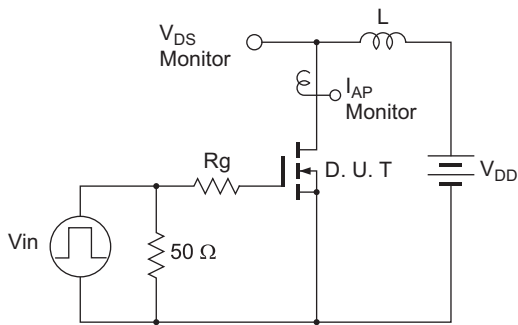
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Normalized Transient Thermal Impedance vs. Pulse Width

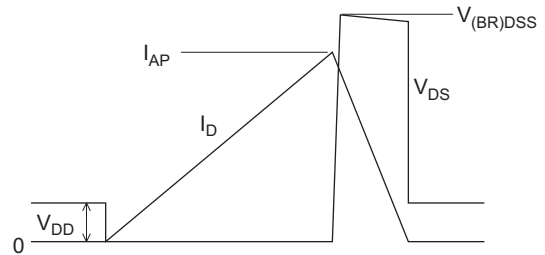


Avalanche Test Circuit

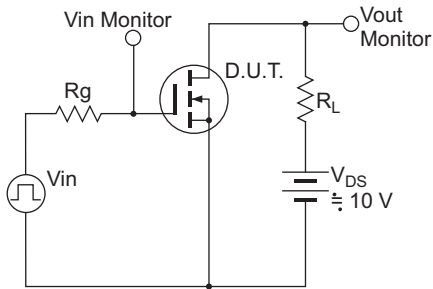


Avalanche Waveform

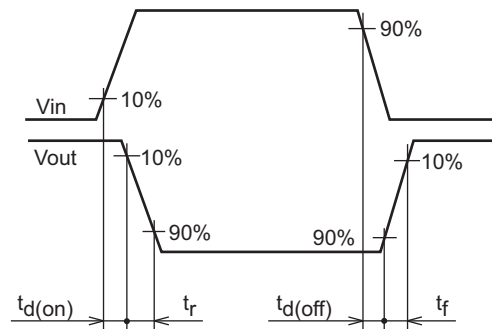
$$E_{AS} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



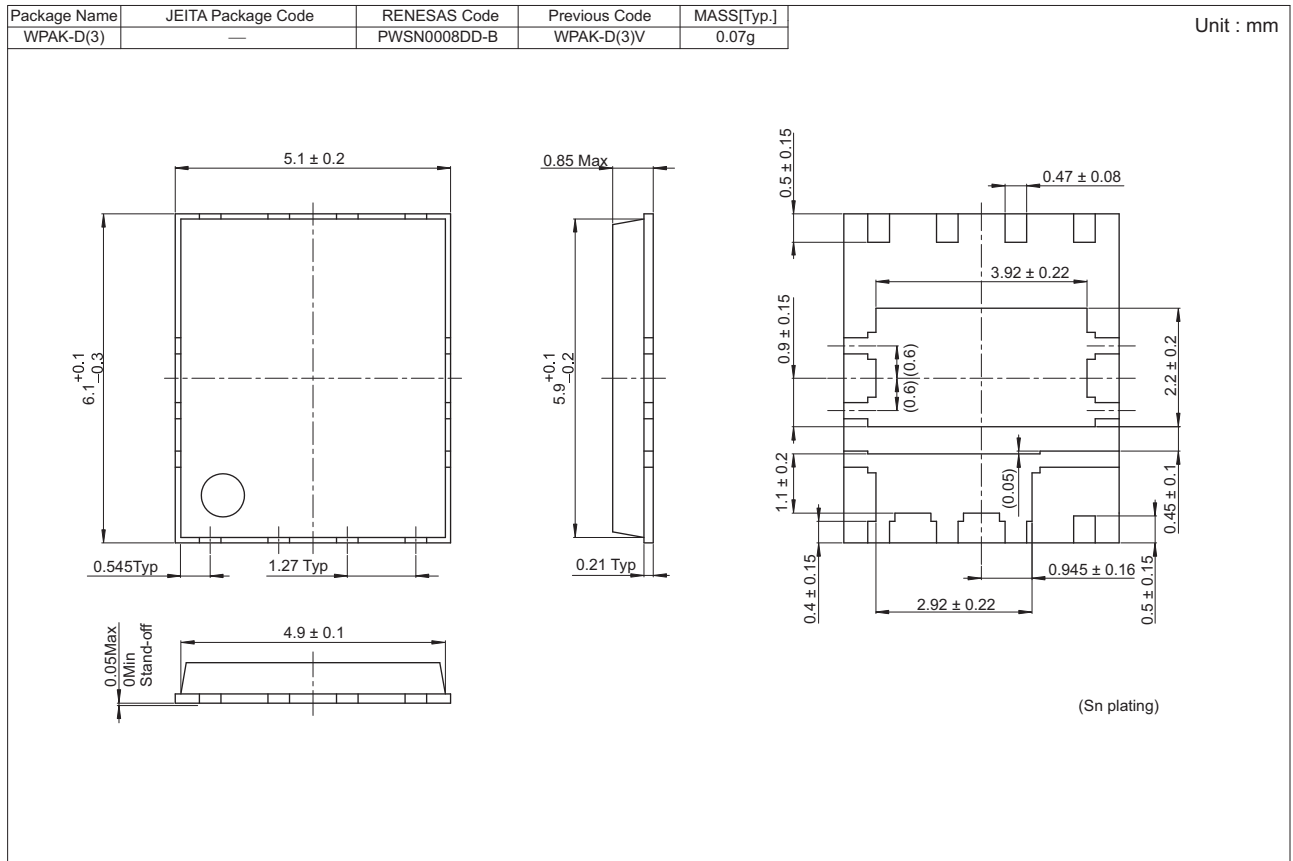
Switching Time Test Circuit



Switching Time Waveform



Package Dimensions



Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJK03P9DPA-00-J5A	3000 pcs	Taping

Note: The symbol of 2nd "-" is occasionally presented as "#".

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

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Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-3390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Laved. or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141