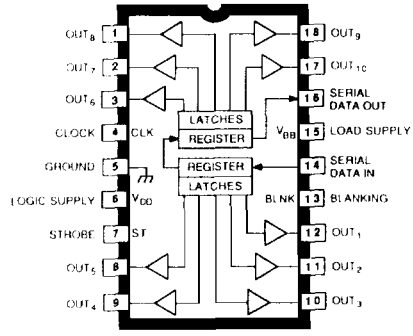
5810

BiMOS II 10-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS WITH ACTIVE DMOS PULL-DOWNS

UCN5810A



Dwg. PP-029

ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature

Output Voltage, V_{OUT} . . . . . **60 V**
(Suffix -1) . . . . . **80 V**
Logic Supply Voltage Range,
V_{DD} . . . . . **4.5 V to 15 V**
Driver Supply Voltage Range,
V_{BB} . . . . . **5.0 V to 60 V**
(Suffix-1) . . . . . **5.0 V to 80 V**
Input Voltage Range,
V_{IN} . . . . . **-0.3 V to V_{DD} + 0.3 V**
Continuous Output Current,
I_{OUT} . . . . . **-40 mA**
Package Power Dissipation,
P_D . . . . . **See Graph**
Operating Temperature Range,
T_A . . . . . **-20°C to +85°C**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

Caution: CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Note that the UCN5810A (dual in-line package) and UCN5810LW (small outline IC package) are electrically identical and share a common pin number assignment.

Designed for use as segment or digit drivers in high-voltage, vacuum-fluorescent display applications, the UCN5810A and UCN5810LW combine a 10-bit CMOS shift register, associated latches, and control circuitry (strobe and blanking) with 60 V bipolar source outputs. The BiMOS drivers can also be used with non-multiplexed LED displays within their output limitation of 40 mA per driver.

Selected devices (suffix-1) have maximum ratings of 80 V and 40 mA per driver. In all other respects, the basic part and the part with the "-1" suffix are identical.

BiMOS II devices have much faster data input rates than the original BiMOS circuits. With a 5 V supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained.

The CMOS inputs cause minimal loading and are compatible with standard CMOS, PMOS, and NMOS circuits. Use of these drivers with TTL or DTL circuits may require appropriate input pull-up resistors to ensure an input logic high. A CMOS serial data output allows cascading for multiple drive-line applications required by many dot matrix, alpha-numeric, and bar graph displays.

The UCN5810A is supplied in an 18-pin dual in-line plastic package. Under normal operating conditions, this device will allow all outputs to source 25 mA continuously at ambient temperatures up to 60°C. The UCN5810LW is furnished in a wide-body, small-outline plastic package for minimum-area surface-mount applications.

FEATURES

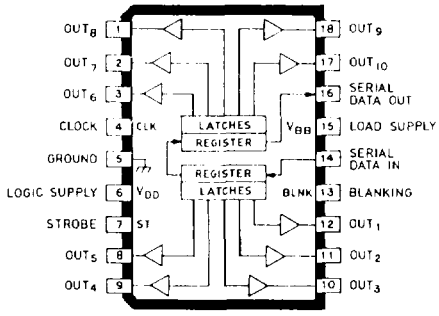
- 5 MHz Typical Data Input Rate
- Low-Power CMOS Logic and Latches
- 60 V or 80 V Source Outputs
- Internal Pull-Down Resistors

Always order by complete part number:

Part Numbers	Package	Max. V_{BB}
UCN5810A	18-Pin DIP	60 V
UCN5810A-1		80 V
UCN5810LW	18-Lead SOIC	60 V
UCN5810LW-1		80 V

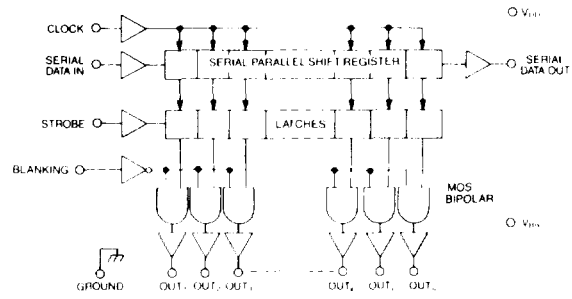
5810
10-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS

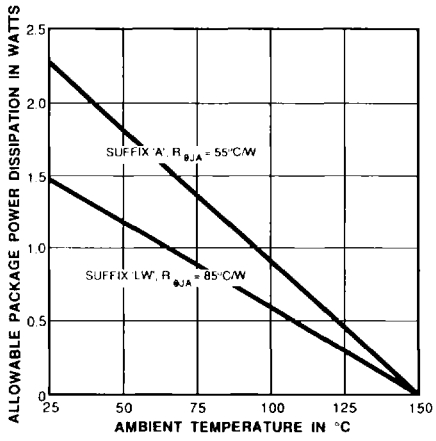
UCN5810LW



Dwg. No. A-14,355

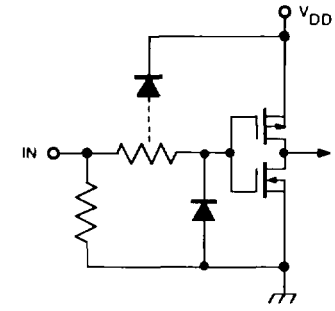
FUNCTIONAL BLOCK DIAGRAM





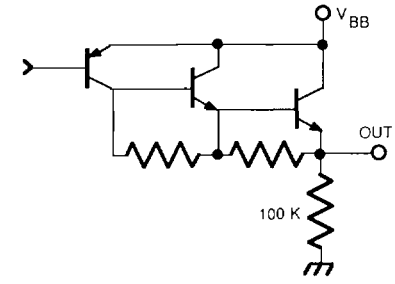
Dwg. GP-018A

TYPICAL INPUT CIRCUIT



Dwg. EP-010-4A

TYPICAL OUTPUT DRIVER



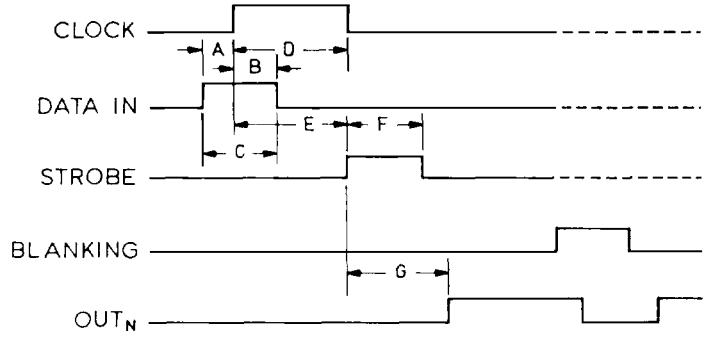
Dwg. EP-021-3

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 60 V, V_{DD} = 5 V to 12 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage	V_{OUT}	I_{OUT} = -25 mA, V_{BB} = 60 V	57.5	—	V
		I_{OUT} = -25 mA, V_{BB} = 80 V ("-1" only)	77.5	—	V
Output Pull-Down Current	I_{OUT}	V_{OUT} = 60 V	400	850	µA
		V_{OUT} = 80 V = V_{BB} ("-1" only)	550	1150	µA
Output Leakage Current	I_{OUT}	T_A = +70°C	—	-15	µA
Input Voltage	$V_{IN(1)}$	V_{DD} = 5.0 V	3.5	5.3	V
		V_{DD} = 12 V	10.5	12.3	V
	$V_{IN(0)}$	V_{DD} = 5 V to 12 V	-0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{DD} = V_{IN} = 5.0 V	—	100	µA
		V_{DD} = V_{IN} = 12 V	—	240	µA
Input Impedance	Z_{IN}	V_{DD} = 5.0 V	50	—	kΩ
Serial Data Output Resistance	R_{OUT}	V_{DD} = 5.0 V	—	20	kΩ
		V_{DD} = 12 V	—	6.0	kΩ
Supply Current	I_{BB}	All outputs ON, All outputs open	—	13	mA
		All outputs OFF, All outputs open	—	200	µA
	I_{DD}	V_{DD} = 5.0 V, All outputs OFF, Inputs = 0 V	—	100	µA
		V_{DD} = 12 V, All outputs OFF, Inputs = 0 V	—	200	µA
		V_{DD} = 5.0 V, One output ON, All inputs = 0 V	—	1.0	mA
		V_{DD} = 12 V, One output ON, All inputs = 0 V	—	3.0	mA

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

5810
10-BIT SERIAL-INPUT, LATCHED SOURCE DRIVERS



Dwg No. 12,649A

TIMING CONDITIONS

(V_{DD} = 5 V, T_A = +25°C, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) . . . . . **75 ns**
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) . . . . . **75 ns**
C. Minimum Data Pulse Width . . . . . **150 ns**
D. Minimum Clock Pulse Width . . . . . **150 ns**
E. Minimum Time Between Clock Activation and Strobe . . . . . **300 ns**
F. Minimum Strobe Pulse Width . . . . . **100 ns**
G. Typical Time Between Strobe Activation and Output Transition . . . . . **500 ns**

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, the output source drivers are disabled (OFF); the DMOS sink drivers are ON. The information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Blanking	Output Contents
		I_1 I_2 I_3 ... I_{N-1} I_N			I_1 I_2 I_3 ... I_{N-1} I_N		I_1 I_2 I_3 ... I_{N-1} I_N
H	⊓	H R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
L	⊓	L R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
X	⊔	R_1 R_2 R_3 ... R_{N-1} R_N	R_N				
		X X X ... X X	X	L	R_1 R_2 R_3 ... R_{N-1} R_N		
		P_1 P_2 P_3 ... P_{N-1} P_N	P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N	L	P_1 P_2 P_3 ... P_{N-1} P_N
					X X X ... X X	H	L L L ... L L

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State