FEATURES

- Supports the following data rates/framing formats
    DS3, C-Bit Parity
    DS3, M13
    E3, ITU-T G.751
    E3, ITU-T G.832
- Includes Transmit and Receive HDLC Controllers
- Includes 88 Bytes of On-chip RAM for Transmit HDLC Controller
- Includes 88 Bytes of On-chip RAM for Receive HDLC Controller
- Microprocessor Interface Easily Interfaces with Both Intel and Motorola Type Microprocessors
- Microprocessor Interface Supports Both Programmed I/O and Burst Mode
- Terminal Interface Accepts and Outputs Data in either a "Serial " or "Nibble-parallel Manner "
- Declares LOS (Loss of Signal) , OOF (Out of Frame) and LCV (Line Code Violations) conditions
- Detects and Flags Parity Error (e.g.,P-bit Errors in DS3 Applications, BIP-4 Errors in E3/ITU-T G.751 Applications, or BIP-8 Errors in E3/ITU-T G.832 Applications)

- Detects and Flags AIS (Alarm Indication Signal) FEBE (Far-end Block Errors) Signaling and FERF (Far-end Receive Failure) Signaling
- Supports "Local" Loopback
- Available in a 100 Pin PQFP Package
- Operates Over the Industrial Temperature Range
- Requires a Single +5V Power Supply
- CMOS Technology

APPLICATIONS

- Interface to E3, DS3
- CSU/DSU Equipment
- PCM Test Equipment
- Fiber Optic Terminals
- Multiplexers

GENERAL DESCRIPTION

The XRT7250 DS3/E3 framer device is designed to support full-duplex data flow between the "Terminal Equipment" and an LIU (or Line Interface Unit) IC. The framer device will transmit, receive and process data in the following data rates and framing formats.

DS3, C-bit Parity
DS3, M13
E3, ITU-T G.751
E3, ITU-T G.832

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XRT7250IQ	100 Pin PQFP (14mm x 20mm)	-40°C to +85°C
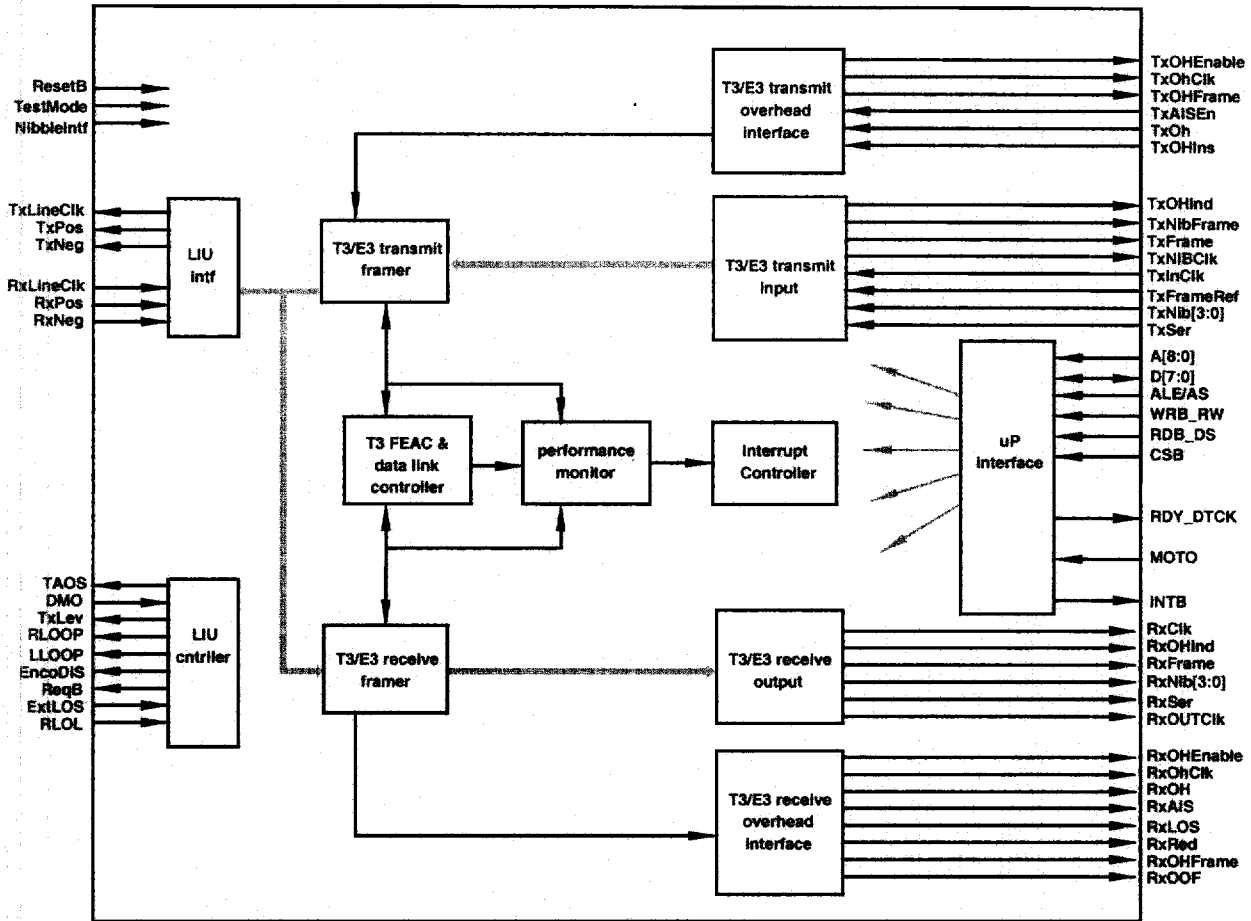
Figure 1. Block Diagram of the XRT7250 DS3/E3 Framer IC

PIN OUT

XRT7250 pinout diagram (100-pin package)

Left side (pins 1–30):
1 NC
2 NC
3 VDD
4 NC
5 GND
6 RDY_DTCK
7 WRB_RW
8 CSB
9 ALE_AS
10 RDB_DS
11 NC
12 NC
13 INTB
14 GND
15 A0
16 A1
17 A2
18 A3
19 A4
20 A5
21 A6
22 A7
23 A8
24 VDD
25 NIBBLEINTF
26 GND
27 MOTO
28 RESETB
29 TESTMODE
30 VDD

Top side (pins 100–81):
100 RXOHFRAME
99 RXOHENABLE
98 RXOH
97 RXOHIND
96 RXOHCLK
95 RXLOS
94 RXOOF
93 RXRED
92 RXOUTCLK
91 RXFRAME
90 VDD
89 GND
88 RXCLK
87 RXAIS
86 RXSER
85 RXNIB0
84 RXNIB1
83 RXNIB2
82 RXNIB3
81 GND

Right side (pins 80–51):
80 VDD
79 DMO
78 EXTLOS
77 RLOL
76 RXPOS
75 RXNEG
74 RXLINECLK
73 NC
72 GND
71 REQB
70 RLOOP
69 LLOOP
68 TAOS
67 TXLEV
66 ENCODIS
65 TXPOS
64 TXNEG
63 TXLINECLK
62 VDD
61 TXFRAME
60 GND
59 TXNIBCLK
58 TXNIBFRAME
57 TXOHFRAME
56 TXOHENABLE
55 TXOHIND
54 TXOH
53 TXOHINS
52 TXOHCLK
51 VDD

Bottom side (pins 31–50):
31 GND
32 D0
33 D1
34 D2
35 D3
36 D4
37 D5
38 D6
39 D7
40 VDD
41 TXFRAMEREF
42 GND
43 TXINCLK
44 TXAISEN
45 TXSER
46 TXNIB0
47 TXNIB1
48 TXNIB2
49 TXNIB3
50 GND

PIN DESCRIPTION

Pin #	Name	Type	Description
1	NC		**Not Bonded Out**
2	NC		**Not Bonded Out**
3	VDD	-	**Power Supply Pin**
4	NC		**Not Bonded Out**
5	GND	-	**Ground Pin**
6	Rdy_Dtck	O	**READY or DTACK** This "active-low" output pin will function as the READY output, when the microprocessor interface is running in the "Intel" Mode; and will function as the DTACK output, when the microprocessor interface is running in the "Motorola" Mode. **"Intel" Mode - READY Output** When the Framer negates this output pin (e.g., toggles it "low"), it indicates (to the µP) that the current **READ or WRITE** cycle is to be extended until this signal is asserted (e.g., toggled "high"). **"Motorola" Mode - DTACK (Data Transfer Acknowledge) Output** The Framer device will assert this pin in order to inform the local microprocessor that the present **READ or WRITE** cycle is nearly complete. If the Framer device requires that the current **READ or WRITE** cycle be extended, then the Framer will delay its assertion of this signal. The 68000 family of µPs requires this signal from its peripheral devices, in order to quickly and properly complete a **READ or WRITE** cycle.
7	WRB_RW	I	**Write Data Strobe (Intel Mode)** If the microprocessor interface is operating in the Intel Mode, then this active-low input pin functions as the WR (Write Strobe) input signal from the µP. Once this active-low signal is asserted, then the Framer will latch the contents of the µP Data Bus, into the addressed register (or RAM location) within the Framer IC. In the Intel Mode, data gets latched on rising edge of WR. **R/W Input Pin (Motorola Mode)** When the Microprocessor Interface Section is operating in the "Motorola Mode", then this pin is functionally equivalent to the "R/W" pin. In the Motorola Mode, a "READ" operation occurs if this pin is at a logic "1". Similarly, a **WRITE** operation occurs if this pin is at a logic "0".

PIN DESCRIPTION (Continued)

Pin #	Name	Type	Description
8	CSB	I	**Chip Select Input** This active-low input signal selects the Microprocessor Interface Section of the Framer device and enables **READ/WRITE** operations between the "local" microprocessor and the Framer on-chip registers and RAM locations.
9	ALE_AS	I	**Address Latch Enable/Address Strobe** This input is used to latch the address (present at the Microprocessor Interface Address Bus, A[8:0]) into the Framer Microprocessor Interface circuitry and to indicate the start of a **READ/WRITE** cycle. This input is active-high in the Intel Mode (MOTO = "low") and active-low in the Motorola Mode (MOTO = "high").
10	RDB_DS	I	**Read Data Strobe (Intel Mode)** If the microprocessor interface is operating in the Intel Mode, then this input will function as the RD* (READ STROBE) input signal from the local μP. Once this active-low signal is asserted, then the Framer will place the contents of the addressed registers (within the Framer) on the Microprocessor Data Bus (D[7:0]). When this signal is negated, the Data Bus will be tri-stated. **Data Strobe (Motorola Mode)** If the microprocessor interface is operating in the Motorola mode, then this pin will function as the active-low Data Strobe signal.
11	NC		**Not Bonded Out**
12	NC		**Not Bonded Out**
13	INTB	O	**Interrupt Request Output** This open-drain, active-low output signal will be asserted when the Framer device is requesting interrupt service from the local microprocessor. This output pin should typically be connected to the "Interrupt Request" input of the local microprocessor.
14	GND	-	**Ground Pin**
15	A0	I	**Address Bus Input (Microprocessor Interface) - LSB (Least Significant Bit)** (Please see description for A8)
16	A1	I	**Address Bus Input (Microprocessor Interface)** (Please see description for A8)

PIN DESCRIPTION (Continued)

Pin #	Name	Type	Description
17	A2	I	**Address Bus Input (Microprocessor Interface)** (Please see description for A8)
18	A3	I	**Address Bus Input (Microprocessor Interface)** (Please see description for A8)
19	A4	I	**Address Bus Input (Microprocessor Interface)** (Please see description for A8)
20	A5	I	**Address Bus Input (Microprocessor Interface)** (Please see description for A8)
21	A6	I	**Address Bus Input (Microprocessor Interface)** (Please see description for A8)
22	A7	I	**Address Bus Input (Microprocessor Interface)** (Please see description for A8)
23	A8	I	**Address Bus Input (Microprocessor Interface) - MSB (Most Significant Bit)** This input pin, along with inputs A0 - A7 are used to select the on-chip Framer register and RAM space for **READ/WRITE** operations with the "local" microprocessor.
24	VDD	-	**Power Supply Pin**
25	NibbleIntf	I	**Nibble Interface Select Input Pin** This input pin allows the user to configure the Transmit and Receive Terminal Interfaces to operate in either the "Serial-Mode" or the "Nibble/Parallel-Mode". Setting this input pin "high" configures the Transmit and Receive Terminal Interfaces to operate in the "Nibble/Parallel-Mode". Setting this input pin "low" configures the Transmit and Receive Terminal Interfaces to operate in the "Serial-Mode".
26	GND	-	**Ground Pin**
27	MOTO	I	**Motorola/Intel Processor Interface Select Mode** This input pin allows the user to configure the Microprocessor Interface to interface with either a "Motorola-type" or "Intel-type" microprocessor/microcontroller. Tying this input pin to VCC, configures the microprocessor interface to operate in the Motorola mode (e.g., the Framer device can be readily interfaced to a "Motorola-type" local microprocessor). Tying this input pin to GND configures the Microprocessor Interface to operate in the Intel Mode (e.g., the Framer device can be readily interfaced to a "Intel-type" local microprocessor).

PIN DESCRIPTION (Continued)

Pin #	Name	Type	Description
28	RESETB	I	**Reset Input** When this "active-low" signal is asserted, the Framer device will be asynchronously reset. Additionally, all outputs will be "tri-stated", and all on-chip registers will be reset to their default values.
29	TESTMODE	I	**Test Mode** The user should tie this pin to ground for proper operation.
30	VDD	-	**Power Supply Pin**
31	GND	-	**Ground Pin**
32	D0	I/O	**Bi-directional Data Bus (Microprocessor Interface Section)** Please see description for D7
33	D1	I/O	**Bi-directional Data Bus (Microprocessor Interface Section)** Please see description for D7
34	D2	I/O	**Bi-directional Data Bus (Microprocessor Interface Section)** Please see description for D7
35	D3	I/O	**Bi-directional Data Bus (Microprocessor Interface Section)** Please see description for D7
36	D4	I/O	**Bi-directional Data Bus (Microprocessor Interface Section)** Please see description for D7
37	D5	I/O	**Bi-directional Data Bus (Microprocessor Interface Section)** Please see description for D7
38	D6	I/O	**Bi-directional Data Bus (Microprocessor Interface Section)** Please see description for D7
39	D7	I/O	**MSB of Bi-Directional Data Bus (Microprocessor Interface Section)** This pin, along with pins D0 - D6, function as the Microprocessor Interface bi-directional data bus, and is intended to be interfaced to the "local" microprocessor.
40	VDD	-	**Power Supply Pin**
41	TxFrameRef	I	**Transmit Framer Reference Input** Framing reference for the transmit framer.

PIN DESCRIPTION (Continued)

Pin #	Name	Type	Description
42	GND	-	**Ground Pin**
43	TxInClk	I	**Transmit Framer Reference Clock Input** For E3 applications, the user should apply a 34.368MHz clock signal. For DS3 applications, the user should apply a 44.736MHz clock signal.
44	TxAISEn	I	**Transmit AIS Command Input** Setting this input pin "high" configures the Transmit Section to generate and transmit an AIS Pattern. Setting this input pin "low" configures the Transmit Section to generate E3 or DS3 in a normal manner.
45	TxSer	I	**Transmit Serial Input** The Terminal Equipment is expected to input data, that is intended to be transmitted to the remote terminal, over an E3 or DS3 transport medium. The Framer IC will take data, applied to this pin, and insert it into an outbound "E3 or DS3" frame. The data at this pin is latched on the "rising" edge of the TxInClk input signal. **Note:** *This input pin is active only if the Serial-Mode has been selected.*
46	TxNib0	I	**Transmit Nibble Input -0** The Terminal Equipment is expected to input data, that is intended to be transmitted to the remote terminal, over an E3 or DS3 transport medium. The Framer IC will take data, applied to this pin (along with TxNib1, TxNib2, and TxNib3), and insert it into an outbound "E3 or DS3" frame. **Note:** *This input pin is active only if the Nibble-Parallel-Mode has been selected.*

PIN DESCRIPTION (Continued)

Pin #	Name	Type	Description
47	TxNib1	I	**Transmit Nibble Input -1** The Terminal Equipment is expected to input data, that is intended to be transmitted to the remote terminal, over an E3 or DS3 transport medium. The Framer IC will take data, applied to this pin, and insert it into an outbound "E3 or DS3" frame. *Note: This input pin is active only if the Nibble-Parallel-Mode has been selected.*
48	TxNib2	I	**Transmit Nibble Input -2** The Terminal Equipment is expected to input data, that is intended to be transmitted to the remote terminal, over an E3 or DS3 transport medium. The Framer IC will take data, applied to this pin, and insert it into an outbound "E3 or DS3" frame. *Note: This input pin is active only if the Nibble-Parallel-Mode has been selected.*
49	TxNib3	I	**Transmit Nibble Input -3** The Terminal Equipment is expected to input data, that is intended to be transmitted to the remote terminal, over an E3 or DS3 transport medium. The Framer IC will take data, applied to this pin, and insert it into an outbound "E3 or DS3" frame. *Note: This input pin is active only if the Nibble-Parallel-Mode has been selected.*
50	GND	-	**Ground Pin**
51	VDD	-	**Power Supply Pin**
52	TxOHClk	O	**Transmit Overhead Clock** This output clock signal is used to latch the data residing on the TxOH input pin. The TxOH input signal is latched on the falling edge of this signal.
53	TxOHIns	I	**Transmit Overhead Data Insert Input** When this input is "high", the values on the TxOH line are inserted into the overhead bits within the outbound DS3 or E3 Frames. Framing and parity bits are not taken from TxOH line. (When TxOHIns is high, TxOH value is taken irrespective of register setting in E3 G.751 mode).
54	TxOH	I	**Transmit Overhead Input Pin** Overhead input to the DS3/E3 Transmit Framer from the Terminal Equipment. This signal is sampled on the rising edge of TxOHClk.

PIN DESCRIPTION (Continued)

Pin #	Name	Type	Description
55	TxOHInd	O	**Transmit Overhead Data Indicator** When this input pin is "high", then it means that the data placed on the TxSer/TxNib line will be ignored by the Framer IC.
56	TxOHEnable	O	**Transmit Overhead Input Enable** When the output is "high", the new OH bit is to be inserted into the frame and can be placed on the TxOH line by external overhead interface. This pin is "high" for one clock period of TxInClk.
57	TxOHFrame	O	**Transmit Overhead Framing Pulse** This output pin pulses "high" when the Transmit Overhead Input is expecting the first Overhead bit, within a frame to be applied to the TxOH input pin. This pin is "high" for one clock period of TxOHClk.
58	TxNibFrame	O	**Transmit Frame Boundary Indicator - Nibble-Parallel Interface** This output pin pulses "high" when the last nibble of a given frame is expected at the TxNib[3:0] input pins.
59	TxNibClk	O	**Transmit Nibble Clock Signal** Reference clock for clocking the transmit nibble data from external interface.
60	GND	-	**Ground Pin**
61	TxFrame	O	**Transmit End of DS3 or E3 Frame Indicator** This output pin indicates that the last bit of an outbound DS3 or E3 frame, is being transmitted from the TxPOS and TxNEG output pins. This pin marks the end of DS3 or E3 frame by pulsing "high" for one bit period at the end of each frame.
62	VDD	-	**Power Supply Pin**
63	TxLineClk	O	**Transmit Line Interface Clock** This clock signal is intended to drive the TCLK input on the XRT7300 output to the Line Interface IC, along with the TxPOS and TxNEG signals. The purpose of this output clock signal is to provide the LIU with timing information that it can use to generate the AMI pulses and deliver them over the transmission medium to the Far-End Receiver. The user can configure the source of this clock to be either the RxLineClk (from the Receiver portion of the Framer) or the TxInClk input. The nominal frequency of this clock signal is 34.368MHz.

PIN DESCRIPTION (Continued)

Pin #	Name	Type	Description
64	TxNEG	O	**Transmit Negative Polarity Pulse** The exact role of this output pin depends upon whether the Framer is operating in the Unipolar or Bipolar Mode. **Unipolar Mode** This output signal pulses "high" for one bit period, at the end of each "outbound" E3 or DS3 frame. This output signal is at a logic "low" for all of the remaining bit-periods of the "outbound" E3 or DS3 frames. **Bipolar Mode** This output pin functions as one of the two dual-rail output signals that commands the sequence of pulses to be driven on the line. TxPOS is the other output pin. This input is typically connected to the TNDATA input of the external Line Interface IC. When this output is asserted, it will command the LIU to generate a negative polarity pulse on the line.
65	TxPOS	O	**Transmit Positive Polarity Pulse** The exact role of this output pin depends upon whether the Framer is operating in the Unipolar or Bipolar Mode. **Unipolar Mode** This output pin functions as the "Single-Rail" output signal for the "outbound" data stream. The signal, at this output pin, will be updated on the "user-selected" edge of the TxLineClk signal. **Bipolar Mode** This output pin functions as one of the two dual rail output signals that commands the sequence of pulses to be driven on the line. TxNEG is the other output pin. This input is typically connected to the TPDATA input of the external Line Interface IC. When this output is asserted, it will command the LIU to generate a positive polarity pulse on the line.

PIN DESCRIPTION (Continued)

Pin #	Name	Type	Description
66	ENCODIS	O	**Encoder (HDB3) Disable Output pin (intended to be connected to the XRT7300 DS3/E3 Line Interface IC)** This output pin is intended to be connected to the Encodis input pin of the XRT7300 DS3/E3 Line Interface IC (provided that XRT7300 device is operating in the hardware mode). The user can control the state of this output pin by writing a "0" or "1" to Bit 3 (Encodis) within the Line Interface Driver Register (Address = 84h). If the user commands this signal to toggle "high" then it will disable the B3ZS/HDB3 encoder circuitry within the XRT7300 IC. Conversely, if the user commands this output signal to toggle "low", then the B3ZS/HDB3 Encoder circuitry, within the XRT7300 IC will be enabled. Writing a "1" to Bit 3 of the Line Interface Driver Register (Address = 84h) will cause this output pin to toggle "high". Writing a "0" to this bit-field will cause this output pin to toggle "low". ***Notes:*** *(1) The user is advised to disable the B3ZS/HDB3 encoder (within the XRT7300 IC) if the Transmit and Receive E3/DS3 Framers (within the Framer) are configured to operate in the B3ZS/HDB3 line code.* *(2) If the customer is not using the XRT7300 DS3/E3 Line Interface IC, then they can use this output pin for a variety of other purposes.*

PIN DESCRIPTION (Continued)

Pin #	Name	Type	Description
67	TxLEV	O	**Transmit Level Select Output (to be connected to the XRT7300 DS3/E3 Line Interface IC)** This output pin is intended to be connected to the TxLev input pin of the XRT7300 DS3/E3 Line Interface IC (provided that the XRT7300 device is operating in the Hardware Mode). The user can control the state of this output pin by writing a "0" or a "1" to Bit 2 (TxLev) within the Line Interface Driver Register (Address = 84h). If the user commands this signal to toggle "high" then it will cause the XRT7300 DS3/E3 Line Interface to increase the amplitude of its output signal on the line, in order to drive the signal over cable lengths of greater than 225 ft. Therefore, the user is recommended to set this output "high", if DS3 line signals over 225 ft (or more) of cable. Conversely, if the user is driving DS3 line signals over less than 225 ft of cable, then it is recommended to set this output pin "low". Writing a "1" to Bit 2 of the Line Interface Drive Register (Address = 84h) will cause this output pin to toggle "high". Writing a "0" to this bit-field will cause this output pin to toggle "low". ***Note:*** *If the customer is not using the XRT7300 DS3/E3 Line Interface IC, then this output pin can be used for a variety of other purposes.*
68	TAOS	O	**"Transmit All Ones Signal" (TAOS) Command (for the XRT7300 Line Interface IC)** This output pin is intended to be connected to the TAOS input pin of the XRT7300 DS3/E3 Line Interface IC (provided that the XRT7300 device is operating in the Hardware Mode). The user can control the state of this output pin by writing a '0' or '1' to Bit 4 (TAOS) of the Line Interface Drive Register (Address = 84h). If the user commands this signal to toggle "high" then it will force the XRT7300 Line Interface IC to transmit an "All Ones" pattern onto the line. Conversely, if the user commands this output signal to toggle "low" then the XRT7300 DS3/E3 Line Interface IC will proceed to transmit data based upon the pattern that it receives via the TxPOS and TxNEG output pins. Writing a "1" to Bit 4 of the Line Interface Drive Register (Address = 84h) will cause this output pin to toggle "high". Writing a "0" to this bit-field will cause this output pin to toggle "low". ***Note:*** *If the customer is not using the XRT7300 DS3/E3 Line Transceiver IC, then this output pin can be used for a variety of other purposes.*

PIN DESCRIPTION (Continued)

Pin #	Name	Type	Description
69	LLOOP	O	**Local Loopback Output Pin (to the XRT7300 DS3/E3 Line Interface IC)** This output pin is intended to be connected to the LLOOP input pin of the XRT7300 LIU IC (provided that the XRT7300 device is operating in the Hardware Mode). The user can command this signal to toggle "high" and, in turn, force the LIU into the "Local Loopback" mode. (For a detailed description of the XRT7300 DS3/E3 Line Interface IC's operation during Local Loopback, please see the XRT7300 DS3/STS-1/E3 Line Interface IC's data sheet). Writing a "1" to bit 1 of the "Line Interface Drive Register (Address = 84h) will cause this output pin to toggle "high". Writing a "0" to this bit-field will cause the LLOOP output to toggle "low". *Note: If the user is not using the XRT7300 DS3/E3 Line Interface IC, then this output pin can be used for a variety of other purposes.*
70	RLOOP	O	**Remote Loopback Output Pin (to the XRT7300 DS3/E3 Line Interface IC)** This output pin is intended to be connected to the RLOOP input pin of the XRT7300 DS3/E3 Line Interface IC (provided that the XRT7300 device is operating in the Hardware Mode). The user can command this signal to toggle "high" and, in turn, force the XRT7300 DS3/E3 Line Interface IC into the "Remote Loopback" mode. Conversely, the user can command this signal to toggle "low" and allow the XRT7300 device to operate in the normal mode. (For a detailed description of the XRT7300 DS3/E3 Line Interface IC's operation during Remote Loopback, please see the XRT7300 DS3/STS-1/ E3 Line Interface IC's Data Sheet). Writing a "1" to bit 1 of the "Line Interface Drive Register (Address = 84h) will cause this output pin to toggle "high". Writing a "0" to this bit-field will cause the RLOOP output to toggle "low". *Note: If the customer is not using the XRT7300 DS3/E3 Line Interface IC, then this output pin can be used for a variety of other purposes.*

PIN DESCRIPTION (Continued)

Pin #	Name	Type	Description
71	REQB	O	**Receive Equalization Bypass Control output pin -** **(to be connected to the XRT7300 DS3/E3 Line Interface IC)** This output pin is intended to be connected to the REQB input pin of the XRT7300 DS3/E3 Line Interface IC (provided that the XRT7300 device is operating in the Hardware Mode). The user can control the state of this output pin by writing a '0' or '1' to Bit 5 (REQB) within the Line Interface Driver Register (Address = 84h). If the user commands this signal to toggle "high" then it will cause the incoming DS3 or E3 line signal to "by-pass" equalization circuitry, within the XRT7300 Device. Conversely, if the user commands this output signal to toggle "low", then the incoming DS3 or E3 line signal will be routed through the equalization circuitry. For information on the criteria that should be used when deciding whether to bypass the equalization circuitry, please consult the "XRT7300 DS3/E3 Line Interface" data sheet. Writing a "1" to Bit 5 of the Line Interface Drive Register (Address = 84h) will cause this output pin to toggle "high". Writing a "0" to this bit-field will cause this output pin to toggle "low". *Note: If the customer is not using the XRT7300 DS3/E3 Line Interface IC, then this output pin can be used for a variety of other purposes.*
72	GND	-	**Ground Pin**
73	NC	-	**Not Bonded Out**
74	RxLineClk	I	**Receiver LIU (Recovered) Clock** This input signal serves three purposes: 1. The Receive Framer uses it to sample and "latch" the signals at the RxPOS and RxNEG input pins (into the Receive Framer circuitry). 2. This input signal functions as the timing reference for the Receive Framer block. 3. The Transmit Framer block can be configured to use this input signal as its timing reference. *Note: This signal is the recovered clock from the external DS3/E3 LIU (Line Interface Unit) IC, which is derived from the incoming line signal.*

PIN DESCRIPTION (Continued)

Pin #	Name	Type	Description
75	RxNEG	I	**Receive Negative Data Input** The exact role of this input pin depends upon whether the Framer is operating in the Unipolar or Bipolar Mode. **Unipolar Mode** This input pin is inactive, and should be pulled "low" when the Framer is operating in the Unipolar Mode. **Bipolar Mode** This input pin functions as one of the dual rail inputs for the incoming AMI/HDB3/B3ZS encoded E3/DS3 data that has been received from an external Line Interface Unit (LIU) IC. RxPOS functions as the other dual rail input for the Framer. When this input pin is asserted, it means that the LIU has received a "negative polarity" pulse from the line.
76	RxPOS	I	**Receive Positive Data Input** The exact role of this input pin depends upon whether the Framer is operating in the Unipolar or Bipolar Mode. **Unipolar Mode** This input pin functions as the "Single-Rail" input for the "incoming" E3 or DS3 data stream. The signal at this input pin will be sampled and latched (into the Receive Framer) on the "user-selected" edge of the RxLineClk signal. **Bipolar Mode** This input functions as one of the dual rail inputs for the incoming AMI/HDB3/B3ZS encoded E3 or DS3 data stream that has been received from an external Line Interface Unit (LIU) IC. RxNEG functions as the other dual rail input for the Framer. When this input pin is asserted, it means that the LIU has received a "positive polarity" pulse from the line.

PIN DESCRIPTION (Continued)

Pin #	Name	Type	Description
77	RLOL	I	**Receive Loss of Lock Indicator - from the XRT7300 DS3/E3 Line Interface IC** This input pin is intended to be connected to the RLOL (Receive Loss of Lock) output pin of the XRT7300 Line Interface IC. The user can monitor the state of this pin by reading the state of Bit 1 (RLOL) within the Line Interface Scan Register (Address = 85h). If this input pin is "low", then it means that the phase-locked-loop circuitry, within the XRT7300 device is properly locked onto the incoming E3 or DS3 data stream; and is properly recovering clock and data from this E3 or DS3 data stream. However, if this input pin is "high", then it means that the phase-locked-loop circuitry, within the XRT7300 device has lost lock with the incoming E3 or DS3 data-stream, and is not properly recovering clock and data. For more information on the operation of the XRT7300 DS3/E3 Line Interface IC, please consult the "XRT7300 DS3/E3 Line Interface" data sheet. *Note: If the customer is not using the XRT7300 DS3/E3 Line Interface IC, this input pin can be used for other purposes.*
78	ExtLOS	I	**Receive LOS (Loss of Signal) Indicator Input (from XRT7300 Line Interface)** This input pin is intended to be connected to the RLOS (Receive Loss of Signal) output pin of the XRT7300 Line Interface IC. The user can monitor the state of this pin by reading the state of Bit 0 (RLOS) within the Line Interface Scan Register (Address = 85h). If this input pin is "low", then it means that the XRT7300 device is detecting a sufficient amount of signal energy on the line, due to the incoming DS3 or E3 data stream. However, if this input pin is "high", then it means that the XRT7300 device is not detecting a sufficient amount of signal energy on the line, due to the incoming data stream, and may be experiencing a "Loss of Signal" condition. For more information on the operation of the XRT7300 DS3/E3 Line IC, please consult the "XRT7300 DS3/STS-1/E3 Line Interface IC" data sheet. *Note: Asserting the RLOS input pin will cause the XRT7250 DS3/E3 Framer device to declare an "LOS" (Loss of Signal) condition. Therefore, this input pin should not be used as a general purpose input.*

PIN DESCRIPTION (Continued)

Pin #	Name	Type	Description
79	DMO	I	**"Drive Monitor Output" Input (from the XRT7300 DS3/E3 Line Interface IC)** This input pin is intended to be tied to the DMO output pin of the XRT7300 DS3/E3 Line Interface IC. The user can determine the state of this input pin by reading Bit 2 (DMO) within the Line Interface Scan Register (Address = 85h). If this input signal is "high", then it means that the drive monitor circuitry (within the XRT7300 DS3/E3 Line Interface IC) has not detected any bipolar signals at the MTIP and MRING inputs within the last 128 ± 32 bit-periods. If this input signal is "low", then it means that bipolar signals are being detected at the MTIP and MRING input pins of the XRT7300 device. *Note: If the customer is not using the XRT7300 DS3/E3 Line Interface IC, then this input pin can be used for a variety of other purposes.*
80	VDD	-	**Power Supply Pin**
81	GND	-	**Ground Pin**
82	RxNib3	O	**Receive Nibble Output - 3** The Framer IC will output "Received" data (from the Remote Terminal) to the local Terminal Equipment via this pin along with RxNib0, RxNib1 and RxNib2. The data at this pin is updated on the rising edge of the RxClk output signal. *Note: This output pin is active only if the Nibble-Parallel-Mode has been selected.*
83	RxNib2	O	**Receive Nibble Output -2** The Framer IC will output "Received" data (from the Remote Terminal) to the local Terminal Equipment via this pin along with RxNib0, RxNib1 and RxNib3. The data at this pin is updated on the rising edge of the RxClk output signal. *Note: This output pin is active only if the Nibble-Parallel-Mode has been selected.*

PIN DESCRIPTION (Continued)

Pin #	Name	Type	Description
84	RxNib1	O	**Receive Nibble Output - 1** The Framer IC will output "Received" data (from the Remote Terminal) to the local Terminal Equipment via this pin along with RxNib0, RxNib2 and RxNib3. The data at this pin is updated on the rising edge of the RxClk output signal. *Note: This output pin is active only if the Nibble-Parallel-Mode has been selected.*
85	RxNib0	O	**Receive Nibble Output - 0** The Framer IC will output "Received" data (from the Remote Terminal) to the local Terminal Equipment via this pin along with RxNib1, RxNib2 and RxNib3. The data at this pin is updated on the rising edge of the RxClk output signal. *Note: This output pin is active only if the Nibble-Parallel-Mode has been selected.*
86	RxSer	O	**Receive Serial Output** The Framer IC will output "Received" data (from the Remote Terminal) to the local Terminal Equipment via this pin. The data at this pin is updated on the "selected" edge of the RxClk output pin. *Note: This output pin is active only if the Serial Mode has been selected.*
87	RxAIS	O	**Receive "Alarm Indication Signal" Output Pin** The Framer will assert this pin to indicate that the Alarm Indication Signal (AIS) has been identified in the Receive E3 or DS3 data stream.
88	RxClk	O	**Receive Clock Output Signal for Serial and Nibble-Parallel Data Interface** A clock output signal for serial-bit or nibble-parallel data interface.
89	GND	-	**Ground Pin**

PIN DESCRIPTION (Continued)

Pin #	Name	Type	Description
90	RxFrame	O	**Receive Boundary of E3 or DS3 Frame Output Indicator** This output pin indicates the boundary of the incoming E3 or DS3 frame as they appear, at the RxPOS and RxNEG inputs. This pin marks the boundary of an E3 or DS3 frame by pulsing high for one bit period at the beginning of each frame.
91	VDD	-	**Power Supply Pin**
92	RxOutClk	O	**Receive Out Clock** This clock signal is the same as the RxLineClk signal.
93	RxRED	O	**Receiver Red Alarm Indicator - Receive Framer** The Framer asserts this output pin to denote that one of the following events has been detected by the Receive Framer: · LOS - Loss of Signal Condition · OOF - Out of Frame Condition · AIS - Alarm Indication Signal Detection
94	RxOOF	O	**Receiver Framer - "Out of Frame" Indicator** The Receive Framer will assert this output signal whenever it has declared an "Out of Frame" (OOF) condition with the incoming E3 or DS3 frames. This signal is negated when the framer correctly regains synchronization with the E3 or DS3 frame.
95	RxLOS	O	**Receive Framer - Loss of Signal Output Indicator** The XRT7250 device will toggle this pin "high" when the receive framer has detected and declared a "Loss of Signal" condition.
96	RxOhClk	O	**Receive Overhead Interface Output Clock Signal** The RxOH is updated on the rising edge of this clock signal.
97	RxOhInd	O	**Receive Overhead Bit Indicator** Rx overhead bit indicator. When high indicates that overhead data is present on RxSer/RxNib line.
98	RxOH	O	**Receive Overhead Output Port** Contains all the overhead bits extracted from the received frame.
99	RxOHEnable	O	**Receive Overhead Enable Indicator** When this output is "high", the external overhead interface can read the new OH bit placed on the RxOH line by the framer. It is high for 1 clock period of RxOutCLK.
100	RxOHFrame	O	**Receive Overhead Frame Boundary Indicator** This output pin pulses "high" whenever the Receive Terminal Output Interface outputs the first bit (or nibble) of a new frame.

PRODUCT DESCRIPTION

The XRT7250 supports transmit frame generation, receive frame synchronization and recovery, frame overhead insertion/extraction, and HDLC data processing. The XRT7250 DS3/E3 framer consists of the following blocks which are described in subsequent sections:

- Transmit
- Receive
- Microprocessor Interface
- Performance Monitor

The Transmit Section
The purpose of the Transmit Section of the XRT7250 DS3/E3 Framer IC is to permit the Terminal Equipment to transmit data to a remote terminal via a public or leased DS3 or E3 transport medium.

The Transmit Section of the XRT7250 DS3/E3 Framer IC consists of the following functional blocks.

- Transmit Terminal Equipment Interface Block
- Transmit HDLC Controller Block
- Transmit E3/DS3 Framer Block
- Transmit Line Interface Block

The transmit section of the framer device will allow the terminal equipment to write data into the "Transmit Terminal Equipment Interface Block" in either a serial or nibble-parallel manner. Additionally, the "Transmit Terminal Equipment Interface Block" also provides a separate "Overhead Port" to permit "Data Link" equipment to have their own access to the XRT7250 framer device.

The Transmit DS3/E3 Framer block will take the data from the "Terminal Equipment" and interleave it with overhead bits in order to form the appropriate DS3 or E3 framing structure. These overhead bits will be sourced from either the "Overhead Port", or the "Transmit LAPD Message Buffer."

The transmit line interface block will transmit these DS3 or E3 frames to a Line Interface Unit (LIU) IC for transmission to the "remote" terminal equipment.

The transmit section will also transmit path maintenance data link information in the form of LAPD message frames or in FEAC messages (for DS3, C-bit parity applications only) to the "remote" terminal equipment.

- Transmit terminal equipment input Interface can accept data in the serial or nibble-parallel mode

- Transmit terminal equipment input Interface also includes the "Transmit Overhead Input Interface" which can be dedicated to "Data Link" equipment

- Includes Transmit HDLC Controller and 88 bytes of on-chip RAM to support the transmission of Path Maintenance Data Link Messages

- Transmits Path Maintenance Data Link Messages via LAPD Message frames, to the remote Terminal Equipment

- Transmits FEAC (Far-End Alarm & Control) Messages to the remote Terminal Equipment (DS3, C-bit Parity Applications only)

- Transmits Trail Trace Buffer Messages to the remote Terminal Equipment (E3, ITU-T G.832 Applications only)

- Automatically transmits FERF when "Receive Section" is declaring an LOS, OOF or AIS condition

- Automatically transmits FEBE when "Receive Section" detects Parity Errors (P-Bit, BIP-4 or BIP-8) in its incoming DS3/E3 data-stream

- Transmits FERF, FEBE and AIS patterns upon software control

- Transmits Idle Pattern upon software control (DS3 Applications only)

- Includes B3ZS/HDB3 Encoder

- Line Interface Outputs can output data (to the LIU) in either Single-Rail or Dual-Rail Formats

The Receive Section

The purpose of the Receive Section of the XRT7250 DS3/E3 Framer IC is to allow a "local" terminal equipment to receive data from a "remote" terminal equipment via a public or leased DS3 or E3 transport medium.

The receive section of the XRT7250 DS3/E3 framer IC consists of the following functional blocks.

- Receive Line Interface Block
- Receive E3/DS3 Framer Block
- Receive HDLC Controller Block
- Receive Terminal Equipment Interface Block

The receive section of the framer device will receive either single-rail or Dual-Rail format data from the LIU device and will (optionally) perform "B3ZS/HDB3 Decoding" on this data. This procedure will result in a binary data stream of data containing either DS3 or E3 frame data.

The receive E3/DS3 framer block will acquire and maintain frame synchronization with the incoming E3 or DS3 frames. The receive E3/DS3 framer block will also extract out the overhead bytes and route them to the appropriate destinations (e.g., the "Receive LAPD Message Buffer" or the "Receive Terminal Equipment Overhead Output Interface").

The receive terminal equipment output interface will output the remaining data to the "local" terminal in either a "Serial" or "Nibble-parallel" manner.

- Line Interface Inputs can accept data (from the LIU) in either Single-Rail or Dual-Rail Formats

- Includes B3ZS/HDB3 Decoder

- Includes Receive HDLC Controller and 88 bytes of on-chip RAM to support the reception of Path Maintenance Data Link Messages

- Receives Path Maintenance Data Link Messages via LAPD Message frames, from the remote Terminal Equipment

- Receives FEAC (Far-End Alarm & Control) Messages from the remote Terminal Equipment (DS3, C-bit Parity Applications only)

- Receives Trail Trace Buffer Message from the remote Terminal Equipment (E3, ITU-T G.832 Applications only)

- Detects and Declares Line Code Violations (LCV)

- Detects and Declares Loss of Signal Condition (LOS)

- Detects and Declares OOF (Out of Frame) Condition.

- Detects and Declares FERF (Far-End Receive Failure) Signaling

- Verifies the P-bits (for DS3 Applications), the BIP-4 (for E3, ITU-T G.751 Applications) or the BIP-8 values (for E3, ITU-T G.832), and Flags Errors

- Detects and Declares FEBE (Far-End Block Error) Signaling

- Detects and Flags AIS and Idle Patterns

- Receive Terminal Equipment Output Interface can output data in the Serial or Nibble-Parallel Mode

- Receive Terminal Equipment Output Interface also includes the "Receive Overhead Output Interface" which can be dedicated to "Data Link" equipment

The Microprocessor Interface Section

The Microprocessor Interface Section allows a user (or a local "housekeeping" processor) to do the following.

- To configure the Framer IC into a wide variety of operating modes; by writing data into any one of a large number of "Read/Write" registers

- To monitor many aspects of the Framer IC's performance by reading data from any one of a large number of "Read-Only" registers

- To operate in a "polling" or "interrupt-driven" environment. The Framer IC contains extensive interrupt structure consisting of a wide range of interrupt enable and interrupt status registers

- To command the Framer IC to transmit FEAC messages and/or LAPD Message frames, upon software command

- To read and process received FEAC messages and/or Path Maintenance Messages from the Framer IC

- The Microprocessor Interface allows the user to interface the XRT7250 DS3/E3 Framer IC to either an Intel-type or Motorola-type processor. Additionally, the Microprocessor can access the XRT7250 device via either the "Programmed I/O" or "Burst" Modes

- The Microprocessor Interface section includes a "Loss of Clock Signal" protection feature that automatically completes (or terminates) a "Read/ Write" operation, should a "Loss of Clock Signal" event occur

The Performance Monitor Section

The Performance Monitor Section of the XRT7250 DS3/E3 Framer IC consists of a large number of "Reset-upon-Read" and "Read-Only" registers that contain cumulative and "one-second" statistics that reflect the performance/status of the Framer IC/system. These cumulative and "one-second" statistics are kept on the following parameters:

- Number of Line Code Violation events detected by the Receive Line Interface Block

- Number of Framing Bit (F- and M-bit) Errors detected by the Receive DS3/E3 Framer Block (DS3 Applications)

- Number of Framing Byte (FA1 or FA2) errors detected by the Receive DS3/E3 Framer Block (E3 Applications)

- Number of Parity Errors (P-bit for DS3 Applications, BIP-4 for E3, ITU-T G.751 Applications or BIP-8 for E3, ITU-T G.832 Applications) detected by the Receive DS3/E3 Framer Block

- Number of FEBE (Far-End-Block Error) Events detected by the Receive DS3/E3 Framer Block.

Contains "Performance Monitor" Registers which increment each time the following events occur:

- Detection of Line Code Violations

- Detection of Framing Bit (or Byte) Errors

- Detection of Parity Errors (e.g., P-bit for DS3 Applications, BIP-4 for E3/ITU-T G.751 Applications, or BIP-8 for E3/ITU-T G.832 Applications)

- Detection of FEBE Events
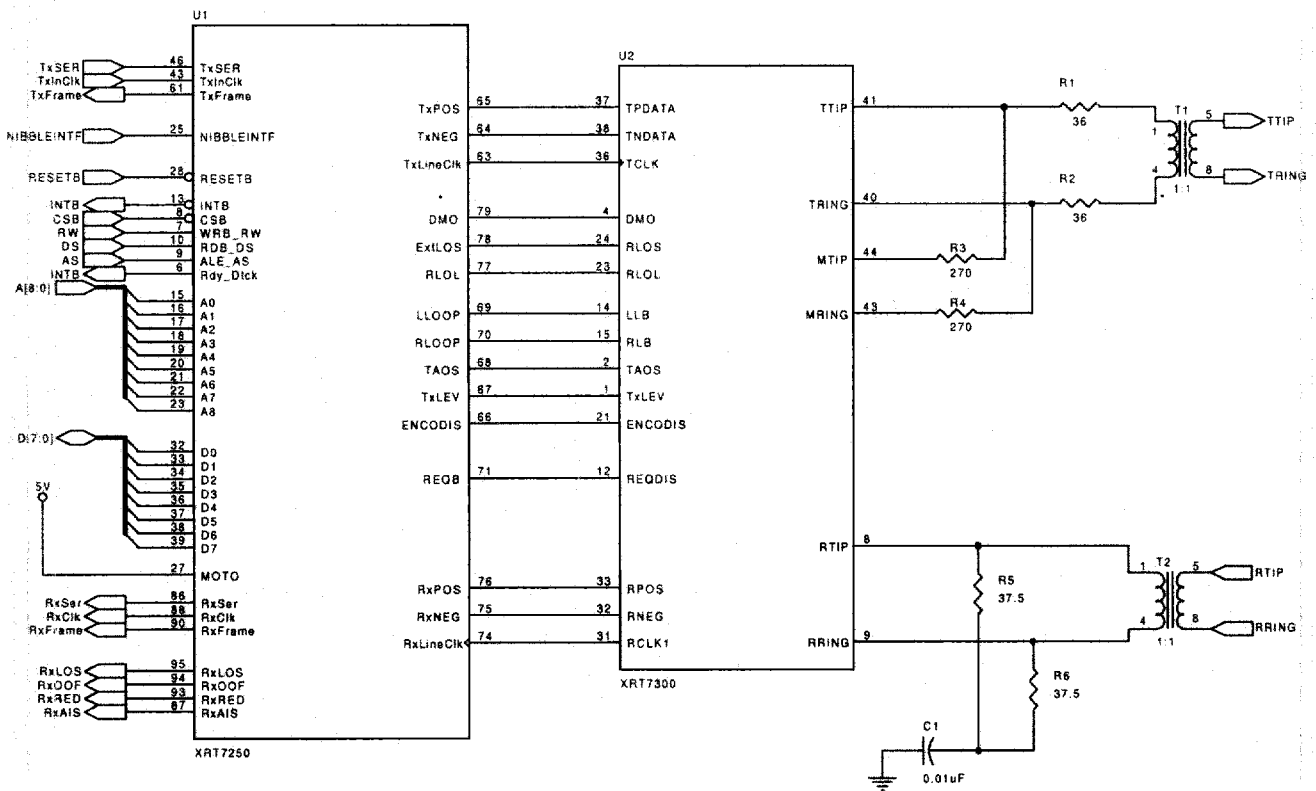
APPLICATIONS INFORMATION

Figure 2. Illustration of the XRT7250 DS3/E3 Framer Interfaced to the XRT7300 DS3/STS-1/E3 LIU IC (Hardware Mode)
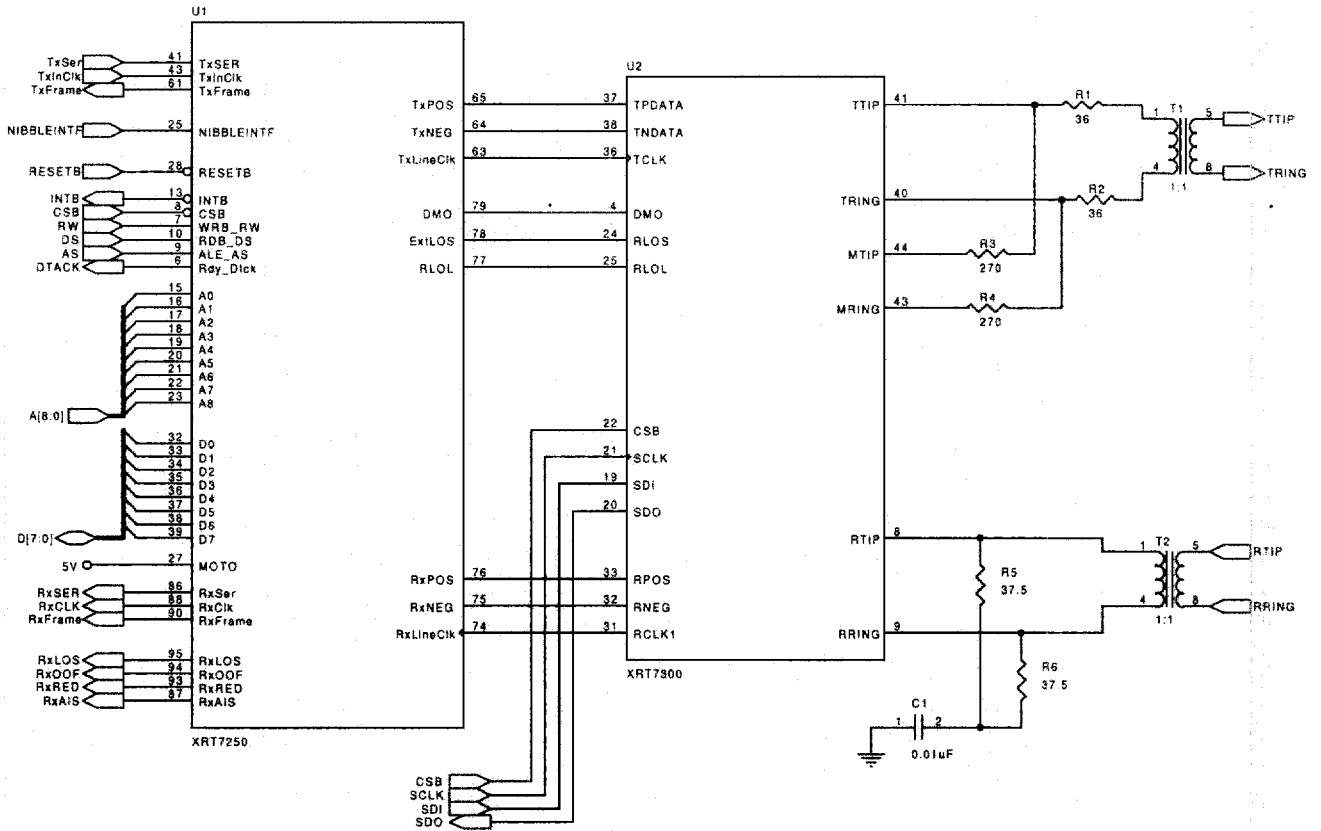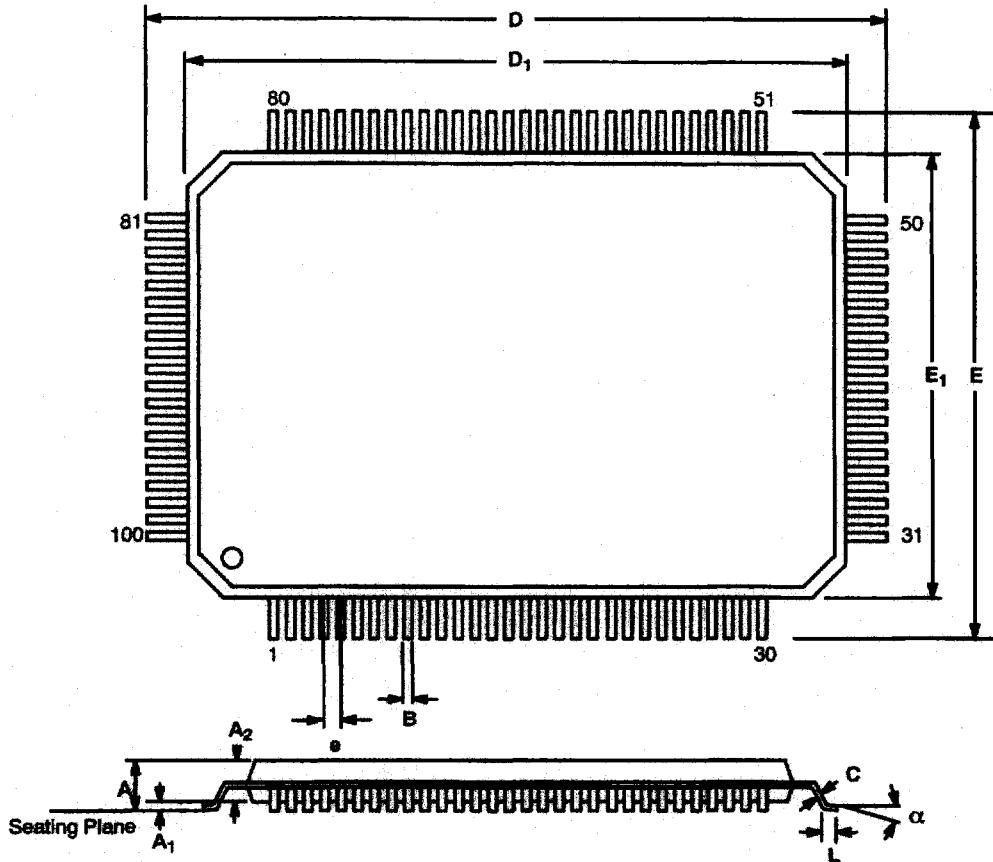
**Figure 3. Illustration of the XRT7250 DS3/E3 Framer Interfaced
to the XRT7300 DS3/STS-1/E3 LIU IC (Host Mode)**

100 LEAD PLASTIC QUAD FLAT PACK
## (14 mm x 20 mm, QFP)
Rev. 2.00

	1.6 mm Form				1.95 mm Form			
	INCHES		MILLIMETERS		INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.102	0.130	2.60	3.30	0.102	0.134	2.60	3.40
A₁	0.002	0.010	0.05	0.25	0.002	0.014	0.05	0.35
A₂	0.100	0.120	2.55	3.05	0.100	0.120	2.55	3.05
B	0.009	0.015	0.22	0.38	0.009	0.015	0.22	0.38
C	0.005	0.009	0.13	0.23	0.005	0.009	0.13	0.23
D	0.904	0.923	22.95	23.45	0.931	0.951	23.65	24.15
D₁	0.783	0.791	19.90	20.10	0.783	0.791	19.90	20.10
E	0.667	0.687	16.95	17.45	0.695	0.715	17.65	18.15
E₁	0.547	0.555	13.90	14.10	0.547	0.555	13.90	14.10
e	0.0256 BSC		0.65 BSC		0.0256 BSC		0.65 BSC	
L	0.029	0.040	0.73	1.03	0.026	0.037	0.65	0.95
α	0°	7°	0°	7°	0°	7°	0°	7°

Note: The control dimension is the millimeter column

Notes
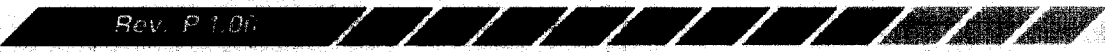
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