



Analog Semiconductor IC

A7B Series

Single-cell Li-ion / Li-polymer
Battery Protection IC

Rev. E09-06

AnaSem Inc.
..... *Future of the analog world*



AnaSem

Products Data Sheet

Analog Semiconductor IC

Single-cell Li-ion / Li-polymer Battery Protection IC

A7B Series

GENERAL DESCRIPTIONS

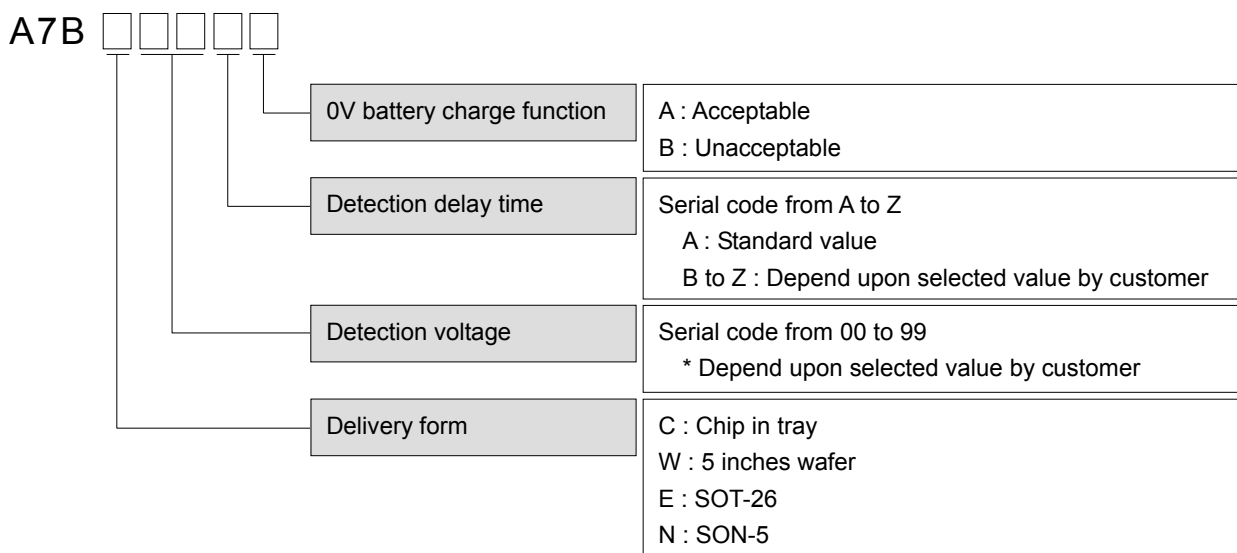
The A7B series are protection ICs for rechargeable Li-ion / Li-polymer battery by high withstand voltage CMOS process. These series protect single-cell Li-ion / Li-polymer battery from over-charge, over-discharge, charge over-current and discharge over-current.



FEATURES

- High accuracy detection voltage Over-charge detection
 - Over-charge hysteresis ±25mV (T_{opr} = 25°C)
 - Over-discharge detection ±30mV (T_{opr} = -5°C ~ +55°C)
 - Charge over-current detection ±25mV
 - Discharge over-current detection ±2.5%
- Selectable detection voltage Over-charge detection 4.0V ~ 4.5V (5mV step)
 - Over-charge hysteresis 0.0V ~ 0.4V (50mV step)
 - Over-discharge detection 2.0V ~ 3.0V (5mV step)
 - Charge over-current detection -0.25V ~ -0.05V (5mV step)
 - Discharge over-current detection 0.05V ~ 0.40V (5mV step)
- Delay time (internal adjustment) Over-charge detection delay time Typ. 1.0s
 - Over-discharge detection delay time Typ. 31.0ms
 - Charge over-current detection delay time Typ. 8.0ms
 - Discharge over-current detection delay time Typ. 8.0ms
 - Load short-circuiting detection delay time Typ. 370μs
 - Release delay time 1 Typ. 2.0ms
 - Release delay time 2 Typ. 16.0ms
- High withstand voltage Absolute maximum rating 28V (VM & CO terminals)
- Low current consumption Operation Typ. 3.0μA
 - Over-discharge condition Max. 0.1μA
- Wide operating temperature range -40°C ~ +85°C
- Selectable 0V battery charging function or 0V battery charge inhibiting function

PRODUCTS NUMBERING GUIDE



STANDARD MODELS LINE-UPS

Model No.	A7BE01AA	A7BE02AA	A7BE03AA	A7BE04AA
Over-charge detection voltage ¹⁾	4.275V	4.280V	4.290V	4.325V
Over-charge hysteresis voltage ²⁾	0.20V	0.20V	0.20V	0.25V
Over-discharge detection voltage ³⁾	2.300V	2.300V	2.300V	2.500V
Charge over-current detection voltage ⁴⁾	-0.100V	-0.100V	-0.100V	-0.150V
Discharge over-current detection voltage ⁵⁾	0.100V	0.100V	0.100V	0.150V
Over-charge detection delay time ⁶⁾	1.0s	1.0s	1.0s	1.0s
Over-discharge detection delay time ⁶⁾	31.0ms	31.0ms	31.0ms	31.0ms
Charge over-current detection delay time ⁶⁾	8.0ms	8.0ms	8.0ms	8.0ms
0V battery charge function	Acceptable	Acceptable	Acceptable	Acceptable

Note : The value of detection voltage and delay time can be changed by customer's request. For details, please contact us.

¹⁾ The over-charge detection voltage can be selected in the range 4.0V to 4.5V in 5mV steps.

²⁾ The over-charge hysteresis voltage can be selected in the range 0.0V to 0.4V in 50mV steps.

³⁾ The over-discharge detection voltage can be selected in the range 2.0V to 3.0V in 5mV steps.

⁴⁾ The charge over-current detection voltage can be selected in the range -0.25V to -0.05V in 5mV steps.

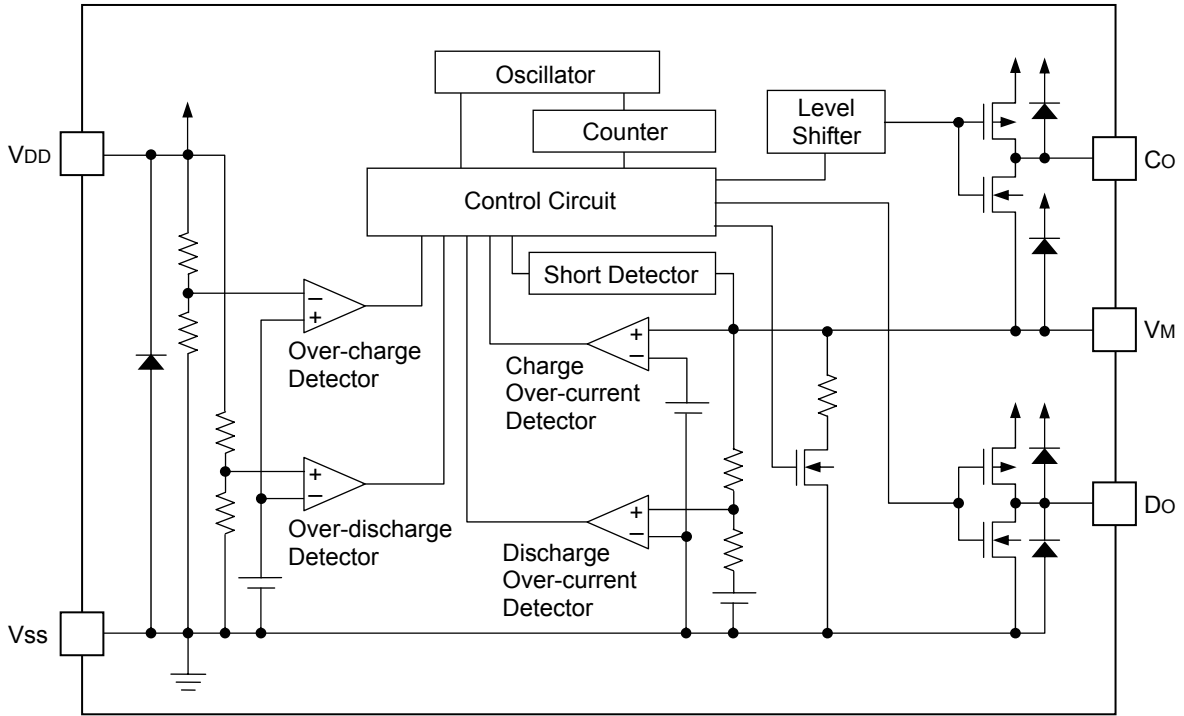
⁵⁾ The discharge over-current detection voltage can be selected in the range 0.05V to 0.40V in 5mV steps.

⁶⁾ The delay time can be changed within the value listed below.

Delay time	Symbol	Selectable value		
Over-charge detection delay time	tc	0.125s	1.0s	3.75s
Over-discharge detection delay time	tdc	31ms	125ms	
Charge over-current detection delay time	tic	8.0ms	125ms	1.0s

* The value in bold is set for standard products

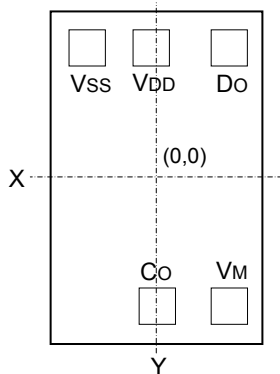
BLOCK DIAGRAM



CHIP PAD CONFIGURATION

(Unit : μm)

No.	Symbol	Descriptions	Chip pad layout	
			X	Y
1	Do	FET gate connection for discharge control (CMOS output)	173.5	428.5
2	VM	Voltage monitoring for charger negative	228.5	-428.5
3	Co	FET gate connection for charge control (CMOS output)	-1.1	-428.5
4	VDD	Positive power input	-37.5	428.5
5	VSS	Negative power input	-228.5	428.5



Chip size : 0.7mm×1.1mm
 Thickness : 0.28mm±0.02mm
 Pad size : 0.085mm×0.085mm
 Chip base level : VDD

ABSOLUTE MAXIMUM RATINGS

Items	Symbol	Ratings	Unit
Supply voltage	V _{DD}	V _{SS} – 0.3 to V _{SS} + 12	V
Input voltage of V _M	V _M	V _{DD} – 28 to V _{DD} + 0.3	V
Output voltage of Co	V _{Co}	V _M – 0.3 to V _{DD} + 0.3	V
Output voltage of Do	V _{Do}	V _{SS} – 0.3 to V _{DD} + 0.3	V
Power dissipation	P _D	250	mW
Operating temperature	T _{opr}	–40 to +85	°C
Storage temperature	T _{stg}	–55 to +125	°C

ELECTRONICAL STATIC DISCHARGE (ESD)

A7B series are equipped ESD protection. However, please keep following conditions for preventing IC from excessive electrical stress.

- Tip of soldering iron, all of tools and testing machines must be connected to an earth plate.
- Power supply must be put first ahead of input signal.
- All input signals must be connected to an earth plate when you do not use IC.
- Do not input beyond absolute maximum ratings even if a moment.

ELECTRICAL CHARACTERISTICS

(Topr=25°C unless otherwise specified)

Items	Symbol	Min.	Typ.	Max.	Conditions	Unit	Test circuit
Detection voltage							
Over-charge detection voltage Vc = 4.0 to 4.5V	Vc	Vc -0.025	Vc	Vc +0.025	R1=330Ω	V	1
		Vc -0.030	Vc	Vc +0.030	R1=330Ω Topr = -5°C to +55°C ¹⁾	V	1
Over-charge hysteresis voltage VHc = 0.0 to 0.4V	VHc	VHc -0.025	VHc	VHc +0.025	R1=330Ω	V	1
Over-discharge detection voltage Vc = 2.0 to 3.0V	Vdc	Vdc ×0.975	Vdc	Vdc ×1.025		V	1
Charge over-current detection voltage Vlc = -0.25 to -0.05V	Vlc	Vlc -0.030	Vlc	Vlc +0.030		V	2
Discharge over-current detection voltage Vldc = 0.05 to 0.40V	Vldc	Vldc -0.020	Vldc	Vldc +0.020		V	2
Load short-circuiting detection voltage	Vshort	-1.7	-1.3	-1.0	Based on VDD, VDD=3.5V	V	2
Input voltage							
Input voltage between VDD and VSS	VDD	1.8	-	8.0	Internal operating voltage	V	-
0V battery charge starting charger voltage	Vcha	-	0.9	1.4	A7BxxxxA	V	3
0V battery charge inhibiting battery voltage	Vinh	0.7	1.2	1.7	A7BxxxxB	V	3
Current consumption							
Current consumption on operation	Iopr	-	3.0	6.0	VDD=3.5V, VM=0V	μA	4
Current consumption on shutdown	Isdn	-	-	0.1	VDD=VM=1.8V	μA	4
Output resistance							
Co : Pch ON resistance	Rcop	1.5	3.0	4.5	Co=3.0V, VDD=3.5V, VM=0V	KΩ	5
Co : Nch ON resistance	Rcon	0.5	1.0	1.5	Co=0.5V, VDD=4.6V, VM=0V	KΩ	5
Do : Pch ON resistance	Rdop	1.7	3.5	5.0	Do=3.0V, VDD=3.5V, VM=0V	KΩ	5
Do : Nch ON resistance	Rdon	1.7	3.5	5.0	Do=0.5V, VDD=VM=1.8V	KΩ	5
Discharge over-current release resistance	Rdwn	15.0	30.0	60.0	VDD=3.5V, VM=1.0V	KΩ	5
Detection delay time							
Over-charge detection delay time tc=0.125s or 1.0s or 3.75s	tc	tc ×0.70	tc	tc ×1.30	VDD=Vc-0.2V→Vc+0.2V, VM=0V	sec	6
Over-discharge detection delay time tdc=31ms or 125ms	tdc	tdc ×0.70	tdc	tdc ×1.30	VDD=Vdc+0.2V→Vdc-0.2V, VM=0V	msec	6
Charge over-current detection delay time tic=8ms or 125ms or 1000ms	tic	tic ×0.70	tic	tic ×1.30	VDD=3.5V, VM=0V→-1.0V	msec	6
Discharge over-current detection delay time	tidc	5.6	8.0	10.4	VDD=3.5V, VM=0V→1.0V	msec	6
Load short-circuiting detection delay time	tshort	190	370	550	VDD=3.5V, VM=0V→3.5V	μsec	6
Release delay time							
Release delay time 1 Over-discharge release Charge over-current release Discharge over-current release Load short-circuiting release	trel1	1.0	2.0	3.0		msec	6
Release delay time 2 Over-charge release	trel2	8.0	16.0	24.0	VDD=Vc+0.2V→Vc-0.2V, VM=1.0V	msec	6

Note :

¹⁾ The specification for this temperature range is guaranteed by design, not tested in production.

MEASUREMENT CONDITIONS

- **Over-charge detection voltage, Over-charge hysteresis voltage --- [Circuit 1]**

Set $V1=3.5V$ and $V2=0V$. Over-charge detection voltage V_c is $V1$ at which V_{Co} goes "Low" from "High" when $V1$ is gradually increased from $3.5V$. Then IC is released from the over-charge state and V_{Co} goes "High" from "Low" at the voltage "Measured V_c-V_{Hc} " when $V1$ is gradually decreased.

If $V2$ is set to the greater value than discharge over-current detection voltage V_{Idc} in the over-charge state, V_{Hc} is canceled and then IC is released from the over-charge state at V_c .

- **Over-discharge detection voltage --- [Circuit 1]**

Set $V1=3.5V$ and $V2=0V$. Over-discharge detection voltage V_{dc} is $V1$ at which V_{Do} goes "Low" from "High" when $V1$ is gradually decreased from $3.5V$. Next, set $V2$ under to charge over-current detection voltage V_{Ic} . Then IC is released from the over-discharge state at V_{dc} and V_{Do} goes "High" from "Low".

- **Charge over-current detection voltage --- [Circuit 2]**

Set $V1=3.5V$ and $V2=0V$. Charge over-current detection voltage V_{Ic} is $V2$ at which V_{Co} goes "Low" from "High" when $V2$ is gradually decreased from $0V$.

- **Discharge over-current detection voltage --- [Circuit 2]**

Set $V1=3.5V$ and $V2=0V$. Discharge over-current detection voltage V_{Idc} is $V2$ at which V_{Do} goes "Low" from "High" when $V2$ is gradually increased from $0V$.

- **Load short-circuiting detection voltage --- [Circuit 2]**

Set $V1=3.5V$ and $V2=0V$. Load short-circuiting detection voltage V_{short} is $V2$ at which V_{Do} goes "Low" from "High" within a time between the minimum and the maximum value of load short-circuiting detection delay time t_{short} , when $V2$ is increased rapidly within $10\mu s$.

- **0V battery charge starting charger voltage --- [Circuit 3]**

Set $V1=V2=0V$ and decrease $V2$ gradually. 0V battery charge starting charger voltage V_{cha} is $V2$ when V_{Co} goes "High" ($V1-0.1V$ or higher).

- **0V battery charge inhibiting battery voltage --- [Circuit 3]**

Set $V1=1.8V$ and $V2=0V$ at first. Then set $V2=V1-4.0V$. Next, decrease $V1$ and $V2$ gradually, maintaining the relation of $V2=V1-4.0V$. 0V battery charge inhibiting battery voltage V_{inh} is $V1$ when V_{Co} goes "Low" ($V2+0.1V$ or lower).

- **Current consumption on operation and shutdown --- [Circuit 4]**

Set $V1=3.5V$ and $V2=0V$ on normal condition. I_{DD} shows current consumption on operation I_{opr} .

Set $V1=V2=1.8V$ on over-discharge condition. I_{DD} shows current consumption on shutdown I_{sdn} .

- **Co : Pch ON resistance, Co : Nch ON resistance --- [Circuit 5]**

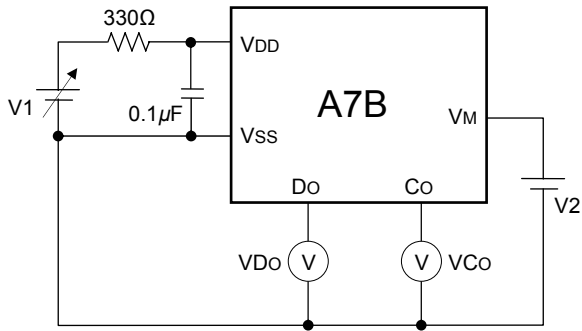
Set $V1=3.5V$, $V2=0V$ and $V3=3.0V$. $(V1-V3)/|I_{Co}|$ is Pch ON resistance R_{cop} .

Set $V1=4.6V$, $V2=0V$ and $V3=0.5V$. $V3/|I_{Co}|$ is Nch ON resistance R_{con} .

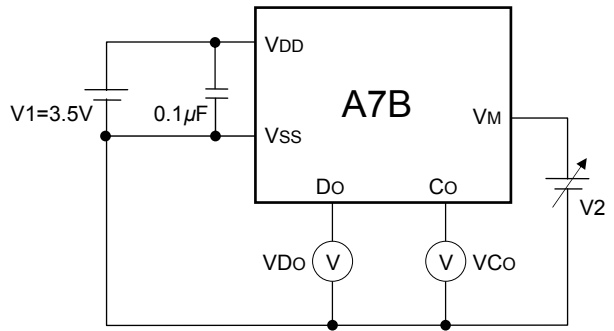
- **Do : Pch ON resistance, Do : Nch ON resistance --- [Circuit 5]**
Set $V1=3.5V$, $V2=0V$ and $V4=3.0V$. $(V1-V4)/|IDo|$ is Pch ON resistance R_{dop} .
Set $V1=V2=1.8V$ and $V4=0.5V$. $V4/|IDo|$ is Nch ON resistance R_{don} .
- **Discharge over-current release resistance --- [Circuit 5]**
Set $V1=3.5V$, $V2=0V$ at first. And then, set $V2=1.0V$. $V2/|IVM|$ is discharge over-current release resistance R_{dwn} .
- **Over-charge detection delay time, Release delay time 2 --- [Circuit 6]**
Set $V2=0V$. Increase $V1$ from the voltage $V_c-0.2V$ to $V_c+0.2V$ rapidly within $10\mu s$. Over-charge detection delay time t_c is the time needed for V_{Co} to go "Low" just after the change of $V1$.
Next, set $V2=1V$ and decrease $V1$ from $V_c+0.2V$ to $V_c-0.2V$ rapidly within $10\mu s$. Over-charge release delay time $t_{rel 2}$ is the time needed for V_{Co} to go "High" just after the change of $V1$.
- **Over-discharge detection delay time, Release delay time 1 --- [Circuit 6]**
Set $V2=0V$. Decrease $V1$ from the voltage $V_{dc}+0.2V$ to $V_{dc}-0.2V$ rapidly within $10\mu s$. Over-discharge detection delay time t_{dc} is the time needed for V_{Do} to go "Low" just after the change of $V1$.
Next, set $V2=-1V$ and increase $V1$ from $V_{dc}-0.2V$ to $V_{dc}+0.2V$ rapidly within $10\mu s$. Release delay time 1 t_{rel1} in case of over-discharge is the time needed for V_{Do} to go "High" just after the change of $V1$.
- **Charge over-current detection delay time, Release delay time 1 --- [Circuit 6]**
Set $V1=3.5V$ and $V2=0V$. Decrease $V2$ from $0V$ to $-1V$ rapidly within $10\mu s$. Charge over-current delay time t_{ic} is the time needed for V_{Co} to go "Low" just after the change of $V2$.
Next, increase $V2$ from $-1V$ to $0V$ rapidly within $10\mu s$. Release delay time 1 t_{rel1} in case of charge over-current is the time needed for V_{Co} to go "High" just after the change of $V2$.
- **Discharge over-current detection delay time, Release delay time 1 --- [Circuit 6]**
Set $V1=3.5V$ and $V2=0V$. Increase $V2$ from $0V$ to $1V$ rapidly within $10\mu s$. Discharge over-current delay time t_{dc} is the time needed for V_{Do} to go "Low" just after the change of $V2$.
Next, decrease $V2$ from $1V$ to $0V$ rapidly within $10\mu s$. Release delay time 1 t_{rel1} in case of discharge over-current is the time needed for V_{Do} to go "High" just after the change of $V2$.
- **Load short-circuiting detection delay time, Release delay time 1 --- [Circuit 6]**
Set $V1=3.5V$ and $V2=0V$. Increase $V2$ from $0V$ to $3.5V$ rapidly within $10\mu s$. Load short-circuiting detection delay time t_{short} is the time needed for V_{Do} to go "Low" just after the change of $V2$. Next, decrease $V2$ from $3.5V$ to $0V$ rapidly within $10\mu s$. Release delay time 1 t_{rel1} in case of load short-circuiting is the time needed for V_{Do} to go "High" just after the change of $V2$.

MEASUREMENT CIRCUITS

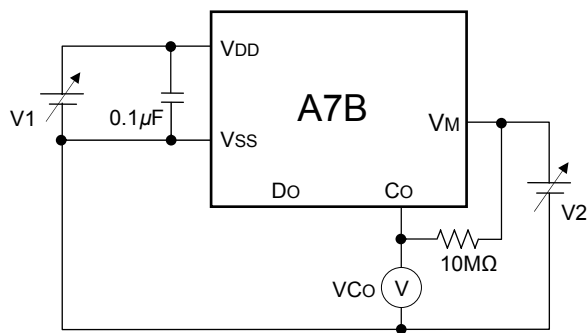
● **Circuit 1**



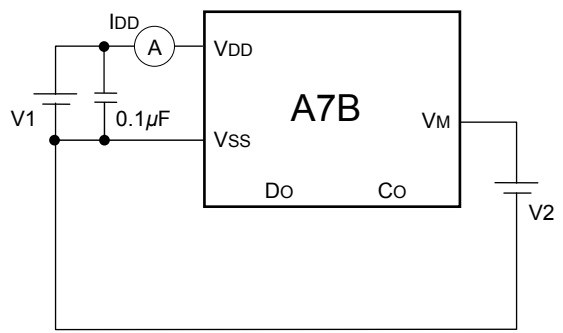
● **Circuit 2**



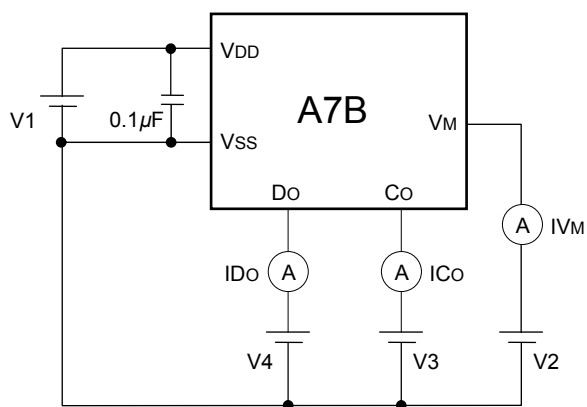
● **Circuit 3**



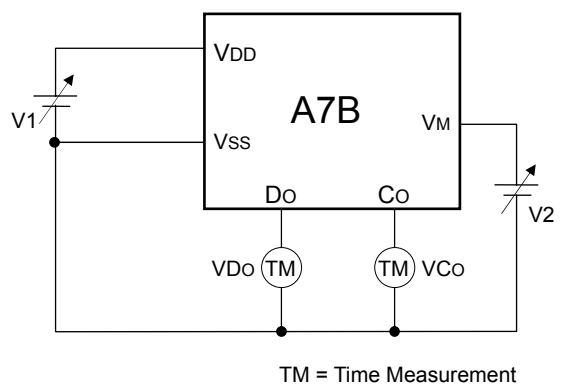
● **Circuit 4**



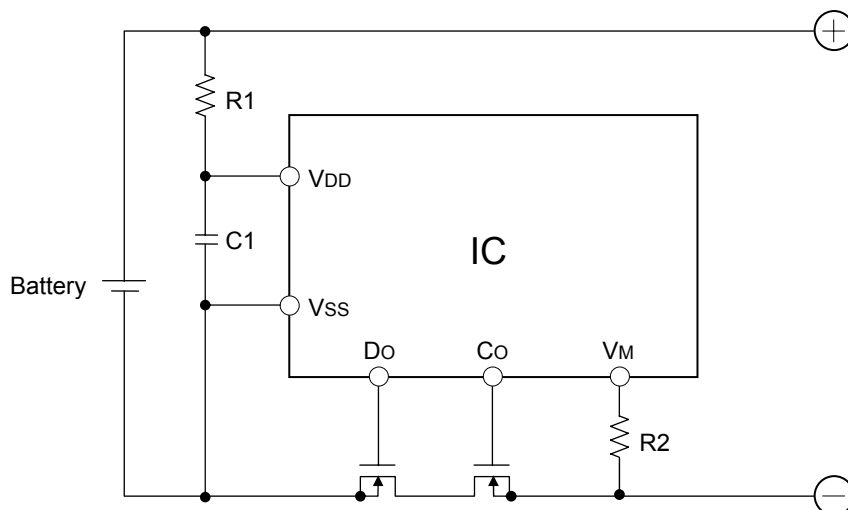
● **Circuit 5**



● **Circuit 6**



TYPICAL CONNECTION DIAGRAM



EXTERNAL COMPONENTS

Items	Symbol	Recommended value	Min.	Max.
Resistor 1	R1	330Ω	100Ω	1.0KΩ
Capacitor 1	C1	0.1μF	0.01μF	1.0μF
Resistor 2	R2	3.9KΩ	500Ω	6.0KΩ

- The supply voltage (VDD) to this IC is stabilized by R1 and C1. Moreover, R1 and R2 act as the current restriction resistances at the time of reverse-connecting a charger, or at the time of connecting a charger which outputs the voltage exceeding the absolute maximum rating of this IC. Please be sure to connect these components.
- If the value of R1 is too large, the over-charge detection voltage and the over-discharge detection voltage will become high due to the current consumption of this IC. Please use the value within the limits shown in the table. 330Ω is recommended.
- If the value of C1 is too small, this IC may be in a shutdown state at the time of the discharge over-current or the load short-circuiting. Please use the value within the limits shown in the table for stable operation. 0.1μF is recommended.
- Please use the value within the limits shown in the table about the value of R2. In order to reduce the current at the time of reverse-connecting a charger, we recommend you to choose R1 and R2 so that the sum total become more than 4KΩ. The recommended value of R2 is 3.9KΩ.

Note)

The connection diagram and each value of external components shown above are just recommendation. Including a battery and FETs, please determine the circuit after sufficient evaluation about your actual application.

DESCRIPTION OF OPERATION

● Normal condition

This IC monitors the battery voltage (V_{DD}) and the voltage of V_M terminal, and controls charge and discharge.

If the battery voltage (V_{DD}) is in the range from the over-discharge detection voltage (V_{dc}) to the over-charge detection voltage (V_c) and the V_M terminal voltage is in the range from the charge over-current detection voltage (V_{lc}) to the discharge over-current detection voltage (V_{ldc}), this IC turns on both the charge and discharge control FETs. This state is called the normal condition, and charge and discharge are possible together.

● Discharge over-current detection, Load short-circuiting detection

When the discharge current becomes equal to or higher than the specified value under the normal condition, and if the V_M terminal voltage is in the range from the discharge over current detection voltage (V_{ldc}) to the short-circuiting detection voltage (V_{short}) and that state is maintained during more than the discharge over-current detection delay time (t_{ldc}), this IC turns off the discharge control FET to stop discharge. This state is called the discharge over-current condition.

At that time, if the V_M terminal voltage is equal to or higher than V_{short} and that state is maintained during more than the load short-circuiting detection delay time (t_{short}), this IC turns off the discharge control FET to stop discharge. This state is called the load short-circuiting detection condition.

While load is connected, in both conditions, the V_M terminal voltage equals to V_{DD} potential due to the load, but it falls by the discharge over-current release resistance (R_{dwn}) when the load is removed and the resistance between (+) and (-) terminals of battery pack (refer to "TYPICAL CONNECTION DIAGRAM") becomes larger than the value which enables the automatic return.

Then the V_M terminal voltage becomes less than V_{ldc} , and if that state is maintained during more than the release delay time 1 (t_{rel1}), this IC returns to normal condition.

Note)

The resistance value between (+) and (-) terminals of battery pack for automatic return changes with battery voltage (V_{DD}) or V_{ldc} . The standard is expressed with the following equation.

$$\text{Resistance value for automatic return} = R_{dwn} \times (V_{DD} / V_{ldc} - 1)$$

● Charge over-current detection

When the charge current becomes equal to or higher than the specified value under the normal condition, if the V_M terminal voltage becomes less than the charge over-current detection voltage (V_{lc}) and that state is maintained during more than the charge over-current detection delay time (t_{lc}), this IC turns off the charge control FET to stop charge. This state is called the charge over-current detection condition.

Then the V_M terminal voltage becomes equal to or higher than V_{lc} and that state is maintained during more than the release delay time 1 (t_{rel1}) when the charger is removed and the load is connected, this IC returns to the normal condition.

Note)

If the V_M terminal voltage becomes equal to or less than $V_{SS}-7V$ (typical), the charge over-current detection delay time (t_{lc}) changes as below.

8msec model	→	8msec (not changed)
125msec model	→	7msec (typical)
1.0sec model	→	56msec (typical)

- **Over-charge detection**

When the battery voltage (V_{DD}) under the normal condition becomes equal to or higher than the over-charge detection voltage (V_c) and that state is maintained during more than the over-charge detection delay time (t_c), this IC turns off the charge control FET and stops charge. This state is called the over-charge detection condition. Release from the over-charge detection condition includes following three cases.

- (1) When V_{DD} falls to $V_c - V_{Hc}$ without load and that state is maintained during more than the delay time 2 (t_{rel2}), this IC turns on the charge control FET and returns to the normal condition.
 - * **V_{Hc} : Over-charge hysteresis voltage**
- (2) When the load is installed and discharge starts, the discharge current flows through the internal parasitic diode of the charge control FET. Then the V_M terminal voltage rises to only the V_f voltage of the internal parasitic diode from V_{SS} potential. At this time, if the V_M terminal voltage is higher than the discharge over-current detection voltage (V_{Idc}) and V_{DD} is equal to or less than V_c , this IC returns to the normal condition when this state continues more than the delay time 2 (t_{rel2}).
- (3) In case (2), if the V_M terminal voltage is higher than the discharge over-current detection voltage (V_{Idc}) and V_{DD} is equal to or higher than V_c , battery is discharged until V_{DD} becomes less than V_c , and then this IC returns to the normal condition when this state continues more than the delay time 2 (t_{rel2}).

- **Over-discharge detection**

When the battery voltage (V_{DD}) under the normal condition becomes equal to or less than the over-discharge detection voltage (V_{dc}) and that state is maintained during more than the over-discharge detection delay time (t_{dc}), this IC turns off the discharge control FET and stops discharge. This state is called the over-discharge detection condition. The over-discharge detection condition is released when the charger is connected and following three cases are included.

- (1) When the charger is connected and charge starts, the charge current flows through the internal parasitic diode of the discharge control FET. V_{DD} is higher than V_{dc} and that state is maintained during more than the delay time 1 (t_{rel1}), this IC is released from over-discharge detection condition automatically and returns to the normal condition.
- (2) In case (1), if V_{DD} is less than V_{dc} , this IC returns to the normal condition when V_{DD} becomes equal to or higher than V_{dc} and this state continues more than the delay time 1 (t_{rel1}).
- (3) Although there is very little possibility, in case (1), if the V_M terminal voltage is higher than the charge over-current detection voltage (V_{Ic}) even if the charge current flows through the internal parasitic diode of the discharge control FET, this IC returns to the normal condition when V_{DD} becomes equal to or higher than $V_{dc} + V_{Hdc}$ and this state continues more than delay time 1 (t_{rel1}).

* **$V_{Hdc} = 0.4V$ (typical)** ---- This voltage is tested in production, but is not specified.

This IC stops all internal circuits (Shutdown condition) after detecting the over-discharge and reduces current consumption. (Max $0.1\mu A$, at $V_{DD}=1.8V$)

- **Charge to 0V battery**

- (1) **0V battery charge function**

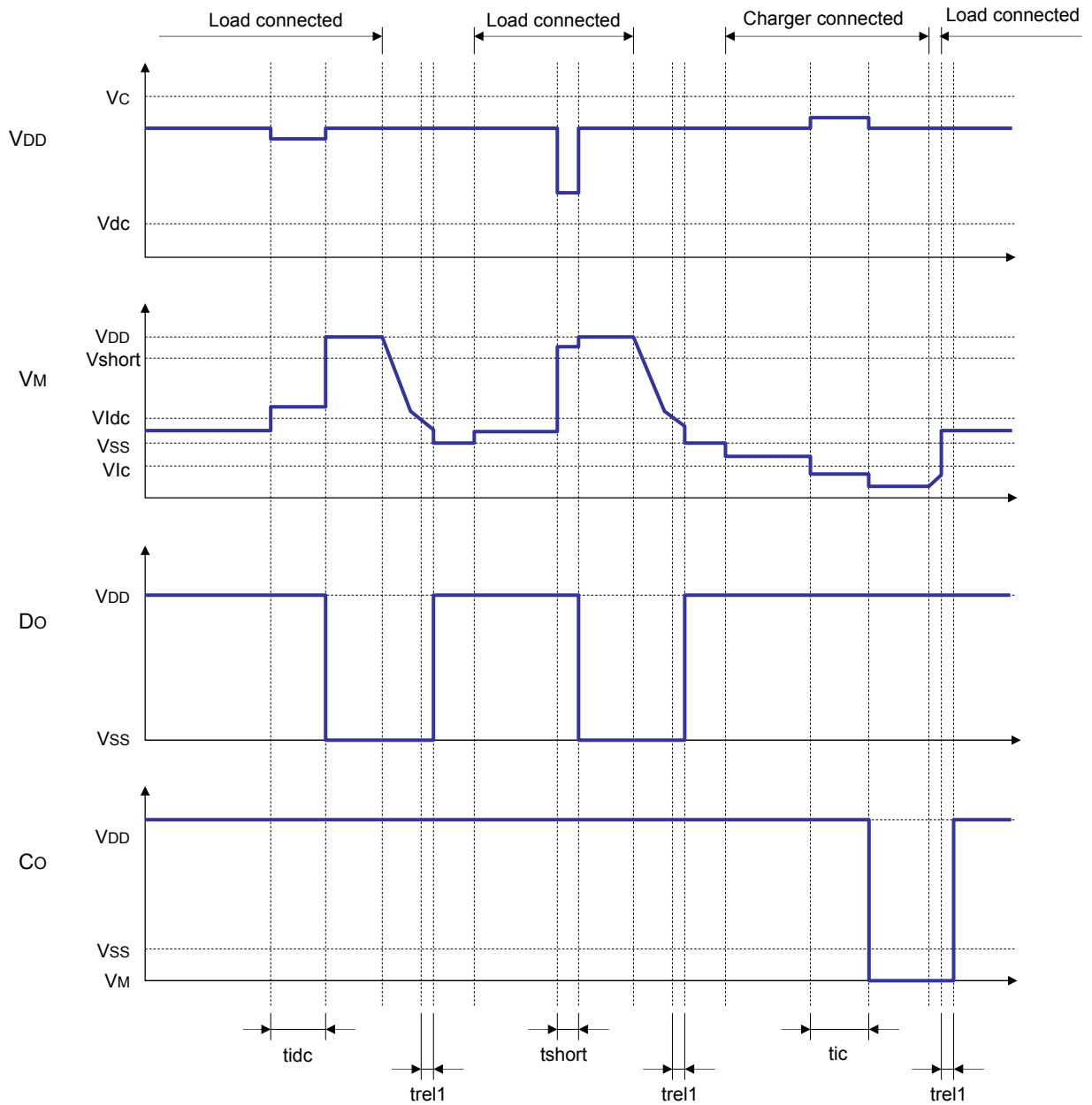
If the voltage of charger (the voltage between V_{DD} and V_M) is larger than the 0V battery charge starting charger voltage (V_{cha}), 0V battery charge becomes possible when C_o terminal outputs V_{DD} terminal potential and turns on the charge control FET.

- (2) **0V battery charge inhibiting function**

If the voltage of the battery (V_{DD}) is equal to or less than the 0V battery charge inhibiting battery voltage (V_{inh}), charge is inhibited when C_o terminal outputs V_M terminal potential and turns off a charge control FET.

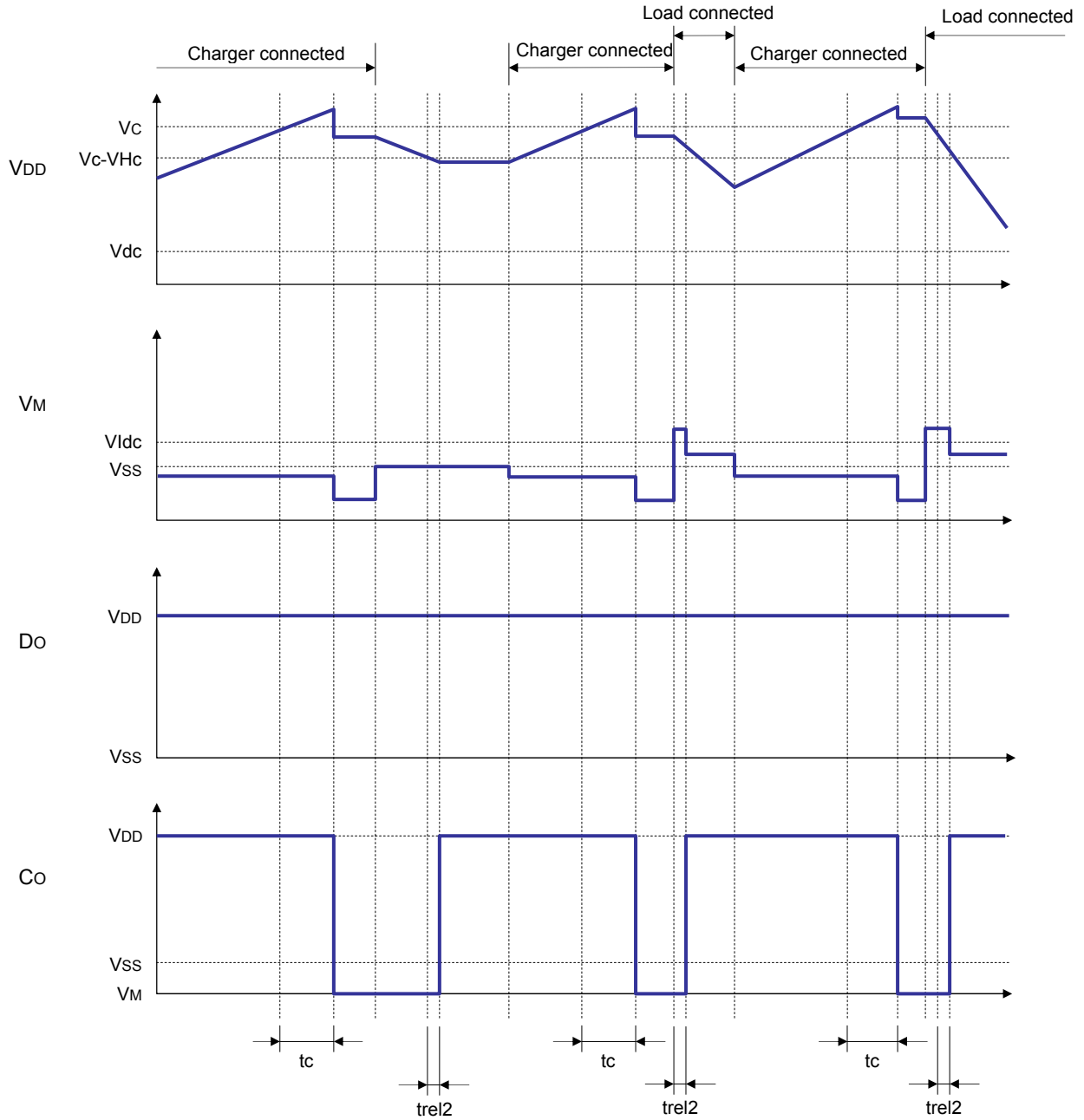
TIMING CHART

- Discharge over-current detection, Load short-circuiting detection, Charge over-current detection



Vc : Over-charge detection voltage	t _{ic} : Charge over-current detection delay time
Vdc : Over-discharge detection voltage	t _{idc} : Discharge over-current detection delay time
Vlc : Charge over-current detection voltage	t _{short} : Load short-circuiting detection delay time
Vldc : Discharge over-current detection voltage	t _{rel1} : Release delay time 1
Vshort : Load short-circuiting detection voltage	

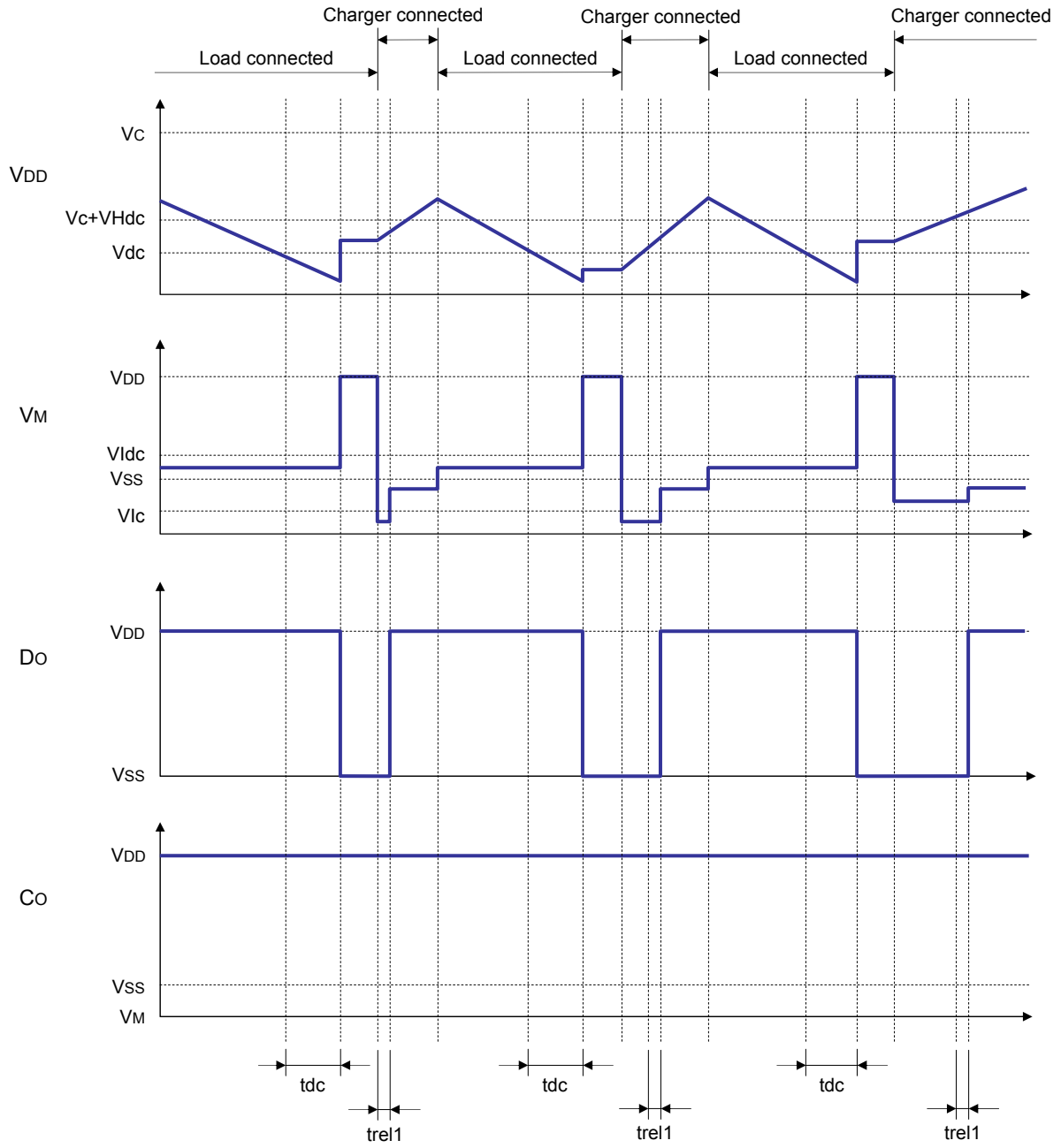
● Over-charge detection



V_c : Over-charge detection voltage
 V_{dc} : Over-discharge detection voltage
 V_{Hc} : Over-charge hysteresis voltage
 V_{Idc} : Discharge over-current detection voltage

t_c : Over-charge detection delay time
 t_{rel2} : Release delay time 2

● **Over-discharge detection**

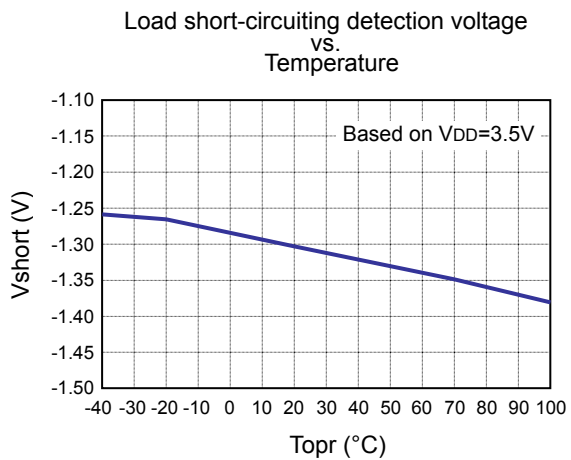
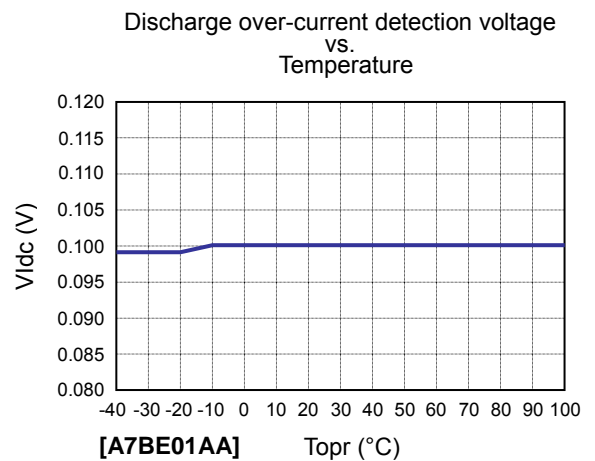
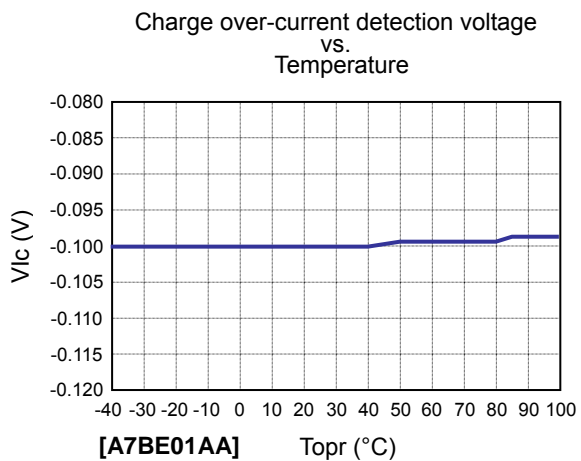
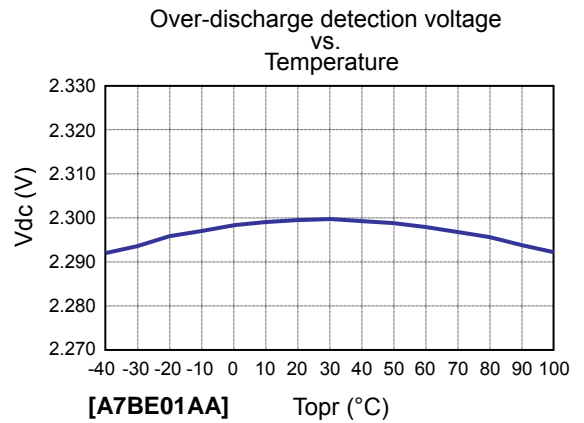
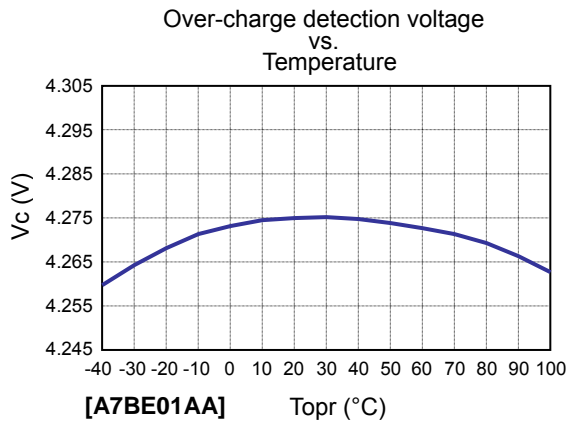


V_c : Over-charge detection voltage
 V_{dc} : Over-discharge detection voltage
 V_{Hdc} : 0.4V (typical)
 V_{Ic} : Charge over-current detection voltage
 V_{Idc} : Discharge over-current detection voltage

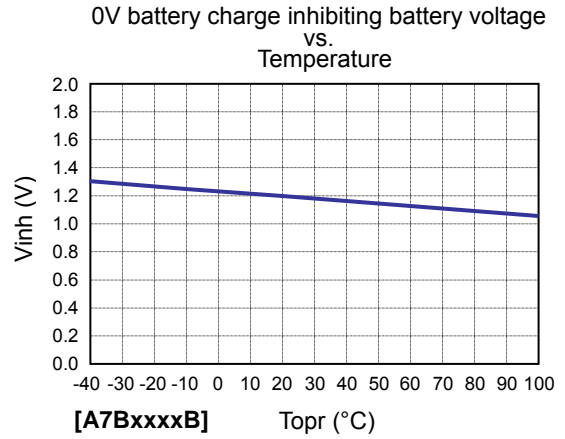
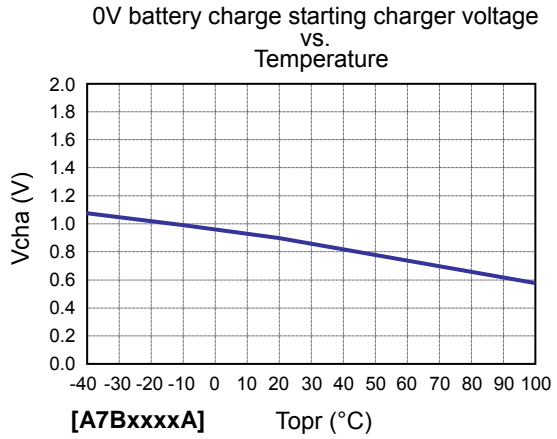
t_{dc} : Over-discharge detection delay time
 t_{rel1} : Release delay time 1

TYPICAL CHARACTERISTICS

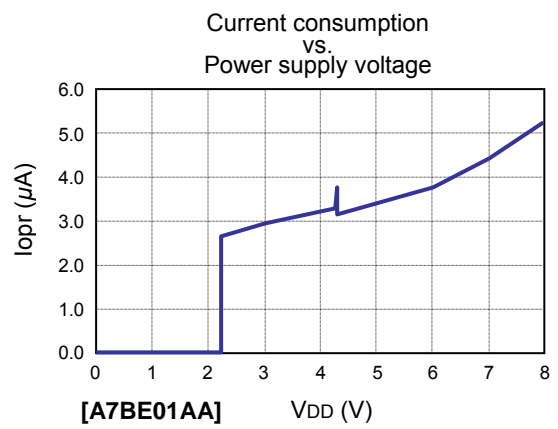
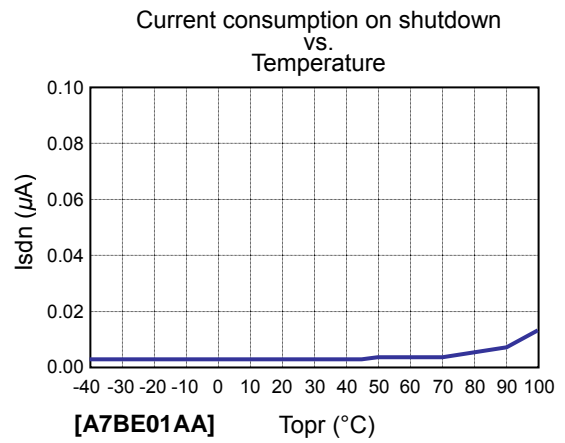
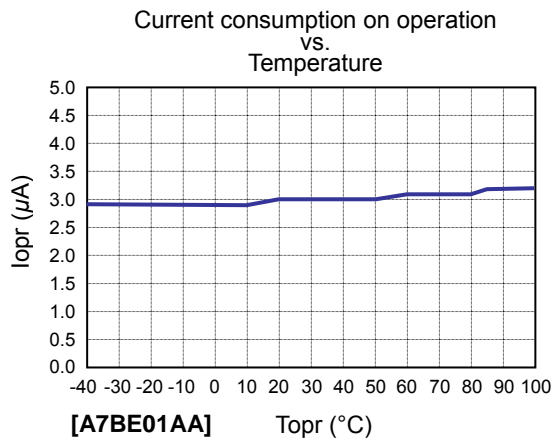
- Detection voltage



● **0V battery charge function**

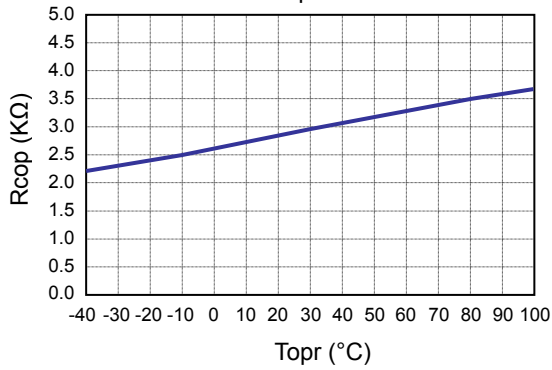


● **Current consumption**

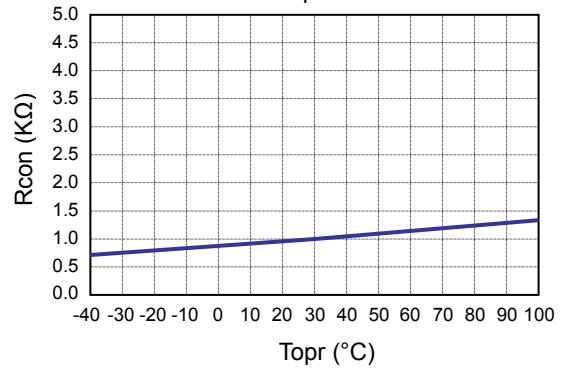


● Resistance

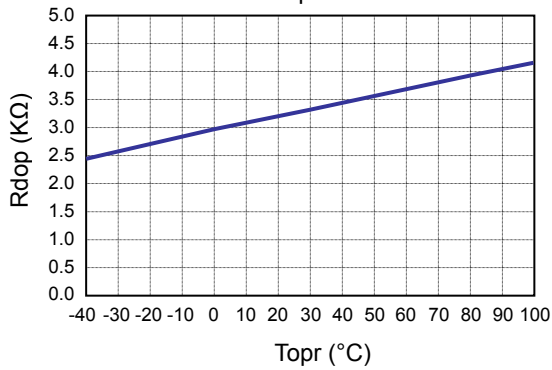
Co terminal Pch ON resistance vs. Temperature



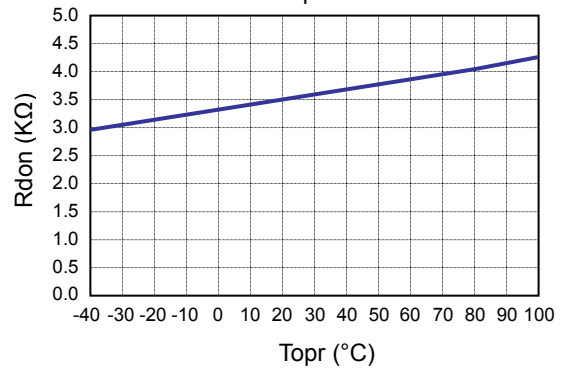
Co terminal Nch ON resistance vs. Temperature



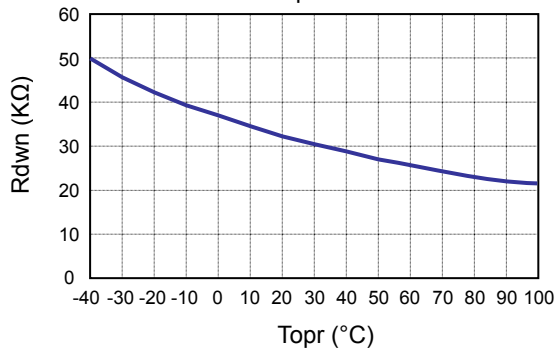
Do terminal Pch ON resistance vs. Temperature



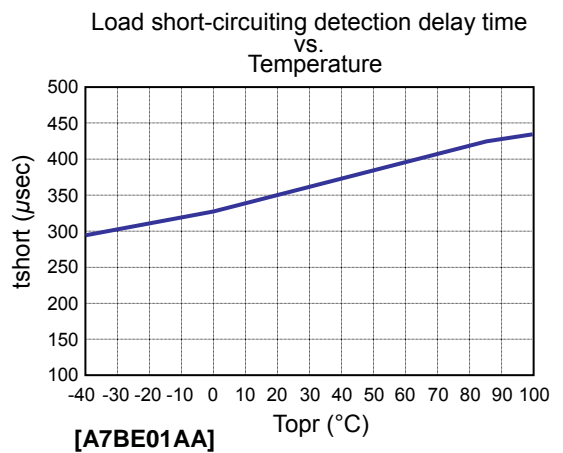
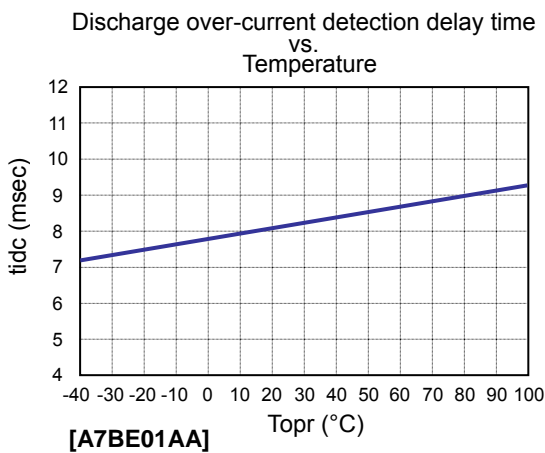
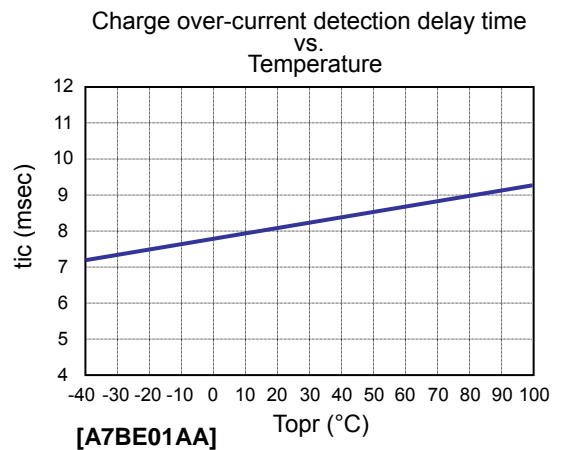
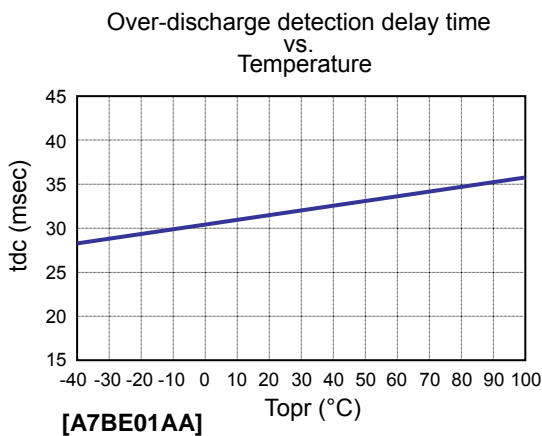
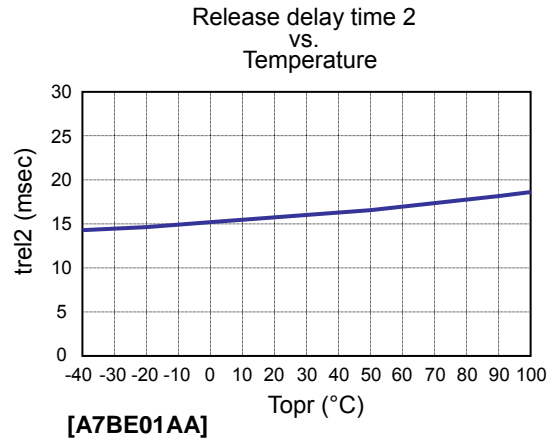
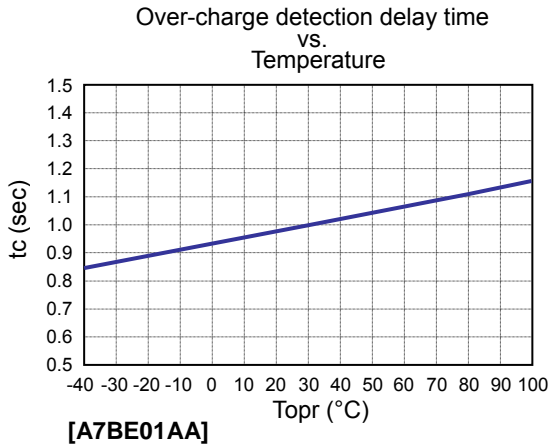
Do terminal Nch ON resistance vs. Temperature

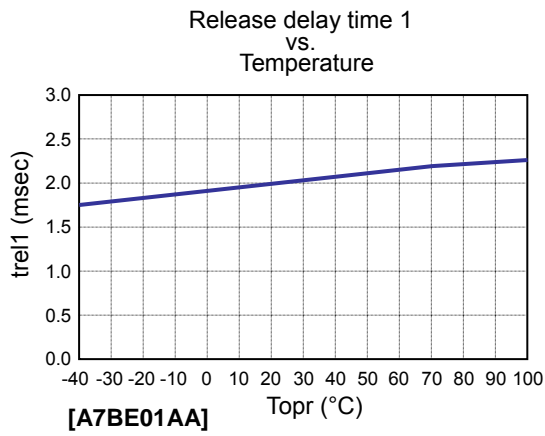


Discharge over-current release resistance vs. Temperature

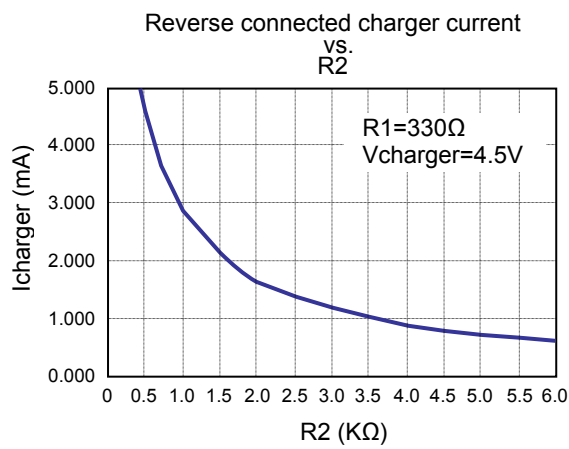
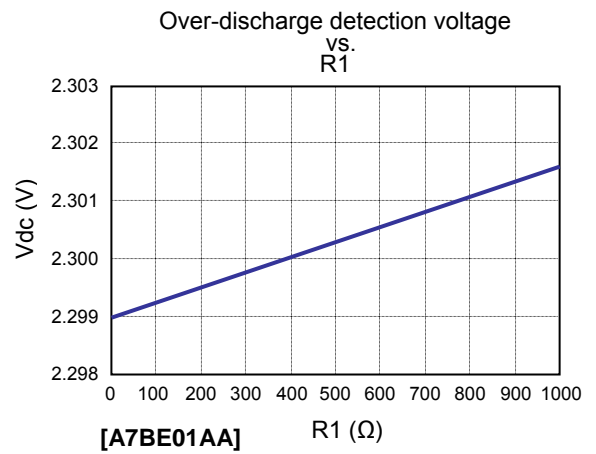
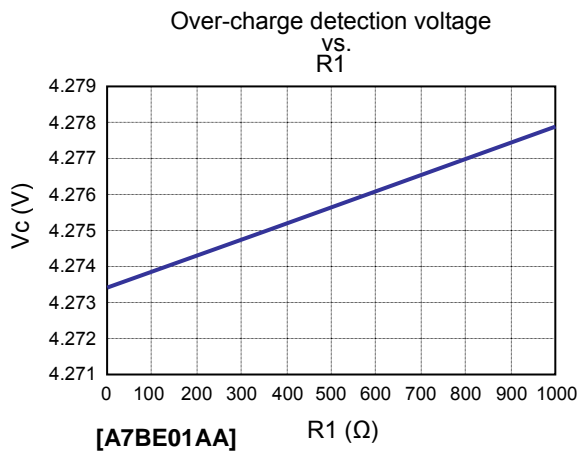


● Delay time

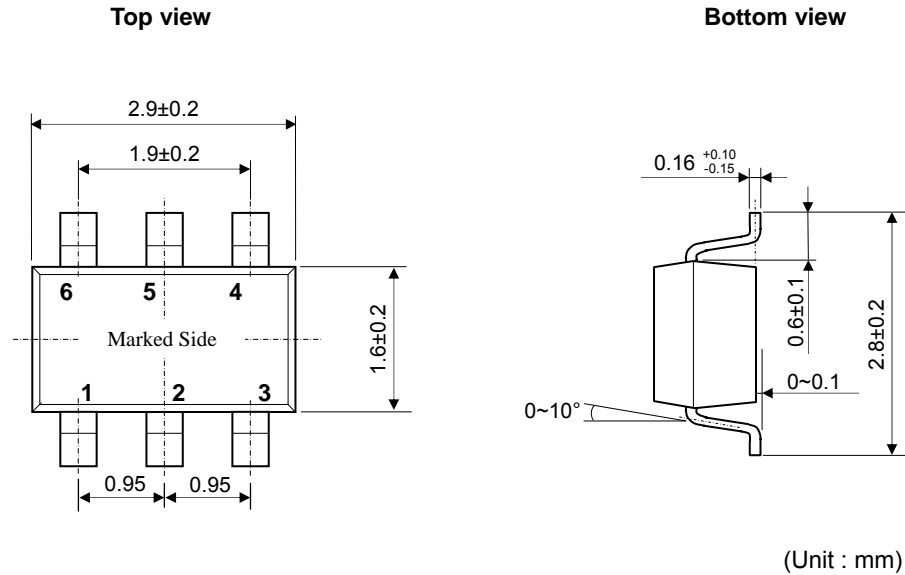




● Characteristics related to the value of external components

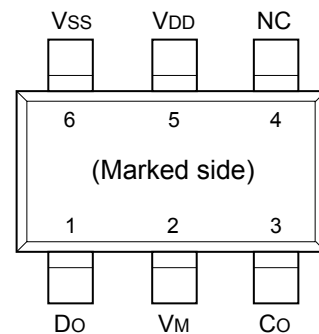


PACKAGE DIMENSIONS (SOT-26)

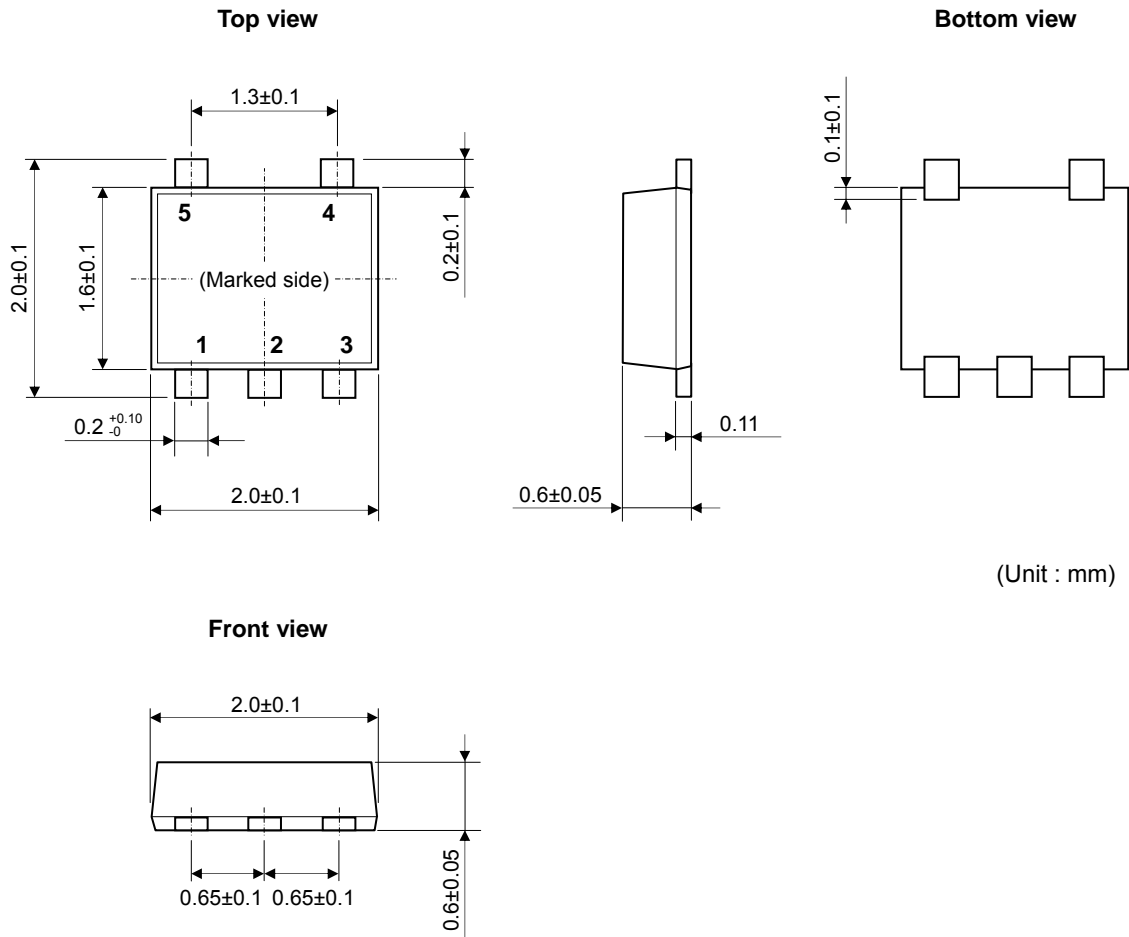


PIN CONFIGURATION

Pin No.	Symbol	Descriptions
1	Do	FET gate connection for discharge control
2	VM	Voltage monitoring for charger negative
3	Co	FET gate connection for charge control
4	NC	N/C
5	VDD	Positive power input
6	VSS	Negative power input



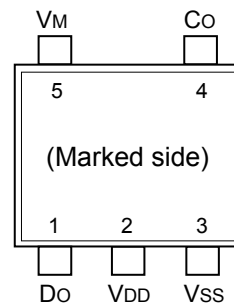
PACKAGE DIMENSIONS (SON-5)

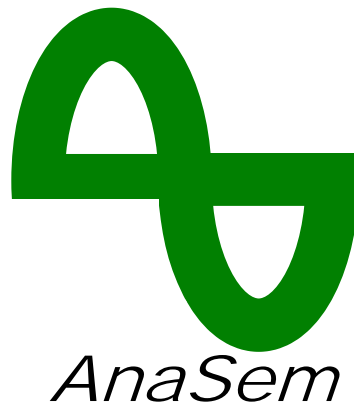


(Unit : mm)

PIN CONFIGURATION

Pin No.	Symbol	Descriptions
1	Do	FET gate connection for discharge control
2	VDD	Positive power input
3	VSS	Negative power input
4	Co	FET gate connection for charge control
5	VM	Voltage monitoring for charger negative





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