

# CERAMIC SMD CRYSTAL CLOCK OSCILLATOR WITH VOLTAGE CONTROL



7.0 x 5.0 x 1.8mm

ALVD



## FEATURES:

- Based on a proprietary digital multiplier
- Tri-State Output
- Low Phase Jitter
- 3.3V +/- 5% operation
- Ceramic SMD, low profile package

## APPLICATIONS:

- SONET, xDSL
- SDH, CPE
- STB

## STANDARD SPECIFICATIONS:

### PARAMETERS

ABRACON P/N:	ALVD Series
Frequency range:	750 KHz to 800 MHz
Operating temperature:	0°C to +70°C (see options)
Storage temperature:	-55°C to +125°C
Overall frequency stability:	±50 ppm max. (see options)
Supply voltage (V <sub>dd</sub> ):	3.3V ± 10%
Voltage control (V <sub>c</sub> ):	0.3VDC min, 1.65VDC typ, 3.0 VDC max.
Symmetry at 1/2 V <sub>dd</sub> :	40/60% max.
Output Level:	See options (PECL, CMOS, or LVDS)
Pullability:	± 50ppm (see option)
Tristate Function:	"1" (V <sub>IH</sub> >= 0.7* V <sub>dd</sub> ) or open: Oscillation "0" (V <sub>IL</sub> < 0.3* V <sub>dd</sub> ) : Hi Z
Aging per year:	±5 ppm max.
RMS Phase Jitter:	3ps typical, 5ps max. (12KHz~20MHz)
Period Jitter (peak to peak):	35 ps typical
Phase Noise:	-112 dBc/Hz @ 1kHz Offset from 155.52MHz -125 dBc/Hz @ 10kHz Offset from 155.52MHz -123 dBc/Hz @ 100kHz Offset from 155.52MHz -109 dBc/Hz @ 1kHz Offset from 622.08MHz -110 dBc/Hz @ 10kHz Offset from 622.08MHz -109 dBc/Hz @ 100kHz Offset from 622.08MHz

#### PECL:

Supply current (I<sub>DD</sub>): 25mA max (for Fo<24MHz), 65mA max (for 24MHz<Fo<96MHz), 100mA max (96MHz<Fo<700MHz)  
Output Logic High: V<sub>dd</sub>-1.025V min, V<sub>dd</sub>-0.880V max.  
Output Logic Low: V<sub>dd</sub>-1.810V min, V<sub>dd</sub>-1.620V max.  
Symmetry (Duty Cycle): 45% min, 50% typ, 55% max,  
Rise time: 0.6nSec typ, 1.5nS max  
Fall time: 0.6nSec typ, 1.5nS max

#### CMOS:

Supply current (I<sub>DD</sub>): 15mA max (for Fo<24MHz), 30mA max (for 24MHz<Fo<96MHz), 40mA max (96MHz<Fo<700MHz)  
Output Clock Rise/ Fall Time [10%~90% VDD with 10pF load]: 1.2ns typ, 1.6ns max.  
Output Clock Duty Cycle [Measured @ 50% VDD]: 45% min, 50% typical, 55% max

#### LVDS:

Supply current (I<sub>DD</sub>): 25mA max (for Fo<24MHz), 45mA max (for 24MHz<Fo<96MHz), 80mA max (96MHz<Fo<700MHz)  
Output Clock Duty Cycle @ 1.25V: 45% min, 50% typical, 55% max  
Output Differential Voltage (V<sub>OD</sub>): 247mV min, 355mV typical, 454mV max  
VDD Magnitude Change (? V<sub>OD</sub>): -50mV min, 50mV max  
Output High Voltage : V<sub>OH</sub> = 1.4V typical, 1.6V max.  
Output Low Voltage: V<sub>OL</sub> = 0.9V min, 1.1V typical  
Offset Voltage [R<sub>L</sub> = 100? : V<sub>OS</sub> = 1.125V min, 1.2V typical, 1.375V max  
Offset Magnitude Change [R<sub>L</sub> = 100? : ΔV<sub>OS</sub> = 0mV min, 3mV typical, 25mV max  
Power-off Leakage (I<sub>OXD</sub>) [V<sub>out</sub>=VDD or GND, VDD=0V] = ±10μA typical, ±10μA max.  
Differential Clock Rise Time (t<sub>r</sub>) [R<sub>L</sub>=100? , CL=10pF]: 0.2nS min, 0.7nS typical, 1.0nS,max  
Differential Clock Fall Time (t<sub>f</sub>) [R<sub>L</sub>=100? , CL=10pF]: 0.2nS min, 0.7nS typical, 1.0nS max



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## PIN ASSIGNMENTS

PIN #	Name	DESCRIPTION
1	V <sub>c</sub>	Voltage Control
2	Tristate	Tristate
3	GND	Ground
4	Q	PECL, LVDS, or CMOS Output.
5	Q	Complimentary PECL, LVDS, or NC.
6	V <sub>DD</sub>	VDD Connection.

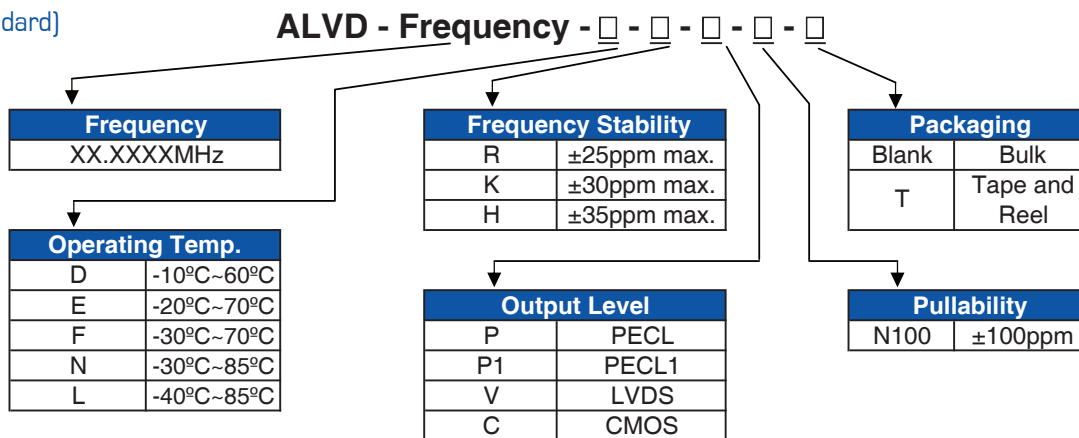
## TRI-STATE PIN OPERATION:

OUTPUT TYPE OPTION		PIN 2 logic level*	Output State (Tri-state)
P	PECL	0 (Default)	Enabled
		1	Disabled
P1	PECL1	0	Disabled
		1	Enabled
V	LVDS	0	Disabled
		1 (Default)	Enabled
C	CMOS	0	Disabled
		1 (Default)	Enabled

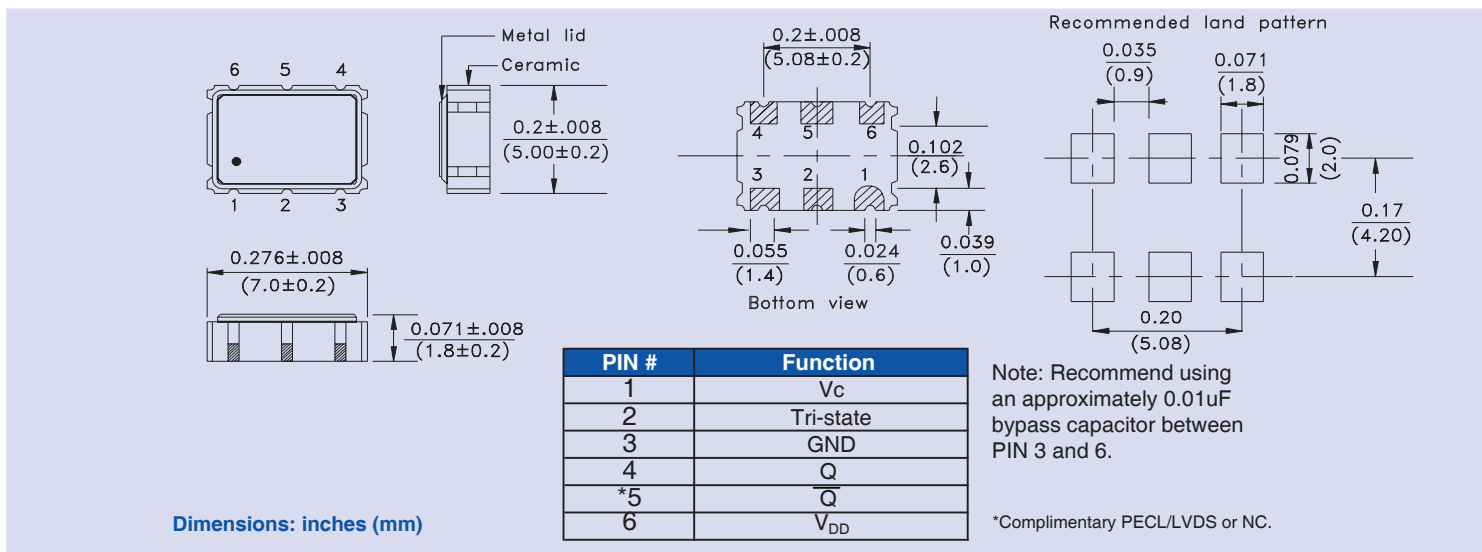
\*Connect to VDD for logic level "1", connect to ground for logic level "0".

## OPTIONS & PART IDENTIFICATION:

(Left blank if standard)



## OUTLINE DRAWING:



# CERAMIC SMD CRYSTAL CLOCK OSCILLATOR WITH VOLTAGE CONTROL

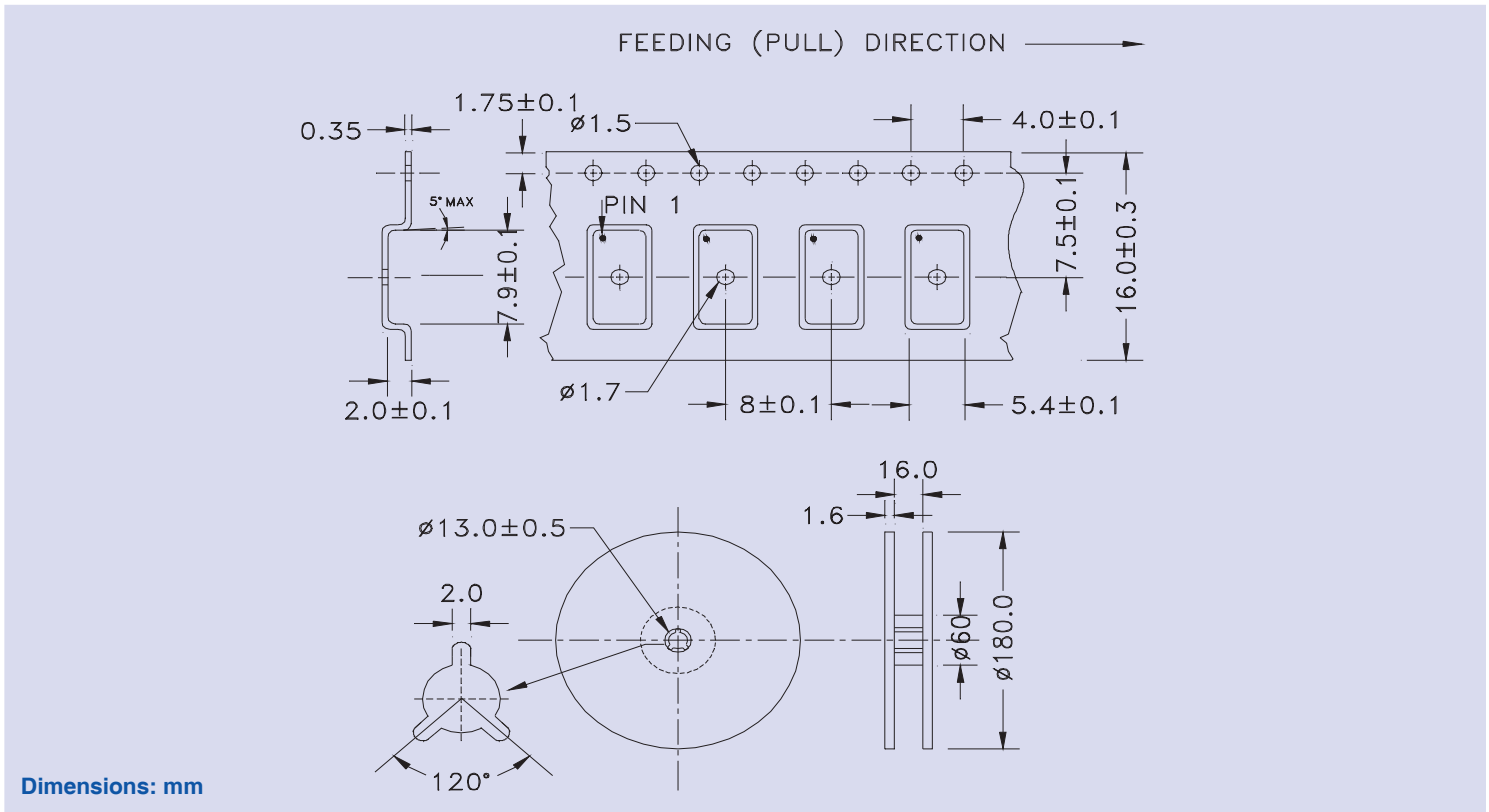


7.0 x 5.0 x 1.8mm

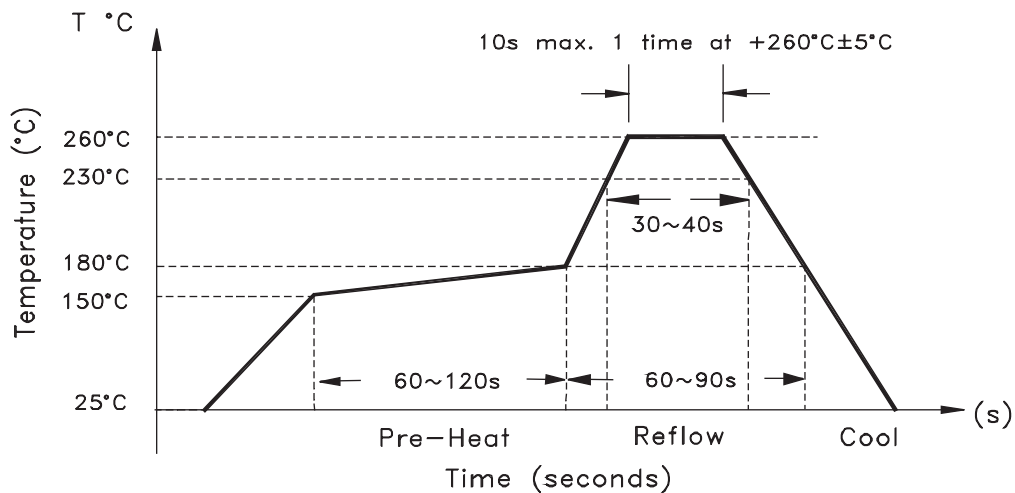


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➤ **TAPE & REEL:** Tape and reel (1,000pcs/reel)



➤ **REFLOW PROFILE:**



**NOTE:** Abracon manufactured products are intended for general commercial and industrial use. For applications requiring high reliability and/or presenting extreme operating environment, written consent & authorization from Abracon is required.

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