80W Power Packaged Transistor

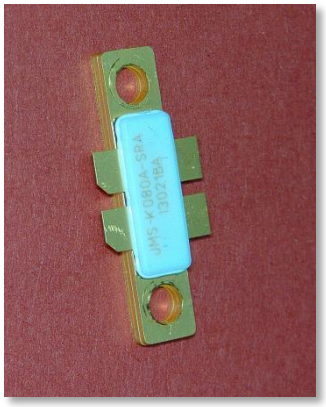
GaN HEMT on SiC

Description

The CHK080A-SRA is an unmatched Packaged Gallium Nitride High Electron Mobility Transistor. It offers general purpose and broadband solutions for a variety of RF power applications. It is well suited for multi-purpose applications such as radar and telecommunication.

The CHK080A-SRA is developed on a 0.5µm gate length GaN HEMT process. It requires an external matching circuitry.

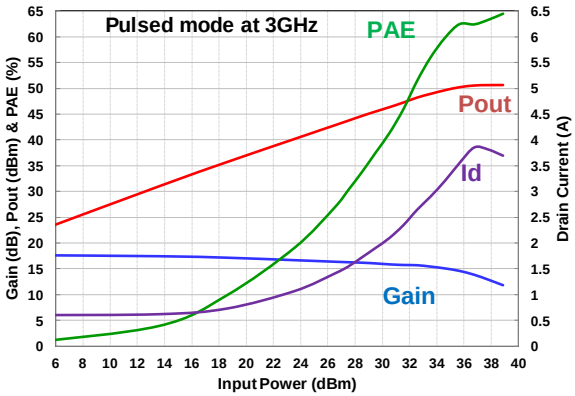
The CHK080A-SRA is available in a ceramic-metal flange power package providing low parasitic and low thermal resistance.



Main Features

- Wide band capability: up to 3.5GHz
- Pulsed and CW operating modes
- High power : > 80W
- High Efficiency : up to 70%
- DC bias: V_{DS} =50V @ I_{D_Q} =600mA
- MTTF > 10^6 hours @ Tj=200°C
- RoHS Flange Ceramic package

V_{DS} = 50V, I_{D_Q} = 600mA, Freq=3GHz
Pulsed mode



Intrinsic performances of the package device

Main Electrical Characteristics

Tcase= +25°C, **Pulsed mode**, F=3GHz, V_{DS}=50V, I_{D_Q}=600mA (I_{D_Q} =300mA on each transistor)

Symbol	Parameter	Min	Typ	Max	Unit
G_{SS}	Small Signal Gain		17	-	dB
P_{SAT}	Saturated Output Power	80	100	-	W
PAE	Max Power Added Efficiency	50	65	-	%
G_{PAE_MAX}	Associated Gain at Max PAE		13	-	dB

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Recommended DC Operating Ratings

Tcase= +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{DS}	Drain to Source Voltage	20		50	V	
V_{GS_Q}	Gate to Source Voltage		-1.8		V	V_D=50V, I_{D_Q}=600mA (I_{D_Q} =300mA on each transistor)
I_{D_Q}	Quiescent Drain Current		0.6	2	A	V_D=50V
I_{D_MAX}	Drain Current		4	(1)	A	V_D=50V, Compressed mode
I_{G_MAX}	Gate Current (forward mode)		0	48	mA	Compressed mode
T_{j_max}	Junction Temperature			200	°C	

(1) Limited by dissipated power

DC Characteristics

Tcase= +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_P	Pinch-Off Voltage	-3	-2	-1	V	V_D=50V, I_D=I_{DSS}/100
I_{D_SAT}	Saturated Drain Current		16 (1)		A	V_D=7V, V_G=2V
I_{G_leak}	Gate Leakage Current (reverse mode)	-6			mA	V_D=50V, V_G=-7V
V_{BDS}	Drain-Source Break-down Voltage		200		V	V_G=-7V, I_D=20mA
R_{TH}	Thermal Resistance		1.8		°C/W	CW Mode

(1) For information, limited by I_{D_MAX} , see on Absolute Maximum Ratings

RF Characteristics (CW)

Tcase= +25°C, **CW mode**, F=3GHz, V_{DS}=50V, I_{D_Q}=600mA (I_{D_Q} =300mA on each transistor)

Symbol	Parameter	Min	Typ	Max	Unit
G_{SS}	Small Signal Gain	14	16		dB
P_{SAT}	Saturated Output Power	70	80		W
PAE	Max Power Added Efficiency	45	50		%
G_{PAE_MAX}	Associated Gain at Max PAE		12		dB

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RF Characteristics (Pulsed)

Tcase= +25°C, **Pulsed mode** (1), F=3GHz, V_D=50V, I_{D_Q}=600mA (I_{D_Q} =300mA on each transistor)

Symbol	Parameter	Min	Typ	Max	Unit
G_{SS}	Small Signal Gain	15	17		dB
P_{SAT}	Saturated Output Power	80	100		W
PAE	Max Power Added Efficiency	55	65		%
G_{PAE_MAX}	Associated Gain at Max PAE		13		dB

(1) Input RF and gate voltage are pulsed. Conditions are 25µs width, 10% duty cycle and 1µs offset between DC and RF pulse.

These values are the intrinsic performance of the packaged device. They are deduced from measurements and simulations. They are considered in the reference plane defined by the leads of the package, at the connection interface with the PCB. The typical performance achievable in more than 20% frequency band around 3GHz was demonstrated using the reference board 61500192 presented hereafter.

Absolute Maximum Ratings

Tcase= +25°C(1), (2), (3)

Symbol	Parameter	Rating	Unit	Note
V_{DS}	Drain-Source Voltage	60	V	
V_{GS_Q}	Gate-Source Voltage	-10, +2	V	(6)
I_{G_MAX}	Maximum Gate Current in forward mode	150	mA	
I_{G_MIN}	Maximum Gate Current in reverse mode	-12	mA	
I_{D_MAX}	Maximum Drain Current	12	A	(4)
P_{IN}	Maximum Input Power (typical)	41	dBm	(5)
T_j	Junction Temperature	220	°C	
T_{STG}	Storage Temperature	-55 to +150	°C	
T_{Case}	Case Operating Temperature	See note	°C	(4)

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Duration < 1s.
(3) The given values must not be exceeded at the same time even momentarily for any parameter, since each parameter is independent from each other, otherwise deterioration or destruction of the device may take place.
(4) Max junction temperature must be considered
(5) @3GHz - Linked to and limited by I_{G_MAX} & I_{G_MIN} values
(6) V_{GS_Q} max limited by I_{D_MAX} and I_{G_MAX} values

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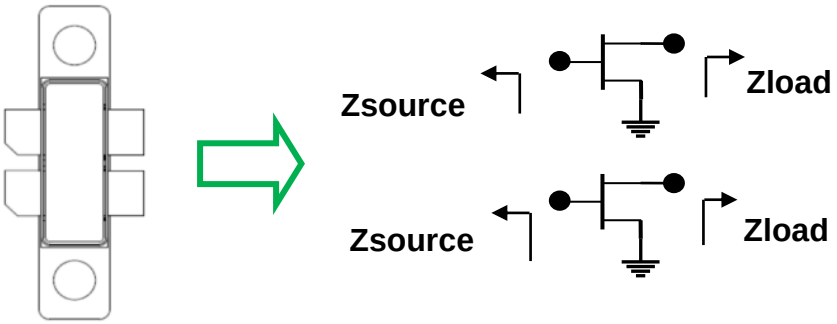
Simulated Source and Load Impedance

The device is composed of 2 independent transistors.
V_{DS}=50V, I_{D_Q}=600mA (300mA on each transistor)



Frequency (MHz)	Source	Load
500	1 + j4.5	21.6 + j7
1000	1 + j1.9	15.3 + j14.3
2000	1.3 - j1.9	5 + j7.9
3000	1.4 - j4.8	2.8 + j2.3
3500	0.8 - j6.7	2.3 + j0.2

These values are relative to each transistor and are given in the reference plane defined by the connection between the package leads and the PCB. A gap of 200µm is considered between the edge of the package and the PCB.

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Typical S-parameters

The device is composed of 2 independent transistors.
Each transistor has the following S-parameters.

Tcase=+25°C, CW mode, V_{DS}=50V, I_{D_Q}=600mA (300mA on each transistor), phase S(i,j) in °.

Freq (GHz)	*Mag S(1,1)*	*Phase S(1,1)*	*Mag S(2,1)*	*Phase S(2,1)*	*Mag S(1,2)*	*Phase S(1,2)*	*Mag S(2,2)*	*Phase S(2,2)*
0	0.99	0.00	102.98	-180.00	0.0000	180.00	0.53	0.00
0.25	0.89	-148.78	26.70	94.89	0.0120	8.67	0.37	-127.84
0.5	0.90	-165.08	13.34	77.63	0.0120	-4.55	0.42	-137.95
0.75	0.90	-171.34	8.59	65.80	0.0110	-11.66	0.50	-141.46
1	0.91	-175.14	6.13	55.96	0.0090	-15.55	0.57	-144.97
1.25	0.92	-178.05	4.64	47.41	0.0080	-16.10	0.63	-148.80
1.5	0.93	179.44	3.65	39.85	0.0060	-12.17	0.69	-152.71
1.75	0.93	177.13	2.95	33.12	0.0050	-2.19	0.73	-156.53
2	0.94	174.95	2.45	27.06	0.0050	13.92	0.77	-160.17
2.25	0.94	172.84	2.06	21.58	0.0050	31.44	0.80	-163.60
2.5	0.95	170.78	1.77	16.56	0.0060	44.67	0.82	-166.83
2.75	0.95	168.74	1.54	11.94	0.0070	52.66	0.84	-169.87
3	0.95	166.71	1.36	7.63	0.0080	56.95	0.86	-172.76
3.25	0.95	164.67	1.22	3.58	0.0100	58.94	0.87	-175.50
3.5	0.95	162.61	1.10	-0.26	0.0120	59.51	0.88	-178.13
3.75	0.95	160.53	1.00	-3.92	0.0130	59.18	0.89	179.33
4	0.96	158.40	0.93	-7.46	0.0150	58.27	0.90	176.87
4.25	0.95	156.21	0.86	-10.90	0.0170	56.96	0.90	174.46
4.5	0.95	153.96	0.81	-14.26	0.0190	55.36	0.91	172.08
4.75	0.95	151.63	0.76	-17.59	0.0200	53.56	0.91	169.73
5	0.95	149.21	0.73	-20.90	0.0220	51.60	0.92	167.39
5.25	0.95	146.67	0.70	-24.22	0.0240	49.50	0.92	165.04
5.5	0.95	144.01	0.68	-27.57	0.0270	47.28	0.92	162.66
5.75	0.95	141.19	0.66	-30.99	0.0290	44.94	0.92	160.25
6	0.94	138.20	0.65	-34.51	0.0310	42.48	0.92	157.78
6.25	0.94	134.99	0.64	-38.14	0.0340	39.89	0.92	155.24
6.5	0.93	131.54	0.64	-41.93	0.0370	37.14	0.92	152.61
6.75	0.93	127.81	0.64	-45.92	0.0400	34.22	0.92	149.87
7	0.92	123.74	0.65	-50.14	0.0430	31.10	0.92	146.99
7.25	0.92	119.28	0.66	-54.64	0.0470	27.73	0.91	143.95
7.5	0.91	114.35	0.68	-59.48	0.0510	24.07	0.91	140.70
7.75	0.90	108.86	0.70	-64.72	0.0550	20.05	0.91	137.23
8	0.89	102.71	0.73	-70.44	0.0610	15.61	0.90	133.46
8.25	0.88	95.78	0.76	-76.71	0.0660	10.66	0.90	129.35
8.5	0.87	87.92	0.80	-83.64	0.0730	5.10	0.89	124.82
8.75	0.85	78.95	0.84	-91.33	0.0800	-1.18	0.89	119.78
9	0.83	68.71	0.89	-99.89	0.0880	-8.30	0.88	114.10
9.25	0.82	57.03	0.95	-109.45	0.0970	-16.37	0.87	107.63
9.5	0.80	43.79	1.00	-120.09	0.1060	-25.51	0.87	100.14
9.75	0.79	28.98	1.05	-131.91	0.1150	-35.83	0.86	91.38
10	0.78	12.80	1.10	-144.94	0.1230	-47.36	0.85	81.00

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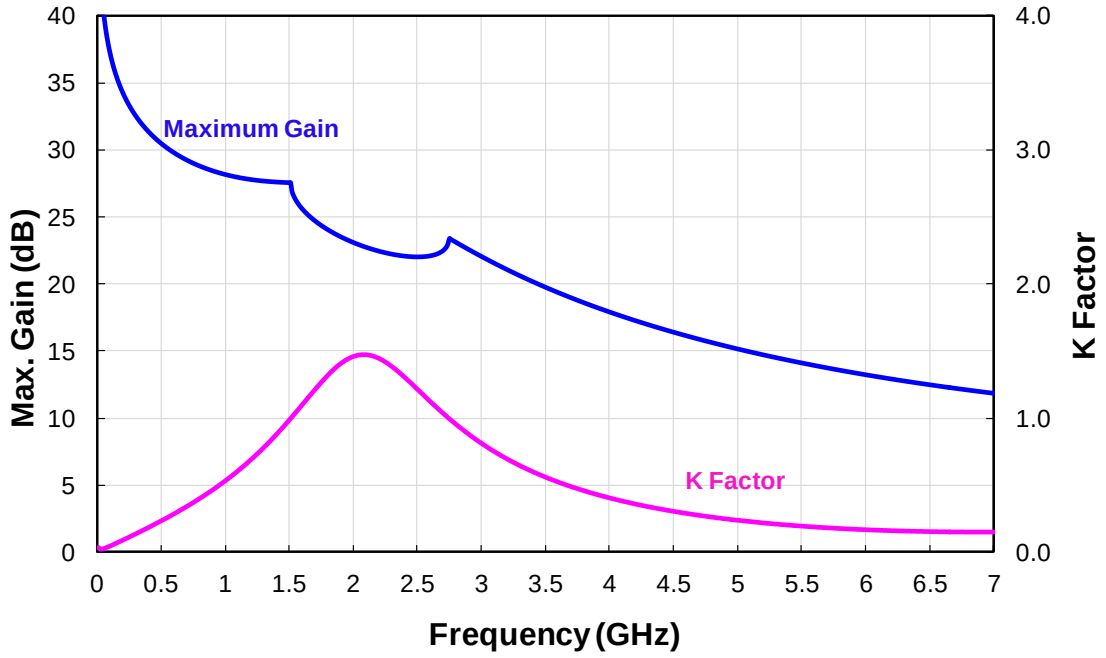
Maximum Gain & Stability Characteristics

The device is composing by 2 independent transistors.
Each transistor has the following parameters.

Tcase= +25°C, CW mode, V_{DS}=50V, I_{D_Q}=600mA (300mA on each transistor)



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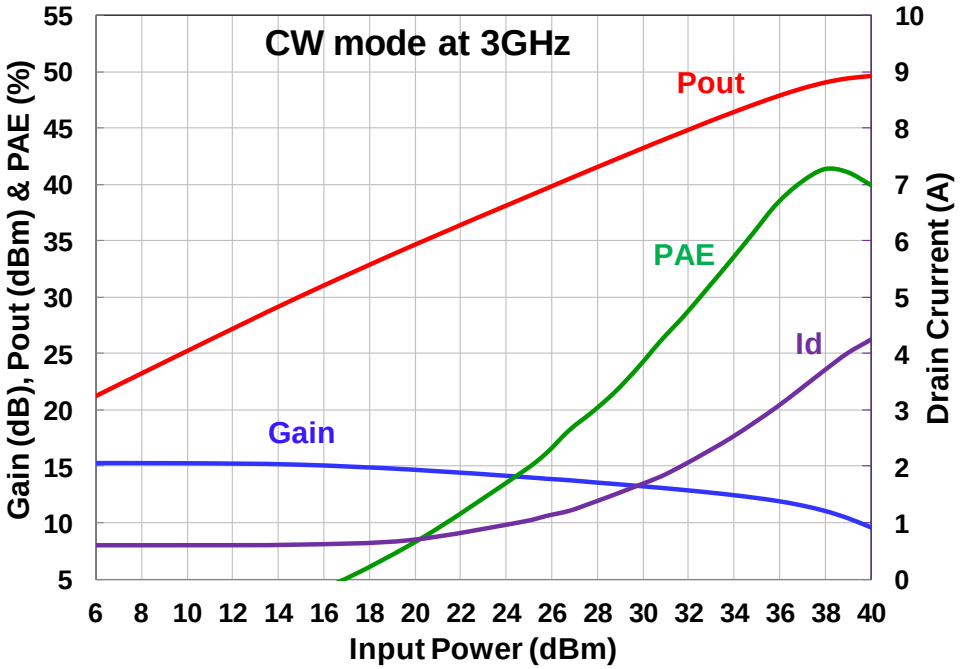
Typical Performance on Demonstration Board (Ref. 61500192)

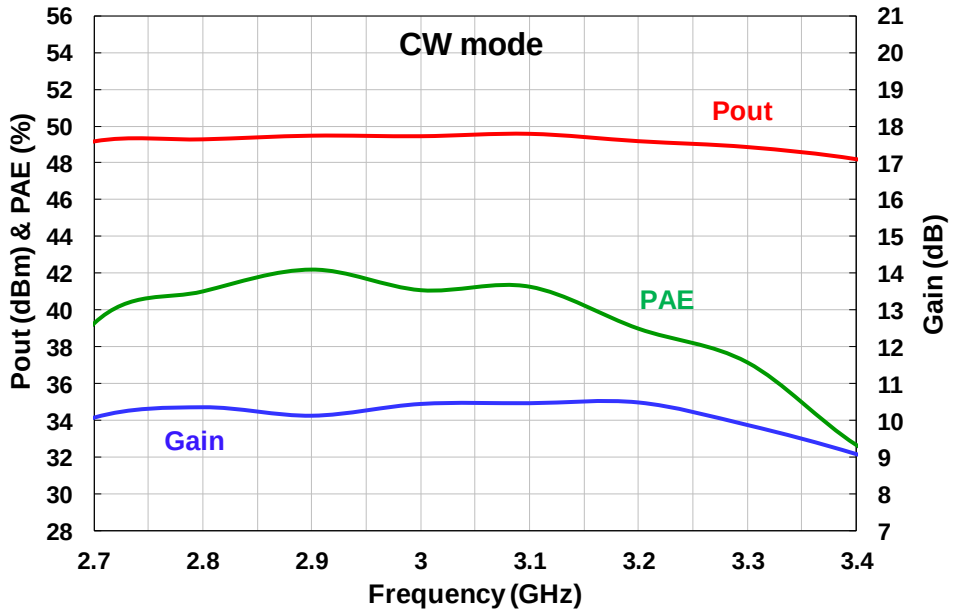
Calibration and measurements are done on the connector reference accesses of the demonstration boards.

Tcase = +25°C, CW mode

Measured Id, Gain, Pout & PAE
F = 3GHz, V_{DS} = 50V, I_{D_Q} = 600mA



Measured Gain, Pout & PAE
Pin = 39dBm, V_{DS} = 50V, $I_{D\ Q}$ = 600mA



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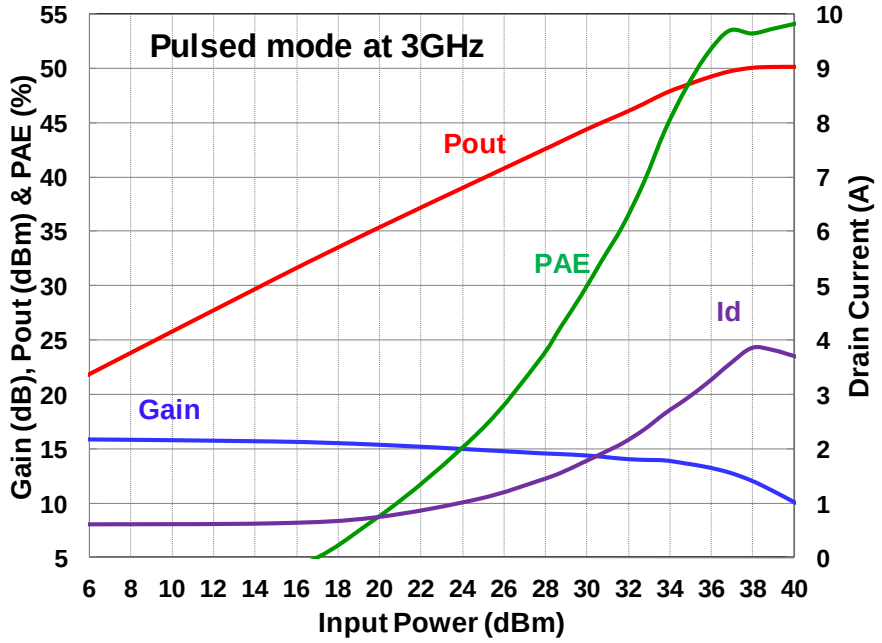
Typical Performance on Demonstration Board (Ref. 61500192)

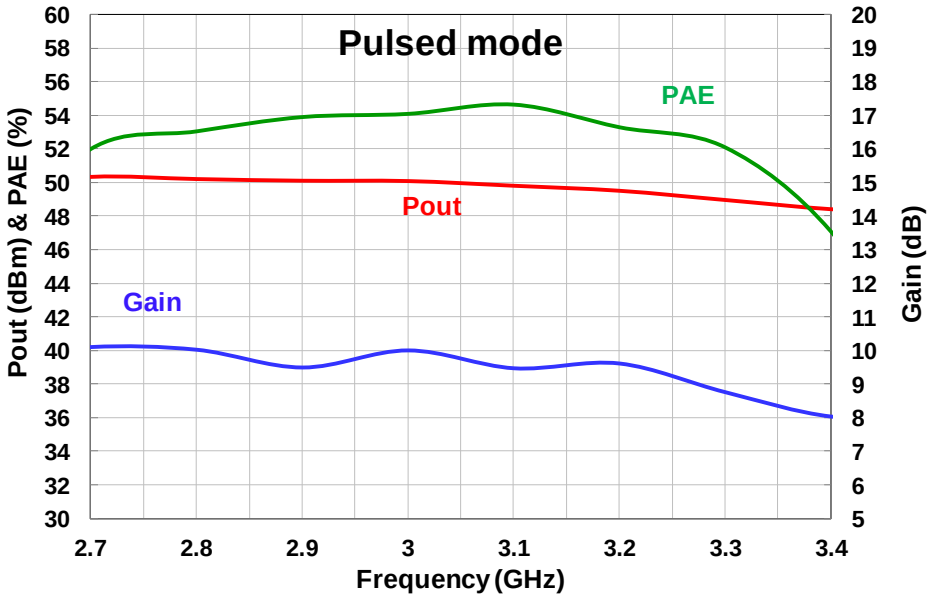
Calibration and measurements are done on the connector reference accesses of the demonstration boards

Tcase = +25°C, Pulsed mode [1]

Measured Id, Gain, Pout & PAE
F = 3GHz, V_{DS} = 50V, I_{D_Q} = 600mA



Measured Gain, Pout & PAE
Pin = 39dBm, V_{DS} = 50V, I_{D_Q} = 600mA



[1] Input RF and gate voltage are pulsed. Conditions are 25µs width, 10% duty cycle and 1µs offset between DC and RF pulse.

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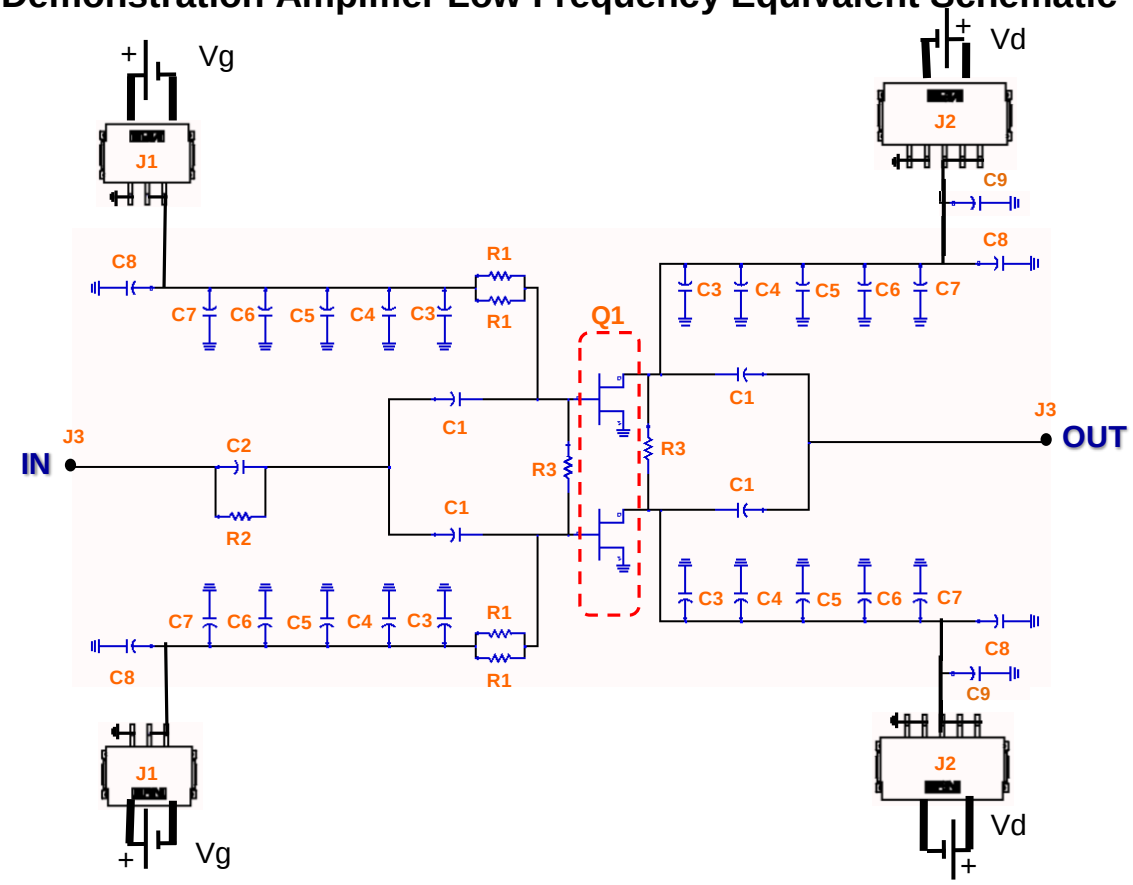
Demonstration Amplifier Low Frequency Equivalent Schematic



Demonstration Amplifier / Bill of Materials (Ref. 61500192)

Designator	Type	Value - Description	Qty
C1	Capacitor	1pF, +/- 0.1pF, 0603	4
C2	Capacitor	3.3pF, +/- 0.1pF, 0603	1
C3	Capacitor	5.6pF, +/- 0.25%, 0603	4
C4	Capacitor	10pF, +/- 5%, 0603	4
C5	Capacitor	120pF, +/- 5%, 0805	4
C6	Capacitor	240pF, +/- 5%, 0805	4
C7	Capacitor	10nF, +/- 10%, 0805	4
C8	Capacitor	1µF, +/- 10%, 1204	4
C9	Capacitor	68µF, +/- 10%, H13	2
R1	Resistor	49.9Ω, +/- 1%, 0603	4
R2	Resistor	220Ω +/- 1%, 0603	1
R3	Resistor	22Ω +/- 1%, MMA0204	2
J1	Connector	CMS 3cts	2
J2	Connector	CMS 5cts	2
J3	Connector	N	2
Q1	Packaged Transistor	CHK080A-SRA	1
-	PCB	RO4003, Er=3.55, h=0.508mm	-

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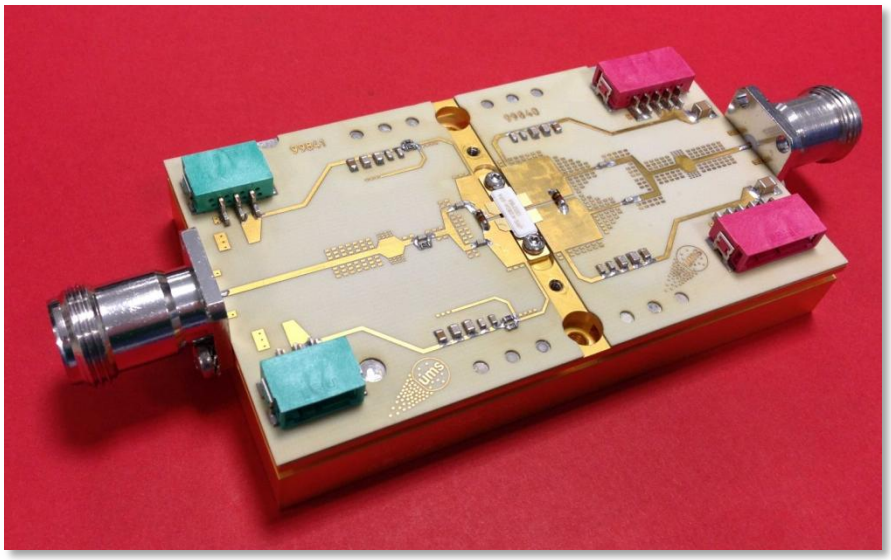
Demonstration Amplifier Circuit (Ref. 61500192)



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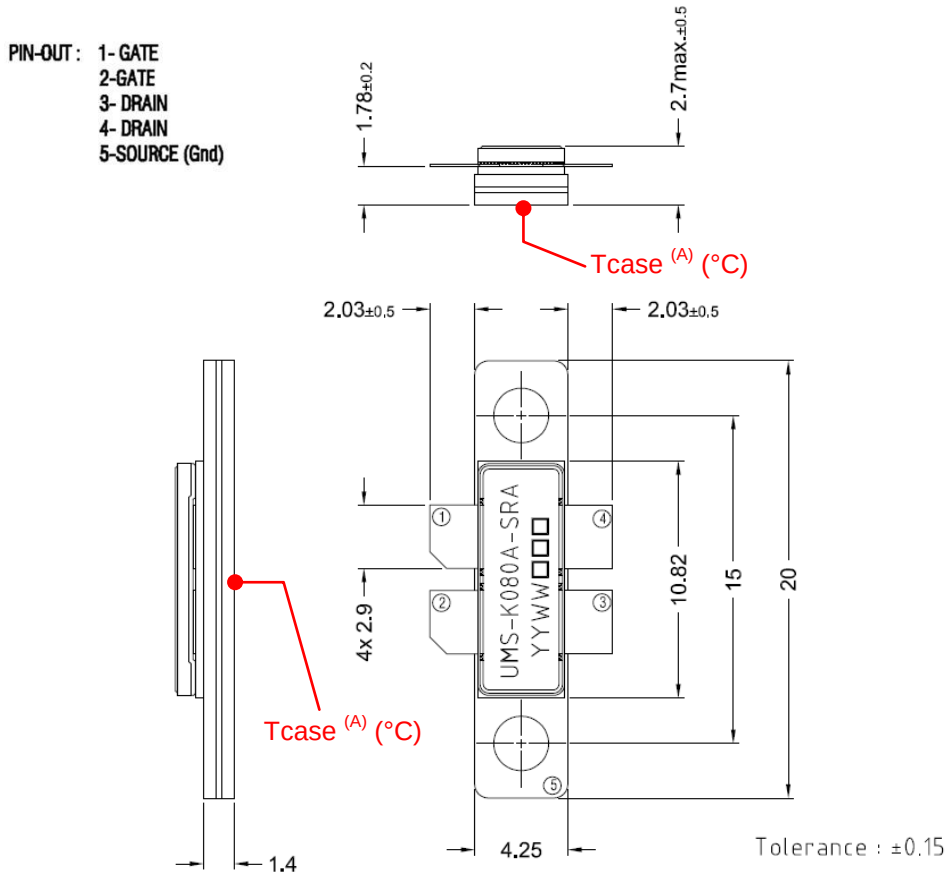
Package outline

All dimensions are in mm



(A) Tcase locates the reference point used to monitor the device temperature. This point has been taken at the device / system interface to ease system thermal design.
Chamfered lead indicates the gate access of the packaged transistor.

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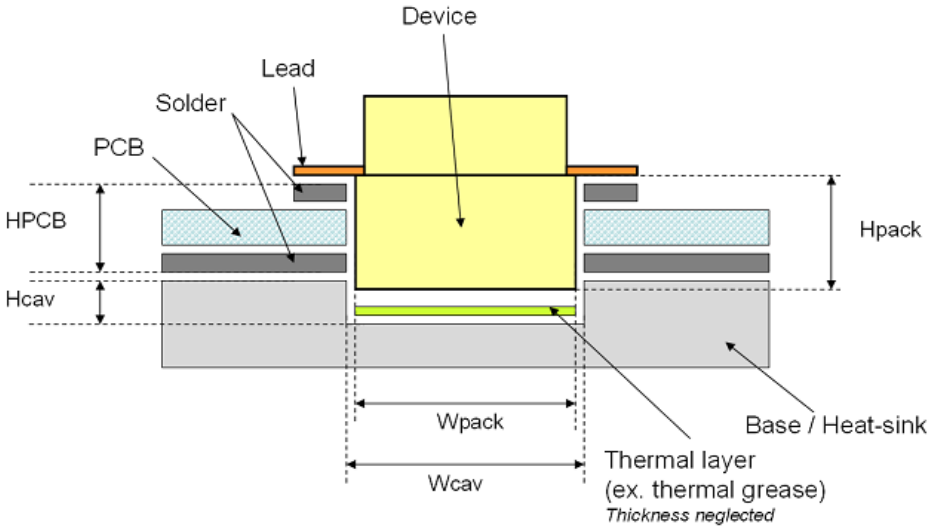
Recommended Assembly Procedure

CHK080A-SRA is available as a flange package to be bolt down onto a thermal heat sink also used as main electrical ground. Use preferably screw M2 and flat washers.
Thermal and electrical resistance at the package to heat sink interface has to be as low as possible. Thermal electrically conductive grease or conductive thin layer like indium sheets are recommended between the package and the heat sink.
In case a thermal grease is selected, we recommend to use material offering thermal conductivity >5W/m.K and electrical resistivity <0.01 ohm.cm. The grease layer thickness should be about 25µm (1 mil).
Contact interface quality can be improved by cleaning process prior device mounting on the heat-sink. Such operation will enhance the thermal and electrical contact by oxide removal at each interface.
Package leads can be soldered on printed circuit board traces by using RoHS solder past.
Cavity depth and width to be performed into the heat-sink where the device will be mounted are important to achieve the best performances. These dimensions have to be optimized in order to minimize the distance between device and signal traces made on the printed circuit board (PCB). But they also have to be calculated in order to accommodate device variations in height. The following drawing gives the relationship between device dimensions (Hpack & Wpack) and optimal cavity depth (Hcav) and width (Wcav) depending on the printed circuit-board configuration (HPCB)



$Hcav = (Hpack_{min} - HPCB_{max})^{+0}{}_{/- 0.05}$
$Wcav = (Wpack_{max} + 0.4)_{+/- 0.05}$

dimensions are in mm

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Notes

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Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

Package :	CHK080A-SRA/XY
	Tray: XY = 26

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