HD66763

384-channel Segment Driver with Internal RAM for 256-color Displays

HITACHI

Rev.1.0
July, 2001

Description

The HD66763, 384-channel segment driver LSI, displays 128RGB-by-176-dot graphics on STN displays in 256 colors. It is for driving STN color LCD displays to a maximum of 128RGB by 176 dots, in combination with the HD66764 common driver. The HD66763's bit-operation functions, 16-bit high-speed bus interface, and high-speed RAM-write functions enable efficient data transfer and high-speed rewriting of data to the graphics RAM.

The HD66763 and HD66764 have various functions for reducing the power consumption of an LCD system. The HD66763 has a low-voltage operation (1.8 V min.) and an internal RAM to display a maximum of 128RGB-by-176-dot color, and the HD66764 has a step-up circuit to generate the LCD-drive voltage, a bleeder resistor for the drive interface with the LCD, and voltage-followers. Since the HD66763 incorporates a circuit that interfaces with the HD66764, it can set instructions for the HD66764. In addition, precise power control can be achieved by combining these hardware functions with software functions, such as a partial display that only requires a low drive-voltage duty, and standby and sleep modes. This LSI is suitable for any medium-sized or small portable battery-driven product requiring long-term driving capabilities, such as digital cellular phones supporting a WWW browser, bidirectional pagers, and small PDAs.

Features

- 128RGB x 176-dot graphics display LCD controller/driver for 256 STN colors (when HD66764 is used)
- Low-voltage drive and flickerless PWM grayscale drive
- 16-/8-bit high-speed bus interface and serial peripheral interface (SPI)
- High-speed burst-RAM write function
- Writing to a window-RAM address area by using a window-address function
- Bit-operation functions for graphics processing:
  - — Write-data mask function in bit units
  - — Swap function of upper and lower bytes

— Logical operation in pixel unit and conditional write function

- Various color-display control functions:
  - 256 of the 4,096 possible colors can be displayed at the same time (grayscale palette included)
  - Vertical scroll display function in raster-row units

- Low-power operation supports:
  - Vcc = 1.8 to 3.6 V (low-voltage range)
  - VLCD = 2.0 to 4.0 V (liquid crystal drive voltage)
  - Power-save functions such as the standby mode and sleep mode
  - Partial LCD drive of two screens in any position
  - Programmable drive duty ratios (1/16–1/176) and bias values (1/4–1/13) displayed on LCD
  - Maximum 12-times step-up circuit for liquid crystal drive voltage (HD66764)
  - Voltage followers to decrease direct current flow in the LCD drive bleeder-resistors (HD66764)
  - 128-step contrast adjuster (HD66764)

- Built-in circuit for interfacing with the HD66764 common driver

- Maximum 128RGB-by-176-dot display in combination with the HD66764 common driver

- Internal RAM capacity: 21,504 bytes

- 384-segment liquid crystal display driver

- n-raster-row AC liquid-crystal drive (C-pattern waveform drive)

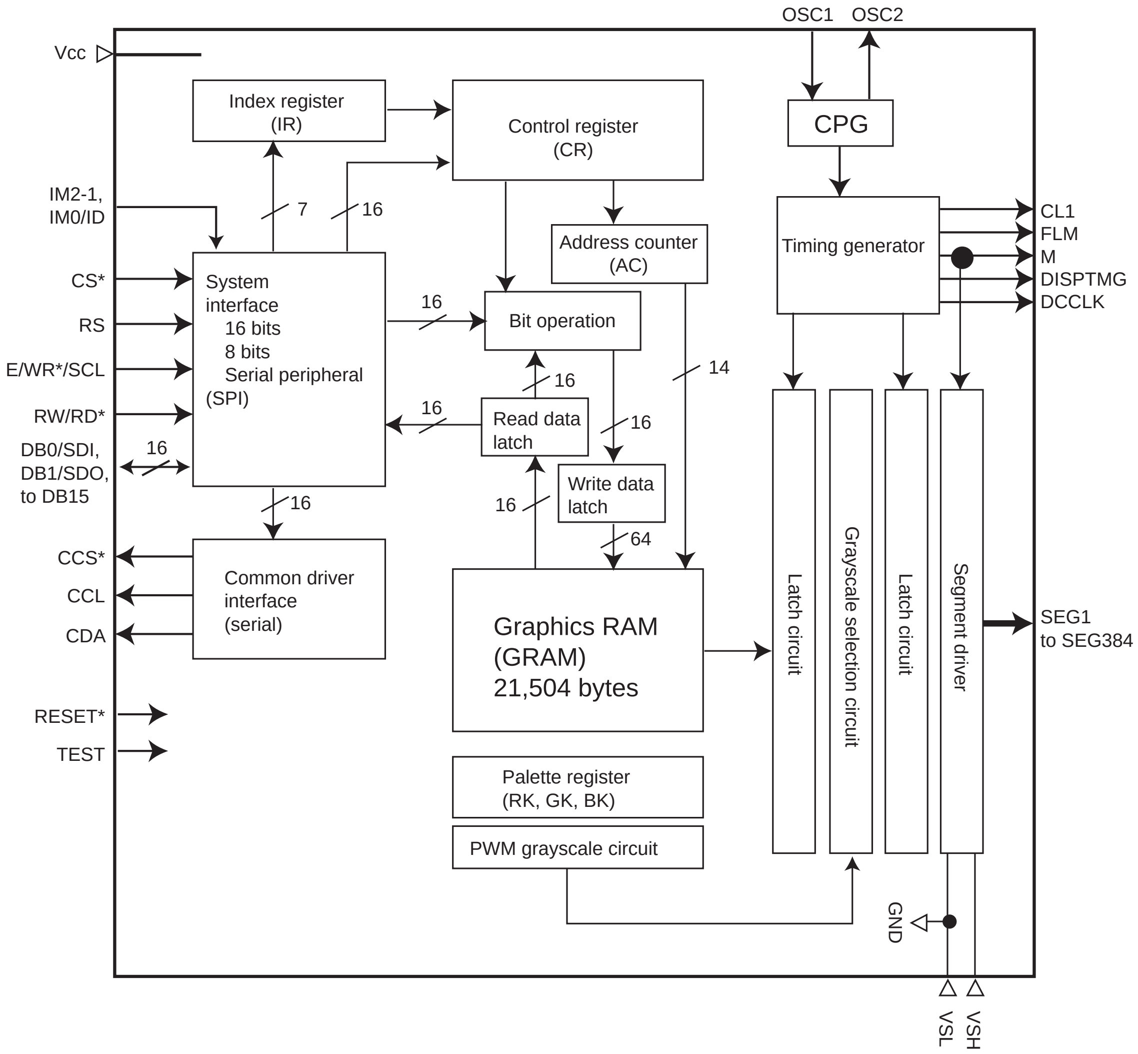
- Internal oscillation and hardware reset

- Shift change of segment driver

Type Number

Type Number	External Appearance
HD66763TB0	Bending TCP
HCD66763BP	Au-bump chip

HD66763 Block Diagram



HD66763 PAD Arrangement

- Chip size : 17.96mm x 2.38mm
- Chip thickness : 550um (typ.)
- PAD coordinates : PAD center
- Coordinate origin : chip center
- Au bump size (PAD number is shown in the bracket) :

(1) 80um x 80um
 Dummy1(1) to Dummy34(96)
 Dummy35(130), Dummy70(483)

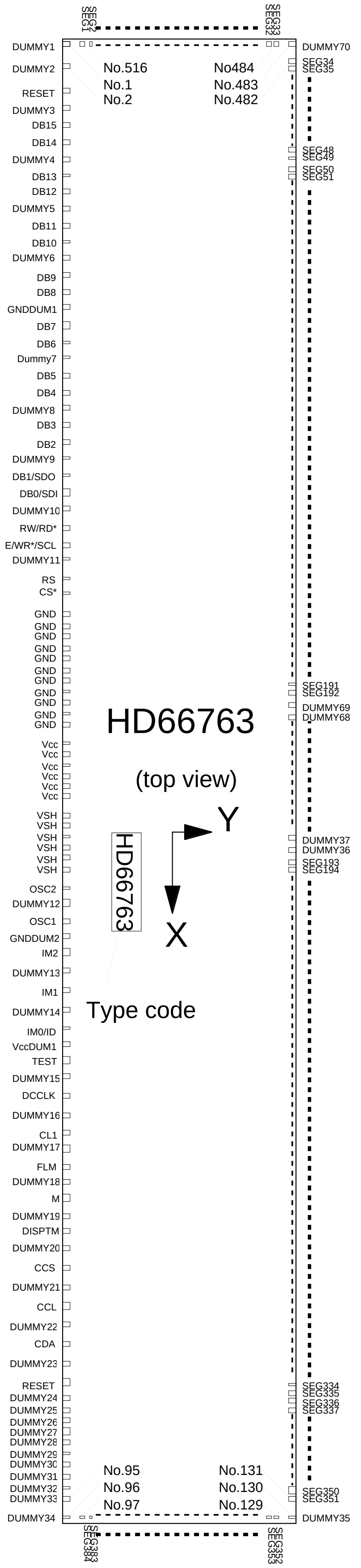
(2) 42um x 80um
 SEG336(146) to SEG351(131)
 SEG34(482) to SEG49(467)

(3) 80um x 42um
 SEG352(129) to SEG384(97)
 SEG1(516) to SEG33(484)

(4)32um x 80um
 SEG50(466) to SEG192(324)
 DUMMY36(290) to DUMMY69(323)
 SEG193(289) to SEG335(147)

- Au bump height : 15um (typ.)

Rev 1.1



HD66763 PAD Coordinate

No.	pad name	X	Y
1	DUMMY1	-8854	-1047
2	DUMMY2	-8620	-1047
3	RESET	-8411	-1047
4	DUMMY3	-8202	-1047
5	DB15	-7993	-1047
6	DB14	-7685	-1047
7	DUMMY4	-7476	-1047
8	DB13	-7267	-1047
9	DB12	-6959	-1047
10	DUMMY5	-6750	-1047
11	DB11	-6541	-1047
12	DB10	-6233	-1047
13	DUMMY6	-6024	-1047
14	DB9	-5815	-1047
15	DB8	-5507	-1047
16	GNDDUM1	-5298	-1047
17	DB7	-5089	-1047
18	DB6	-4781	-1047
19	DUMMY7	-4572	-1047
20	DB5	-4363	-1047
21	DB4	-4055	-1047
22	DUMMY8	-3846	-1047
23	DB3	-3637	-1047
24	DB2	-3329	-1047
25	DUMMY9	-3120	-1047
26	DB1/SDO	-2911	-1047
27	DB0/SDI	-2603	-1047
28	DUMMY10	-2394	-1047
29	RW/RD*	-2185	-1047
30	E/WR*/SCL	-1877	-1047
31	DUMMY11	-1668	-1047
32	RS	-1459	-1047
33	CS*	-1151	-1047
34	GND	-931	-1047
35	GND	-831	-1047
36	GND	-731	-1047
37	GND	-630	-1047
38	GND	-530	-1047
39	GND	-430	-1047
40	GND	-330	-1047
41	GND	-230	-1047
42	GND	-130	-1047
43	GND	-30	-1047
44	GND	70	-1047
45	VCC	228	-1047
46	VCC	328	-1047
47	VCC	428	-1047
48	VCC	528	-1047
49	VCC	629	-1047
50	VCC	729	-1047
51	VSH	886	-1047
52	VSH	986	-1047
53	VSH	1087	-1047
54	VSH	1187	-1047
55	VSH	1287	-1047
56	VSH	1387	-1047
57	OSC2	1607	-1047
58	DUMMY12	1816	-1047
59	OSC1	2025	-1047
60	GNDDUM2	2234	-1047
61	IM2	2443	-1047
62	DUMMY13	2652	-1047
63	IM1	2861	-1047
64	DUMMY14	3070	-1047
65	IM0/ID	3279	-1047
66	VCCDUM1	3488	-1047
67	TEST	3697	-1047
68	DUMMY15	3907	-1047
69	DCCLK	4116	-1047
70	DUMMY16	4325	-1047
71	CL1	4534	-1047
72	DUMMY17	4743	-1047
73	FLM	4952	-1047
74	DUMMY18	5161	-1047
75	M	5370	-1047
76	DUMMY19	5579	-1047
77	DISPTMG	5788	-1047
78	DUMMY20	5997	-1047
79	CCS	6206	-1047
80	DUMMY21	6415	-1047
81	CCL	6624	-1047
82	DUMMY22	6833	-1047
83	CDA	7042	-1047
84	DUMMY23	7251	-1047
85	RESET	7460	-1047
86	DUMMY24	7669	-1047
87	DUMMY25	7775	-1047
88	DUMMY26	7881	-1047
89	DUMMY27	7987	-1047
90	DUMMY28	8092	-1047
91	DUMMY29	8198	-1047
92	DUMMY30	8304	-1047
93	DUMMY31	8409	-1047
94	DUMMY32	8515	-1047
95	DUMMY33	8621	-1047
96	DUMMY34	8854	-1047
97	SEG384	8854	-914
98	SEG383	8854	-857
99	SEG382	8854	-800
100	SEG381	8854	-742
101	SEG380	8854	-685
102	SEG379	8854	-628
103	SEG378	8854	-571
104	SEG377	8854	-514

No.	pad name	X	Y
105	SEG376	8854	-457
106	SEG375	8854	-400
107	SEG374	8854	-343
108	SEG373	8854	-286
109	SEG372	8854	-228
110	SEG371	8854	-171
111	SEG370	8854	-114
112	SEG369	8854	-57
113	SEG368	8854	0
114	SEG367	8854	57
115	SEG366	8854	114
116	SEG365	8854	171
117	SEG364	8854	228
118	SEG363	8854	286
119	SEG362	8854	343
120	SEG361	8854	400
121	SEG360	8854	457
122	SEG359	8854	514
123	SEG358	8854	571
124	SEG357	8854	628
125	SEG356	8854	685
126	SEG355	8854	742
127	SEG354	8854	800
128	SEG353	8854	857
129	SEG352	8854	914
130	DUMMY35	8854	1060
131	SEG351	8598	1060
132	SEG350	8538	1060
133	SEG349	8478	1060
134	SEG348	8417	1060
135	SEG347	8357	1060
136	SEG346	8297	1060
137	SEG345	8237	1060
138	SEG344	8177	1060
139	SEG343	8117	1060
140	SEG342	8057	1060
141	SEG341	7997	1060
142	SEG340	7937	1060
143	SEG339	7877	1060
144	SEG338	7817	1060
145	SEG337	7756	1060
146	SEG336	7696	1060
147	SEG335	7642	1060
148	SEG334	7595	1060
149	SEG333	7547	1060
150	SEG332	7500	1060
151	SEG331	7452	1060
152	SEG330	7404	1060
153	SEG329	7357	1060
154	SEG328	7309	1060
155	SEG327	7262	1060
156	SEG326	7214	1060
157	SEG325	7166	1060
158	SEG324	7119	1060
159	SEG323	7071	1060
160	SEG322	7023	1060
161	SEG321	6976	1060
162	SEG320	6928	1060
163	SEG319	6881	1060
164	SEG318	6833	1060
165	SEG317	6785	1060
166	SEG316	6738	1060
167	SEG315	6690	1060
168	SEG314	6643	1060
169	SEG313	6595	1060
170	SEG312	6547	1060
171	SEG311	6500	1060
172	SEG310	6452	1060
173	SEG309	6404	1060
174	SEG308	6357	1060
175	SEG307	6309	1060
176	SEG306	6262	1060
177	SEG305	6214	1060
178	SEG304	6166	1060
179	SEG303	6119	1060
180	SEG302	6071	1060
181	SEG301	6024	1060
182	SEG300	5976	1060
183	SEG299	5928	1060
184	SEG298	5881	1060
185	SEG297	5833	1060
186	SEG296	5785	1060
187	SEG295	5738	1060
188	SEG294	5690	1060
189	SEG293	5643	1060
190	SEG292	5595	1060
191	SEG291	5547	1060
192	SEG290	5500	1060
193	SEG289	5452	1060
194	SEG288	5404	1060
195	SEG287	5357	1060
196	SEG286	5309	1060
197	SEG285	5262	1060
198	SEG284	5214	1060
199	SEG283	5166	1060
200	SEG282	5119	1060
201	SEG281	5071	1060
202	SEG280	5024	1060
203	SEG279	4976	1060
204	SEG278	4928	1060
205	SEG277	4881	1060
206	SEG276	4833	1060
207	SEG275	4785	1060
208	SEG274	4738	1060

No.	pad name	X	Y
209	SEG273	4690	1060
210	SEG272	4643	1060
211	SEG271	4595	1060
212	SEG270	4547	1060
213	SEG269	4500	1060
214	SEG268	4452	1060
215	SEG267	4405	1060
216	SEG266	4357	1060
217	SEG265	4309	1060
218	SEG264	4262	1060
219	SEG263	4214	1060
220	SEG262	4166	1060
221	SEG261	4119	1060
222	SEG260	4071	1060
223	SEG259	4024	1060
224	SEG258	3976	1060
225	SEG257	3928	1060
226	SEG256	3881	1060
227	SEG255	3833	1060
228	SEG254	3786	1060
229	SEG253	3738	1060
230	SEG252	3690	1060
231	SEG251	3643	1060
232	SEG250	3595	1060
233	SEG249	3547	1060
234	SEG248	3500	1060
235	SEG247	3452	1060
236	SEG246	3405	1060
237	SEG245	3357	1060
238	SEG244	3309	1060
239	SEG243	3262	1060
240	SEG242	3214	1060
241	SEG241	3167	1060
242	SEG240	3119	1060
243	SEG239	3071	1060
244	SEG238	3024	1060
245	SEG237	2976	1060
246	SEG236	2928	1060
247	SEG235	2881	1060
248	SEG234	2833	1060
249	SEG233	2786	1060
250	SEG232	2738	1060
251	SEG231	2690	1060
252	SEG230	2643	1060
253	SEG229	2595	1060
254	SEG228	2547	1060
255	SEG227	2500	1060
256	SEG226	2452	1060
257	SEG225	2405	1060
258	SEG224	2357	1060
259	SEG223	2309	1060
260	SEG222	2262	1060
261	SEG221	2214	1060
262	SEG220	2167	1060
263	SEG219	2119	1060
264	SEG218	2071	1060
265	SEG217	2024	1060
266	SEG216	1976	1060
267	SEG215	1928	1060
268	SEG214	1881	1060
269	SEG213	1833	1060
270	SEG212	1786	1060
271	SEG211	1738	1060
272	SEG210	1690	1060
273	SEG209	1643	1060
274	SEG208	1595	1060
275	SEG207	1548	1060
276	SEG206	1500	1060
277	SEG205	1452	1060
278	SEG204	1405	1060
279	SEG203	1357	1060
280	SEG202	1309	1060
281	SEG201	1262	1060
282	SEG200	1214	1060
283	SEG199	1167	1060
284	SEG198	1119	1060
285	SEG197	1071	1060
286	SEG196	1024	1060
287	SEG195	976	1060
288	SEG194	929	1060
289	SEG193	881	1060
290	DUMMY36	786	1060
291	DUMMY37	738	1060
292	DUMMY38	690	1060
293	DUMMY39	643	1060
294	DUMMY40	595	1060
295	DUMMY41	548	1060
296	DUMMY42	500	1060
297	DUMMY43	452	1060
298	DUMMY44	405	1060
299	DUMMY45	357	1060
300	DUMMY46	310	1060
301	DUMMY47	262	1060
302	DUMMY48	214	1060
303	DUMMY49	167	1060
304	DUMMY50	119	1060
305	DUMMY51	71	1060
306	DUMMY52	24	1060
307	DUMMY53	-24	1060
308	DUMMY54	-71	1060
309	DUMMY55	-119	1060
310	DUMMY56	-167	1060
311	DUMMY57	-214	1060
312	DUMMY58	-262	1060

No.	pad name	X	Y
313	DUMMY59	-310	1060
314	DUMMY60	-357	1060
315	DUMMY61	-405	1060
316	DUMMY62	-452	1060
317	DUMMY63	-500	1060
318	DUMMY64	-548	1060
319	DUMMY65	-595	1060
320	DUMMY66	-643	1060
321	DUMMY67	-690	1060
322	DUMMY68	-738	1060
323	DUMMY69	-786	1060
324	SEG192	-881	1060
325	SEG191	-929	1060
326	SEG190	-976	1060
327	SEG189	-1024	1060
328	SEG188	-1071	1060
329	SEG187	-1119	1060
330	SEG186	-1167	1060
331	SEG185	-1214	1060
332	SEG184	-1262	1060
333	SEG183	-1309	1060
334	SEG182	-1357	1060
335	SEG181	-1405	1060
336	SEG180	-1452	1060
337	SEG179	-1500	1060
338	SEG178	-1548	1060
339	SEG177	-1595	1060
340	SEG176	-1643	1060
341	SEG175	-1690	1060
342	SEG174	-1738	1060
343	SEG173	-1786	1060
344	SEG172	-1833	1060
345	SEG171	-1881	1060
346	SEG170	-1928	1060
347	SEG169	-1976	1060
348	SEG168	-2024	1060
349	SEG167	-2071	1060
350	SEG166	-2119	1060
351	SEG165	-2167	1060
352	SEG164	-2214	1060
353	SEG163	-2262	1060
354	SEG162	-2309	1060
355	SEG161	-2357	1060
356	SEG160	-2405	1060
357	SEG159	-2452	1060
358	SEG158	-2500	1060
359	SEG157	-2547	1060
360	SEG156	-2595	1060
361	SEG155	-2643	1060
362	SEG154	-2690	1060
363	SEG153	-2738	1060
364	SEG152	-2786	1060
365	SEG151	-2833	1060
366	SEG150	-2881	1060
367	SEG149	-2928	1060
368	SEG148	-2976	1060
369	SEG147	-3024	1060
370	SEG146	-3071	1060
371	SEG145	-3119	1060
372	SEG144	-3167	1060
373	SEG143	-3214	1060
374	SEG142	-3262	1060
375	SEG141	-3309	1060
376	SEG140	-3357	1060
377	SEG139	-3405	1060
378	SEG138	-3452	1060
379	SEG137	-3500	1060
380	SEG136	-3547	1060
381	SEG135	-3595	1060
382	SEG134	-3643	1060
383	SEG133	-3690	1060
384	SEG132	-3738	1060
385	SEG131	-3786	1060
386	SEG130	-3833	1060
387	SEG129	-3881	1060
388	SEG128	-3928	1060
389	SEG127	-3976	1060
390	SEG126	-4024	1060
391	SEG125	-4071	1060
392	SEG124	-4119	1060
393	SEG123	-4166	1060
394	SEG122	-4214	1060
395	SEG121	-4262	1060
396	SEG120	-4309	1060
397	SEG119	-4357	1060
398	SEG118	-4405	1060
399	SEG117	-4452	1060
400	SEG116	-4500	1060
401	SEG115	-4547	1060
402	SEG114	-4595	1060
403	SEG113	-4643	1060
404	SEG112	-4690	1060
405	SEG111	-4738	1060
406	SEG110	-4785	1060
407	SEG109	-4833	1060
408	SEG108	-4881	1060
409	SEG107	-4928	1060
410	SEG106	-4976	1060
411	SEG105	-5024	1060
412	SEG104	-5071	1060
413	SEG103	-5119	1060
414	SEG102	-5166	1060
415	SEG101	-5214	1060
416	SEG100	-5262	1060

No.	pad name	X	Y
417	SEG99	-5309	1060
418	SEG98	-5357	1060
419	SEG97	-5404	1060
420	SEG96	-5452	1060
421	SEG95	-5500	1060
422	SEG94	-5547	1060
423	SEG93	-5595	1060
424	SEG92	-5643	1060
425	SEG91	-5690	1060
426	SEG90	-5738	1060
427	SEG89	-5785	1060
428	SEG88	-5833	1060
429	SEG87	-5881	1060
430	SEG86	-5928	1060
431	SEG85	-5976	1060
432	SEG84	-6024	1060
433	SEG83	-6071	1060
434	SEG82	-6119	1060
435	SEG81	-6166	1060
436	SEG80	-6214	1060
437	SEG79	-6262	1060
438	SEG78	-6309	1060
439	SEG77	-6357	1060
440	SEG76	-6404	1060
441	SEG75	-6452	1060
442	SEG74	-6500	1060
443	SEG73	-6547	1060
444	SEG72	-6595	1060
445	SEG71	-6643	1060
446	SEG70	-6690	1060
447	SEG69	-6738	1060
448	SEG68	-6785	1060
449	SEG67	-6833	1060
450	SEG66	-6881	1060
451	SEG65	-6928	1060
452	SEG64	-6976	1060
453	SEG63	-7023	1060
454	SEG62	-7071	1060
455	SEG61	-7119	1060
456	SEG60	-7166	1060
457	SEG59	-7214	1060
458	SEG58	-7262	1060
459	SEG57	-7309	1060
460	SEG56	-7357	1060
461	SEG55	-7404	1060
462	SEG54	-7452	1060
463	SEG53	-7500	1060
464	SEG52	-7547	1060
465	SEG51	-7595	1060
466	SEG50	-7642	1060
467	SEG49	-7696	1060
468	SEG48	-7756	1060
469	SEG47	-7817	1060
470	SEG46	-7877	1060
471	SEG45	-7937	1060
472	SEG44	-7997	1060
473	SEG43	-8057	1060
474	SEG42	-8117	1060
475	SEG41	-8177	1060
476	SEG40	-8237	1060
477	SEG39	-8297	1060
478	SEG38	-8357	1060
479	SEG37	-8417	1060
480	SEG36	-8478	1060
481	SEG35	-8538	1060
482	SEG34	-8598	1060
483	DUMMY70	-8854	1060
484	SEG33	-8854	914
485	SEG32	-8854	857
486	SEG31	-8854	800
487	SEG30	-8854	742
488	SEG29	-8854	685
489	SEG28	-8854	628
490	SEG27	-8854	571
491	SEG26	-8854	514
492	SEG25	-8854	457
493	SEG24	-8854	400
494	SEG23	-8854	343
495	SEG22	-8854	286
496	SEG21	-8854	228
497	SEG20	-8854	171
498	SEG19	-8854	114
499	SEG18	-8854	57
500	SEG17	-8854	0
501	SEG16	-8854	-57
502	SEG15	-8854	-114
503	SEG14	-8854	-171
504	SEG13	-8854	-228
505	SEG12	-8854	-286
506	SEG11	-8854	-343
507	SEG10	-8854	-400
508	SEG9	-8854	-457
509	SEG8	-8854	-514
510	SEG7	-8854	-571
511	SEG6	-8854	-628
512	SEG5	-8854	-685
513	SEG4	-8854	-742
514	SEG3	-8854	-800
515	SEG2	-8854	-857
516	SEG1	-8854	-914

Pin Functions

Table 1 Pin Functional Description

<table>
<tr><th>Signals</th><th>Number of Pins</th><th>I/O</th><th>Connected to</th><th>Functions</th></tr>
<tr><td>IM2-1,
IM0/ID</td><td>3</td><td>I</td><td>GND or V_{CC}</td><td>Selects the MPU interface mode:
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0/ID</th><th>MPU interface mode</th></tr>
<tr><td>GND</td><td>GND</td><td>GND</td><td>68-system 16-bit bus interface</td></tr>
<tr><td>GND</td><td>GND</td><td>Vcc</td><td>68-system 8-bit bus interface</td></tr>
<tr><td>GND</td><td>Vcc</td><td>GND</td><td>80-system 16-bit bus interface</td></tr>
<tr><td>GND</td><td>Vcc</td><td>Vcc</td><td>80-system 8-bit bus interface</td></tr>
<tr><td>Vcc</td><td>GND</td><td>ID</td><td>Serial peripheral interface (SPI)</td></tr>
</table>
When a serial interface is selected, the IM0 pin is used as the ID setting for a device code.</td></tr>
<tr><td>CS*</td><td>1</td><td>I</td><td>MPU</td><td>Selects the HD66763:
Low: HD66763 is selected and can be accessed
High: HD66763 is not selected and cannot be accessed
Must be fixed at GND level when not in use.</td></tr>
<tr><td>RS</td><td>1</td><td>I</td><td>MPU</td><td>Selects the register.
Low: Index/status High: Control</td></tr>
<tr><td>E/WR*/SCL</td><td>1</td><td>I</td><td>MPU</td><td>For a 68-system bus interface, serves as an enable signal to activate data read/write operation.
For an 80-system bus interface, serves as a write strobe signal and writes data at the low level.
For a synchronous clock interface, serves as the synchronous clock signal.</td></tr>
<tr><td>RW/RD*</td><td>1</td><td>I</td><td>MPU</td><td>For a 68-system bus interface, serves as a signal to select data read/write operation.
Low: Write High: Read
For an 80-system bus interface, serves as a read strobe signal and reads data at the low level.</td></tr>
<tr><td>DB0/SDI</td><td>1</td><td>I/O</td><td>MPU</td><td>Serves as a 16-bit bidirectional data bus.
For an 8-bit bus interface, data transfer uses DB15-DB8; fix unused DB7-DB0 to the Vcc or GND level.
For a clock-synchronous serial interface, serves as the serial data input pin (SDI). The input level is read on the rising edge of the SCL signal.</td></tr>
</table>

Table 1 Pin Functional Description (cont)

Signals	Number of Pins	I/O	Connected to	Functions
DB1/SDO	1	I/O	MPU	Serves as a 16-bit bidirectional data bus. For an 8-bit bus interface, data transfer uses DB15-DB8; fix unused DB7-DB0 to the Vcc or GND level. For a clock-synchronous serial interface, serves as a serial data output pin (SDO). Successive bit values are output on the falling edge of the SCL signal.
DB2-DB15	14	I/O	MPU	Serves as a 16-bit bidirectional data bus. For an 8-bit bus interface, data transfer uses DB15-DB8; fix unused DB7-DB0 to the Vcc or GND level.
SEG1–SEG384	384	O	LCD	Output signals for segment drive. In the display-off period (D1–0 = 00, 01) or standby mode (STB = 1), all pins output GND level. The SGS bit can change the shift direction of the segment signal. For example, if SGS = 0, RAM address 0000 is output from SEG1. If SGS = 1, it is output from SEG384. SEG1, SEG4, SEG7, ... display red (R), SEG2, SEG5, SEG8, ... display green (G), and SEG3, SEG6, SEG9, ... display blue (B) (SGS = 0).
CL1	1	O	HD66764	The one-raster-row-cycle pulse is output.
M	1	O	HD66764	The AC-cycle signal is output.
FLM	1	O	HD66764	The frame-start pulse is output.
DISPTMG	1	O	HD66764	Outputs the display period signal.
DCCLK	1	O	HD66764	Outputs clocks for the step-up.
CCL	1	O	HD66764	Clock signal for a serial transfer of register setting values to the common driver. Data is output on the falling edge of this clock.
CDA	1	O	HD66764	Data signal for serial transfer as register setting values to the common driver.
CCS*	1	O	HD66764	Chip-select for the HD66763. Low: the HD66763 is selected and can receive a serial transfer. High: the HD66763 is not selected and cannot receive a serial transfer.
VSH	1	I	HD66764	Input for the LCD-drive voltage for the segment driver, which can be provided by the HD66764's on-chip power supply. VSH ≤ 4.0 V
V_{CC}, GND	2	—	Power supply	V_{CC}: + 1.8 V to + 3.6 V; GND (logic): 0

Table 1 Pin Functional Description (cont)

Signals	Number of Pins	I/O	Connected to	Functions
OSC1, OSC2	2	I or O	Oscillation-resistor	Connect an external resistor for R-C oscillation. When providing clocks from outside, open OSC2.
RESET*	1	I	MPU or external R-C circuit	Reset pin. Initializes the LSI when low. Must be reset after power-on.
VccDUM		O	Input pins	Outputs the internal V_{CC} level; shorting this pin sets the adjacent input pin to the V_{CC} level.
GNDDUM		O	Input pins	Outputs the internal GND level; shorting this pin sets the adjacent input pin to the GND level.
Dummy		—	—	Dummy pad. Must be left disconnected.
TEST	1	I	GND	Test pin. Must be fixed at GND level.

Block Function Description

System Interface

The HD66763 has five high-speed system interfaces: an 80-system 16-bit/8-bit bus, a 68-system 16-bit/8-bit bus, and a serial peripheral (SPI: Serial Peripheral Interface port). The interface mode is selected by the IM2-0 pins.

The HD66763 has three 16-bit registers: an index register (IR), a write data register (WDR), and a read data register (RDR). The IR stores index information from the control registers and the GRAM. The WDR temporarily stores data to be written into control registers and the GRAM, and the RDR temporarily stores data read from the GRAM. Data written into the GRAM from the MPU is first written into the WDR and then is automatically written into the GRAM by internal operation. Data is read through the RDR when reading from the GRAM, and the first read data is invalid and the second and the following data are normal. When a logic operation is performed inside of the HD66763 by using the display data set in the GRAM and the data written from the MPU, the data read through the RDR is used. Accordingly, the MPU does not need to read data twice nor to fetch the read data into the MPU. This enables high-speed processing.

Execution time for instruction excluding oscillation start is 0 clock cycle and instructions can be written in succession.

Table 2 Register Selection (8/16 Parallel Interface)

80-system Bus		68-system Bus		
WR Bits	RD Bits	R/W Bits	RS Bits	Operations
0	1	0	0	Writes indexes into IR
1	0	1	0	Reads internal status
0	1	0	1	Writes into control registers and GRAM through WDR
1	0	1	1	Reads from GRAM through RDR

Table 3 Register Selection (Serial Peripheral Interface)

Start bytes		
R/W Bits	RS Bits	Operations
0	0	Writes indexes into IR
1	0	Reads internal status
0	1	Writes into control registers and GRAM through WDR
1	1	Reads from GRAM through RDR

Bit Operation

The HD66763 supports the following functions: a swap function that writes the data written from the MPU into the GRAM by reversing the display position vertically in byte units, a write data mask function that selects and writes data into the GRAM in bit units, and a logic operation function that performs logic operations or conditional determination on the display data set in the GRAM and writes into the GRAM. With the 16-bit bus interface, these functions can greatly reduce the processing loads of the MPU graphics software and can rewrite the display data in the GRAM at high speed. For details, see the Graphics Operation Function section.

Address Counter (AC)

The address counter (AC) assigns addresses to the GRAM. When an address set instruction is written into the IR, the address information is sent from the IR to the AC.

After writing into the GRAM, the AC is automatically incremented by 1 (or decremented by 1). After reading from the data, the AC is not updated. A window address function allows for data to be written only to a window area specified by GRAM.

Graphics RAM (GRAM)

The graphics RAM (GRAM) has eight bits/pixel and stores the bit-pattern data of 128 x 176 bytes.

PWM Grayscale Circuit

The PWM grayscale circuit generates a PWM signal that corresponds to the grayscale levels as specified in the grayscale palette register. Any 256 of the 4,096 possible colors can be displayed at the same time. For details, see the Grayscale Palette section.

Grayscale Selection Circuit

The grayscale selection circuit reads data from the GRAM and controls the signal generated in the PWM grayscale circuit. PWM (pulse width modulation) is used to control each color in the display. For details, see the Grayscale Palette section.

Timing Generator

The timing generator generates timing signals for the operation of internal circuits such as the GRAM. The RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interference with one another. The timing generator generates the interface signals (M, FLM, CL1, DISPTMG, and DCCLK) for the common driver.

Oscillation Circuit (OSC)

The HD66763 can provide R-C oscillation simply through the addition of an external oscillation-resistor between the OSC1 and OSC2 pins. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the external-resistor value. Clock pulses can also be supplied externally. Since R-C oscillation stops during the standby mode, current consumption can be reduced. For details, see the Oscillation Circuit section.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 384 segment signal drivers (SEG1 to SEG384).

Display pattern data is latched when 384-bit data has arrived. The latched data then enables the segment signal drivers to generate drive waveform outputs. The shift direction of 384-bit data can be changed by the SGS bit by selecting an appropriate direction for the device mounting configuration.

When multiplexing drive is not used, or during standby mode, all of the common and segment signal drivers listed above, and the common drivers from the HD66764, output the GND level, halting the display.

Interface with Common Driver

A serial interface circuit provides an interface with the HD66764 common driver. When sending an instruction setting from the HD66763 to a common driver, a register setting value from within the HD66763 is transferred via the serial interface circuit. A transfer is started by setting a serial transfer enable in the HD66763. However, transfer to and reading from the common driver are not possible during standby. For details, see the Common Serial Transfer section.

Table Relationship between GRAM address and display position (SGS=0, SWP=0)

SEG/COM pins		SEG1 SEG2 SEG3 SEG4 SEG5 SEG6	SEG7 SEG8 SEG9 SEG10 SEG11 SEG12	• • • • •	SEG373 SEG374 SEG375 SEG376 SEG377 SEG378	SEG379 SEG380 SEG381 SEG382 SEG383 SEG384
CMS=0	CMS=1	DB15 ••• DB8 DB7 ••• DB0	DB15 ••• DB8 DB7 ••• DB0		DB15 ••• DB8 DB7 ••• DB0	DB15 ••• DB8 DB7 ••• DB0
COM1	COM176	"0000"H	"0001"H	• • • • • •	"003E"H	"003F"H
COM2	COM175	"0100"H	"0101"H	• • • • • •	"013E"H	"013F"H
COM3	COM174	"0200"H	"0201"H	• • • • • •	"023E"H	"023F"H
COM4	COM173	"0300"H	"0301"H	• • • • • •	"033E"H	"033F"H
COM5	COM172	"0400"H	"0401"H	• • • • • •	"043E"H	"043F"H
COM6	COM171	"0500"H	"0501"H	• • • • • •	"053E"H	"053F"H
COM7	COM170	"0600"H	"0601"H	• • • • • •	"063E"H	"063F"H
COM8	COM169	"0700"H	"0701"H	• • • • • •	"073E"H	"073F"H
COM9	COM168	"0800"H	"0801"H	• • • • • •	"083E"H	"083F"H
COM10	COM167	"0900"H	"0901"H	• • • • • •	"093E"H	"093F"H
COM11	COM166	"0A00"H	"0A01"H	• • • • • •	"0A3E"H	"0A3F"H
COM12	COM165	"0B00"H	"0B01"H	• • • • • •	"0B3E"H	"0B3F"H
COM13	COM164	"0C00"H	"0C01"H	• • • • • •	"0C3E"H	"0C3F"H
COM14	COM163	"0D00"H	"0D01"H	• • • • • •	"0D3E"H	"0D3F"H
COM15	COM162	"0E00"H	"0E01"H	• • • • • •	"0E3E"H	"0E3F"H
COM16	COM161	"0F00"H	"0F01"H	• • • • • •	"0F3E"H	"0F3F"H
COM17	COM160	"1000"H	"1001"H	• • • • • •	"103E"H	"103F"H
COM18	COM159	"1100"H	"1101"H	• • • • • •	"113E"H	"113F"H
COM19	COM158	"1200"H	"1201"H	• • • • • •	"123E"H	"123F"H
COM20	COM157	"1300"H	"1301"H	• • • • • •	"133E"H	"133F"H
• •	• •	• •	• •		• •	• •
COM169	COM8	"A800"H	"A801"H	• • • • • •	"A83E"H	"A83F"H
COM170	COM7	"A900"H	"A901"H	• • • • • •	"A93E"H	"A93F"H
COM171	COM6	"AA00"H	"AA01"H	• • • • • •	"AA3E"H	"AA3F"H
COM172	COM5	"AB00"H	"AB01"H	• • • • • •	"AB3E"H	"AB3F"H
COM173	COM4	"AC00"H	"AC01"H	• • • • • •	"AC3E"H	"AC3F"H
COM174	COM3	"AD00"H	"AD01"H	• • • • • •	"AD3E"H	"AD3F"H
COM175	COM2	"AE00"H	"AE01"H	• • • • • •	"AE3E"H	"AE3F"H
COM176	COM1	"AF00"H	"AF01"H	• • • • • •	"AF3E"H	"AF3F"H

Table Relationship between GRAM data and output pin (SGS=0)

GRAM data	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Selected palette	RK palette			GK palette			BK palette		RK palette			GK palette			BK palette	
Output pin	SEG (6n+1)			SEG (6n+2)			SEG (6n+3)		SEG (6n+4)			SEG (6n+5)			SEG (6n+6)	

n = Lower 6-bits address (0 to 63)

Table Relationship between GRAM address and display position (SGS=1, SWP=0)

SEG/COM pins		SEG1 SEG2 SEG3 SEG4 SEG5 SEG6	SEG7 SEG8 SEG9 SEG10 SEG11 SEG12	• • • • •	SEG373 SEG374 SEG375 SEG376 SEG377 SEG378	SEG379 SEG380 SEG381 SEG382 SEG383 SEG384
CMS=0	CMS=1	DB0 • • • DB7 ⋮ DB8 • • • DB15	DB0 • • • DB7 ⋮ DB8 • • • DB15	• • • • •	DB0 • • • DB7 ⋮ DB8 • • • DB15	DB0 • • • DB7 ⋮ DB8 • • • DB15
COM1	COM176	"003F"H	"003E"H	• • • • •	"0001"H	"0000"H
COM2	COM175	"013F"H	"013E"H	• • • • •	"0101"H	"0100"H
COM3	COM174	"023F"H	"023E"H	• • • • •	"0201"H	"0200"H
COM4	COM173	"033F"H	"033E"H	• • • • •	"0301"H	"0300"H
COM5	COM172	"043F"H	"043E"H	• • • • •	"0401"H	"0400"H
COM6	COM171	"053F"H	"053E"H	• • • • •	"0501"H	"0500"H
COM7	COM170	"063F"H	"063E"H	• • • • •	"0601"H	"0600"H
COM8	COM169	"073F"H	"073E"H	• • • • •	"0701"H	"0700"H
COM9	COM168	"083F"H	"083E"H	• • • • •	"0801"H	"0800"H
COM10	COM167	"093F"H	"093E"H	• • • • •	"0901"H	"0900"H
COM11	COM166	"0A3F"H	"0A3E"H	• • • • •	"0A01"H	"0A00"H
COM12	COM165	"0B3F"H	"0B3E"H	• • • • •	"0B01"H	"0B00"H
COM13	COM164	"0C3F"H	"0C3E"H	• • • • •	"0C01"H	"0C00"H
COM14	COM163	"0D3F"H	"0D3E"H	• • • • •	"0D01"H	"0D00"H
COM15	COM162	"0E3F"H	"0E3E"H	• • • • •	"0E01"H	"0E00"H
COM16	COM161	"0F3F"H	"0F3E"H	• • • • •	"0F01"H	"0F00"H
COM17	COM160	"103F"H	"103E"H	• • • • •	"1001"H	"1000"H
COM18	COM159	"113F"H	"113E"H	• • • • •	"1101"H	"1100"H
COM19	COM158	"123F"H	"123E"H	• • • • •	"1201"H	"1200"H
COM20	COM157	"133F"H	"133E"H	• • • • •	"1301"H	"1300"H
• •	• •	• •	• •		• •	• •
COM169	COM8	"A83F"H	"A83E"H	• • • • •	"A801"H	"A800"H
COM170	COM7	"A93F"H	"A93E"H	• • • • •	"A901"H	"A900"H
COM171	COM6	"AA3F"H	"AA3E"H	• • • • •	"AA01"H	"AA00"H
COM172	COM5	"AB3F"H	"AB3E"H	• • • • •	"AB01"H	"AB00"H
COM173	COM4	"AC3F"H	"AC3E"H	• • • • •	"AC01"H	"AC00"H
COM174	COM3	"AD3F"H	"AD3E"H	• • • • •	"AD01"H	"AD00"H
COM175	COM2	"AE3F"H	"AE3E"H	• • • • •	"AE01"H	"AE00"H
COM176	COM1	"AF3F"H	"AF3E"H	• • • • •	"AF01"H	"AF00"H

Table Relationship between GRAM data and output pin (SGS=1)

GRAM data	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
Selected palette	RK palette			GK palette			BK palette		RK palette			GK palette			BK palette	
Output pin	SEG (384-6n)			SEG (383-6n)			SEG (382-6n)		SEG (381-6n)			SEG (380-6n)			SEG (379-6n)	

n = Lower 6-bits address (0 to 63)

Instructions

Outline

The HD66763 uses the 16-bit bus architecture. Before the internal operation of the HD66763 starts, control information is temporarily stored in the registers described below to allow high-speed interfacing with a high-performance microcomputer. The internal operation of the HD66763 is determined by signals sent from the microcomputer. These signals, which include the register selection signal (RS), the read/write signal (R/W), and the data bus signals (DB15 to DB0), make up the HD66763 instructions. There are nine categories of instructions that:

- Specify the index
- Read the status
- Control the display
- Control power management
- Process the graphics data
- Set internal GRAM addresses
- Transfer data to and from the internal GRAM
- Set grayscale level for the internal grayscale palette table
- Interface with the common driver

Normally, instructions that write data are used the most. However, an auto-update of internal GRAM addresses after each data write can lighten the microcomputer program load.

Because instructions are executed in 0 cycles, they can be written in succession.

Instruction Descriptions

Index

The index instruction specifies the RAM control indexes (R00h to R39h). It sets the register number in the range of 00000 to 111001 in binary form. However, R40 to R44 are disabled since they are test registers.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Figure 1 Index Instruction

Status Read

The status read instruction reads the internal status of the HD66763.

L7–0: Indicate the driving raster-row position where the liquid crystal display is being driven.

C6–0: Read the contrast setting values (CT6–0).

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	C6	C5	C4	C3	C2	C1	C0

Figure 2 Status Read Instruction

Start Oscillation (R00h)

The start oscillation instruction restarts the oscillator from the halt state in the standby mode. After issuing this instruction, wait at least 10 ms for oscillation to stabilize before issuing the next instruction. (See the Standby Mode section.)

If this register is read forcibly, *763H is read.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1	0	0	0	0	0	1	1	1	0	1	1	0	0	0	1	1

Figure 3 Start Oscillation Instruction

Driver Output Control (R01h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	0	CMS	SGS	0	0	0	NL4	NL3	NL2	NL1	NL0

Figure 4 Driver Output Control Instruction

CMS: Selects the output shift direction of a common driver. When CMS = 0, COM1 shifts to COM168. When CMS = 1, COM168 shifts to COM1.

SGS: Selects the output shift direction of a segment driver by using with the SWP bit. When SGS = 0 and SWP = 0, SEG1 shifts to SEG384. When SGS = 1 and SWP=1, SEG384 shifts to SEG1. When SGS = 0 and SWP = 0, the SEG1 pin assigns the color display to R, G, or B. When SGS = 1 and SWP = 1, the SEG384 pin assigns R, G, or B to the color display. Re-write to the RAM when intending to change the SGS bit.

Note: The CMS bit is for setting the common driver. Control according to the bit's value is executed by the common driver. For details, see the data sheet for the common driver.

NL4–0: Specify the LCD drive duty ratio. The duty ratio can be adjusted for every eight raster-rows. GRAM address mapping does not depend on the setting value of the drive duty ratio.

Table 8 NL Bits and Drive Duty

NL4	NL3	NL2	NL1	NL0	Display Size	LCD Drive Duty	Common Driver Used
0	0	0	0	0	Setting disabled	Setting disabled	Setting disabled
0	0	0	0	1	384 x 16 dots	1/16 Duty	COM1–COM16
0	0	0	1	0	384 x 24 dots	1/24 Duty	COM1–COM24
0	0	0	1	1	384 x 32 dots	1/32 Duty	COM1–COM32
0	0	1	0	0	384 x 40 dots	1/40 Duty	COM1–COM40
0	0	1	0	1	384 x 48 dots	1/48 Duty	COM1–COM48
0	0	1	1	0	384 x 56 dots	1/56 Duty	COM1–COM56
0	0	1	1	1	384 x 64 dots	1/64 Duty	COM1–COM64
0	1	0	0	0	384 x 72 dots	1/72 Duty	COM1–COM72
0	1	0	0	1	384 x 80 dots	1/80 Duty	COM1–COM80
0	1	0	1	0	384 x 88 dots	1/88 Duty	COM1–COM88
0	1	0	1	1	384 x 96 dots	1/96 Duty	COM1–COM96
0	1	1	0	0	384 x 104 dots	1/104 Duty	COM1–COM104
0	1	1	0	1	384 x 112 dots	1/112 Duty	COM1–COM112
0	1	1	1	0	384 x 120 dots	1/120 Duty	COM1–COM120
0	1	1	1	1	384 x 128 dots	1/128 Duty	COM1–COM128
1	0	0	0	0	384 x 136 dots	1/136 Duty	COM1–COM136
1	0	0	0	1	384 x 144 dots	1/144 Duty	COM1–COM144
1	0	0	1	0	384 x 152 dots	1/152 Duty	COM1–COM152
1	0	0	1	1	384 x 160 dots	1/160 Duty	COM1–COM160
1	0	1	0	0	384 x 168 dots	1/168 Duty	COM1–COM168
1	0	1	0	1	384 x 176 dots	1/176 Duty	COM1–COM176

LCD-Driving-Waveform Control (R02h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	0	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0

Figure 5 LCD-Driving-Waveform Control Instruction

B/C: When B/C = 0, a B-pattern waveform is generated and alternates in every frame for LCD drive. When B/C = 1, a C-pattern waveform is generated and alternates in each raster-row specified by bits EOR and NW4–NW0 in the LCD-driving-waveform control register. For details, see the n-raster-row Reversed AC Drive section.

EOR: When the C-pattern waveform is set (B/C = 1) and EOR = 1, the odd/even frame-select signals and the n-raster-row reversed signals are EORed for alternating drive. EOR is used when the LCD is not alternated by combining the set values of the LCD drive duty ratio and the n raster-row. For details, see the n-raster-row Reversed AC Drive section.

NW5–0: Specify the number of raster-rows n that will alternate at the C-pattern waveform setting (B/C = 1). NW4–NW0 alternate for every set value + 1 raster-row, and the first to the 64th raster-rows can be selected.

Power Control 1 (R03h)

Power Control 2 (R0Ch)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	BS2	BS1	BS0	BT3	BT2	BT1	BT0	0	DC2	DC1	DC0	AP1	AP0	SLP	STB
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VC2	VC1	VC0

Figure 6 Power Control Instruction

BS2–0: The LCD drive bias value is set. The LCD drive bias value can be selected according to its drive duty ratio and voltage.

BT3–0: The output factor of step-up is switched. The LCD drive voltage level can be selected according to its drive duty ratio and bias. Lower amplification of the step-up circuit consumes less current.

DC2–0: The operating frequency in the step-up circuit is selected. When the step-up operating frequency is high, the driving ability of the step-up circuit and the display quality become high, but the current consumption is increased. Adjust the frequency considering the display quality and the current consumption.

AP1–0: The amount of fixed current from the fixed current source in the operational amplifier for the LCD is adjusted. When the amount of fixed current is large, the LCD driving ability and the display quality become high, but the current consumption is increased. Adjust the fixed current considering the display quality and the current consumption.

During no display, when AP1–0 = 00, the current consumption can be reduced by ending the operational amplifier and step-up circuit operation.

VC2-0: Sets an adjustment factor for the Vci voltage (VC2-0).

SLP: When SLP = 1, the HD66763 enters the sleep mode, where the internal display operations are halted except for the R-C oscillator, thus reducing current consumption. Only the following instructions can be executed during the sleep mode.

Power control (BS2–0, BT3–0, DC2–0, AP1–0, SLP, and STB bits)

Common interface control (TE, IDX)

During the sleep mode, the other GRAM data and instructions cannot be updated although they are retained.

Note: BS2-0, BT3-0, DC2-0, AP1-0, VC2-0 and SLP bits are for setting the common driver. Control according to the bits' values is executed by the common driver. For details, see the data sheet for the common driver.

STB: When STB = 1, the HD66763 enters the standby mode, where display operation completely stops, halting all the internal operations including the internal R-C oscillator. Further, no external clock pulses are supplied. For details, see the Standby Mode section.

Only the following instructions can be executed during the standby mode.

a. Standby mode cancel (STB = 0)
b. Start oscillation

During the standby mode, the GRAM data and instructions may be lost. To prevent this, they must be set again after the standby mode is canceled. Serial transfer to the common driver is not possible when it is in standby mode. Transfer the data again after it has been released from standby mode.

Contrast Control (R04h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	VR3	VR2	VR1	VR0	0	CT6	CT5	CT4	CT3	CT2	CT1	CT0

Figure 7 Contrast Control Instruction

CT6–0: These bits control the LCD drive voltage (potential difference between V1 and GND) to adjust 128-step contrast. For details, see the Contrast Adjuster section.

VR3–0: These bits adjust the output voltage in the LCD drive reference generator.

Note: CT6-0 and VR3-0 bits are for setting the common driver. Control according to the bits' values is executed by the common driver. For details, see the data sheet for the common driver.

Entry Mode (R05h)

Compare Register (R06h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	0	HWM	SWP	0	0	I/D1	I/D0	AM	LG2	LG1	LG0
W	1	0	0	0	0	0	0	0	0	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0

Figure 8 Entry Mode and Compare Register Instruction

The write data sent from the microcomputer is modified in the HD66763 and written to the GRAM. The display data in the GRAM can be quickly rewritten to reduce the load of the microcomputer software processing. For details, see the Graphics Operation Function section.

HWM: When HWM=1, data can be written to the GRAM at high speed. In high-speed write mode, four words of data are written to the GRAM in a single operation after writing to RAM four times. Write to RAM four times, otherwise the four words cannot be written to the GRAM. Thus, set the lower 2 bits to 0 when setting the RAM address. For details, see High-Speed RAM Write Mode section.

SWP: When SWP = 1, the upper and lower bytes in the two-byte data sent from the microcomputer are swapped and written to the GRAM. When SWP = 0, this bit directly writes the two-byte data sent from the microcomputer to the GRAM. This swap processing is performed only for the data sent from the microcomputer before logical operation. When SWP = 1, the upper and lower bytes in the write data mask (WM15–0) are swapped to be executed with the write data.

I/D1-0: When I/D1-0 = 1, the address counter (AC) is automatically incremented by 1 after the data is written to the GRAM. When I/D1-0 = 0, the AC is automatically decremented by 1 after the data is written to the GRAM. The increment/decrement setting of the address counter by I/D1-0 is done independently for the upper (AD15-8) and lower (AD5-0) addresses. The direction of moving through the addresses when the GRAM is written to is set by the AM bit.

AM: Set the automatic update method of the AC after the data is written to the GRAM. When AM = 0, the data is continuously written in parallel. When AM = 1, the data is continuously written vertically. When window address range is specified, the GRAM in the window address range can be written to according to the I/D1-0 and AM settings.

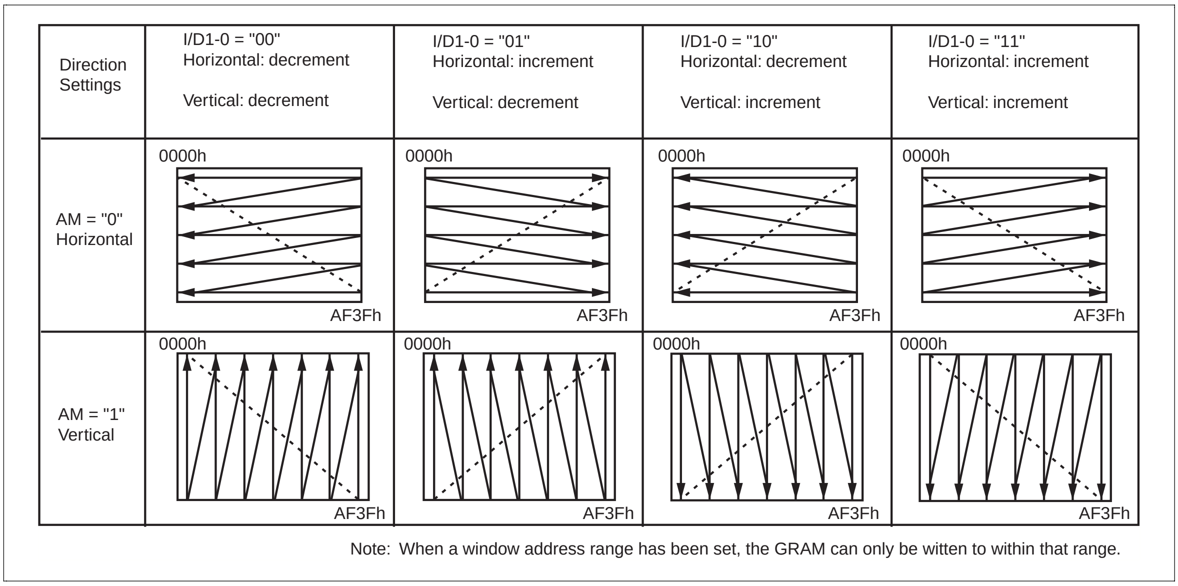


Figure 9 Address Direction Settings

LG2–0: Compare the data read from the GRAM by the microcomputer with the compare registers (CP7–0) by a compare/logical operation and write the results to GRAM. For details, see the Logical/Compare Operation Function.

CP7–0: Set the compare register for the compare operation with the data read from the GRAM or written by the microcomputer.

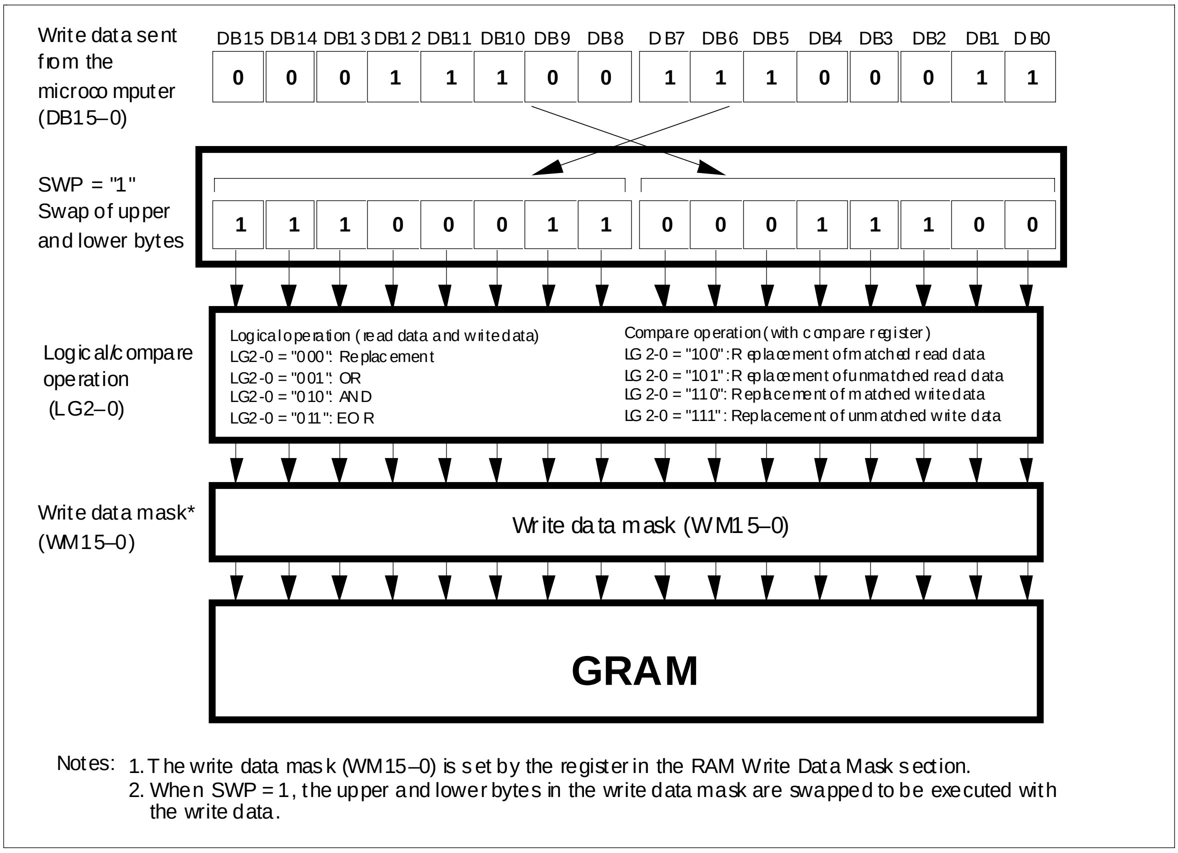


Figure 10 Logical/Compare Operation and Swapping for the GRAM

Display Control (R07h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	VLE2	VLE1	SPT	0	0	0	0	0	REV	D1	D0

Figure 11 Display Control Instruction

VLE2–1: When VLE1 = 1, a vertical scroll is performed in the 1st screen. When VLE2 = 1, a vertical scroll is performed in the 2nd screen. Vertical scrolling on the two screens can be independently controlled.

SPT: When SPT = 1, the 2-division LCD drive is performed. For details, see the Screen-division Driving Function section.

REV: Displays all character and graphics display sections with reversal when REV = 1. For details, see the Reversed Display Function section. Since the grayscale level can be reversed, display of the same data is enabled on normally-white and normally-black panels.

D1–0: Display is on when D1 = 1 and off when D1 = 0. When off, the display data remains in the GRAM, and can be displayed instantly by setting D1 = 1. When D1 is 0, the display is off with all of the SEG/COM pin outputs set to the GND level. Because of this, the HD66763 can control the charging current for the LCD with AC driving.

When D1–0 = 01, the internal display of the HD66763 is performed although the display is off. When D1-0 = 00, the internal display operation halts and the display is off.

Table 9 D Bits and Operation

D1	D0	SEG/COM Output	HD66763 Internal Display Operation	Master/Slave Signal (CL1, FLM, M, and DISPTMG)
0	0	GND	Halt	Halt
0	1	GND	Operate	Operate
1	0	Unlit display	Operate	Operate
1	1	Display	Operate	Operate

Notes: 1. Writing from the microcomputer to the GRAM is independent from D1–0.
2. In the sleep and standby modes, D1–0 = 00. However, the register contents of D1–0 are not modified.

Note: SPT and D1 bits are for setting the common driver. Control according to the bits' values is executed by the common driver. For details, see the data sheet for the common driver.

COM Driver Interface Control (R0Ah)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	0	0	TE	0	0	0	0	0	IDX2	IDX1	IDX0
R	1	0	0	0	0	0	0	0	TE	0	0	0	0	0	IDX2	IDX1	IDX0

Figure 12 COM Driver Interface Control Instruction

IDX2-0: Index bits that select instructions for the common driver. The instruction that corresponds to the setting made here is transferred, with the index, to the common driver via the serial interface. These instructions are transferred in bit rows as shown below. The upper 3 bits correspond to IDX2-0. The IDX2-0 setting at the time of transfer selects the instruction for the common driver as listed below.

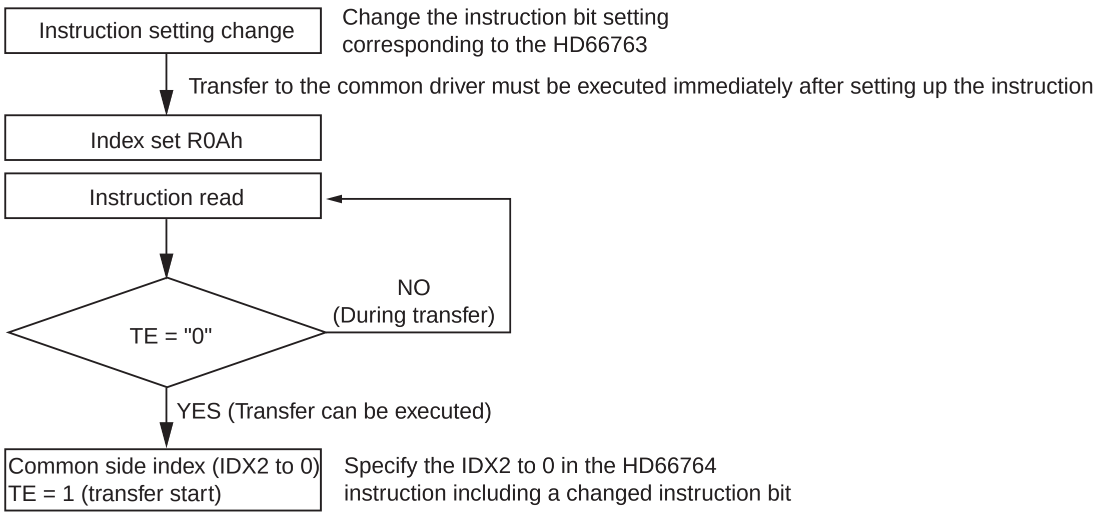
To change an instruction setting on the common driver, first change the instruction bit on the HD66763, select the instruction, which includes the changed instruction bit, from the list below, by setting IDX2-0 as required. The instruction is transferred to the common driver as the transfer starts (TE=1), and is the executed.

TE: Serial transfer enable for the common driver. When TE=0, serial transfer is possible. Do not change the instruction during transfer. When TE=1, transfer starts. TE returning to 0 indicates the end of the transfer. Note that, serial transfer to the common driver requires 18 clock cycles at most. Do not change the instruction during the transfer.

* New instructions should be transferred to the common driver soon after they have been set on the HD66763.

Table of common driver (HD66764) instructions

IDX2	IDX1	IDX0	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	BS2	BS1	BS0	BT3	BT2	BT1	BT0	DC2	DC1	DC0	AP1	AP0	SLP
0	0	1	0	0	0	0	0	0	0	0	0	0	VC2	VC1	VC0
0	1	0	0	VR3	VR2	VR1	VR0	0	CT6	CT5	CT4	CT3	CT2	CT1	CT0
0	1	1	0	0	D1	CMS	SPT	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
1	0	0	0	0	0	0	0	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10
1	0	1	0	0	0	0	0	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20
1	1	0	0	0	0	0	0	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20



Notes:
1. Transfer to the common driver must take place immediately after setting up the instruction.
2. The serial transfer period takes a maximum of 1/fosc x 18 clock cycles (sec).
3. Serial transfer cannot be executed in standby mode. If the chip enters standbymode during transfer, the serial transfer is forcibly suspended. Transfer must be executed again because correct transfer is not guaranteed in this situation.
4. Serial transfer can be forcibly suspended by writing TE = 0. Transfer must be executed again because correct transfer is not guaranteed in this situation.
5. Do not enter standby mode during transfer or forcibly terminate transfer except in case of emergency. Before executing, confirm that the transfer is completed.

Figure 13 Common Interface: Serial Transfer Sequence

Frame Cycle Control (R0Bh)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	0	DIV1	DIV0	0	0	0	0	RTN 3	RTN 2	RTN 1	RTN 0

Figure 14 Frame Cycle Control Instruction

RTN3-0: Set the line retrace period (RTN3-0) to be added to raster-row cycles. The raster-row cycle becomes longer according to the number of clocks set at RTN3-0.

DIV1-0: Set the division ratio of clocks for internal operation (DIV1-0). Internal operations are driven by clocks which are frequency divided according to the DIV1-0 setting. Frame frequency can be adjusted along with the line retrace period (RTN3-0). When changing the drive-duty cycle, adjust the frame frequency. For details, see the Frame Frequency Adjustment Function section.

Table 10 RTN Bits and Clock Cycles

RTN3	RTN2	RTN1	RTN0	Line Retrace Period (Clock Cycles)	Clock Cycles per Raster-row
0	0	0	0	0	17
0	0	0	1	1	18
0	0	1	0	2	19
0	0	1	1	3	20
:	:	:	:	:	:
1	1	1	0	14	31
1	1	1	1	15	32

Table 11 DIV Bits and Clock Frequency

DIV1	DIV0	Division Ratio	Internal Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

* fosc = R-C oscillation frequency

Formula for the frame frequency

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{Clock cycles per raster-row} \times \text{division ratio} \times 1/\text{duty cycle}} \text{ [Hz]}$$

fosc: R-C oscillation frequency

Duty: drive duty (NL bit)

Division ratio: DIV bit

Clock cycles per raster-row: (RTN + 17) clock cycles

Vertical Scroll Control (R11h)

VL17–10: Specify the display-start raster-row at the 1st screen display for vertical smooth scrolling. Any raster-row from the first to 176th can be selected. After the 176th raster-row is displayed, the display restarts from the first raster-row. The display-start raster-row (VL17–10) is valid only when VLE1 = 1. The raster-row display is fixed when VLE1 = 0. (VLE1 is the 1st-screen vertical-scroll enable bit.)

VL27–20: Specify the display-start raster-row at the 2nd screen display. The display-start raster-row (VL27–20) is valid only when VLE2 = 1. The raster-row display is fixed when VLE2 = 0. (VLE2 is the 2nd-screen vertical-scroll enable bit.) The vertical scroll for the 1st and 2nd screens can be independently set.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	VL 27	VL 26	VL 25	VL 24	VL 23	VL 22	VL 21	VL 20	VL 17	VL 16	VL 15	VL 14	VL 13	VL 12	VL 11	VL 10

Figure 15 Vertical Scroll Control Instruction

Table 22 VL Bits and Display-start Raster-row

VL27 VL17	VL26 VL16	VL25 VL15	VL24 VL14	VL23 VL13	VL22 VL12	VL21 VL11	VL20 VL10	Display-start Raster-row
0	0	0	0	0	0	0	0	1st raster-row
0	0	0	0	0	0	0	1	2nd raster-row
0	0	0	0	0	0	1	0	3rd raster-row
:	:	:	:	:	:	:	:	:
1	0	1	0	1	1	1	0	175th raster-row
1	0	1	0	1	1	1	1	176th raster-row

Note: Do not set over the 176th (AFH) raster-row.

1st Screen Driving Position (R14h)

2nd Screen Driving Position (R15h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
W	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20

Figure 16 1st Screen Driving Position and 2nd Screen Driving Position Instructions

SS17–0: Specify the driving start position for the first screen in a line unit. The LCD driving starts from the 'set value + 1' common driver.

SE17–0: Specify the driving end position for the first screen in a line unit. The LCD driving is performed to the 'set value + 1' common driver. For instance, when SS17–10 = 07H and SE17–10 = 10H are set, the LCD driving is performed from COM8 to COM17, and non-selection driving is performed for COM1 to COM7, COM18, and others. Ensure that SS17–10 ≤ SE17–10 ≤ AFH. For details, see the Screen-division Driving Function section.

SS27–0: Specify the driving start position for the second screen in a line unit. The LCD driving starts from the 'set value + 1' common driver. The second screen is driven when SPT = 1.

SE27–0: Specify the driving end position for the second screen in a line unit. The LCD driving is performed to the 'set value + 1' common driver. For instance, when SPT = 1, SS27–20 = 20H, and SE27–20 = AFH are set, the LCD driving is performed from COM33 to COM80. Ensure that SS17–10 ≤ SE17–10 ≤ SS27–20 ≤ SE27–20 ≤ 4FH. For details, see the Screen-division Driving Function section.

Horizontal RAM Address Position (R16h)

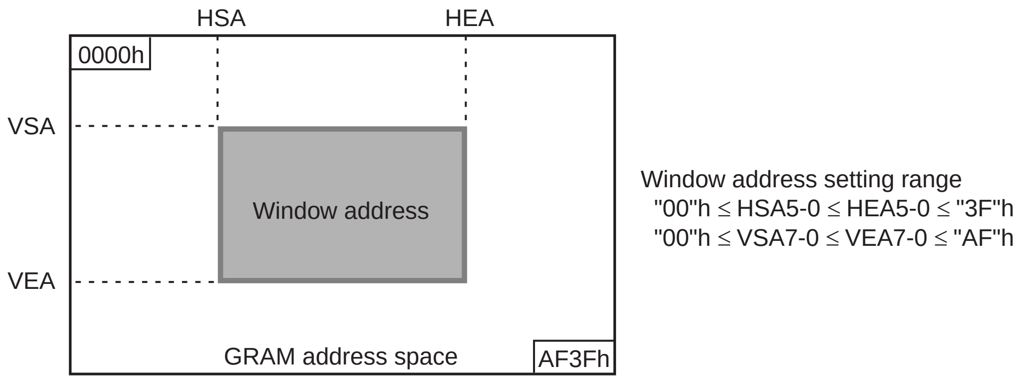
Vertical RAM Address Position (R17h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	HEA 5	HEA 4	HEA 3	HEA 2	HEA 1	HEA 0	0	0	HSA 5	HSA 4	HSA 3	HSA 2	HSA 1	HSA 0
W	1	VEA 7	VEA 6	VAE 5	VEA 4	VEA 3	VEA 2	VEA 1	VEA 0	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0

Figure 17 Horizontal/Vertical RAM Address Position Instruction

HSA5-0/HEA5-0: Specify the horizontal start/end positions of a window for access in memory. Data can be written to the GRAM from the address specified by HEA5-0 from the address specified by HSA5-0. Note that an address must be set before RAM is written to. Ensure 00h ≤ HSA5-0 ≤ HEA5-0 ≤ 3Fh.

VSA7-0/VEA7-0: Specify the vertical start/end positions of a window for access in memory. Data can be written to the GRAM from the address specified by VEA7-0 from the address specified by VSA7-0. Note that an address must be set before RAM is written to. Ensure 00h ≤ VSA7-0 ≤ VEA7-0 ≤ AFh.



Note: 1. Ensure that the window address area is within the GRAM address space.
2. In high-speed write mode, data are written to GRAM in four-words. Thus, dummy write operations should be inserted depending on the window address area. For details, see the High-Speed Burst RAM Write Function section.

Figure 18 Window Address Setting Range

RAM Write Data Mask (R20h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	WM 15	WM 14	WM 13	WM 12	WM 11	WM 10	WM 9	WM 8	WM 7	WM 6	WM 5	WM 4	WM 3	WM 2	WM 1	WM 0

Figure 19 RAM Write Data Mask Instruction

WM15–0: In writing to the GRAM, these bits mask writing in a bit unit. When WM15 = 1, this bit masks the write data of DB15 and does not write to the GRAM. Similarly, the WM14–0 bits mask the write data of DB14–0 in a bit unit. When SWP = 1, the upper and lower bytes in the write data mask are swapped. For details, see the Graphics Operation Function section.

RAM Address Set (R21h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	AD 15	AD 14	AD 13	AD 12	AD 11	AD 10	AD9	AD8	0	0	AD5	AD4	AD3	AD2	AD1	AD0

Figure 20 RAM Address Set Instruction

AD15–0: Initially set GRAM addresses to the address counter (AC). Once the GRAM data is written, the AC is automatically updated according to the AM and I/D bit settings. This allows consecutive accesses without resetting addresses. Once the GRAM data is read, the AC is not automatically updated. GRAM address setting is not allowed in the standby mode. Ensure that the address is set within the specified window address.

Table 13 GRAM Address Range in Eight-grayscale Mode

AD14–AD0	GRAM Setting
"0000"H–"003F"H	Bitmap data for COM1
"0100"H–"013F"H	Bitmap data for COM2
"0200"H–"023F"H	Bitmap data for COM3
"0300"H–"033F"H	Bitmap data for COM4
:	:
"AC00"H–"AC3F"H	Bitmap data for COM173
"AD00"H–"AD3F"H	Bitmap data for COM174
"AE00"H–"AE3F"H	Bitmap data for COM175
"AF00"H–"AF3F"H	Bitmap data for COM176

Write Data to GRAM (R22h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	WD 15	WD 14	WD 13	WD 12	WD 11	WD 10	WD 9	WD 8	WD 7	WD 6	WD 5	WD 4	WD 3	WD 2	WD 1	WD 0

Figure 21 Write Data to GRAM Instruction

WD15–0 : Write 16-bit data to the GRAM. This data calls each grayscale palette. After a write, the address is automatically updated according to the AM and I/D bit settings. During the standby mode, the GRAM cannot be accessed.

	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
[GRAM write data]	WD 15	WD 14	WD 13	WD 12	WD 11	WD 10	WD 9	WD 8	WD 7	WD 6	WD 5	WD 4	WD 3	WD 2	WD 1	WD 0
[Eight-grayscale mode]	R2	R1	R0	G2	G1	G0	B1	B0	R2	R1	R0	G2	G1	G0	B1	B0

1 pixel

Figure 22 GRAM Write Data Instruction

Table 14 GRAM Data in the Eight-grayscale Mode (R Grayscale Palette)

GRAM Data Setting						
R2	**R1**	**R0**	**<R> Grayscale Palette**			
0	0	0	RK03	RK02	RK01	RK00
0	0	1	RK13	RK12	RK11	RK10
0	1	0	RK23	RK22	RK21	RK20
0	1	1	RK33	RK32	RK31	RK30
1	0	0	RK43	RK42	RK41	RK40
1	0	1	RK53	RK52	RK51	RK50
1	1	0	RK63	RK62	RK61	RK60
1	1	1	RK73	RK72	RK71	RK70

Table 15 GRAM Data in the Eight-grayscale Mode (G Grayscale Palette)

GRAM Data Setting						
G2	**G1**	**G0**	**<G> Grayscale Palette**			
0	0	0	GK03	GK02	GK01	GK00
0	0	1	GK13	GK12	GK11	GK10
0	1	0	GK23	GK22	GK21	GK20
0	1	1	GK33	GK32	GK31	GK30
1	0	0	GK43	GK42	GK41	GK40
1	0	1	GK53	GK52	GK51	GK50
1	1	0	GK63	GK62	GK61	GK60
1	1	1	GK73	GK72	GK71	GK70

Table 16 GRAM Data in the Eight-grayscale Mode (B Grayscale Palette)

GRAM Data Setting					
B1	**B0**	**<B> Grayscale Palette**			
0	0	BK03	BK02	BK01	BK00
0	1	BK13	BK12	BK11	BK10
1	0	BK23	BK22	BK21	BK20
1	1	BK33	BK32	BK31	BK30

Read Data from GRAM (R22h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R	**1**	**RD 15**	**RD 14**	**RD 13**	**RD 12**	**RD 11**	**RD 10**	**RD 9**	**RD 8**	**RD 7**	**RD 6**	**RD 5**	**RD 4**	**RD 3**	**RD 2**	**RD 1**	**RD 0**

Figure 23 Read Data from GRAM Instruction

RD15–0: Read 16-bit data from the GRAM. When the data is read to the microcomputer, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data on the data bus (DB15–0) becomes invalid and the second-word read is normal.

When bit processing, such as a logical operation, is performed within the HD66763, only one read can be processed since the latched data in the first word is used.

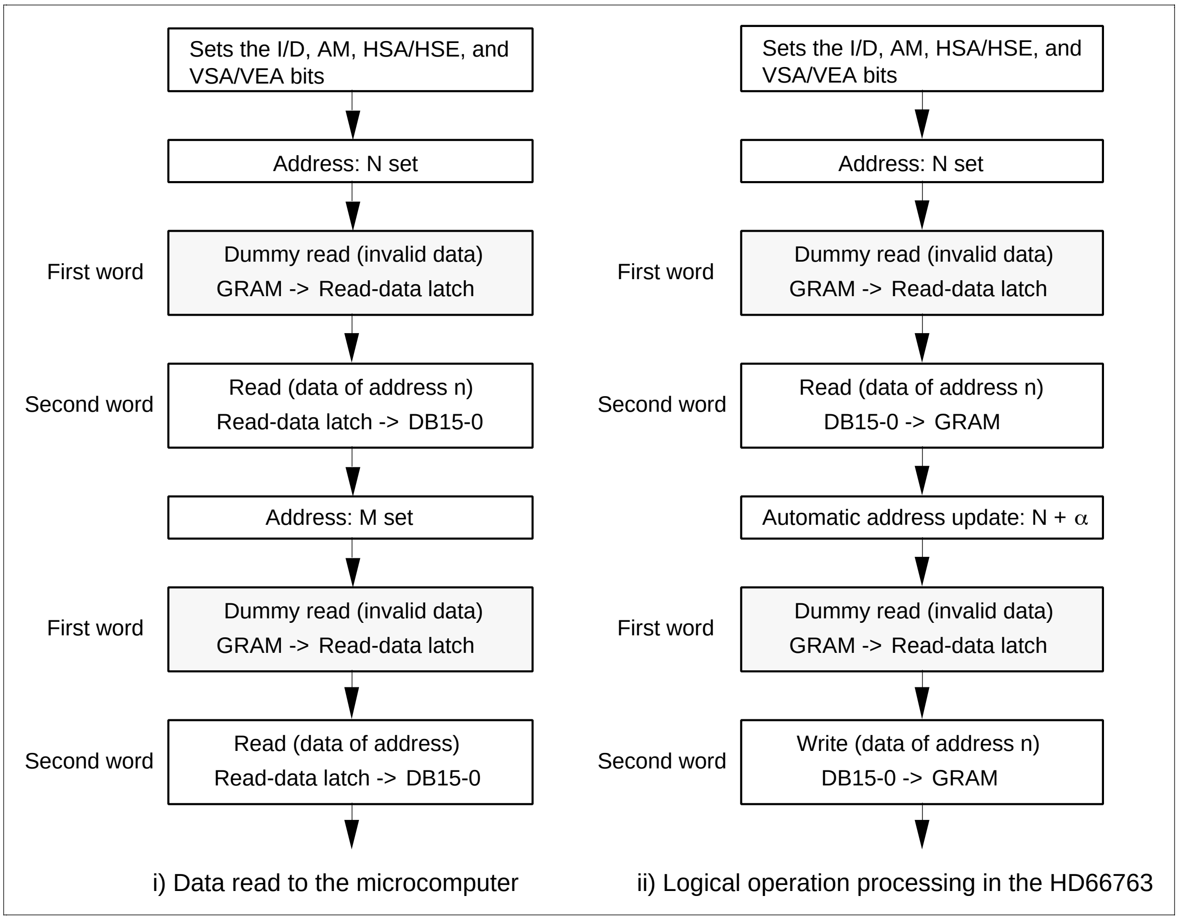


Figure 24 GRAM Read Sequence

Grayscale Palette Control (R30h to R39h)

	R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R30	W	1	0	0	0	0	RK 13	RK 12	RK 11	RK 10	0	0	0	0	RK 03	RK 02	RK 01	RK 00
R31	W	1	0	0	0	0	RK 33	RK 32	RK 31	RK 30	0	0	0	0	RK 23	RK 22	RK 21	RK 20
R32	W	1	0	0	0	0	RK 53	RK 52	RK 51	RK 50	0	0	0	0	RK 43	RK 42	RK 41	RK 40
R33	W	1	0	0	0	0	RK 73	RK 72	RK 71	RK 70	0	0	0	0	RK 63	RK 62	RK 61	RK 60
R34	W	1	0	0	0	0	GK 13	GK 12	GK 11	GK 10	0	0	0	0	GK 03	GK 02	GK 01	GK 00
R35	W	1	0	0	0	0	GK 33	GK 32	GK 31	GK 30	0	0	0	0	GK 23	GK 22	GK 21	GK 20
R36	W	1	0	0	0	0	GK 53	GK 52	GK 51	GK 50	0	0	0	0	GK 43	GK 42	GK 41	GK 40
R37	W	1	0	0	0	0	GK 73	GK 72	GK 71	GK 70	0	0	0	0	GK 63	GK 62	GK 61	GK 60
R38	W	1	0	0	0	0	BK 13	BK 12	BK 11	BK 10	0	0	0	0	BK 03	BK 02	BK 01	BK 00
R39	W	1	0	0	0	0	BK 33	BK 32	BK 31	BK 30	0	0	0	0	BK 23	BK 22	BK 21	BK 20

Figure 25 Grayscale Palette Control Instruction

RK73–00: Specify the R-grayscale level for eight palettes from the 16-grayscale level. For details, see the Grayscale Palette and Grayscale Palette Table sections.

GK73–00: Specify the G-grayscale level for eight palettes from the 16-grayscale level. For details, see the Grayscale Palette and Grayscale Palette Table sections.

BK33–00: Specify the B-grayscale level for four palettes from the 16-grayscale level. For details, see the Grayscale Palette and Grayscale Palette Table sections.

Reset Function

The HD66763 is internally initialized by RESET input. Reset the common driver as its settings are not automatically reinitialized when the HD66763 is reset. The reset input must be held for at least 1 ms. Do not access the GRAM or initially set the instructions until the R-C oscillation frequency is stable after power has been supplied (10 ms).

Instruction Set Initialization:

1. Start oscillation executed
2. Driver output control (NL4–0 = 10101, SGS = 0, CMS = 0)
3. B-pattern waveform AC drive (B/C = 0, ECR = 0, NW5–0 = 00000)
4. Power control 1 (DC2–0 = 000, AP1–0 = 00: LCD power off, STB = 0: Standby mode off, SLP = 0, BS2-0 = 000, BT2-0 = 000)
5. Contrast control (Weak contrast (VR3-0 = 0000, CT6–0 = 0000000))
6. Entry mode set (HWM = 0, SWP = 0, I/D1-0 = 11: Increment by 1, AM = 0: Horizontal move, LG2–0 = 000: Replace mode)
7. Compare register (CP7–0: 00000000)
8. Display control (VLE2–1 = 00: No vertical scroll, SPT = 0, REV = 0, D1–0 = 00: Display off)
9. COM driver interface control (TE = 0, IDX2-0 = 000)
10. Frame cycle control (DIV1-0 = 00: 1-divided clock, RTN2-0: No retrace line period)
11. Power control 2 (VC2-0 = 000)
12. Vertical scroll (VL27–20 = 00000000, VL17–10 = 00000000)
13. 1st screen division (SE17-10 = 11111111, SS17-10 = 00000000)
14. 2nd screen division (SE27-20 = 11111111, SS27-20 = 00000000)
15. Horizontal RAM address position (HEA5-0 = 111111, HSA5-0 = 000000)
16. Vertical RAM address position (VEA7-0 = 10101111, VSA7-0 = 00000000)
17. RAM write data mask (WM15–0 = 0000H: No mask)
18. RAM address set (AD14–0 = 0000H)
19. Grayscale palette
(RK03–00 = 0000, RK13–10 = 0011, RK23–20 = 0101, RK33–30 = 0111,
RK43–40 = 1001, RK53–50 = 1011, RK63–60 = 1101, RK73–70 = 1111,
GK03–00 = 0000, GK13–10 = 0011, GK23–20 = 0101, GK33–30 = 0111,
GK43–40 = 1001, GK53–50 = 1011, GK63–60 = 1101, GK73–70 = 1111,
BK03–00 = 0000, BK23–20 = 0101, BK43–40 = 1001, BK63–60 = 1111)

GRAM Data Initialization:

This is not automatically initialized by reset input but must be initialized by software while display is off (D1–0 = 00).

Output Pin Initialization:

1. LCD driver output pins (SEG/COM): Output GND level
2. Oscillator output pin (OSC2): Outputs oscillation signal
3. Common interface signals (CCS*, CCL, and CDA): Halt
4. Timing signals (CL1, M, FLM, DISPTMG, and DCCLK): Halt

Parallel Data Transfer

16-bit Bus Interface

Setting the IM2/1/0 (interface mode) to the GND/GND/GND level allows 68-system E-clock-synchronized 16-bit parallel data transfer. Setting the IM2/1/0 to the GND/Vcc/GND level allows 80-system 16-bit parallel data transfer. When the number of buses or the mounting area is limited, use an 8-bit bus interface.

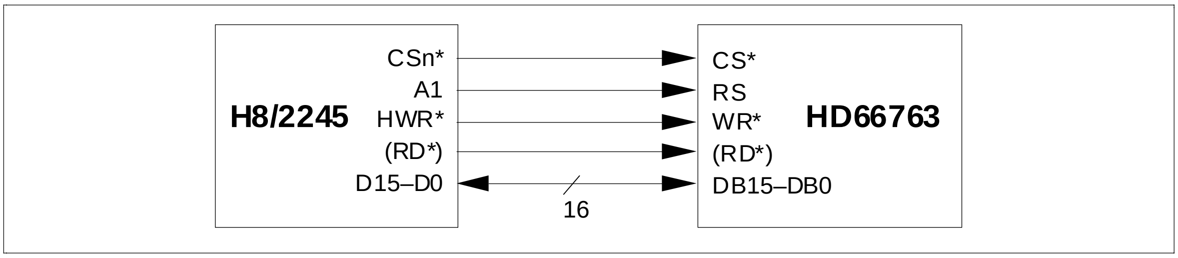


Figure 26 Interface to 16-bit Microcomputer

8-bit Bus Interface

Setting the IM2/1/0 (interface mode) to the GND/GND/Vcc level allows 68-system E-clock-synchronized 8-bit parallel data transfer using pins DB15–DB8. Setting the IM1/0 to the Vcc/Vcc level allows 80-system 8-bit parallel data transfer. The 16-bit instructions and RAM data are divided into eight upper/lower bits and the transfer starts from the upper eight bits. Fix unused pins DB7–DB0 to the Vcc or GND level. Note that the upper bytes must also be written when the index register is written to.

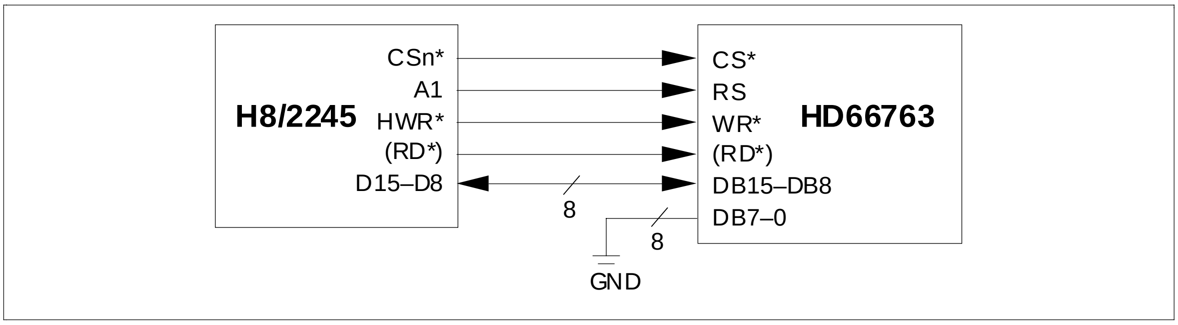


Figure 27 Interface to 8-bit Microcomputer

Note: Transfer synchronization function for an 8-bit bus interface
The HD66763 supports the transfer synchronization function which resets the upper/lower counter to count upper/lower 8-bit data transfer in the 8-bit bus interface. Noise causing transfer mismatch between the eight upper and lower bits can be corrected by a reset triggered by consecutively writing a 00H instruction four times. The next transfer starts from the upper eight bits. Executing synchronization function periodically can recover any runaway in the display system.

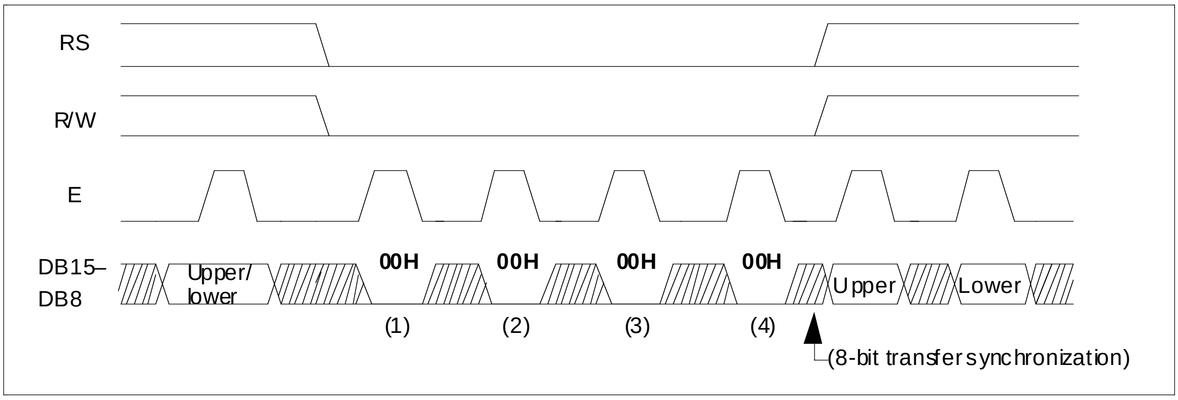


Figure 28 8-bit Transfer Synchronization

Serial Data Transfer

Setting the IM1 pin to the GND level and the IM2 pin to the Vcc level allows standard clock-synchronized serial data (SPI) transfer, using the chip select line (CS*), serial transfer clock line (SCL), serial input data (SDI), and serial output data (SDO). For a serial interface, the IM0/ID pin function uses an ID pin. If the chip is set up for serial interface, the DB15-2 pins which are not used must be fixed at Vcc or GND.

The HD66763 initiates serial data transfer by transferring the start byte at the falling edge of CS* input. It ends serial data transfer at the rising edge of CS* input.

The HD66763 is selected when the 6-bit chip address in the start byte transferred from the transmitting device matches the 6-bit device identification code assigned to the HD66763. The HD66763, when selected, receives the subsequent data string. The least significant bit of the identification code can be determined by the ID pin. The five upper bits must be 01110. Two different chip addresses must be assigned to a single HD66763 because the seventh bit of the start byte is used as a register select bit (RS): that is, when RS = 0, data can be written to the index register or status can be read, and when RS = 1, an instruction can be issued or data can be written to or read from RAM. Read or write is selected according to the eighth bit of the start byte (R/W bit). The data is received when the R/W bit is 0, and is transmitted when the R/W bit is 1.

After receiving the start byte, the HD66763 receives or transmits the subsequent data byte-by-byte. The data is transferred with the MSB first. All HD66763 instructions are 16 bits. Two bytes are received with the MSB first (DB15 to 0), then the instructions are internally executed. After the start byte has been received, the first byte is fetched internally as the upper eight bits of the instruction and the second byte is fetched internally as the lower eight bits of the instruction.

Five bytes of RAM read data after the start byte are invalid. The HD66763 starts to read correct RAM data from the sixth byte.

Table 18 Start Byte Format

Transfer Bit	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note: ID bit is selected by the IM0/ID pin.

Table 19 RS and R/W Bit Function

RS	R/W	Function
0	0	Sets index register
0	1	Reads status
1	0	Writes instruction or RAM data
1	1	Reads instruction or RAM data

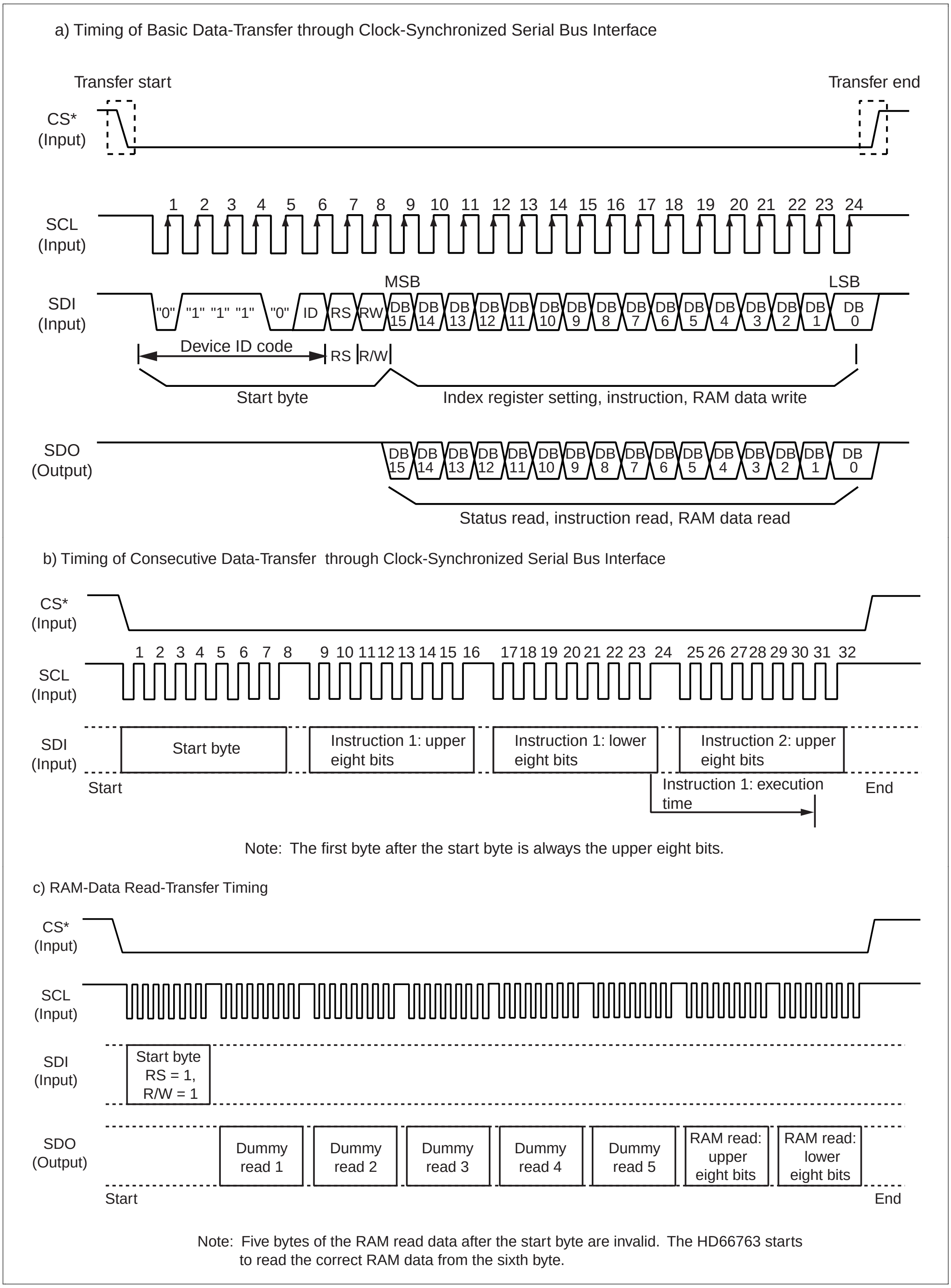


Figure 29 Procedure for Transfer on Clock-Synchronized Serial Bus Interface

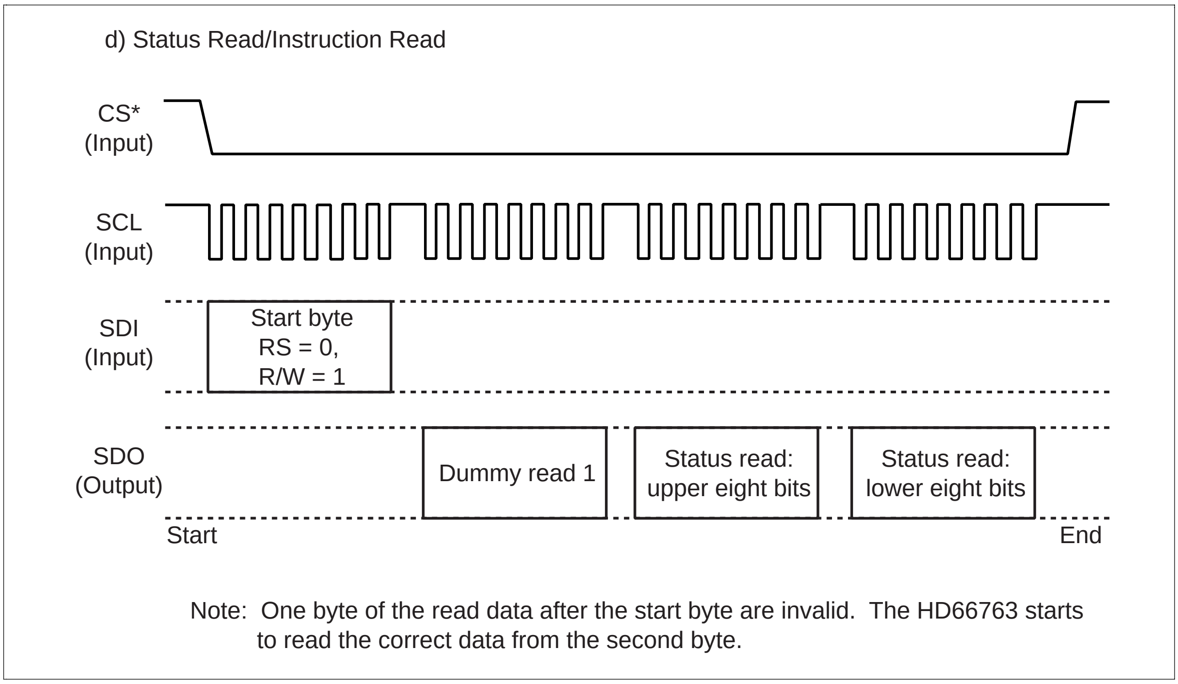


Figure 29 Procedure for Transfer on Clock-Synchronized Serial Bus Interface (cont)

High-Speed Burst RAM Write Function

The HD66763 has a high-speed burst RAM-write function that can be used to write data to RAM in one-fourth the access time required for an equivalent standard RAM-write operation. This function is especially suitable for applications which require the high-speed rewriting of the display data, for example, display of color animations, etc.

When the high-speed RAM-write mode (HWM) is selected, data for writing to RAM is once stored to the HD66763 internal register. When data is selected four times per word, all data is written to the on-chip RAM. While this is taking place, the next data can be written to an internal register so that high-speed and consecutive RAM writing can be executed for animated displays, etc.

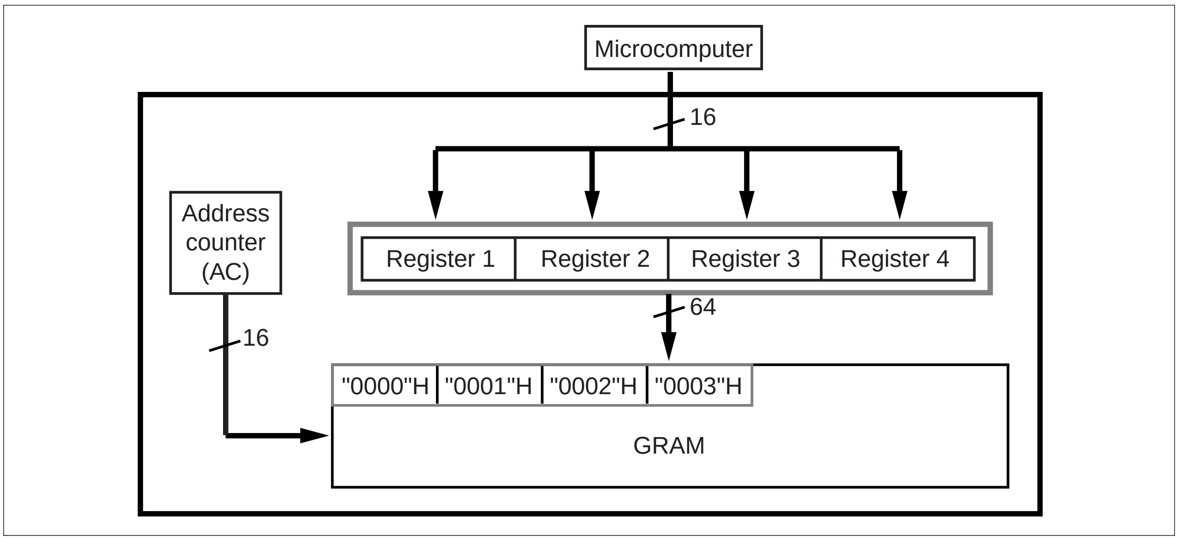


Figure 30 Flow of Operation in High-Speed Consecutive Writing to RAM

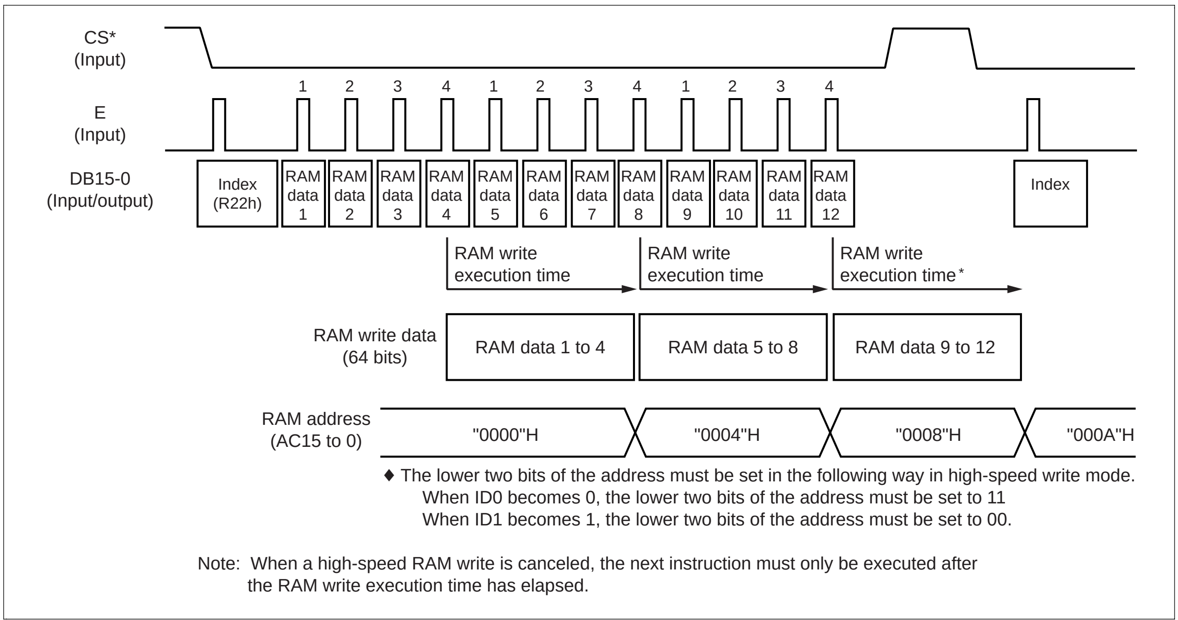


Figure 31 Example of the Operation of High-Speed Consecutive Writing to RAM

When high-speed RAM write mode is used, note the following.

Notes: 1. The logical and compare operations cannot be used.

2. Data is written to RAM each four words. When an address is set, the lower two bits in the address must be set to the following values.

   *When ID0=0, the lower two bits in the address must be set to 11 and be written to RAM.

   *When ID0=1, the lower two bits in the address must be set to 00 and be written to RAM.

3. Data is written to RAM each four words. If less than four words of data is written to RAM, the last data will not be written to RAM.

4. When the index register and RAM data write (22H) have been selected, the data is always written first. RAM cannot be written to and read from at the same time. HWM must be set to 0 while RAM is being read.

5. High-speed and normal RAM write operations cannot be executed at the same time. The mode must be switched and the address must then be set.

6. When high-speed RAM write is used with a window address-range specified, dummy write operation may be required to suit the window address range-specification. Refer to the High-Speed RAM Write in the Window Address section.

Table 20 Comparison between Normal and High-Speed RAM Write Operations

	Normal RAM Write (HWM=0)	**High-Speed RAM Write (HWM=1)**
Logical operation function	Can be used	Cannot be used
Compare operation function	Can be used	Cannot be used
Swap function	Can be used	Can be used
Write mask function	Can be used	Can be used
RAM address set	Can be specified by word	ID0 bit=0: Set the lower two bits to 11 ID0 bit=1: Set the lower two bits to 00
RAM read	Can be read by word	Cannot be used
RAM write	Can be written by word	Dummy write operations may have to be inserted according to a window address-range specification
Window address	Can be set by word	Can be set by word

High-Speed RAM Write in the Window Address

When a window address range is specified, RAM data which is in an optional window area can be rewritten consecutively and quickly by inserting dummy write operations so that RAM access counts become 4N as shown in the tables below.

Dummy write operations may have to be inserted as the first or last operations for a row of data, depending on the horizontal window-address range specification bits (HSA1 to 0, HEA1 to 0). Number of dummy write operations of a row must be 4N.

Table 21 Number of Dummy Write Operations in High-Speed RAM Write (HSA Bits)

HSA1	HSA0	Number of Dummy Write Operations to be Inserted at the Start of a Row
0	0	0
0	1	1
1	0	2
1	1	3

Table 22 Number of Dummy Write Operations in High-Speed RAM Write (HEA Bits)

HEA1	HEA0	Number of Dummy Write Operations to be Inserted at the End of a Row
0	0	3
0	1	2
1	0	1
1	1	0

Each row of access must consist of 4 × N operations, including the dummy writes.

Horizontal access count =

first dummy write count + write data count + last dummy write count = 4 × N

An example of high-speed RAM write with a window address-range specified is shown below.

The window address-range can be rewritten to consecutively and quickly by inserting two dummy writes at the start of a row and three dummy writes at the end of a row, as determined by using the window address-range specification bits (HSA1 to 0=10, HEA1 to 0=00).

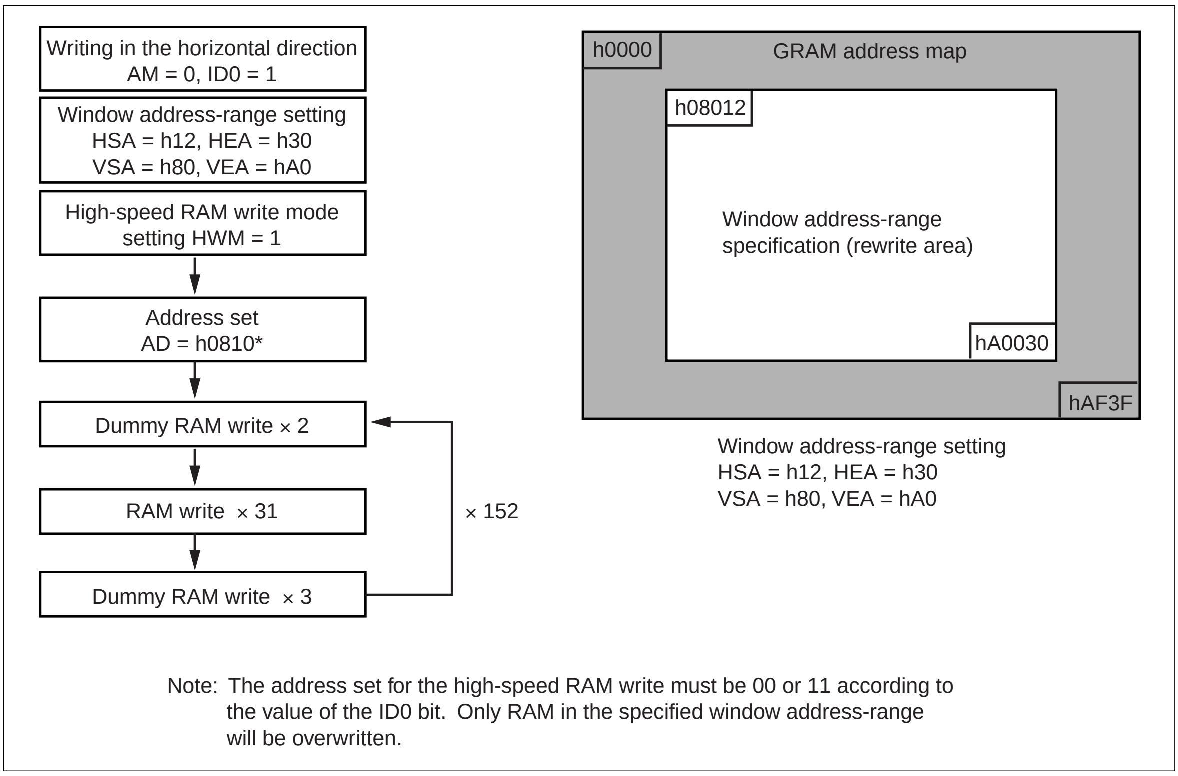


Figure 32 Example of the High-Speed RAM Write with a Window Address-Range Specification

Window Address Function

When data is written to the on-chip GRAM, a window address-range which is specified by the horizontal address register (start: HSA5 to 0, end: HEA 5 to 0) or the vertical address register (start: VSA7 to 0, end: VEA7 to 0) can be written to consecutively.

Data is written to addresses in the direction specified by the AM bit (increment/decrement). When image data, etc. is being written, data can be written consecutively without thinking a data wrap by doing this.

The window must be specified to be within the GRAM address area described below. Addresses must be set within the window address.

[Restriction on window address-range settings]

(horizontal direction) 00H ≤ HSA5 to 0 ≤ HEA5 to 0 ≤ 3FH

(vertical direction) 00H ≤ VSA7 to 0 ≤ VEA7 to 0 ≤ AFH

[Restriction on address settings during the window address]

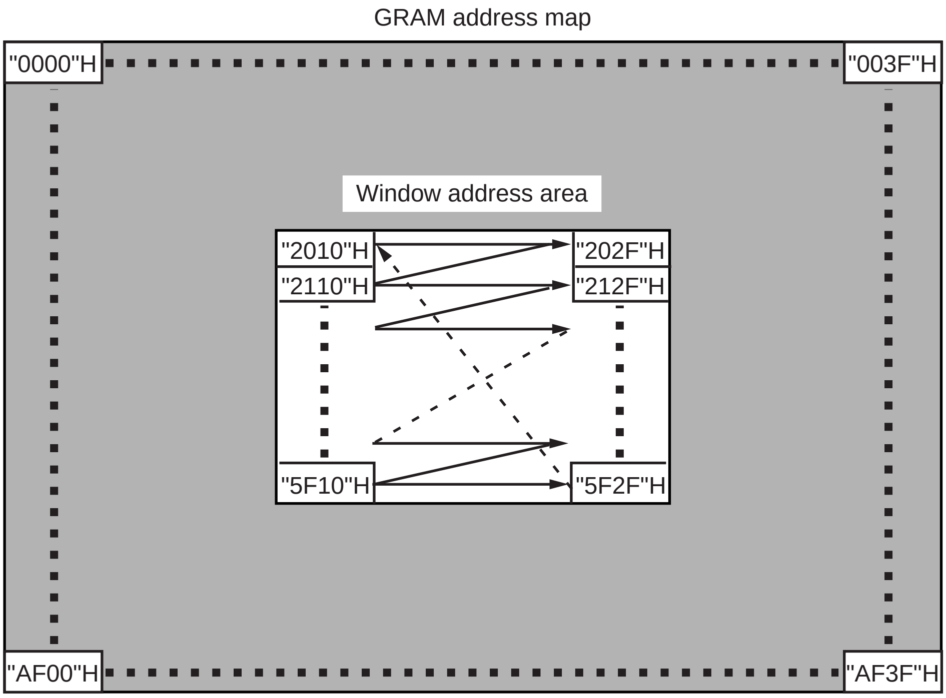
(RAM address) HSA5 to 0 ≤ AD5 to 0 ≤ HEA5 to 0

VSA7 to 0 ≤ AD15 to 8 ≤ VEA7 to 0

Note: In high-speed RAM-write mode, the lower two bits of the address must be set as shown below according to the value of the ID0 bit.

ID0=0: The lower two bits of the address must be set to 11.

ID0=1: The lower two bits of the address must be set to 00.



- Window address-range specification area
  HSA5 to 0 = 10H, HSE5 to 0 = 2FH   I/D = 1 (increment)
  VSA7 to 0 = 20H, VEA7 to 0 = 5FH   AM = 0 (horizontal writing)

Figure 33 Example of Address Operation in the Window Address Specification

Graphics Operation Function

The HD66763 can greatly reduce the load of the microcomputer graphics software processing through the 16-bit bus architecture and internal graphics-bit operation function. This function supports the following:

1. A swap function that exchanges the upper and lower bytes in the 16-bit data sent from the microcomputer.
2. A write data mask function that selectively rewrites some of the bits in the 16-bit write data.
3. A logical operation write function that writes the data sent from the microcomputer and the original RAM data by a logical operation.
4. A conditional write function that compares the original RAM data or write data and the compare-bit data and writes the data sent from the microcomputer only when the conditions match.

Even if the display size is large, the display data in the graphics RAM (GRAM) can be quickly rewritten.

The graphics bit operation can be controlled by combining the entry mode register, the bit set value of the RAM-write-data mask register, and the read/write from the microcomputer.

Table 23 Graphics Operation

Operation Mode	Bit Setting			Operation and Usage
	I/D	AM	LG2–0	
Write mode 1	0/1	0	000	Horizontal data replacement, horizontal-border drawing
Write mode 2	0/1	1	000	Vertical data replacement, vertical-border drawing
Write mode 3	0/1	0	110 111	Conditional horizontal data replacement, horizontal-border drawing
Write mode 4	0/1	1	110 111	Conditional vertical data replacement, vertical-border drawing
Read/write mode 1	0/1	0	001 010 011	Horizontal data write with logical operation, horizontal-border drawing
Read/write mode 2	0/1	1	001 010 011	Vertical data write with logical operation, vertical-border drawing
Read/write mode 3	0/1	0	100 101	Conditional horizontal data replacement, horizontal-border drawing
Read/write mode 4	0/1	1	100 101	Conditional vertical data replacement, vertical-border drawing

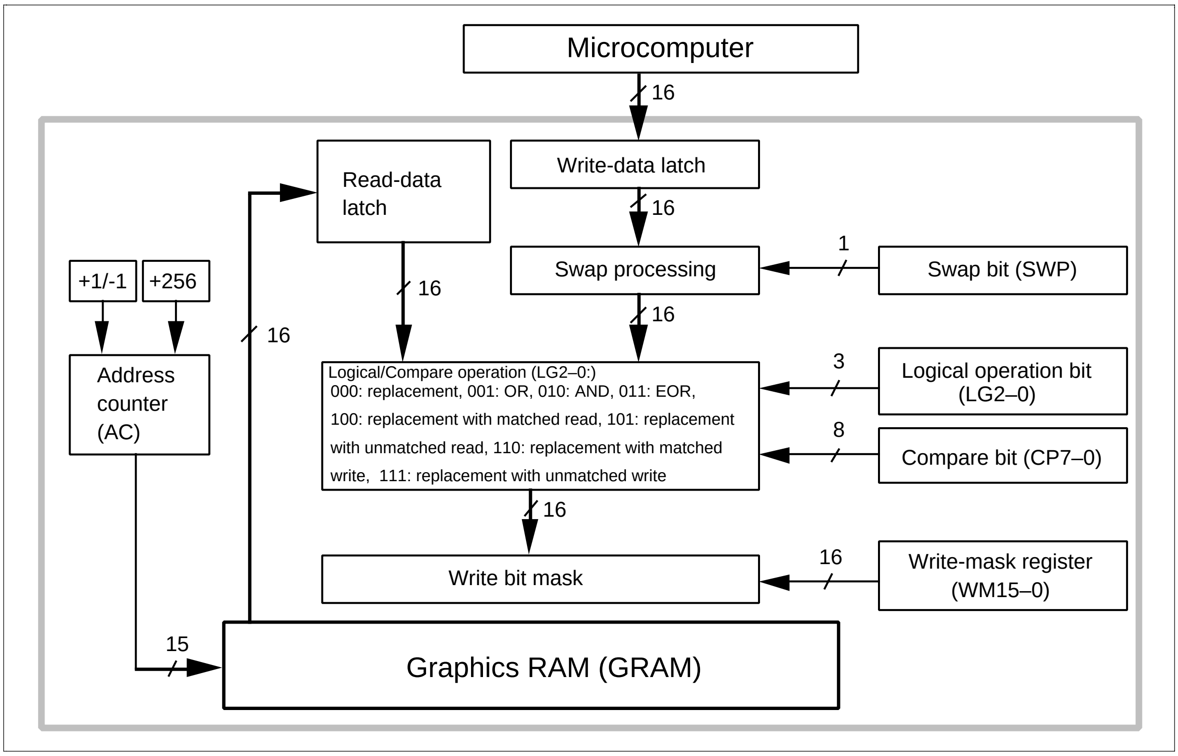


Figure 34 Data Processing Flow of the Graphics Operation

Swap Function

The HD66763 has a byte-wise swap function that exchanges the upper and lower bytes in the two-byte data sent from the microcomputer. When SWP = 0, the data written by the microcomputer is directly transferred to the inside. When SWP = 1, the data written by the microcomputer is internally transferred by exchanging the upper and lower bytes.

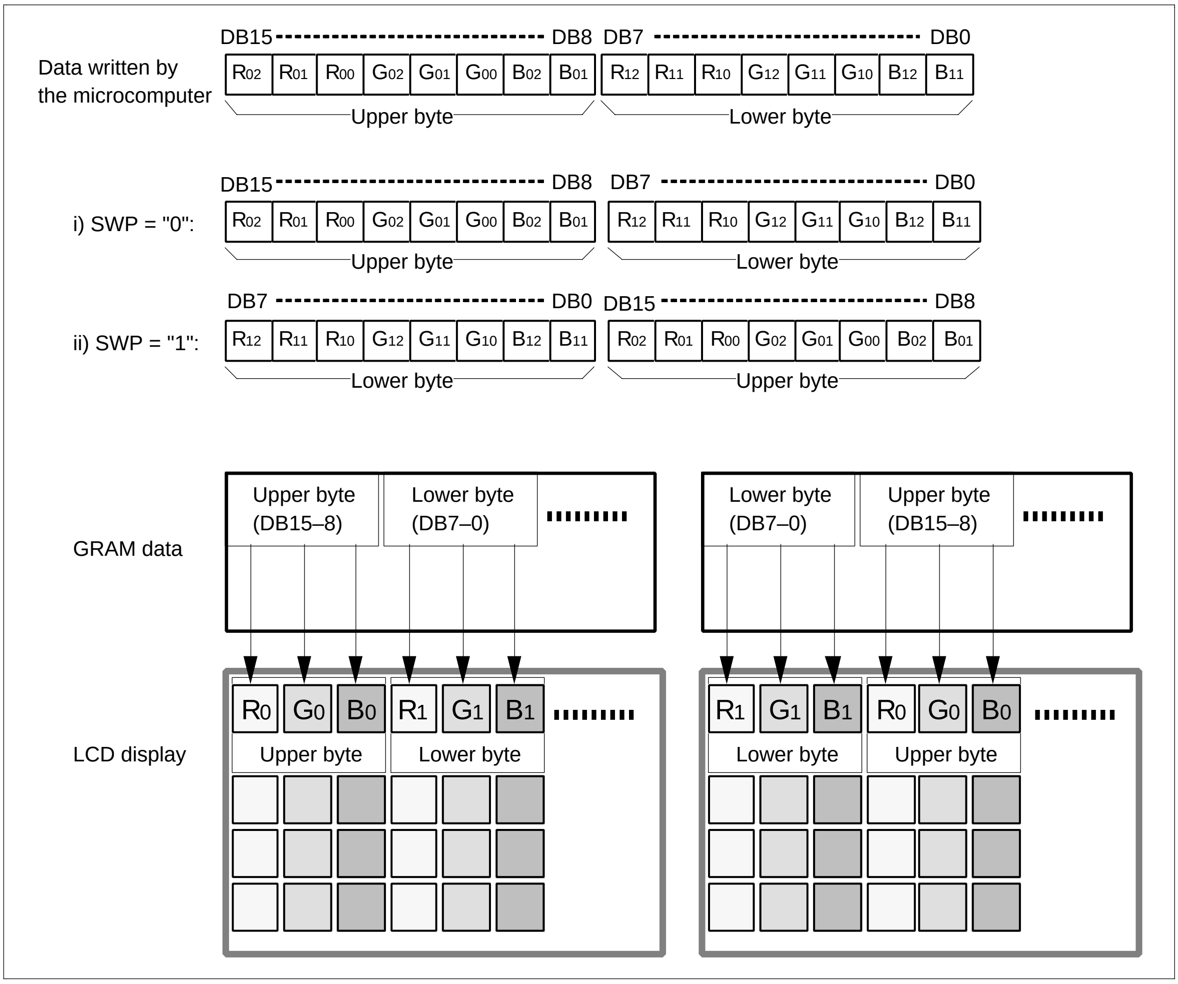


Figure 35 Example of Swap Function Operation

Write-data Mask Function

The HD66763 has a bit-wise write-data mask function that controls writing the two-byte data from the microcomputer to the GRAM. Bits that are 0 in the write-data mask register (WM15–0) cause the corresponding DB bit to be written to the GRAM. Bits that are 1 prevent writing to the corresponding GRAM bit to the GRAM; the data in the GRAM is retained. This function can be used when only one-pixel data is rewritten or the particular display color is selectively rewritten.

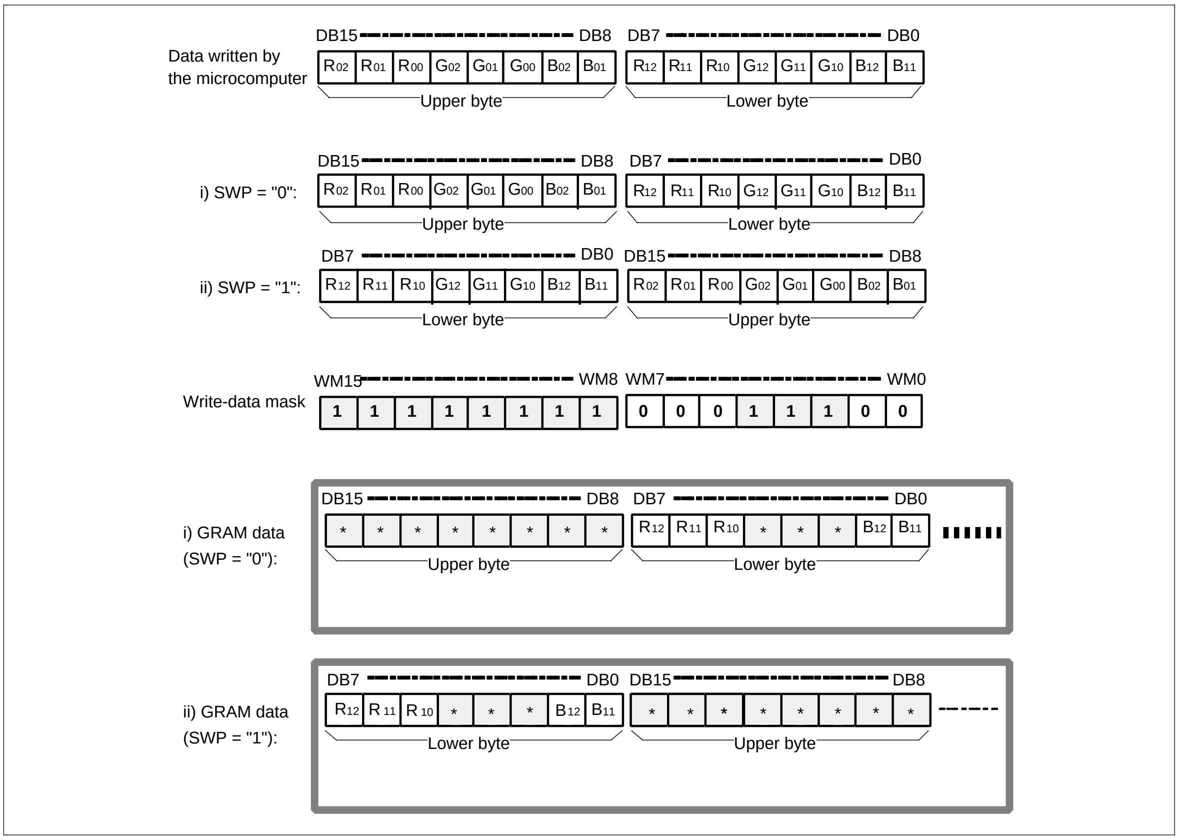


Figure 36 Example of Write-data Mask Function Operation

Logical/Compare Operation Function

The HD66763 performs a logical operation or conditional replacement between the two-byte write data sent from the microcomputer and the read data from the GRAM. The logical operation function has four types: replacement, OR, AND, and EOR. The conditional replacement performs a compare operation for the set value of the compare register (CP7–0) and the read data value from the GRAM, and rewrites only the pixel data in the GRAM that satisfies the conditions (in a byte unit). This function can be used when a particular color is selectively rewritten. The swap function or write-data mask function can be effectively used.

Table 24 Logical/Compare Operation

Bit Setting			
LG2	**LG1**	**LG0**	**Description of Logical/Compare Operation Function**
0	0	0	Writes the data written from the microcomputer directly to the GRAM. Only write processing is performed since the data in the read-data latch is not used.
0	0	1	ORs the data in the read-data latch and the data written by the microcomputer. Writes the result to GRAM. Read, modify, or write processing is performed.
0	1	0	ANDs the data in the read-data latch and the data written by the microcomputer. Writes the result to GRAM.
0	1	1	EORs the data in the read-data latch and the data written by the microcomputer. Writes the result to GRAM.
1	0	0	Compares the data in the read-data latch and the set value of the compare register (CP7–0). When the read data matches CP7–0, the data from the microcomputer is written to the GRAM. Only the particular color specified in the compare register can be rewritten. Read, modify, or write processing is performed.
1	0	1	Compares the data in the read-data latch and the set value of the compare register (CP7–0). When the read data does not match CP7–0, the data from the microcomputer is written to the GRAM. Colors other than the particular one specified in the compare register can be rewritten. Read, modify, or write processing is performed.
1	1	0	Compares the data written to the GRAM by the microcomputer and the set value of the compare register (CP7–0). When the write data matches CP7–0, the data from the microcomputer is written to the GRAM. Only write processing is performed.
1	1	1	Compares the data written to the GRAM by the microcomputer and the set value of the compare register (CP7–0). When the write data does not match CP7–0, the data from the microcomputer is written to the GRAM. Only write processing is performed.

Graphics Operation Processing

1. Write mode 1: AM = 0, LG2–0 = 000

   This mode is used when the data is horizontally written at high speed. It can also be used to initialize the graphics RAM (GRAM) or to draw borders. The swap function (SWP) and write-data mask function (WM15–0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edge of the GRAM.

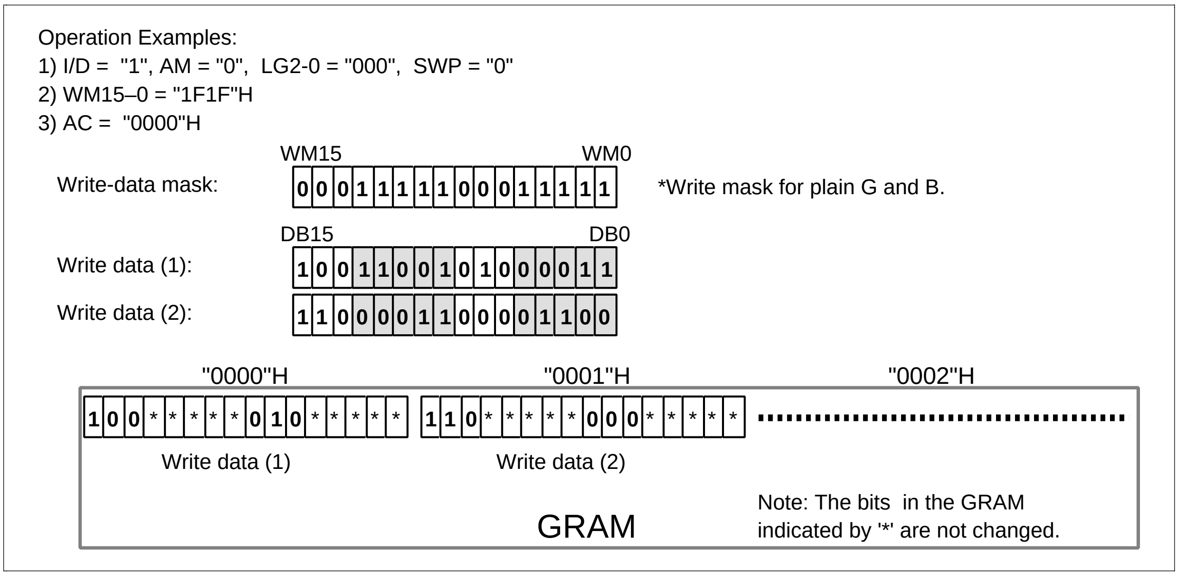


Figure 37 Writing Operation of Write Mode 1

2. Write mode 2: AM = 1, LG2–0 = 000

This mode is used when the data is vertically written at high speed. It can also be used to initialize the GRAM, develop the font pattern in the vertical direction, or draw borders. The swap function (SWP) and write-data mask function (WM15–0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the GRAM.

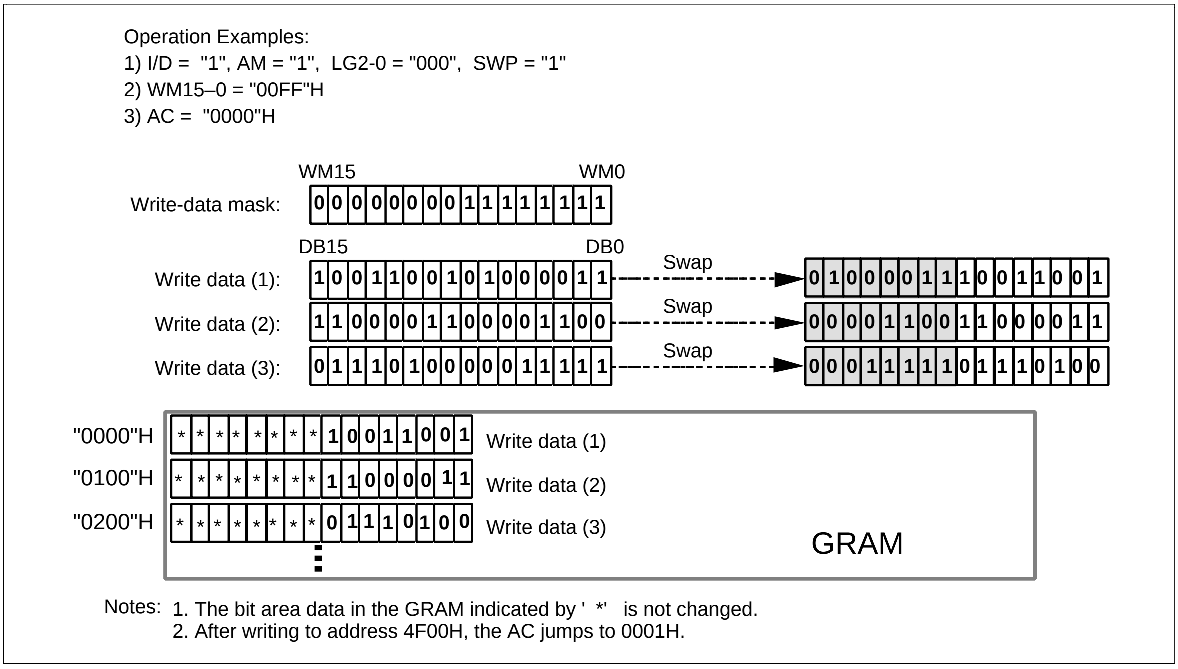


Figure 38 Writing Operation of Write Mode 2

3. Write mode 3: AM = 0, LG2–0 = 110/111

This mode is used when the data is horizontally written by comparing the write data and the set value of the compare register (CP7–0). When the result of the comparison in a byte unit satisfies the condition, the write data sent from the microcomputer is written to the GRAM. In this operation, the swap function (SWP) and write-data mask function (WM15–0) are also enabled. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edge of the GRAM.

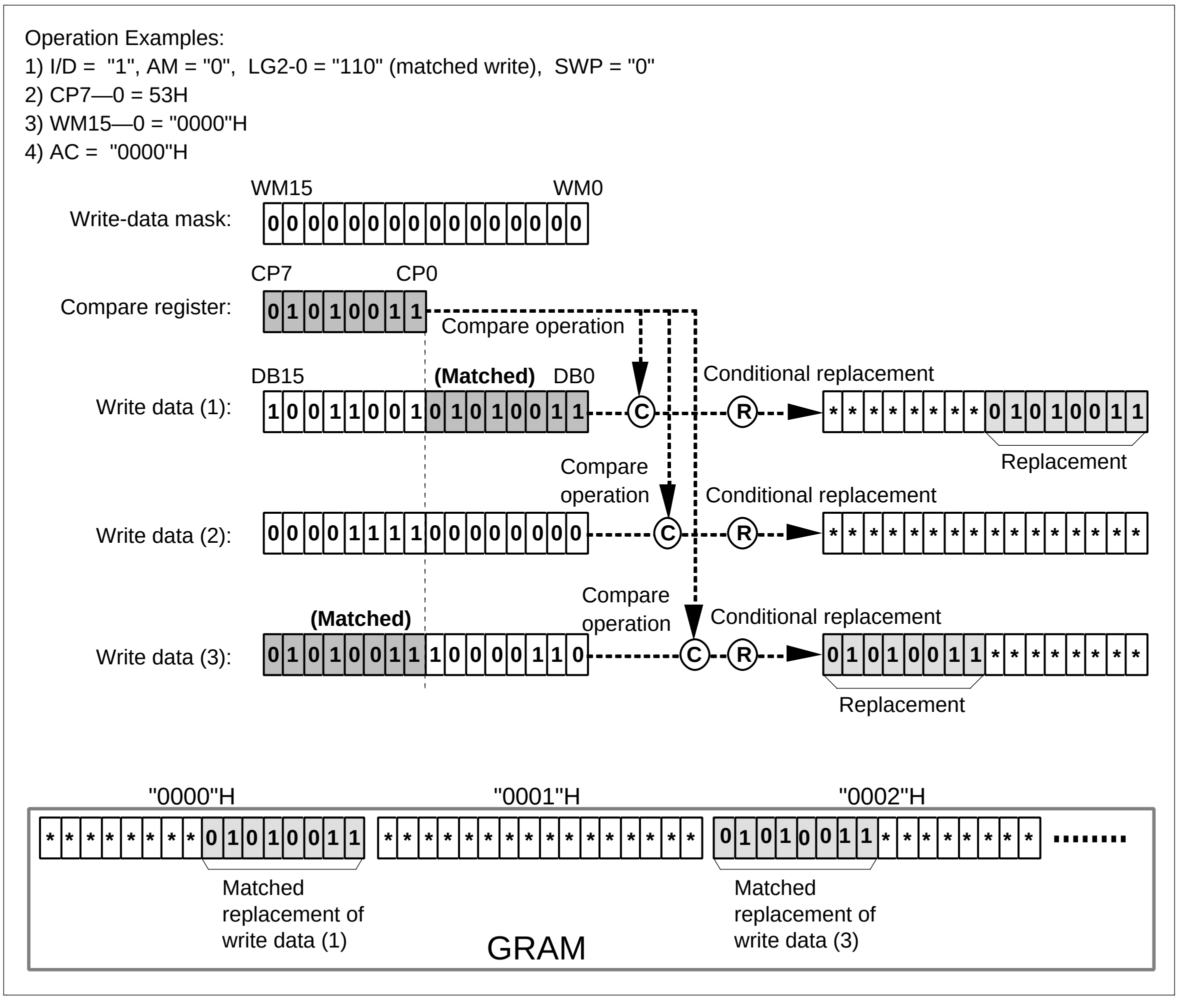


Figure 39 Writing Operation of Write Mode 3

4. Write mode 4: AM = 1, LG2–0 = 110/111

This mode is used when a vertical comparison is performed between the write data and the set value of the compare register (CP7–0) to write the data. When the result by the comparison in a byte unit satisfies the condition, the write data sent from the microcomputer is written to the GRAM. In this operation, the swap function (SWP) and write-data mask function (WM15–0) are also enabled. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the GRAM.

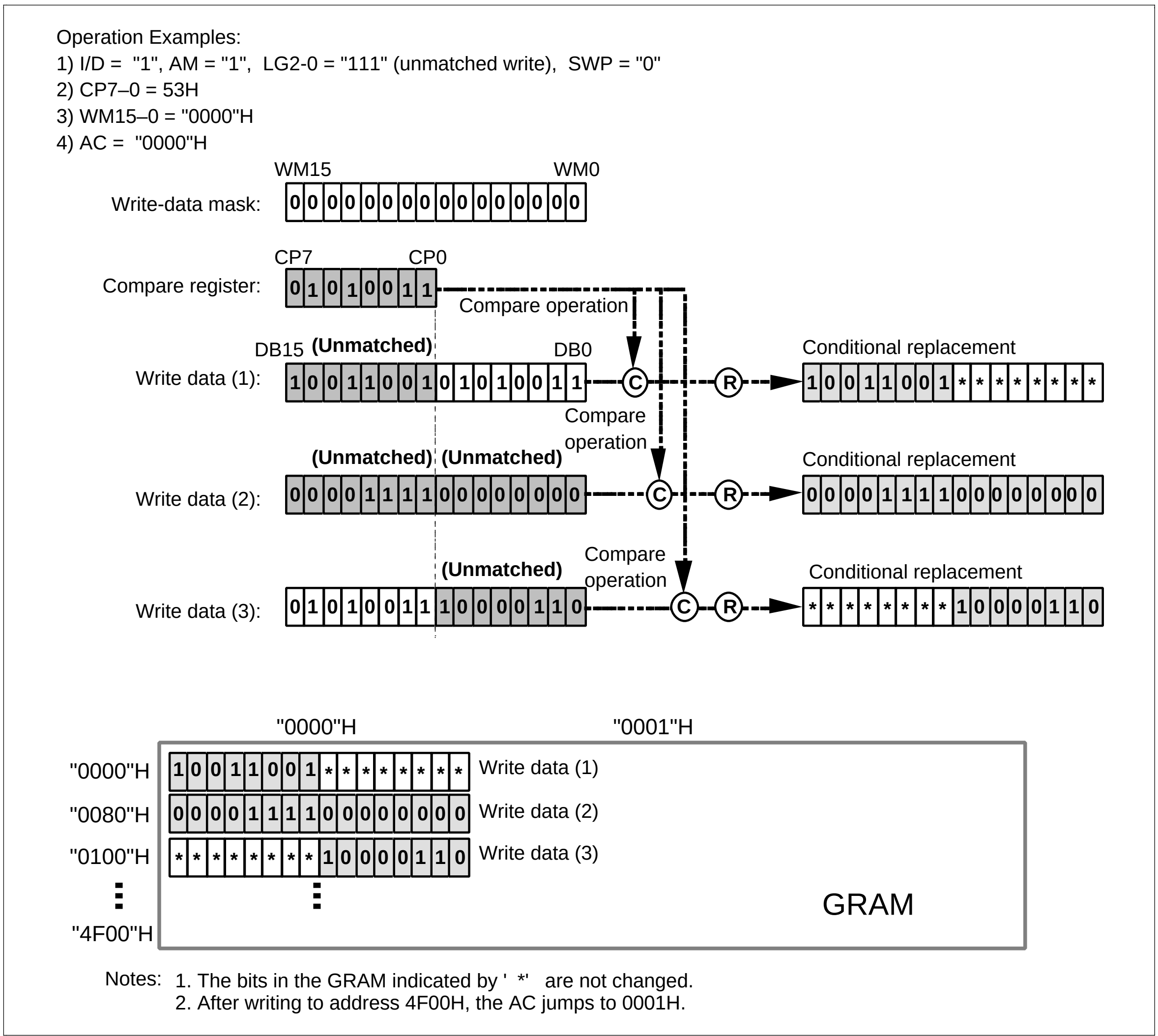


Figure 40 Writing Operation of Write Mode 4

5. Read/Write mode 1: AM = 0, LG2–0 = 001/010/011

This mode is used when the data is horizontally written at high speed by performing a logical operation with the original data. It reads the display data (original data), which has already been written in the GRAM, performs a logical operation with the write data sent from the microcomputer, and rewrites the data to the GRAM. This mode reads the data during the same access-pulse width (68-system: enabled high level, 80-system: RD* low level) as the write operation since reading the original data does not latch the read data into the microcomputer but temporarily holds it in the read-data latch. However, the bus cycle requires the same time as the read operation. The swap function (SWP) or write-data mask function (WM15–0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edges of the GRAM.

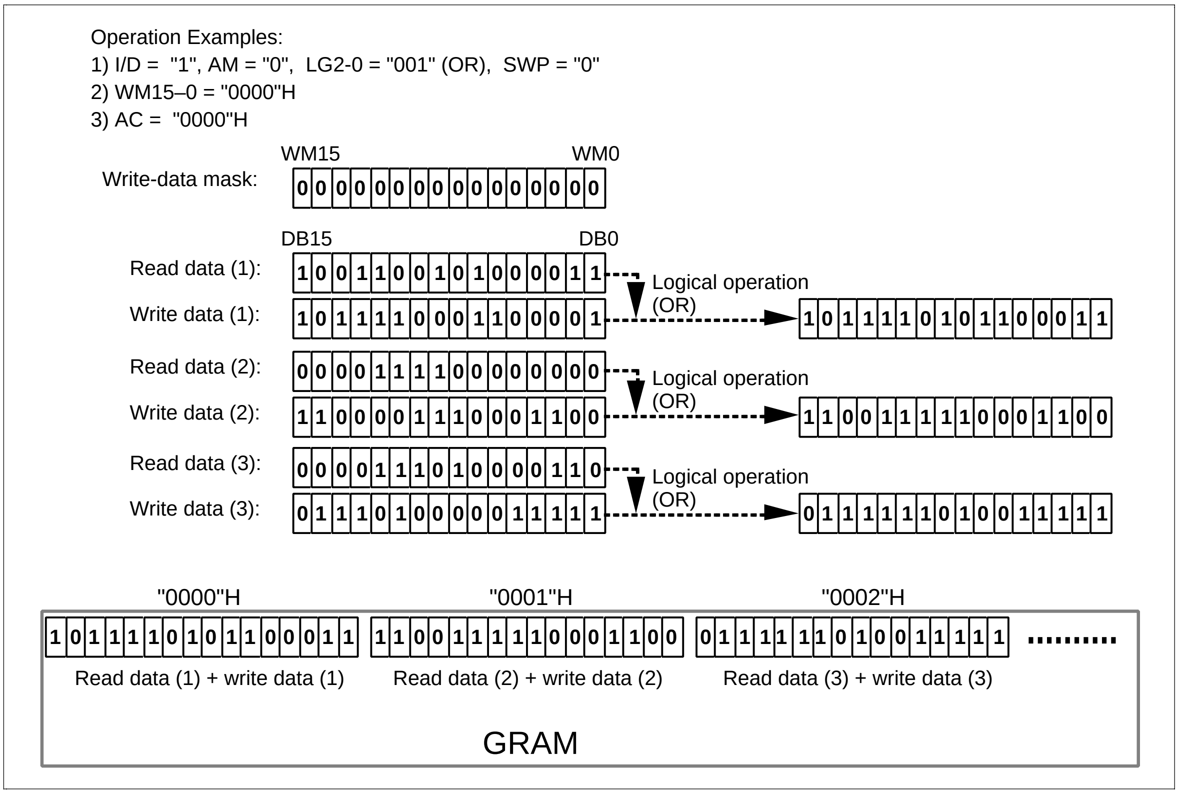


Figure 41 Writing Operation of Read/Write Mode 1

6. Read/Write mode 2: AM = 1, LG1–0 = 001/010/011

This mode is used when the data is vertically written at high speed by performing a logical operation with the original data. It reads the display data (original data), which has already been written in the GRAM, performs a logical operation with the write data sent from the microcomputer, and rewrites the data to the GRAM. This mode can read the data during the same access-pulse width (68-system: enabled high level, 80-system: RD* low level) as for the write operation since the read operation of the original data does not latch the read data into the microcomputer and temporarily holds it in the read-data latch. However, the bus cycle requires the same time as the read operation. The swap function (SWP) or write-data mask function (WM15–0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the GRAM.

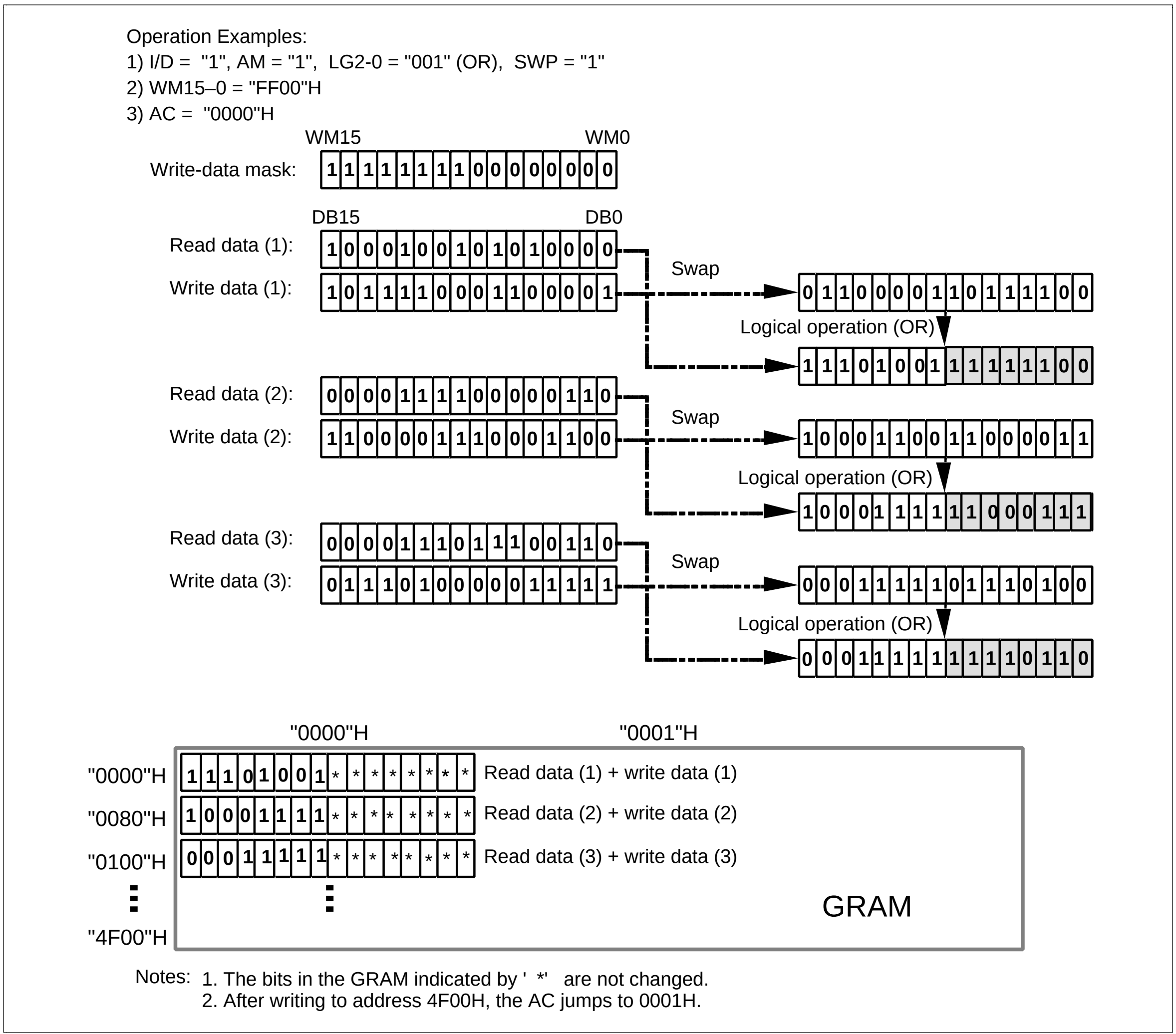


Figure 42 Writing Operation of Read/Write Mode 2

7. Read/Write mode 3: AM = 0, LG2–0 = 100/101

   This mode is used when the data is horizontally written by comparing the original data and the set value of compare register (CP7–0). It reads the display data (original data), which has already been written in the GRAM, compares the original data and the set value of the compare register in byte units, and writes the data sent from the microcomputer to the GRAM only when the result of the comparison satisfies the condition. This mode reads the data during the same access-pulse width (68-system: enabled high level, 80-system: RD* low level) as write operation since reading the original data does not latch the read data into the microcomputer but temporarily holds it in the read-data latch. However, the bus cycle requires the same time as the read operation. The swap function (SWP) and write-data mask function (WM15–0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edges of the GRAM.

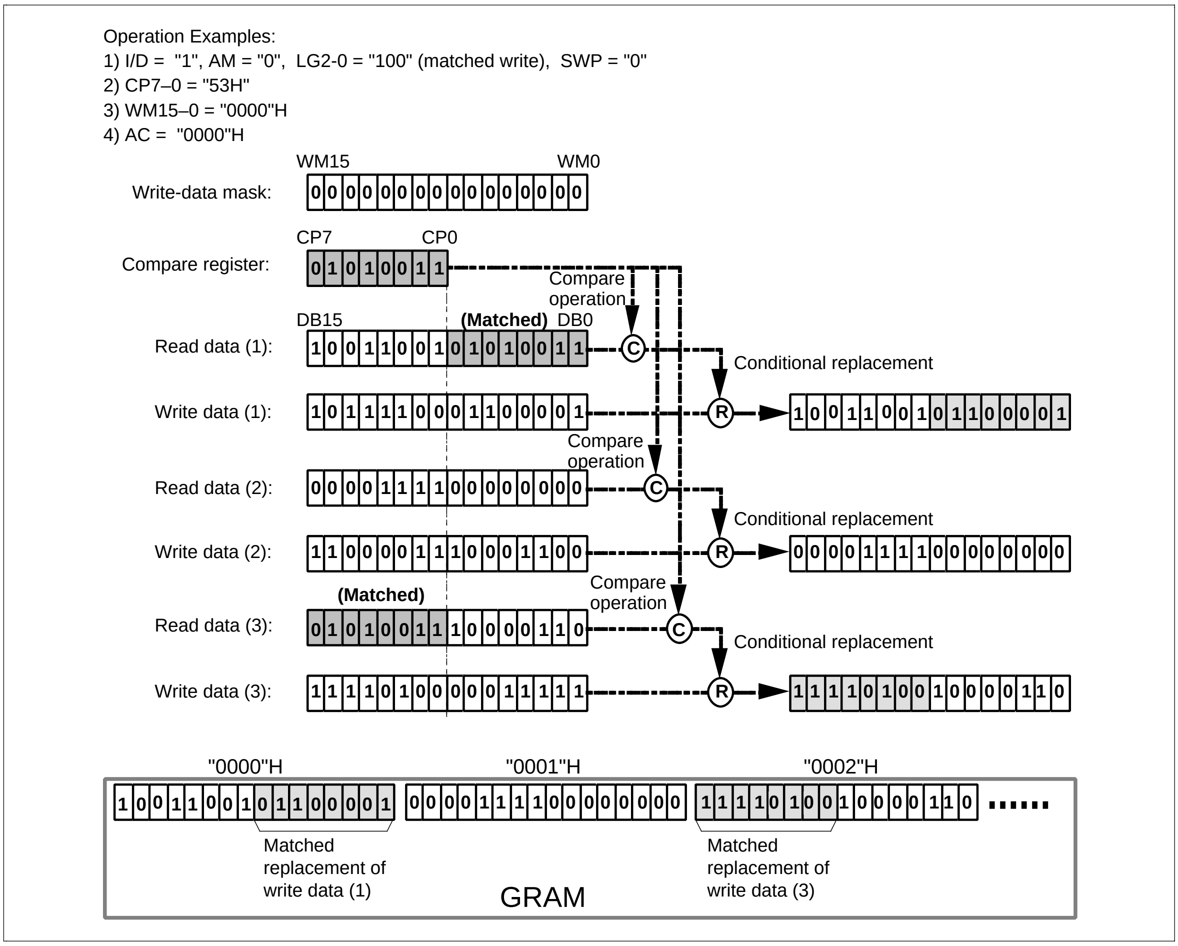


Figure 43 Writing Operation of Read/Write Mode 3

8. Read/Write mode 4: AM = 1, LG2–0 = 100/101

This mode is used when the data is vertically written by comparing the original data and the set value of the compare register (CP7–0). It reads the display data (original data), which has already been written in the GRAM, compares the original data and the set value of the compare register in byte units, and writes the data sent from the microcomputer to the GRAM only when the result of the compare operation satisfies the condition. This mode reads the data during the same access-pulse width (68-system: enabled high level, 80-system: RD* low level) as the write operation since reading the original data does not latch the read data into the microcomputer but temporarily holds it in the read-data latch. However, the bus cycle requires the same time as the read operation. The swap function (SWP) and write-data mask function (WM15–0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the GRAM.

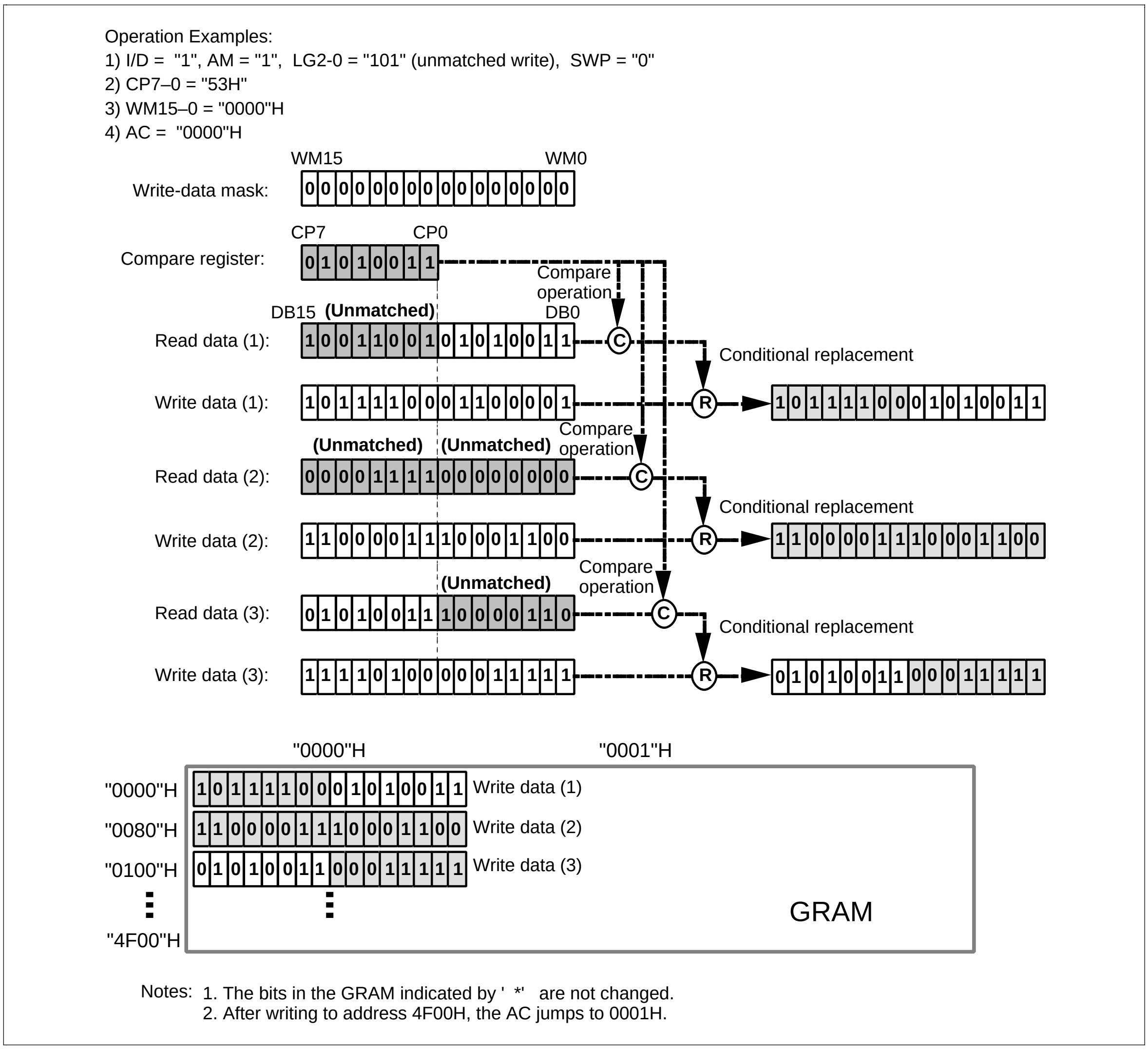


Figure 44 Writing Operation of Read/Write Mode 4

Grayscale Palette

The HD66763 incorporates a grayscale palette to simultaneously display 256 of the 4,096 possible colors. The R and G grayscales consist of eight four-bit palettes, and the B grayscale consists of four four-bit palettes. The 16-stage grayscale levels can be selected from the four-bit palette data.

For the display data of R and G, the three-bit data in the GRAM written from the microcomputer is used. For the display data of B, the two-bit data in the GRAM is used.

In this palette, a pulse-width control system (PWM) is used to eliminate flicker in the LCD display. The time over which the LCDs are switched on is adjusted according to the level and grayscales are displayed so that flicker is reduced and grayscales are clearly displayed.

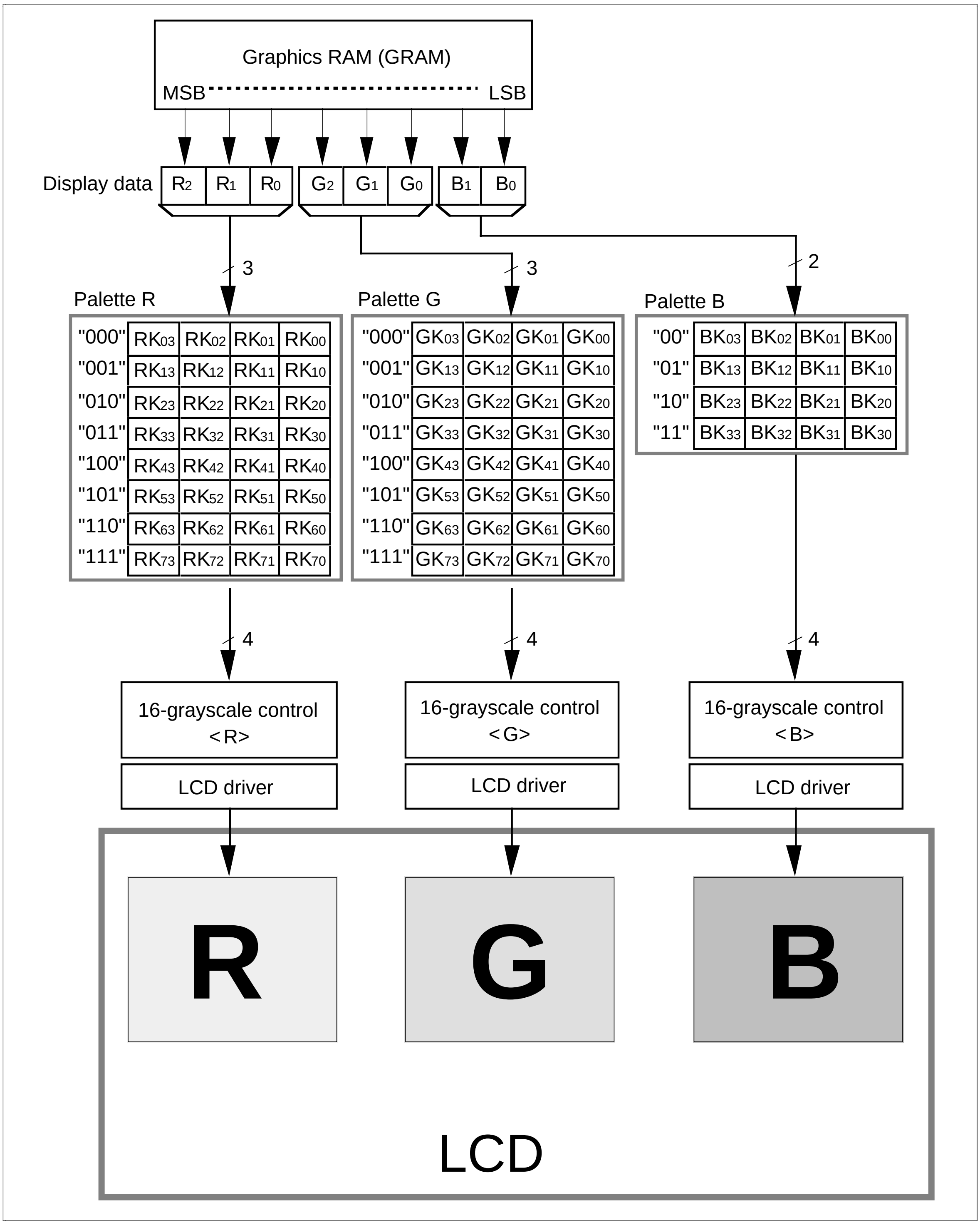


Figure 45 Grayscale Palette Control

Grayscale Palette Table

The grayscale register that is set for each palette register (RK, GK, or BK) can be set to any level. 16-grayscale lighting levels can be set according to palette values (0000 to 1111).

Table 25 Grayscale Control Level

Palette Register Value (RK, GK, or BK)				Grayscale Control Level
0	0	0	0	Unlit level*1
0	0	0	1	2/16 level
0	0	1	0	3/16 level
0	0	1	1	4/16 level
0	1	0	0	5/16 level
0	1	0	1	6/16 level
0	1	1	0	7/16 level
0	1	1	1	8/16 level
1	0	0	0	9/16 level
1	0	0	1	10/16 level
1	0	1	0	11/16 level
1	0	1	1	12/16 level
1	1	0	0	13/16 level
1	1	0	1	14/16 level
1	1	1	0	15/16 level
1	1	1	1	All-lit level*2

Notes: 1. The unlit level corresponds to a black display when a normally-black color-LCD panel is used, and a white display when a normally-white color-LCD panel is used.

2. The all-lit level corresponds to a white display when a normally-black color-LCD panel is used, and a black display when a normally-white color-LCD panel is used.

Common Driver Interface

The HD66763 and the HD66764 common driver can drive displays of up to 128 (RGB) × 176 dots in size. Signals to set instructions for CR oscillation, the display timing signal, and the common driver are supplied from the HD66763 to the common driver. The LCD drive voltage is generated by the common driver. The LCD segment drive level (VSH) is also supplied from the common driver. On/off control of the display is required to be controlled by both the common and segment driver. Follow the on/off sequence of the display.

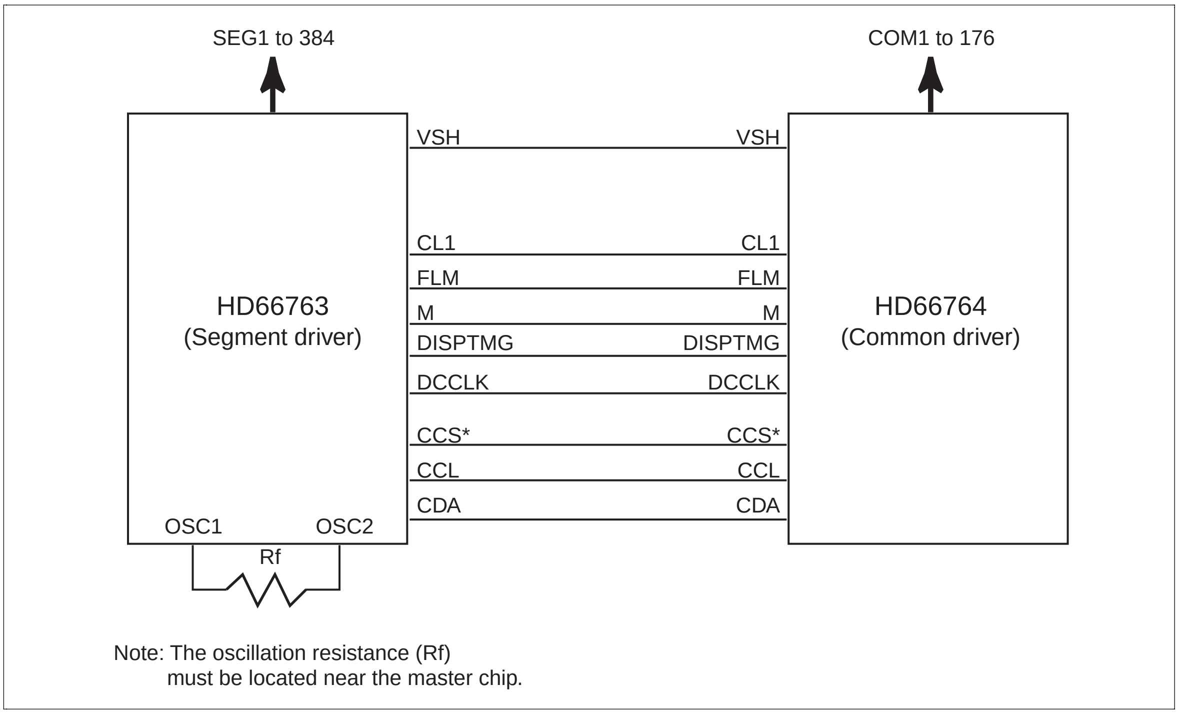


Figure 46 Connection to the Common Driver

Common Driver Serial Transfer

The HD66763 has an on-chip serial circuit to interface with the common driver (HD66764). Registers of the common driver can be set by transferring register settings from the HD66763. The serial interface consists of the serial chip select (CCS*), serial transfer clock (CCL), and serial transfer data (CDA) lines. The HD66763 serial interface circuit is only for transmitting, and cannot be used for receiving data from the common driver.

Serial transfer is started by setting the serial transfer register (TE) in the HD66763 to 1. After TE has been set to 1, CDA will be output in synchronization with CCS*, CCL, and CCL. Transfer is in 16-bit blocks. The data transferred consists of a common driver index register (IDX2 to 0) and an instruction for a register selected by IDX2 to 0. For more information on the common driver indices and instructions, refer to the common-driver data sheet. Serial transfer is independent of the HD66763′s internal operation, so other instructions can be executed during transfer. Serial transfer to the common driver requires a maximum of 18 clock cycles.

When the serial transfer is finished, TE is automatically cleared to 0. After reading the register to confirm that TE=0, serial transfer of the next instruction may be started.

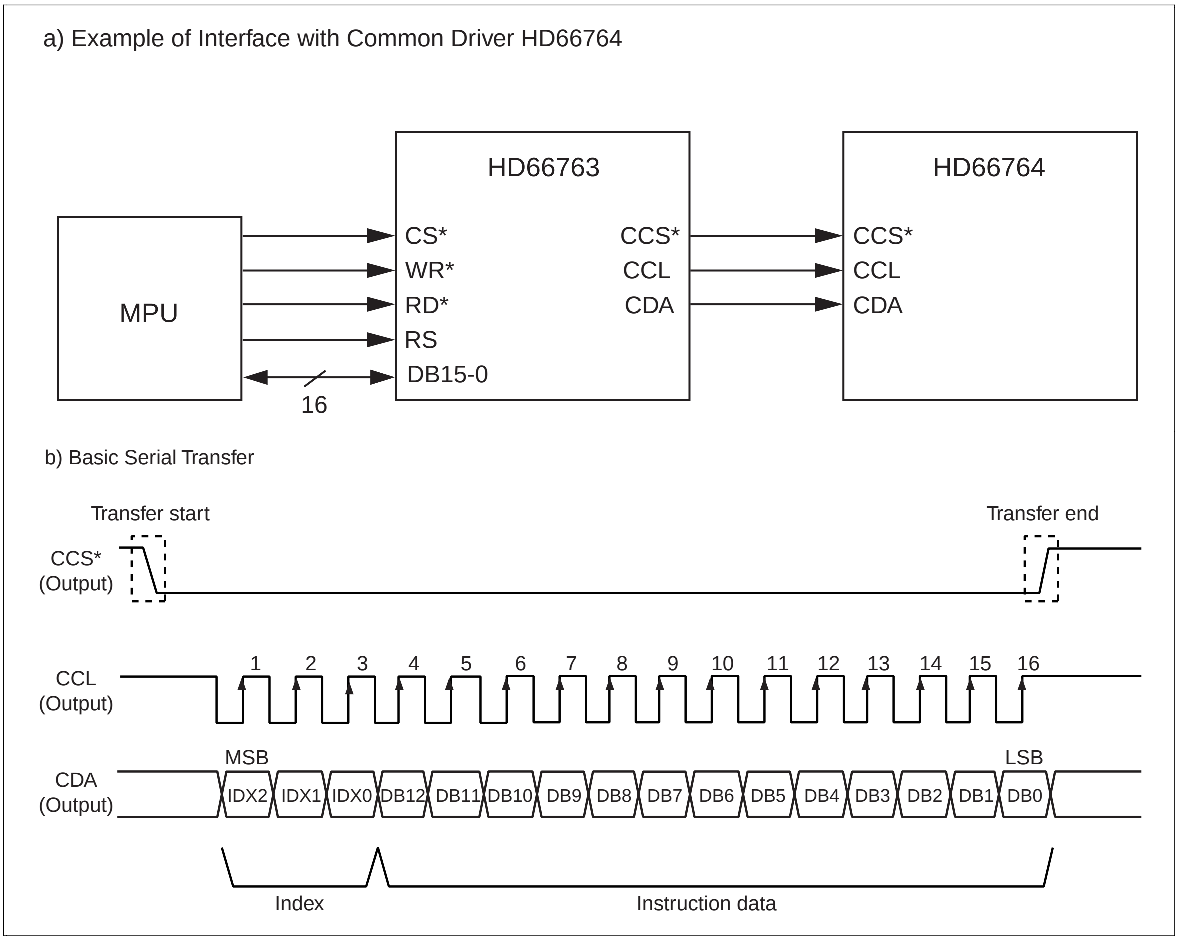


Figure 47 Common Driver Serial Transfer

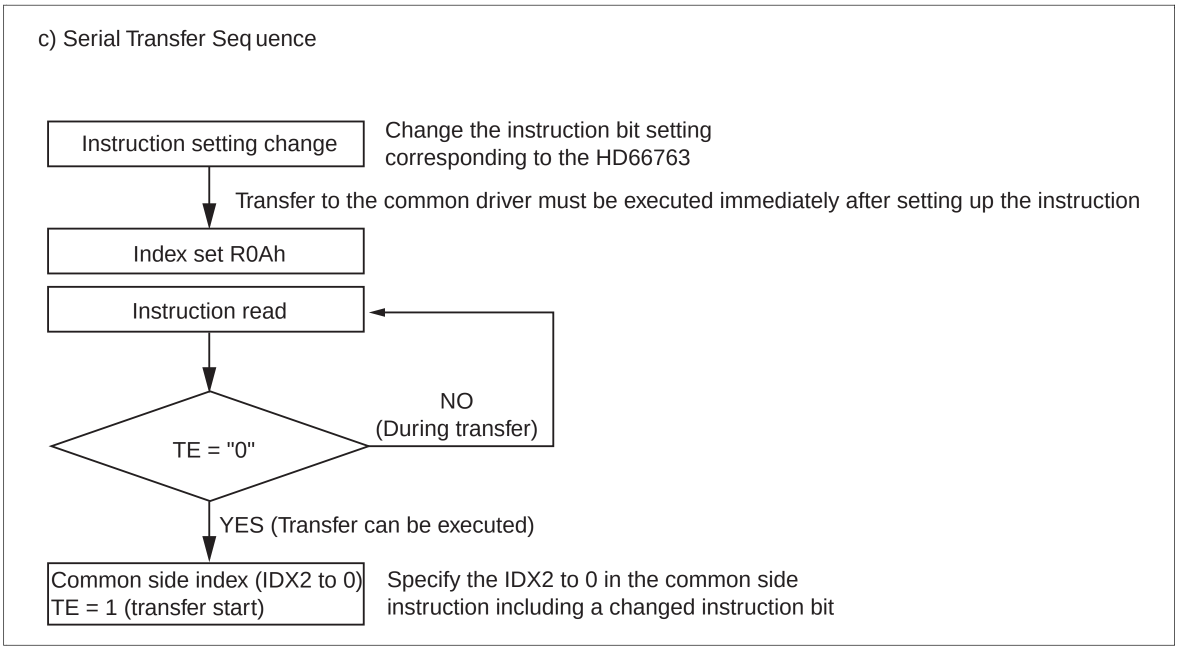


Figure 47 Common Driver Serial Transfer (cont)

Notes:
1. Transfer to the common driver must take place immediately after setting up the instruction.
2. The serial transfer period takes a maximum of 1/fosc × 18 clock cycles (sec).
3. Serial transfer cannot be executed in standby mode. If the chip enters standby mode during transfer, the serial transfer is forcibly suspended. Transfer must be executed again after standby has been canceled because correct transfer is not guaranteed in this situation.
4. Serial transfer can be forcibly suspended by writing TE=0. Transfer must be executed again because correct transfer is not guaranteed in this situation.
5. The instruction bit for the common driver is not executed when it is not transferred to the common driver. When the setting is changed, transfer must be executed again.

When transfer to the common driver is executed, the transfer is executed by using one of the following common driver (HD66764) instructions, corresponding to the value set by the IDX2 to 0.

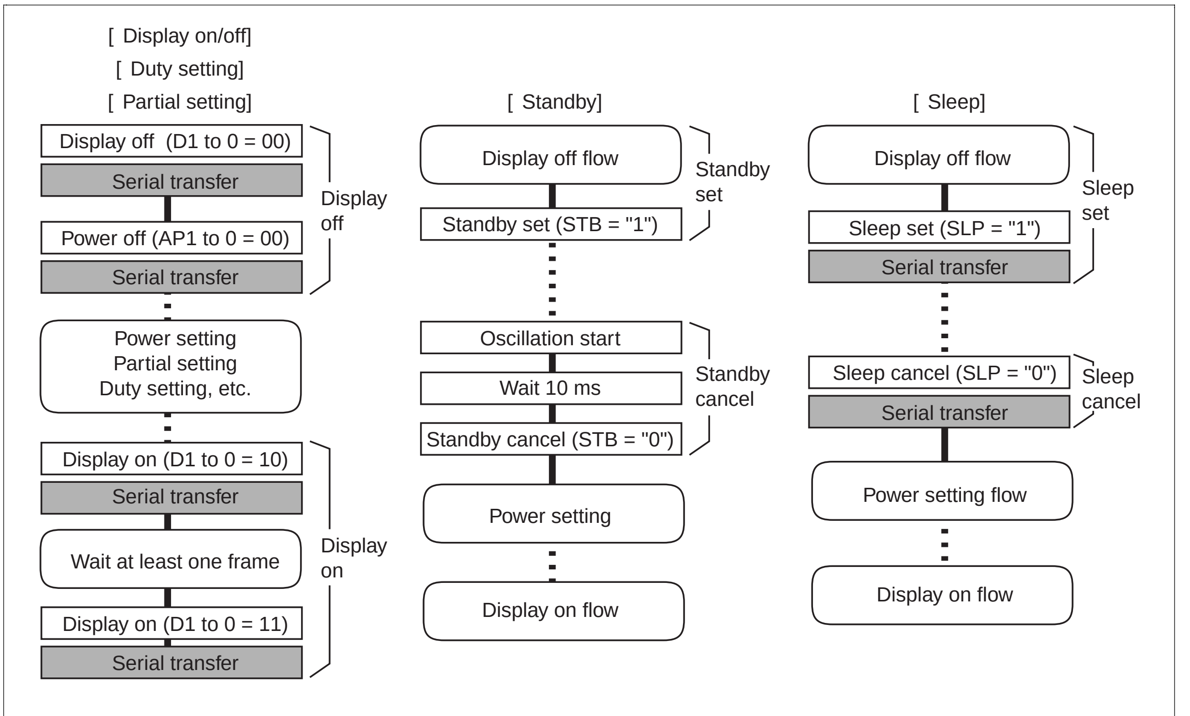
Table 26 Common Driver (HD66764) Instructions

IDX2	IDX1	IDX0	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	BS2	BS1	BS0	BT3	BT2	BT1	BT0	DC2	DC1	DC0	AP1	AP0	SLP
0	0	1	0	0	0	0	0	0	0	0	0	0	VC2	VC1	VC0
0	1	0	0	VR3	VR2	VR1	VR0	0	CT6	CT5	CT4	CT3	CT2	CT1	CT0
0	1	1	0	0	D1	CMS	SPT	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
1	0	0	0	0	0	0	0	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10
1	0	1	0	0	0	0	0	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20
1	1	0	0	0	0	0	0	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20

Instruction Setting Flow

When the common driver HD66764 is used, follow the below about each instruction setting. The instruction setting for the common driver is executed by the serial interface. When the instruction for the common driver is set, the serial transfer must be executed to the common driver. The transfer to the common driver must be executed immediately after the instruction set.

Follow the below serial transfer flow about each setting and then transfer must be executed.



Note: For more information on the flow for power settings, refer to the common-driver data sheet.

Figure 48 Instruction Setting Flow

Oscillation Circuit

The HD66763 can oscillate between the OSC1 and OSC2 pins using an internal R-C oscillator with an external oscillation resistor. Note that in R-C oscillation, the oscillation frequency is changed according to the external resistance value, wiring length, or operating power-supply voltage. If Rf is increased or power supply voltage is decrease, the oscillation frequency decreases. For the relationship between Rf resistor value and oscillation frequency, see the Electric Characteristics Notes section.

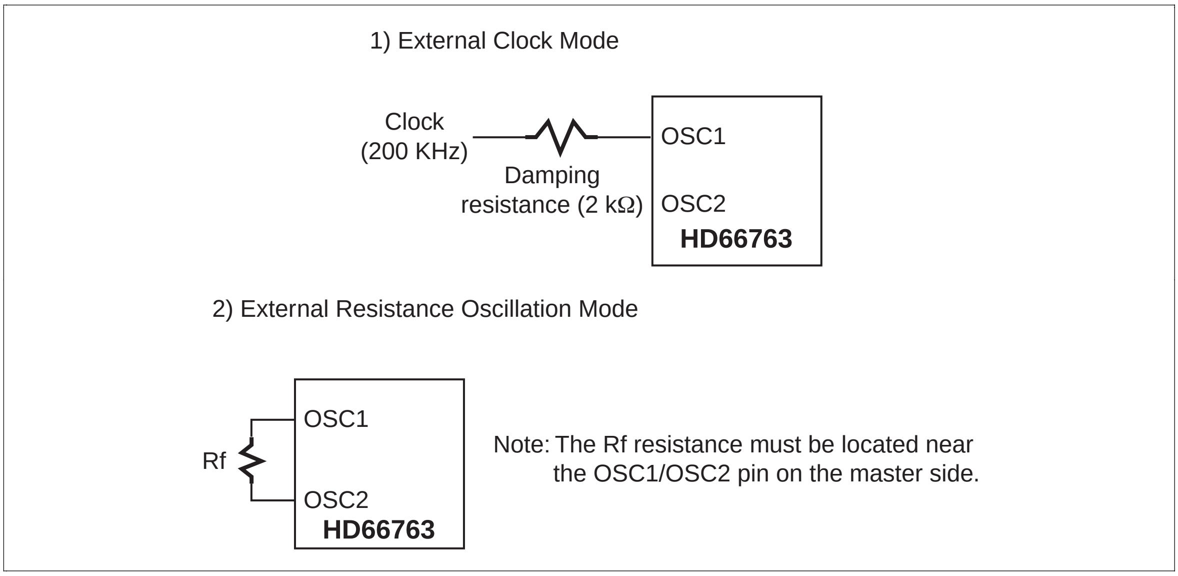


Figure 49 Oscillation Circuits

When using the HD66763 with the HD66764 common driver, the relationship between the SEG and COM output levels is as shown in the following figure. The LCD drive level (VSH, VSL) which is used by the HD66763 is supplied from the HD66764 common driver. While the display is off, SEG and COM outputs go to GND level.

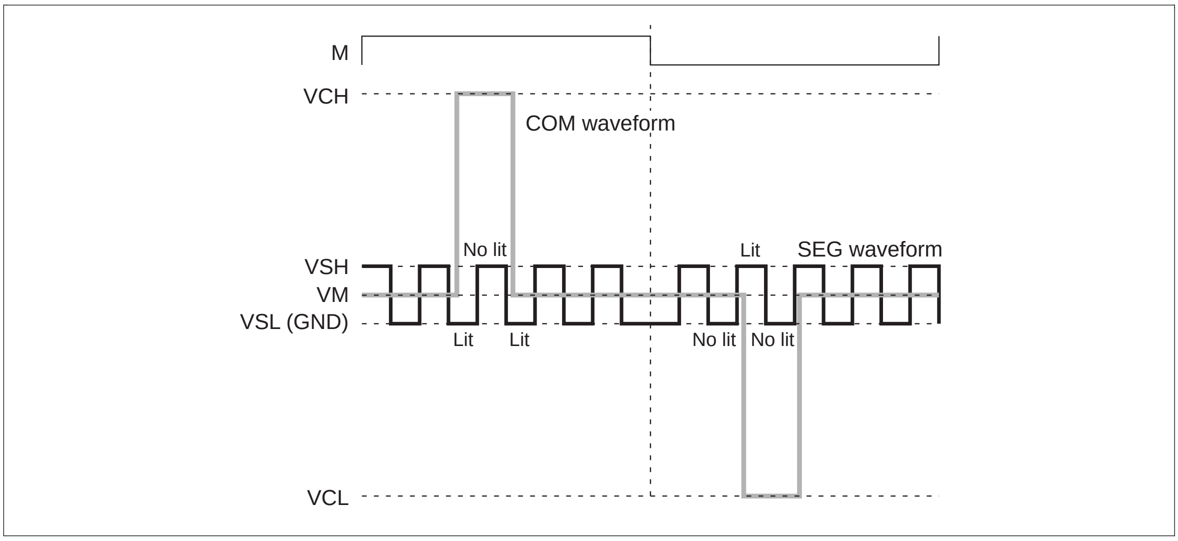


Figure 50 Relationship with SEG/COM Output Level

Frame-Frequency Adjustment Function

The HD66763 has an on-chip frame-frequency adjustment function. The frame frequency can be adjusted by the instruction setting (DIV, RTN) during the LCD drive as the oscillation frequency is always same. When the display duty is changed, the frame frequency can be adjusted to be the same.

If the oscillation frequency is set to high, an animation or a static image can be displayed in suitable ways by changing the frame frequency. When a static image is displayed, the frame frequency can be set low and the low-power consumption mode can be entered. When high-speed screen switching, for an animated display, etc. is required, the frame frequency can be set high.

Relationship between LCD Drive Duty and Frame Frequency

The relationship between the LCD drive duty and the frame frequency is calculated by the following expression. The frame frequency can be adjusted in the retrace-line period bit (RTN) and in the operation clock division bit (DIV) by the instruction.

(Formula for the frame frequency)

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{Clock cycles per raster-row} \times \text{division ratio} \times 1/\text{duty cycle}} \quad [\text{Hz}]$$

fosc: R-C oscillation frequency

Duty: drive duty (NL bit)

Division ratio: DIV bit

Clock cycles per raster-row: (RTN + 17) clock cycles

Example Calculation 1 To set the maximum frame frequency to 60 Hz

Display duty: 1/168

Retrace-line period: 0 clock (RTN3 to 0 = 0000)

Operation clock division ratio: 1 division

$$\text{fosc} = 60\ \text{Hz} \times (0 + 17)\ \text{clock} \times 1\ \text{division} \times 168\ \text{lines} = 171\ (\text{kHz})$$

In this case, the CR oscillation frequency becomes 171 kHz. The external resistance value of the CR oscillator must be adjusted to be 171 kHz. The display duty can be changed by the partial display, etc. and the frame frequency can be the same by setting the RNT bit and DIV bit to achieve the following.

Partial display

Display duty: 1/40

Retrace-line period: 1 clock (RTN3 to 0 = 0001)

Operation clock division ratio: 4 division

$$\text{Frame frequency} = 171\ \text{kHz}/\ ((1 + 17)\ \text{clock} \times 4\ \text{division} \times 40\ \text{lines}) = 59.3\ (\text{Hz})$$

Example Calculation 2 Switching the frame frequency to suit animation/static image display

(Animation display)

Frame frequency: 120 Hz

Display duty: 1/168

Retrace-line period: 0 clock (RTN3 to 0 = 0000)

Operation clock division ratio: 1 division

$$\text{fosc} = 120\ \text{Hz} \times (0 + 17)\ \text{clock} \times 1\ \text{division} \times 168\ \text{lines} = 342\ (\text{kHz})$$

(Static image display)

Frame frequency: 60 Hz

Display duty: 1/168

Retrace-line period: 0 clock (RTN3 to 0 = 0000)

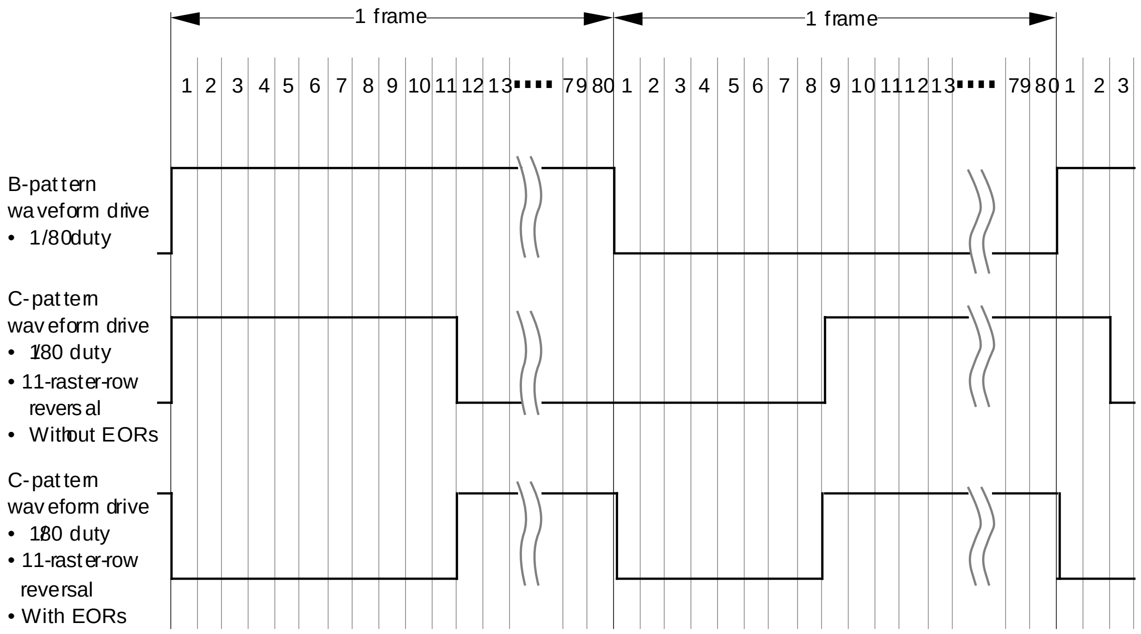
Operation clock division ratio: 1 division

$$\text{Frame frequency: } 342\ \text{kHz}/\ ((0 + 17)\ \text{clock} \times 2\ \text{division} \times 168\ \text{lines}) = 59.8\ (\text{Hz})$$

n-raster-row Reversed AC Drive

The HD66763 supports not only the LCD reversed AC drive in a one-frame unit (B-pattern waveform) but also the n-raster-row reversed AC drive which alternates in an n-raster-row unit from one to 64 raster-rows (C-pattern waveform). When a problem affecting display quality occurs, such as crosstalk at high-duty driving of more than 1/64 duty, the n-raster-row reversed AC drive (C-pattern waveform) can improve the quality.

Determine the number of raster-rows n (NW bit set value + 1) for alternating after confirmation of the display quality with the actual LCD panel. However, if the number of AC raster-rows is reduced, the LCD alternating frequency becomes high. Because of this, the charge or discharge current is increased in the LCD cells.



Note: Specify the number of AC drive raster-rows and the necessity of EOR so that the DC bias is not generated the liquid crystal.

Figure 51 Example of an AC Signal under n-raster-row Reversed AC Drive

Screen-division Driving Function

The HD66763 can select and drive two screens at any position with the screen-driving position registers (R14h and R15h). Any two screens required for display are selectively driven and a duty ratio is lowered by LCD-driving duty setting (NL4-0), thus reducing LCD-driving voltage and power consumption.

For the 1st division screen, start line (SS17-10) and end line (SE17-10) are specified by the 1st screen-driving position register (R14h). For the 2nd division screen, start line (SS27-20) and end line (SE27-20) are specified by the 2nd screen-driving position register (R15h). The 2nd screen control is effective when the SPT bit is 1. The total count of selection-driving lines for the 1st and 2nd screens must correspond to the LCD-driving duty set value.

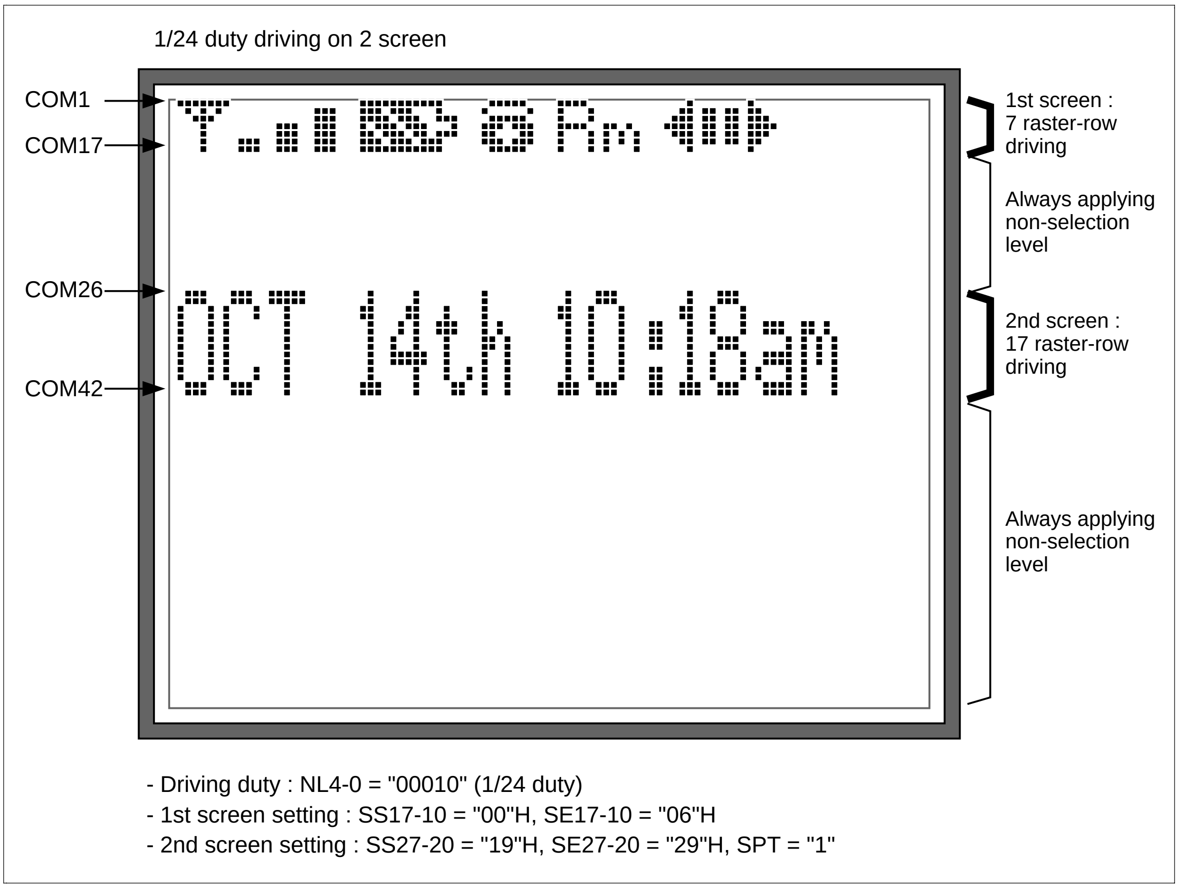


Figure 52 Display example in 2-screen division driving

Restrictions on the 1st/2nd Screen Driving Position Register Settings

The following restrictions must be satisfied when setting the start line (SS17-10) and end line (SE17-10) of the 1st screen driving position register (R14) and the start line (SS27-20) and end line (SE27-20) of the 2nd screen driving position register (R15) for the HD66763. Note that incorrect display may occur if the restrictions are not satisfied.

Table 27 Restrictions on the 1st/2nd Screen Driving Position Register Settings

	1st Screen Driving (SPT = 0)	2nd Screen Driving (SPT = 1)
Register setting	SS17-10 ≤ SE17-0 ≤ AFH	SS17-10 ≤ SE17-10 < SS27-20 ≤ SE27-20 ≤ AFH
Display operation	• Time-sharing driving for COM pins (SS1+1) to (SE1+1) • Non-selection level driving for others	• Time-sharing driving for COM pins (SS1+1) to (SE1+1) and (SS2+1) to (SE2+1) • Non-selection level driving for others

Notes: 1. When the total line count in screen division driving settings is less than the duty setting, non-selection level driving is performed without the screen division driving setting range.

2. When the total line count in screen division driving settings is larger than the duty setting, the start line, the duty-setting line, and the lines between them are displayed and non-selection level driving is performed for other lines.

3. For the 1st screen driving, the SS27-20 and SE27-20 settings are ignored.

Absolute Maximum Ratings

Item	Symbol	Unit	Value	Notes*
Power supply voltage (1)	V_{CC}	V	–0.3 to +4.6	1, 2
Power supply voltage (2)	V_{SH} – GND	V	–0.3 to +4.6	1, 3
Input voltage	Vt	V	–0.3 to V_{CC} + 0.3	1
Operating temperature	Topr	°C	–40 to +85	1, 4
Storage temperature	Tstg	°C	–55 to +110	1, 5

Notes: 1. If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristics limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

2. VCC > GND must be maintained.
3. VSH > GND must be maintained.
4. For die and wafer products, specified up to 85˚C.
5. This temperature specifications apply to the TCP package.

DC Characteristics (V_{CC} = 1.8 to 3.6 V, Ta = –40 to +85°C*[1])

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	0.7 V_{CC}	—	V_{CC}	V	V_{CC} = 1.8 to 3.6 V	2, 3
Input low voltage	V_{IL}	–0.3	—	0.15 V_{CC}	V	V_{CC} = 1.8 to 3.6 V	2, 3
Output high voltage (1) (DB0-15 pins)	V_{OH1}	0.75 V_{CC}	—	—	V	I_{OH} = –0.1 mA	2
Output low voltage (1) (DB0-15 pins)	V_{OL1}	—	—	0.2 V_{CC}	V	V_{CC} = 1.8 to 2.4 V, I_{OL} = 0.1 mA	2
		—	—	0.15 V_{CC}	V	V_{CC} = 2.4 to 3.6 V, I_{OL} = 0.1 mA	2
Driver ON resistance (SEG pins)	R_{SEG}	—	0.35	3	kΩ	±Id = 0.05 mA, V_{SH} = 3 V	4
I/O leakage current	I_{Li}	–1	—	1	µA	Vin = 0 to V_{CC}	5
Current consumption during normal operation (V_{CC} – GND)	I_{OP}	—	140	200	µA	R-C oscillation, V_{CC} = 3.0V, Ta = 25 °C, f_{OSC} = 180 kHz (1/176 duty) Writing to RAM: checker	6, 7
Current consumption during standby mode (V_{CC} – GND)	I_{ST}	—	0.1	5	µA	V_{CC} = 3.0 V, Ta = 25°C	6, 7
LCD drive power supply current (V_{SH} – GND)	I_{LCD}	—	40	60	µA	V_{CC} = 3 V, V_{LCD} = 4 V, R-C oscillation; f_{OSC} = 180 kHz (1/176 duty), Ta = 25 °C, Writing to RAM: checker	7
LCD drive voltage (V_{SH} – GND)	V_{LCD}	2.0	—	4.0	V		8

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

AC Characteristics (V_{CC} = 1.8 to 3.6 V, Ta = –40 to +85°C*[1])

Clock Characteristics (V_{CC} = 1.8 to 3.6 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
External clock frequency	fcp	140	210	315	kHz	V_{CC} = 1.8 to 3.6 V	9
External clock duty ratio	Duty	45	50	55	%	V_{CC} = 1.8 to 3.6 V	9
External clock rise time	trcp	—	—	0.2	µs	V_{CC} = 1.8 to 3.6 V	9
External clock fall time	tfcp	—	—	0.2	µs	V_{CC} = 1.8 to 3.6 V	9
R-C oscillation clock	f_{OSC}	168	210	252	kHz	Rf = 220 kΩ, V_{CC} = 3 V	10

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

68-system Bus Interface Timing Characteristics

<Normal write mode (HWM = 0), Vcc = 1.8 to 2.4 V>

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	Write	t_{CYCE}	600	—	—	ns	Figure 58
	Read	t_{CYCE}	800	—	—		
Enable high-level pulse width	Write	PW_{EH}	90	—	—	ns	Figure 58
	Read	PW_{EH}	350	—	—		
Enable low-level pulse width	Write	PW_{EL}	300	—	—	ns	Figure 58
	Read	PW_{EL}	400	—	—		
Enable rise/fall time		t_{Er}, t_{Ef}	—	—	25	ns	Figure 58
Setup time (RS, R/W to E, CS*)		t_{ASE}	10	—	—	ns	Figure 58
Address hold time		t_{AHE}	5	—	—	ns	Figure 58
Write data setup time		t_{DSWE}	60	—	—	ns	Figure 58
Write data hold time		t_{HE}	15	—	—	ns	Figure 58
Read data delay time		t_{DDRE}	—	—	200	ns	Figure 58
Read data hold time		t_{DHRE}	5	—	—	ns	Figure 58

<High-speed write mode (HWM = 1), Vcc = 1.8 to 2.4 V>

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	Write	t_{CYCE}	200	—	—	ns	Figure 58
	Read	t_{CYCE}	800	—	—		
Enable high-level pulse width	Write	PW_{EH}	90	—	—	ns	Figure 58
	Read	PW_{EH}	350	—	—		
Enable low-level pulse width	Write	PW_{EL}	90	—	—	ns	Figure 58
	Read	PW_{EL}	400	—	—		
Enable rise/fall time		t_{Er}, t_{Ef}	—	—	25	ns	Figure 58
Setup time (RS, R/W to E, CS*)		t_{ASE}	10	—	—	ns	Figure 58
Address hold time		t_{AHE}	5	—	—	ns	Figure 58
Write data setup time		t_{DSWE}	60	—	—	ns	Figure 58
Write data hold time		t_{HE}	15	—	—	ns	Figure 58
Read data delay time		t_{DDRE}	—	—	200	ns	Figure 58
Read data hold time		t_{DHRE}	5	—	—	ns	Figure 58

<Normal write mode (HWM = 0), Vcc = 2.4 to 3.6 V>

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	Write	t_{CYCE}	250	—	—	ns	Figure 58
	Read	t_{CYCE}	500	—	—		
Enable high-level pulse width	Write	PW_{EH}	40	—	—	ns	Figure 58
	Read	PW_{EH}	250	—	—		
Enable low-level pulse width	Write	PW_{EL}	100	—	—	ns	Figure 58
	Read	PW_{EL}	200	—	—		
Enable rise/fall time		t_{Er}, t_{Ef}	—	—	25	ns	Figure 58
Setup time (RS, R/W to E, CS*)		t_{ASE}	10	—	—	ns	Figure 58
Address hold time		t_{AHE}	5	—	—	ns	Figure 58
Write data setup time		t_{DSWE}	60	—	—	ns	Figure 58
Write data hold time		t_{HE}	15	—	—	ns	Figure 58
Read data delay time		t_{DDRE}	—	—	200	ns	Figure 58
Read data hold time		t_{DHRE}	5	—	—	ns	Figure 58

<High-speed write mode (HWM = 1), Vcc = 2.4 to 3.6 V>

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	Write	t_{CYCE}	100	—	—	ns	Figure 58
	Read	t_{CYCE}	500	—	—		
Enable high-level pulse width	Write	PW_{EH}	40	—	—	ns	Figure 58
	Read	PW_{EH}	250	—	—		
Enable low-level pulse width	Write	PW_{EL}	50	—	—	ns	Figure 58
	Read	PW_{EL}	200	—	—		
Enable rise/fall time		t_{Er}, t_{Ef}	—	—	25	ns	Figure 58
Setup time (RS, R/W to E, CS*)		t_{ASE}	10	—	—	ns	Figure 58
Address hold time		t_{AHE}	5	—	—	ns	Figure 58
Write data setup time		t_{DSWE}	60	—	—	ns	Figure 58
Write data hold time		t_{HE}	15	—	—	ns	Figure 58
Read data delay time		t_{DDRE}	—	—	200	ns	Figure 58
Read data hold time		t_{DHRE}	5	—	—	ns	Figure 58

80-system Bus Interface Timing Characteristics

<Normal write mode (HWM = 0), Vcc = 1.8 to 2.4 V>

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Bus cycle time	Write	t_{CYCW}	600	—	—	ns	Figure 59
	Read	t_{CYCR}	800	—	—	ns	Figure 59
Write low-level pulse width		PW_{LW}	90	—	—	ns	Figure 59
Read low-level pulse width		PW_{LR}	350	—	—	ns	Figure 59
Write high-level pulse width		PW_{HW}	300	—	—	ns	Figure 59
Read high-level pulse width		PW_{HR}	400	—	—	ns	Figure 59
Write/Read rise/fall time		t_{WRr}, $_{WRf}$	—	—	25	ns	Figure 59
Setup time (RS to CS*, WR*, RD*)		t_{AS}	10	—	—	ns	Figure 59
Address hold time		t_{AH}	5	—	—	ns	Figure 59
Write data setup time		t_{DSW}	60	—	—	ns	Figure 59
Write data hold time		t_H	15	—	—	ns	Figure 59
Read data delay time		t_{DDR}	—	—	200	ns	Figure 59
Read data hold time		t_{DHR}	5	—	—	ns	Figure 59

<High-speed write mode (HWM = 0), Vcc = 1.8 to 2.4 V>

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Bus cycle time	Write	t_{CYCW}	200	—	—	ns	Figure 59
	Read	t_{CYCR}	800	—	—	ns	Figure 59
Write low-level pulse width		PW_{LW}	90	—	—	ns	Figure 59
Read low-level pulse width		PW_{LR}	350	—	—	ns	Figure 59
Write high-level pulse width		PW_{HW}	90	—	—	ns	Figure 59
Read high-level pulse width		PW_{HR}	400	—	—	ns	Figure 59
Write/Read rise/fall time		t_{WRr}, $_{WRf}$	—	—	25	ns	Figure 59
Setup time (RS to CS*, WR*, RD*)		t_{AS}	10	—	—	ns	Figure 59
Address hold time		t_{AH}	5	—	—	ns	Figure 59
Write data setup time		t_{DSW}	60	—	—	ns	Figure 59
Write data hold time		t_H	15	—	—	ns	Figure 59
Read data delay time		t_{DDR}	—	—	200	ns	Figure 59
Read data hold time		t_{DHR}	5	—	—	ns	Figure 59

<Normal write mode (HWM = 0), Vcc = 2.4 to 3.6 V>

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Bus cycle time	Write	t_{CYCW}	250	—	—	ns	Figure 59
	Read	t_{CYCR}	500	—	—	ns	Figure 59
Write low-level pulse width		PW_{LW}	40	—	—	ns	Figure 59
Read low-level pulse width		PW_{LR}	250	—	—	ns	Figure 59
Write high-level pulse width		PW_{HW}	100	—	—	ns	Figure 59
Read high-level pulse width		PW_{HR}	200	—	—	ns	Figure 59
Write/Read rise/fall time		$t_{WRr, WRf}$	—	—	25	ns	Figure 59
Setup time (RS to CS*, WR*, RD*)		t_{AS}	10	—	—	ns	Figure 59
Address hold time		t_{AH}	5	—	—	ns	Figure 59
Write data setup time		t_{DSW}	60	—	—	ns	Figure 59
Write data hold time		t_{H}	15	—	—	ns	Figure 59
Read data delay time		t_{DDR}	—	—	200	ns	Figure 59
Read data hold time		t_{DHR}	5	—	—	ns	Figure 59

<High-speed write mode (HWM = 1), Vcc = 2.4 to 3.6 V>

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Bus cycle time	Write	t_{CYCW}	100	—	—	ns	Figure 59
	Read	t_{CYCR}	500	—	—	ns	Figure 59
Write low-level pulse width		PW_{LW}	40	—	—	ns	Figure 59
Read low-level pulse width		PW_{LR}	250	—	—	ns	Figure 59
Write high-level pulse width		PW_{HW}	50	—	—	ns	Figure 59
Read high-level pulse width		PW_{HR}	200	—	—	ns	Figure 59
Write/Read rise/fall time		$t_{WRr, WRf}$	—	—	25	ns	Figure 59
Setup time (RS to CS*, WR*, RD*)		t_{AS}	10	—	—	ns	Figure 59
Address hold time		t_{AH}	5	—	—	ns	Figure 59
Write data setup time		t_{DSW}	60	—	—	ns	Figure 59
Write data hold time		t_{H}	15	—	—	ns	Figure 59
Read data delay time		t_{DDR}	—	—	200	ns	Figure 59
Read data hold time		t_{DHR}	5	—	—	ns	Figure 59

Clock Synchronized Serial Interface Timing Characteristics

(Vcc = 1.8 to 2.4 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	At write (receive)	t_{SCYC}	0.1	—	20	us	Figure 60
	At read (send)	t_{SCYC}	0.25	—	20	us	Figure 60
Serial clock high-level pulse width	At write (receive)	t_{SCH}	40	—	—	ns	Figure 60
	At read (send)	t_{SCH}	120	—	—	ns	Figure 60
Serial clock low-level pulse width	At write (receive)	t_{SCL}	40	—	—	ns	Figure 60
	At read (send)	t_{SCL}	120	—	—	ns	Figure 60
Serial clock rise/fall time		t_{SCr} , t_{SCf}	—	—	20	ns	Figure 60
CS* Setup time		t_{CSU}	20	—	—	ns	Figure 60
CS* hold time		t_{CH}	60	—	—	ns	Figure 60
Serial input data setup time		t_{SISU}	30	—	—	ns	Figure 60
Serial input data hold time		t_{SIH}	30	—	—	ns	Figure 60
Serial output data delay time		t_{SOD}	—	—	200	ns	Figure 60
Serial output data hold time		t_{SOH}	5	—	—	ns	Figure 60

(Vcc = 2.4 to 3.6 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	At write (receive)	t_{SCYC}	0.1	—	20	us	Figure 60
	At read (send)	t_{SCYC}	0.15	—	20	us	Figure 60
Serial clock high-level pulse width	At write (receive)	t_{SCH}	40	—	—	ns	Figure 60
	At read (send)	t_{SCH}	70	—	—	ns	Figure 60
Serial clock low-level pulse width	At write (receive)	t_{SCL}	40	—	—	ns	Figure 60
	At read (send)	t_{SCL}	70	—	—	ns	Figure 60
Serial clock rise/fall time		t_{SCr} , t_{SCf}	—	—	20	ns	Figure 60
CS* Setup time		t_{CSU}	20	—	—	ns	Figure 60
CS* hold time		t_{CH}	60	—	—	ns	Figure 60
Serial input data setup time		t_{SISU}	30	—	—	ns	Figure 60
Serial input data hold time		t_{SIH}	30	—	—	ns	Figure 60
Serial output data delay time		t_{SOD}	—	—	130	ns	Figure 60
Serial output data hold time		t_{SOH}	5	—	—	ns	Figure 60

Reset Timing Characteristics (V_{CC} = 1.8 to 3.6 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Reset low-level width	t_{RES}	1	—	—	ms	Figure 61
Reset rise time	t_{rRES}	—	—	10	us	Figure 61

Electrical Characteristics Notes

1. For bare die and wafer products, specified up to 85˚C.
2. The following three circuits are I/O pin configurations.

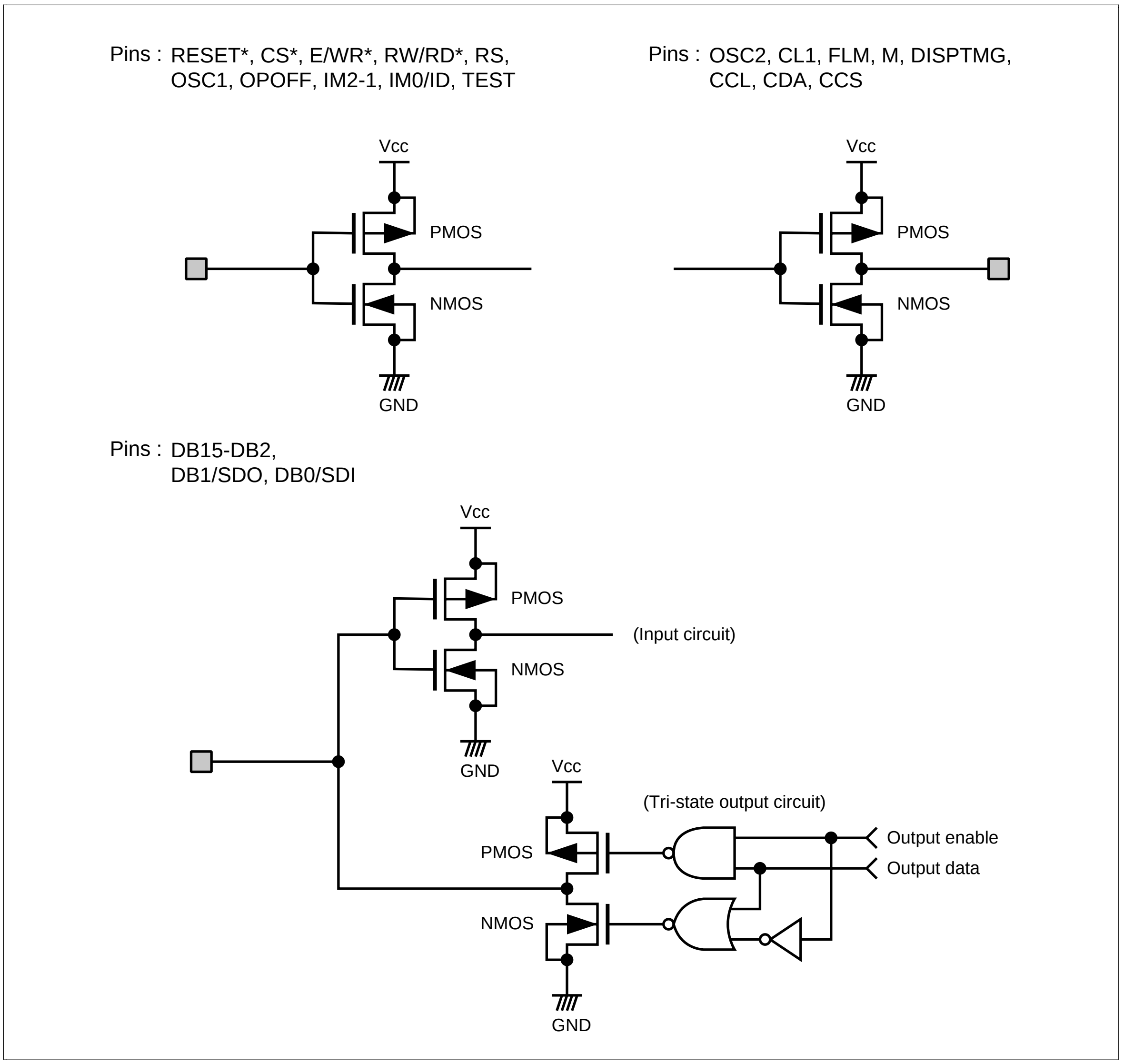


Figure 53 I/O Pin Configuration

3. The TEST pin must be grounded and the IM2/IM1/0 pins must be grounded or connected to Vcc.
4. Applies to the resistor value (RSEG) between power supply pins VSH, GND and segment signal pins.
5. This excludes the current flowing through output drive MOSs.
6. This excludes the current flowing through the input/output units. The input level must be fixed high or low because through current increases if the CMOS input is left floating.
7. The following shows the relationship between the operation frequency and current consumption.

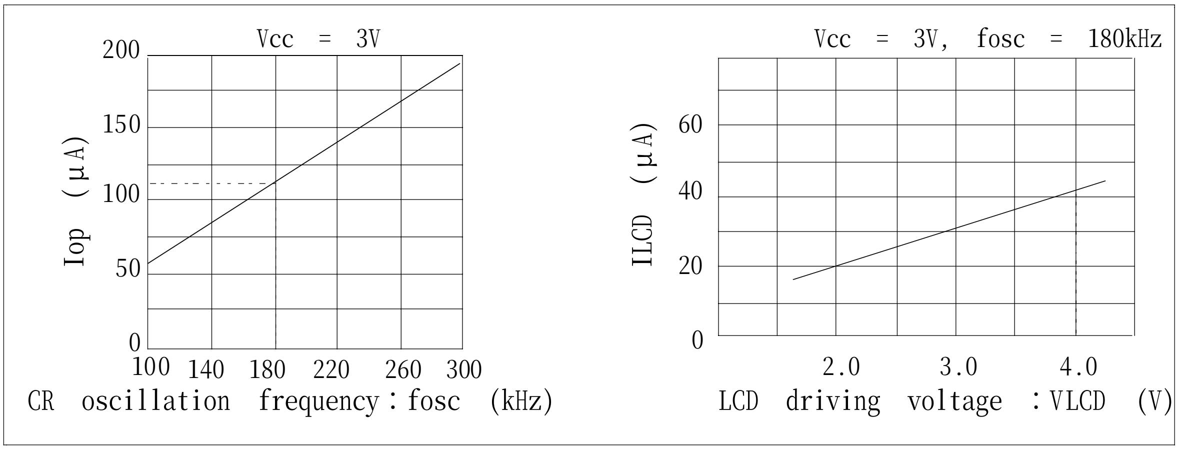


Figure 54 Relationship between the Operation Frequency and Current Consumption

8. Each SEG output voltage is within ±0.15 V of the LCD voltage (VSH, GND) when there is no load.
9. Applies to the external clock input.

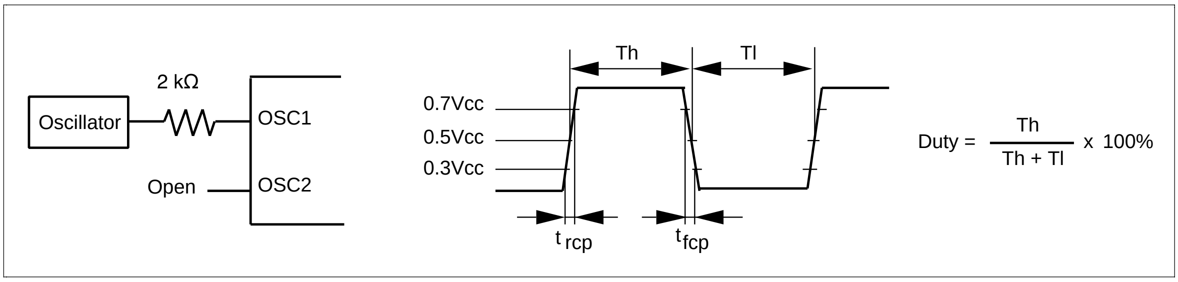
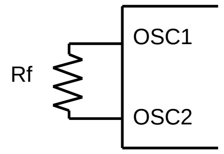


Figure 55 External Clock Supply

10. Applies to the internal oscillator operations using external oscillation resistor Rf.



Since the oscillation frequency varies depending on the OSC1 and OSC2 pin capacitance, the wiring length to these pins should be minimized.

Figure 56 Internal Oscillation

Table 30 External Resistance Value and R-C Oscillation Frequency (Referential Data)

External Resistance (Rf)	R-C Oscillation Frequency: fosc				
	Vcc = 1.8 V	Vcc = 2.2 V	Vcc = 2.4 V	Vcc = 3.0 V	Vcc = 3.6 V
91 kΩ	252 kHz	315 kHz	339 kHz	389 kHz	424 kHz
120 kΩ	216 kHz	267 kHz	286 kHz	326 kHz	353 kHz
150 kΩ	187 kHz	228 kHz	243 kHz	274 kHz	294 kHz
200 kΩ	159 kHz	191 kHz	202 kHz	225 kHz	240 kHz
240 kΩ	139 kHz	166 kHz	175 kHz	193 kHz	205 kHz
270 kΩ	129 kHz	152 kHz	160 kHz	176 kHz	186 kHz
320 kΩ	114 kHz	133 kHz	140 kHz	152 kHz	161 kHz
360 kΩ	104 kHz	121 kHz	126 kHz	138 kHz	145 kHz
390 kΩ	96 kHz	113 kHz	118 kHz	128 kHz	134 kHz
440 kΩ	90 kHz	103 kHz	108 kHz	116 kHz	122 kHz

Load Circuits

AC Characteristics Test Load Circuits

Data bus: DB15 to DB0

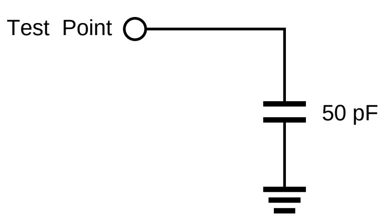
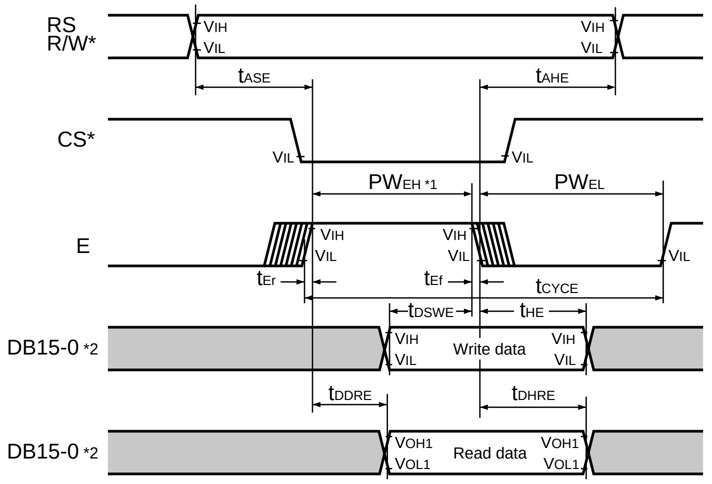


Figure 57 Load Circuit

Timing Characteristics

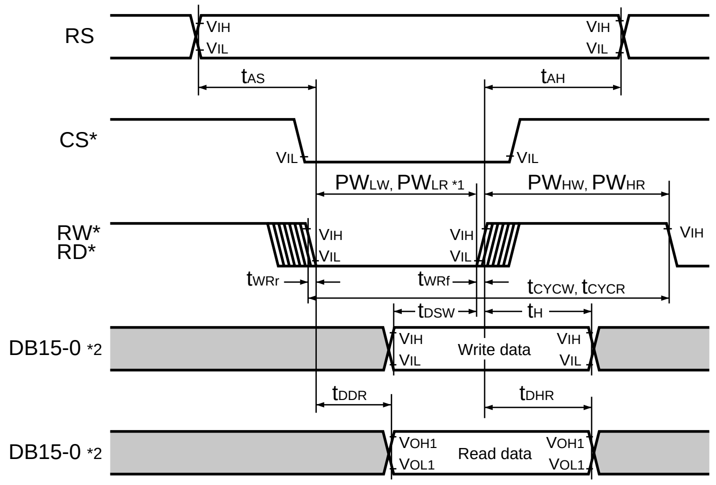
68-system Bus Operation



Note 1 : PWEH is specified in the overlapped period when CS* is low and E is high.
Note 2 : In case of 8-bit interface mode, DB15-8 are used for parallel interface.
Fixed unused DB7-0 to the Vcc or GND level.

Figure 58 68-system Bus Timing

80-system Bus Operation



Note 1 : PWLW and PWLR are specified in the overlapped period when CS* is low and WR* or RD* is low.
Note 2 : In case of 8-bit interface mode, DB15-8 are used for parallel interface.
Fixed unused DB7-0 to the Vcc or GND level.

Figure 59 80-system Bus Timing

Clock Synchronized Serial Interface Operation

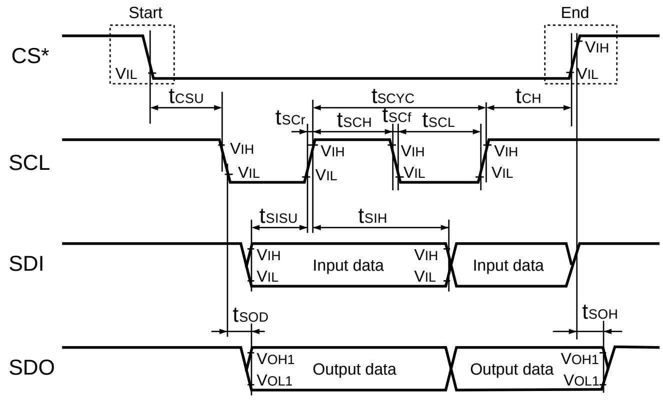


Figure 60 Clock Synchronized Serial Interface Input Timing

Reset Operation

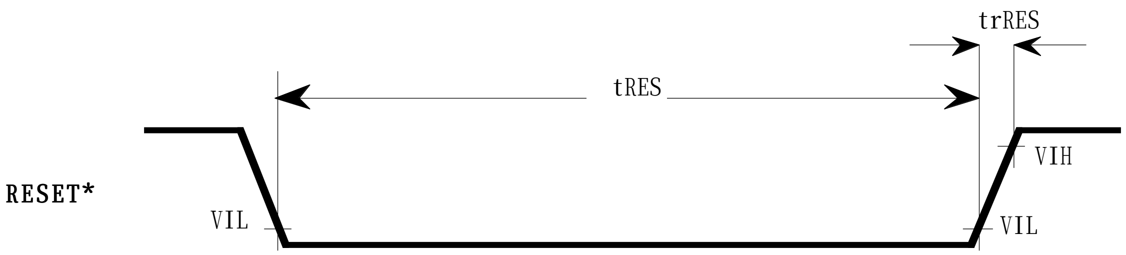


Figure 61 Reset Timing

Modification history

Revision 0.3

- First release

Revision 0.4

- Added electrical characteristics section (preliminary)