HMC987LP5E

LOW NOISE 1:9 FANOUT BUFFER DC - 8 GHz

Typical Applications

The is suitable for:

- SONET, Fibre Channel, GigE Clock Distribution
- ADC/DAC Clock Distribution
- Low Skew and Jitter Clock or Data Fanout
- Wireless/Wired Communications
- Level Translation
- High Performance Instrumentation
- Medical Imaging
- Single-Ended to Differential Conversion

Features

Ultra Low Noise Floor: -166 dBc/Hz @ 2 GHz

Wideband: DC - 8 GHz Operating Frequency

Flexible Input Interface:

LVPECL, LVDS, CML, CMOS Compatible

AC or DC Coupling

On-Chip Termination 50 or 150 Ω (100/300 Ω Diff.)

Multiple Output Drivers:

Up to 8 Differential or 16 Single-Ended LVPECL Outputs:

800 mVpp into 50 Ω Single-Ended (+3 dBm Fo)

One Adjustable Power CML/RF Output:

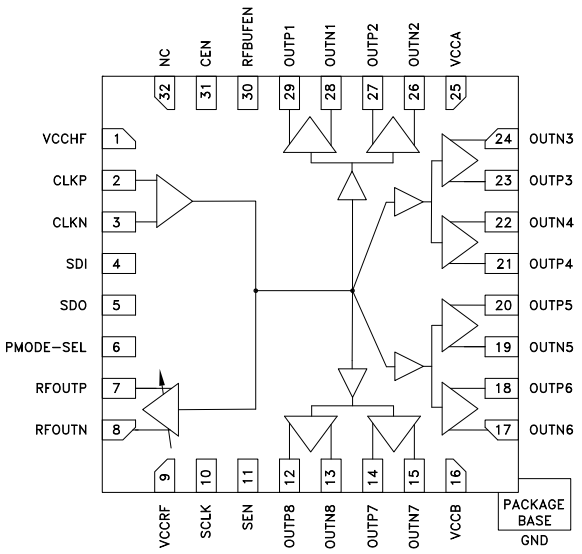
-9 to 3 dBm Single-Ended

Serial or Parallel Control, Hardware Chip-Enable

Power-Down Current < 1 uA

32 Lead 5x5 mm SMT Package 25 mm^2

Functional Diagram



General Description

The 1-to-9 fanout buffer is designed for low noise clock distribution. It is intended to generate relatively square wave outputs with rise/fall times < 100 ps. The low skew and jitter outputs of the, combined with its fast rise/fall times, leads to controllable low-noise switching of downstream circuits such as mixers, ADCs/DACs or SERDES devices. The noise floor is particularly important in these applications, when the clock-network bandwidth is wide enough to allow square-wave switching. Driven at 2 GHz, outputs of the have a noise floor of -166 dBc/Hz, corresponding to a jitter density of 0.6 asec/rtHz - or 50 fs over an 8 GHz bandwidth.

The input stage can be driven single-ended or differentially, in a variety of signal formats (CML, LVDS, LVPECL or CMOS), AC or DC coupled. The input stage also features adjustable input impedance. It has 8 LVPECL outputs, and 1 CML output with adjustable swing/power-level in 3 dB steps.

Individual output stages may be enabled or disabled for power-savings when not required using either hardware control pins, or under control of a serial-port interface.

Table 1. Electrical Specifications

Unless otherwise specified: T = 27 °C, Regulated VDD of 3.3 V, 2 GHz, 6 dBm in, AC coupled single ended input and output, 120 Ω/leg DC termination, AC coupled into 50 Ω measuring load. Effects of customer eval board ("Evaluation PCB Schematic") are de-embedded. For convenience, all voltages are referenced to GND (0V), but negative supply references are acceptable.

Parameter	Conditions	Min.	Typ.	Max.	Units
DC Input Characteristics					
VDD (VCCHF=VCCA=VCCB=VCCRF)		3.0	3.3	3.6	V
Input Common Mode Voltage		1.35	2	VDD - 0.2	V
Input Swing (Single Ended)		0.2		2	Vpp
Input Capacitance			0.5		pF
Input Impedance					
Single-Ended	Selectable		50 / 150		Ω
Differential	Selectable		100 / 300		Ω
Input Bias Current	Base current under external DC bias, Internal termination open.		165		µA
Logic Inputs					
Switching Threshold (Vsw)	VIH/VIL within 50 mV of Vsw	38	47	54	%VDD
LVPECL DC Output Characteristics					
Output Voltage High Level	@ 3.3 V = 2.25	VDD - 1.2	VDD - 1.0	VDD - 0.8	V
Ouput Voltage Common Mode	@ 3.3 V = 1.82	VDD - 1.7	VDD - 1.5	VDD - 1.3	V
Output Voltage Low Level	@ 3.3 V = 1.42	VDD - 2.1	VDD - 1.9	VDD - 1.7	V
Output Voltage, Single-Ended			800		mVpp
AC Performance					
Input/Output Frequency [1]	> 400 Vpp single-ended	DC		8000	MHz
3 dB Bandwidth			4000		MHz
Output Rise/Fall Time	20% to 80%		65		ps
Typical Channel Skew	Across all LVPECL outputs relative to channel 1	0	1.5	3.1	ps
Small Signal Gain S21					
1000 MHz			26		dB
4000 MHz			15		dB
Input P1dB					
1000 MHz			-20		dBm
4000 MHz			-10		dBm
Saturated Power in fundamental tone (Single-Ended)					
1000 MHz			2.5		dBm
4000 MHz			-0.5		dBm
Output Voltage Swing (Vppd into 100 Ω)					
700 MHz		1.5	1.6	1.7	V
2000 MHz		1.2	1.3	1.4	V

[1] For frequencies < 700 MHz, square wave signals should be used to maintain high quality phase noise performance.

Table 1. Electrical Specifications (Continued...)

Parameter	Conditions	Min.	Typ.	Max.	Units
4000 MHz		1.1	1.2	1.3	V
Harmonics					
Fo			2		dBm
2Fo			-25		dBc
3Fo			-8		dBc
4Fo			-28		dBc
5Fo			-12		dBc
SSB Phase Noise at 100 Hz Offset					
622.08 MHz Carrier Frequency			-147		dBc/Hz
1750 MHz Carrier Frequency			-147		dBc/Hz
4000 MHz Carrier Frequency			-147		dBc/Hz
SSB Phase Noise Floor [2]					
100 MHz Carrier Frequency			-167		dBc/Hz
622.08 MHz Carrier Frequency			-167		dBc/Hz
1750 MHz Carrier Frequency			-166		dBc/Hz
2000 MHz Carrier Frequency			-166		dBc/Hz
4000 MHz Carrier Frequency			-163		dBc/Hz
4200 MHz Carrier Frequency			-162		dBc/Hz
Floor Jitter Density					
622.08 MHz Carrier Frequency			1.8		asec/√Hz
1750 MHz Carrier Frequency			0.7		asec/√Hz
4000 MHz Carrier Frequency			0.5		asec/√Hz
Integrated RMS Jitter					
622.08 MHz Carrier Frequency	100 Hz to 100 MHz		17		fs rms
	12 kHz to 20 MHz		8		fs rms
	20 kHz to 80 MHz		17		fs rms
	50 kHz to 80 MHz		17		fs rms
	4 MHz to 80 MHz		16		fs rms
1750 MHz Carrier Frequency	100 Hz to 100 MHz		7		fs rms
	12 kHz to 20 MHz		3		fs rms
	20 kHz to 80 MHz		6		fs rms
	50 kHz to 80 MHz		6		fs rms
	4 MHz to 80 MHz		6		fs rms
4000 MHz Carrier Frequency	100 Hz to 100 MHz		4		fs rms
	12 kHz to 20 MHz		2		fs rms
	20 kHz to 80 MHz		4		fs rms
	50 kHz to 80 MHz		4		fs rms
	4 MHz to 80 MHz		4		fs rms
Output Return Loss	500 MHz to 4 GHz	-16	-12	-8	dB

[2] CML buffer has similar phase noise characteristics at maximum output power level.

Table 1. Electrical Specifications *(Continued...)*

Parameter	Conditions	Min.	Typ.	Max.	Units
Isolation					
In to Out - Chip Disabled			47		dB
Off isolation - Relative to Power of neighboring driven port					
700 MHz		60		48	dB
4000 MHz		50		32	dB
Output to Output Isolation with 500 MHz Aggressor Signal Injected into Output Port					
To Locally paired output buffer			25		dB
To other buffers			45		dB
RF Output Buffer					
3 dB Bandwidth			5000		MHz
Max Output Power (vs Temperature at 2 GHz)	Single-Ended	3		3.2	dBm
Power Control Range (3 dB steps)	Single-Ended	-9		3	dBm
Delay Relative to LVPECL Output			-140		ps
Power Supply Rejection					
FM/Phase Pushing			0.8		ps/V
AM Rejection			7		dB
Current Consumption (3.3 V Unloaded Outputs)					
Chip Disabled			1		µA
1 Output			60		mA
2 Outputs			71		mA
3 Outputs			97		mA
4 Outputs			108		mA
5 Outputs			134		mA
6 Outputs			144		mA
7 Outputs			170		mA
8 Outputs			180		mA
8 + RF Buffer (Min to Max Power)		198		234	mA

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified: T = 27 °C, Regulated VDD = 3.3 V, 2 GHz, 6 dBm in, AC coupled single ended input and output, 120 Ω/leg DC termination, AC coupled into 50 Ω measuring load.

Figure 1. LVPECL Output vs. Frequency [1]

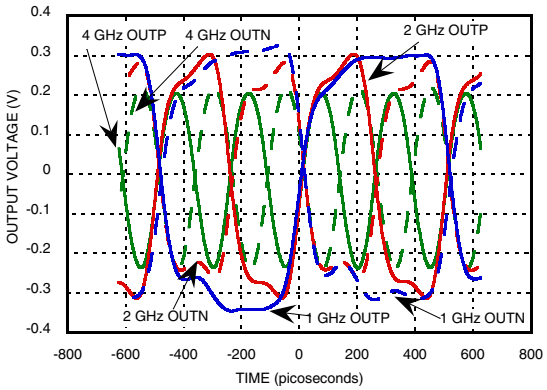


Figure 2. LVPECL Output vs. Frequency [1]

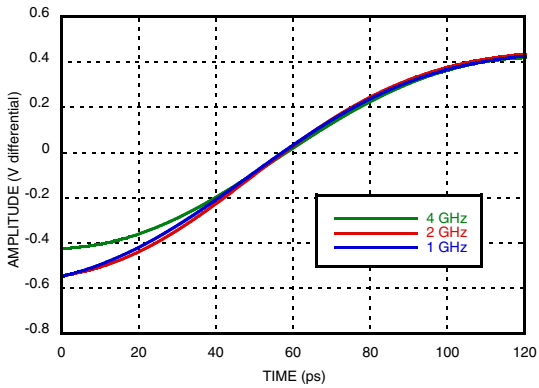


Figure 3. Current Consumption vs. Num. of Enabled Buffers & Load Resistors[2]

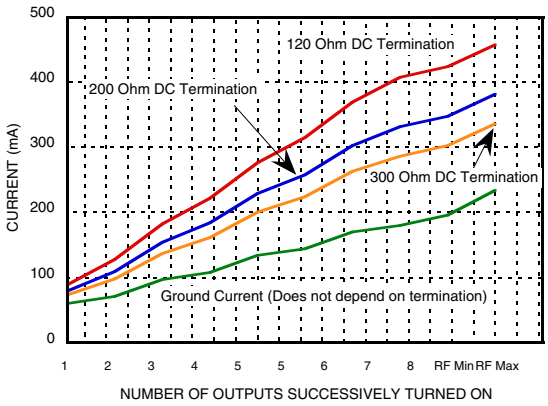


Figure 4. Skew of LVPECL Outputs Relative to Output Channel 1 [4]

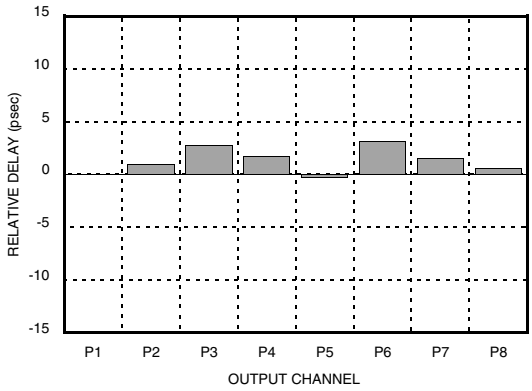


Figure 5. Fundamental Output Power vs. Input Power [3]

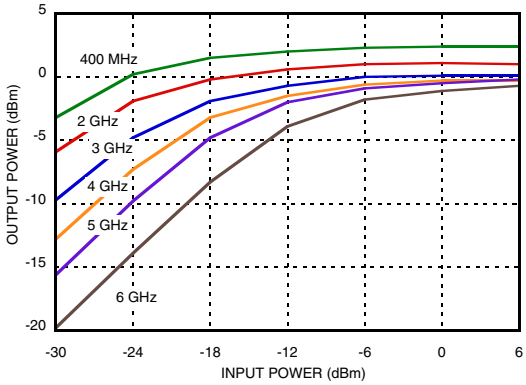
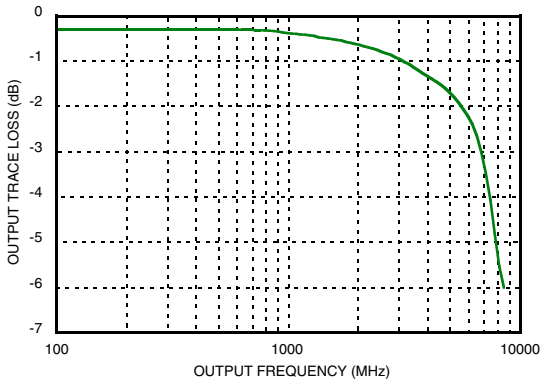


Figure 6. Evaluation Board LVPECL Output Trace Loss vs. Frequency [5]



[1] +2dBm input, Uncorrected for board loss. Measurement is band limited by the trace bandwidth of 7 GHz.
[2] Buffers 1 through 8 are successively turned on. RF Min - RF buffer turned on with minimum gain, RF Max - RF buffer turned on with maximum gain
[3] 200 Ω Termination, Corrected for board loss.
[4] Characterized at 2 GHz, Effects of customer evaluation board skew and loss are embedded.
[5] The graph shows only output trace distortion.

Figure 7. RF Buffer Fo Output Power vs. Frequency & Temperature (Max Gain)

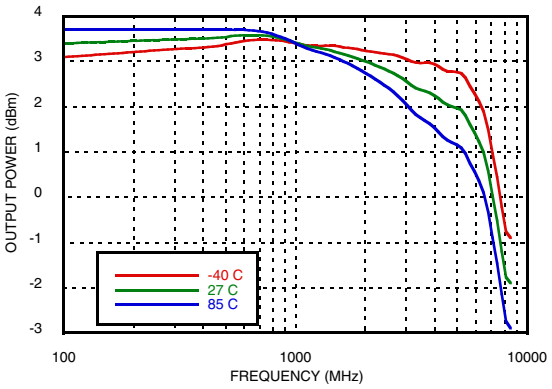


Figure 8. RF Output Power Control

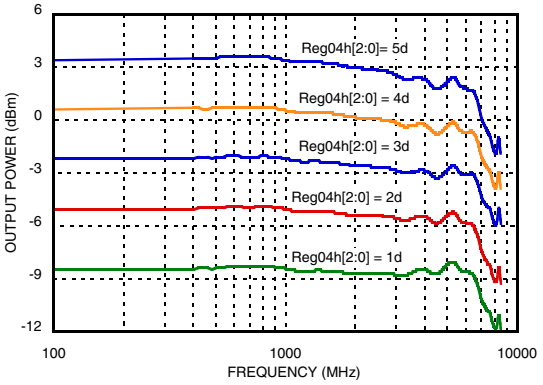


Figure 9. Fundamental Output Power vs. Frequency & Temperature [6]

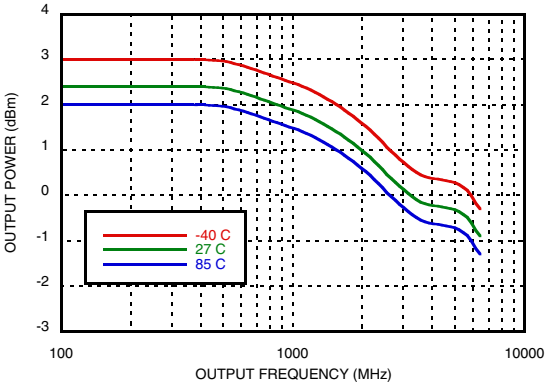


Figure 10. Fundamental Output Power vs. Frequency & Supply Voltage at 27 °C [6]

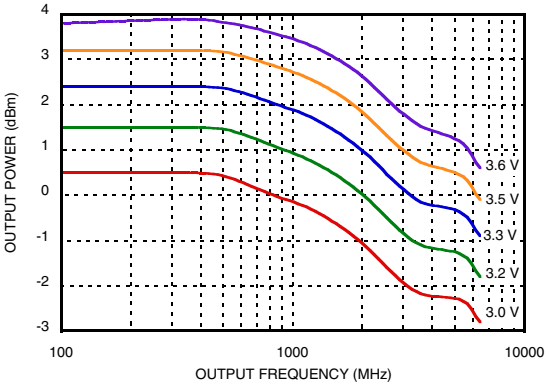


Figure 11. Fundamental Output Power vs. Frequency & Termination at 27 °C [6]

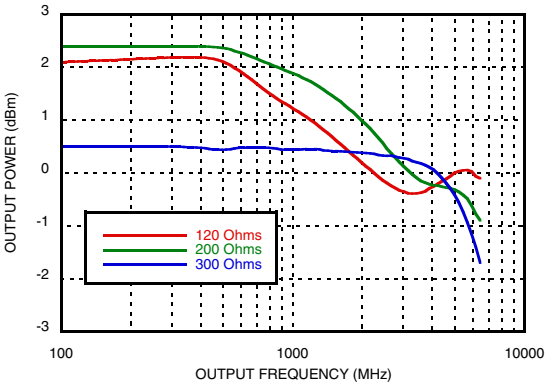
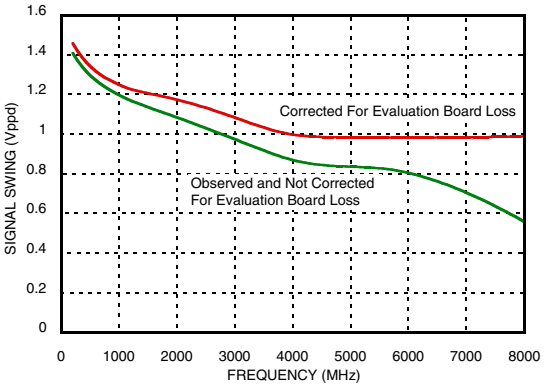


Figure 12. Signal Swing vs. Frequency [7]



[6] Measured single-ended. Corrected for trace loss. 200 Ω DC termination, 3.3 V +6 dBm single-ended input. HMC987LP5E AC coupled to 50 Ω instrument.

[7] Input signal power = + 6 dBm. 120 Ω/leg DC termination. AC coupled via 50 pF to 26 GHz Oscilloscope (50 Ohm/leg termination).

Figure 13. Phase Noise Performance at 2 GHz (Differential Drive) [9]

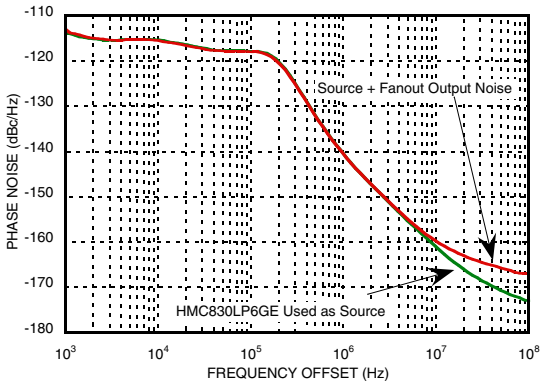


Figure 14. Phase Noise Floor vs. Slew Rate

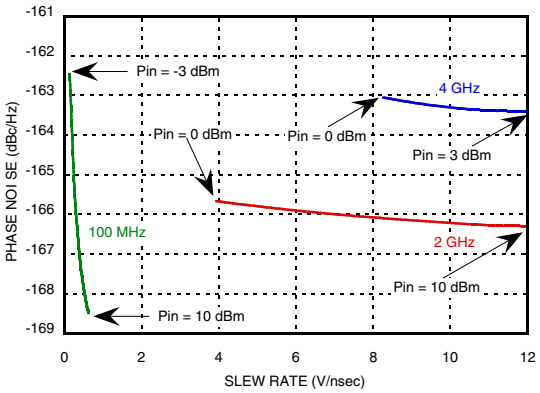


Figure 15. Phase Noise Floor at 1.6 GHz vs. Input Power

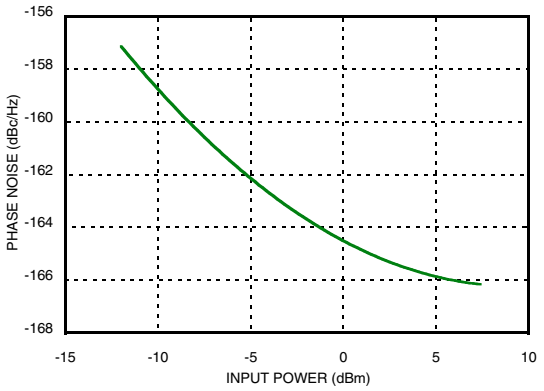


Figure 16. Phase Noise Performance with Low Frequency Sinusoidal Inputs [8]

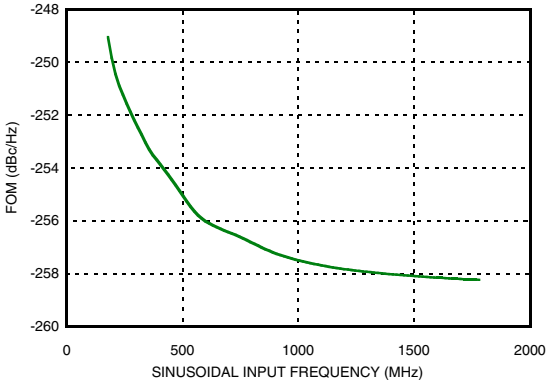


Figure 17. Phase Noise Floor at 2 GHz vs. VDD and DC Termination

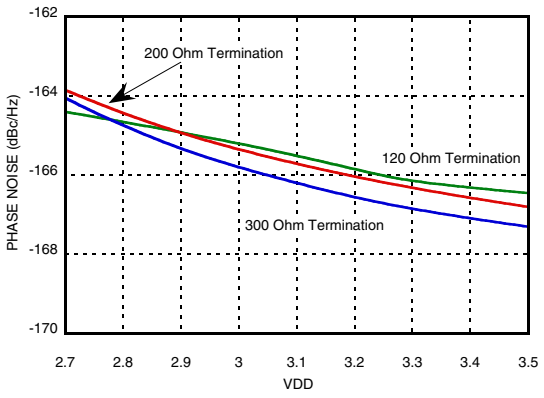
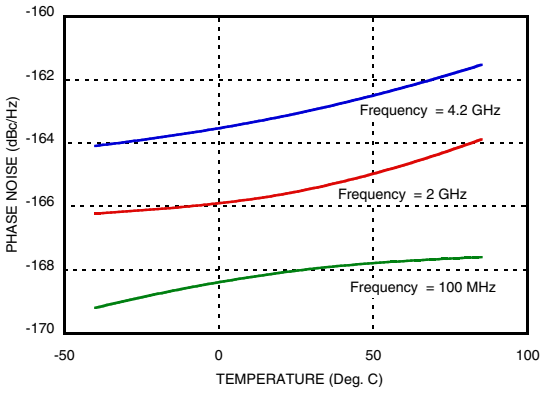


Figure 18. Phase Noise Floor vs. Temperature



[8] Input power = 10 dBm single-ended. Phase Noise Floor (dBc/Hz) = FOM (dBc/Hz)) + 10log(Fout [Hz])
[9] HMC830LP6GE used as signal source, Driving +9 dBm differentially.

Figure 19. Harmonic Performance (Single-Ended Input & Output) [10]

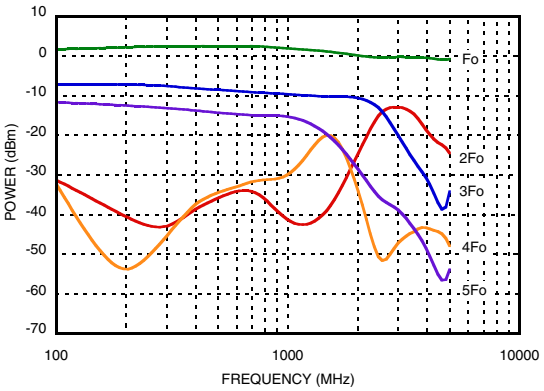


Figure 20. S-Parameters - S11 [11]

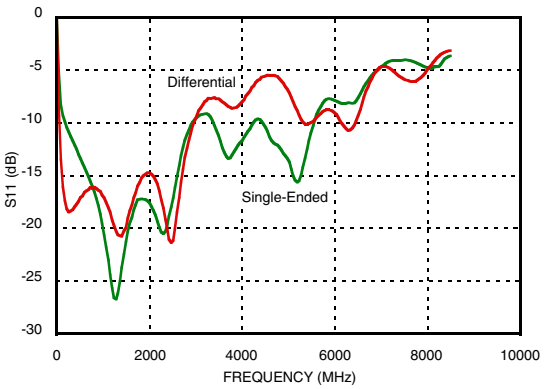


Figure 21. S-Parameters - S12 [11]

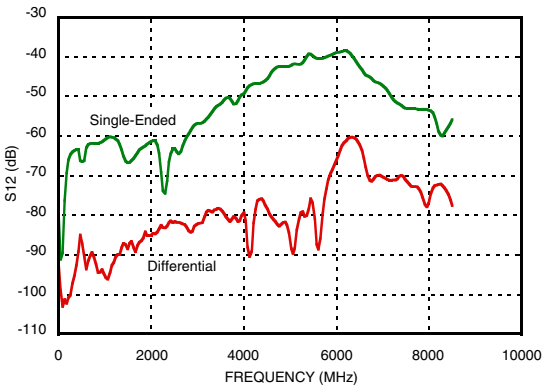
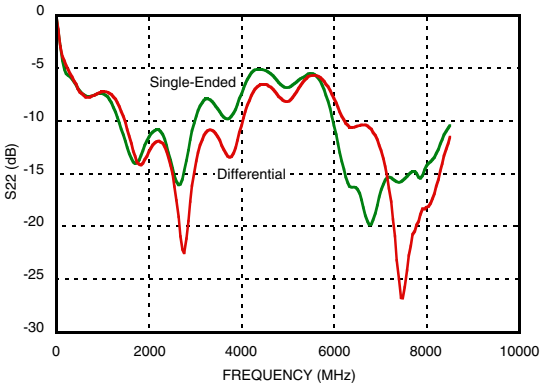


Figure 22. S-Parameters - S22 [11]



[10] Not corrected for board/cable loss.

[11] Effects of the customer evaluation board are not corrected. Improvements in S11 and S22 are possible under different evaluation board configurations

Table 2. Pin Descriptions

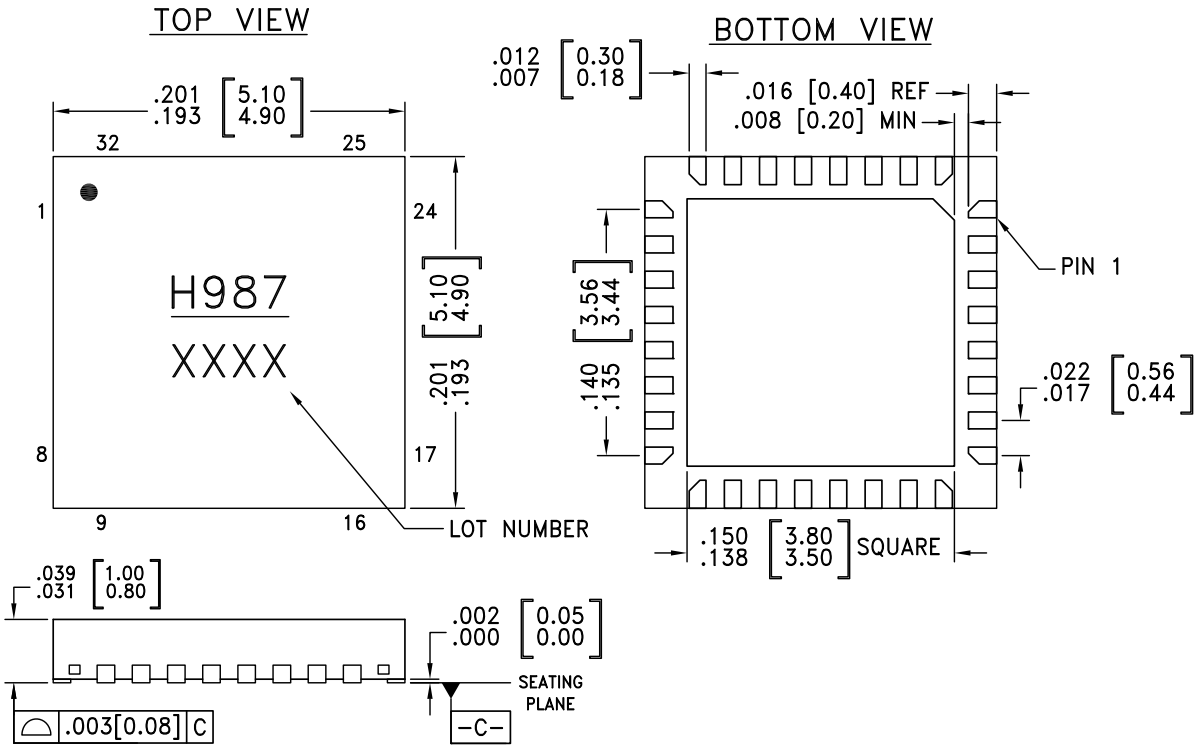
Pin Number	Function	Description
1	VCCHF	Power Supply
2	CLKP	Differential clock inputs
3	CLKN	
4	SDI	Serial port data input
5	SDO	Serial port data output
6	PMODE-SEL	Parallel mode select. If 1, pins (SCLK, SDI, SEN) are interpreted as a control-word which enables different buffers. See section "Parallel Port Control"
7	RFOUTP	Differential signal output
8	RFOUTN	
9	VCCRF	Power supply
10	SCLK	Serial port clock
11	SEN	Serial port latch enable
12	OUTP8	Differential signal output
13	OUTN8	
14	OUTP7	Differential signal output
15	OUTN7	
16	VCCB	Power supply
17	OUTN6	Differential signal output
18	OUTP6	
19	OUTN5	Differential signal output
20	OUTP5	
21	OUTP4	Differential signal output
22	OUTN4	
23	OUTP3	Differential signal output
24	OUTN3	
25	VCCA	Power supply
26	OUTN2	Differential signal output
27	OUTP2	
28	OUTN1	Differential signal output
29	OUTP1	
30	RFBUFEN	Active high RF buffer enable. The polarity of this control input can be swapped via SPI bit Reg03h[4].
31	CEN	Hardware chip enable
32	NC	No Connect

Table 3. Absolute Maximum Ratings

Parameter	Rating
Max Vdc to paddle on supply pins 1, 9, 16, 25	-0.3 V to +4 V
Max RF Power CLKP, CLKN	15 dBm single-ended
CLKP, CLKN	- 0.3 V to 3.6 V
LVPECL Min Output Load Resistor	100 Ohms to GND
LVPECL Output Load Current	40 mA/leg
Digital Load	1 kΩ min
Digital Input Voltage Range	-0.3 to 3.6 V
Thermal Resistance (junction to ground paddle)	25 °C/W
Operating Temperature Range	-40 °C to +85 °C
Storage Temperature Range	-65 °C to + 125 °C
Maximum Junction Temperature	+125 °C
Reflow Soldering	
Peak Temperature	260 °C
Time at Peak Temperature	40 sec
ESD Sensitivity HBM	Class 1B

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Outline Drawing



NOTES:

[1] PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.

[2] LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.

[3] LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.

[4] DIMENSIONS ARE IN INCHES [MILLIMETERS].

[5] LEAD SPACING TOLERANCE IS NON-CUMULATIVE.

[6] PAD BURR LENGTH SHALL BE 0.15 mm MAX. PAD BURR HEIGHT SHALL BE 0.05 mm MAX.

[7] PACKAGE WARP SHALL NOT EXCEED 0.05 mm

[8] ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.

[9] REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

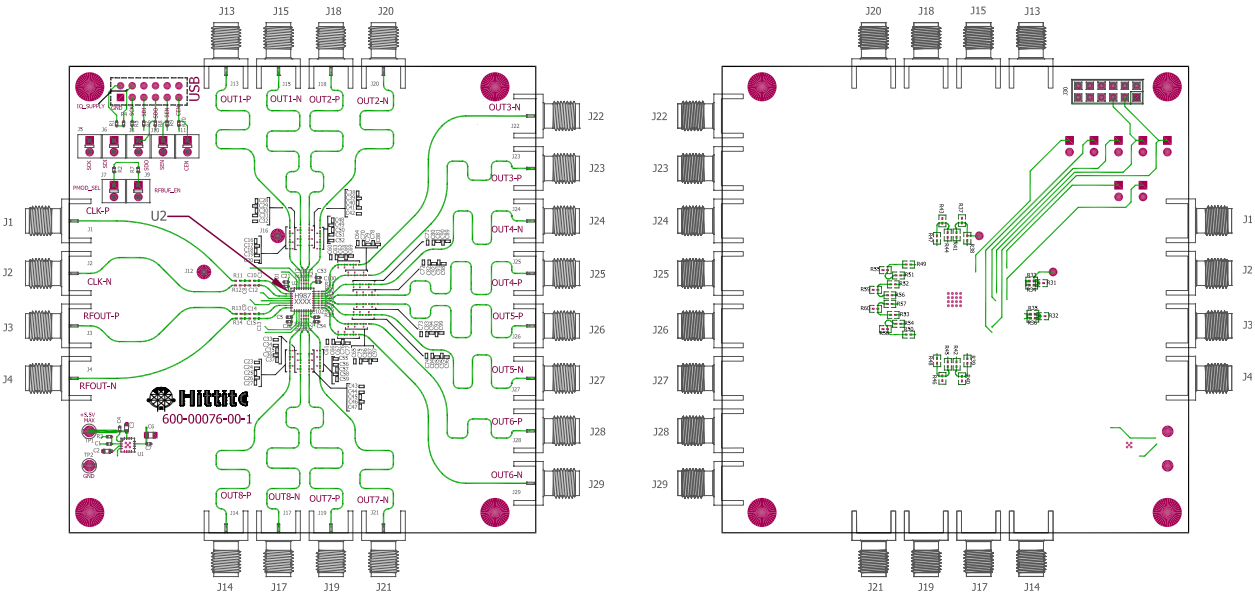
Table 4. Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1[2]	H987 XXXX

[1] 4-Digit lot number XXXX

[2] Max peak reflow temperature of 260°C

Evaluation PCB

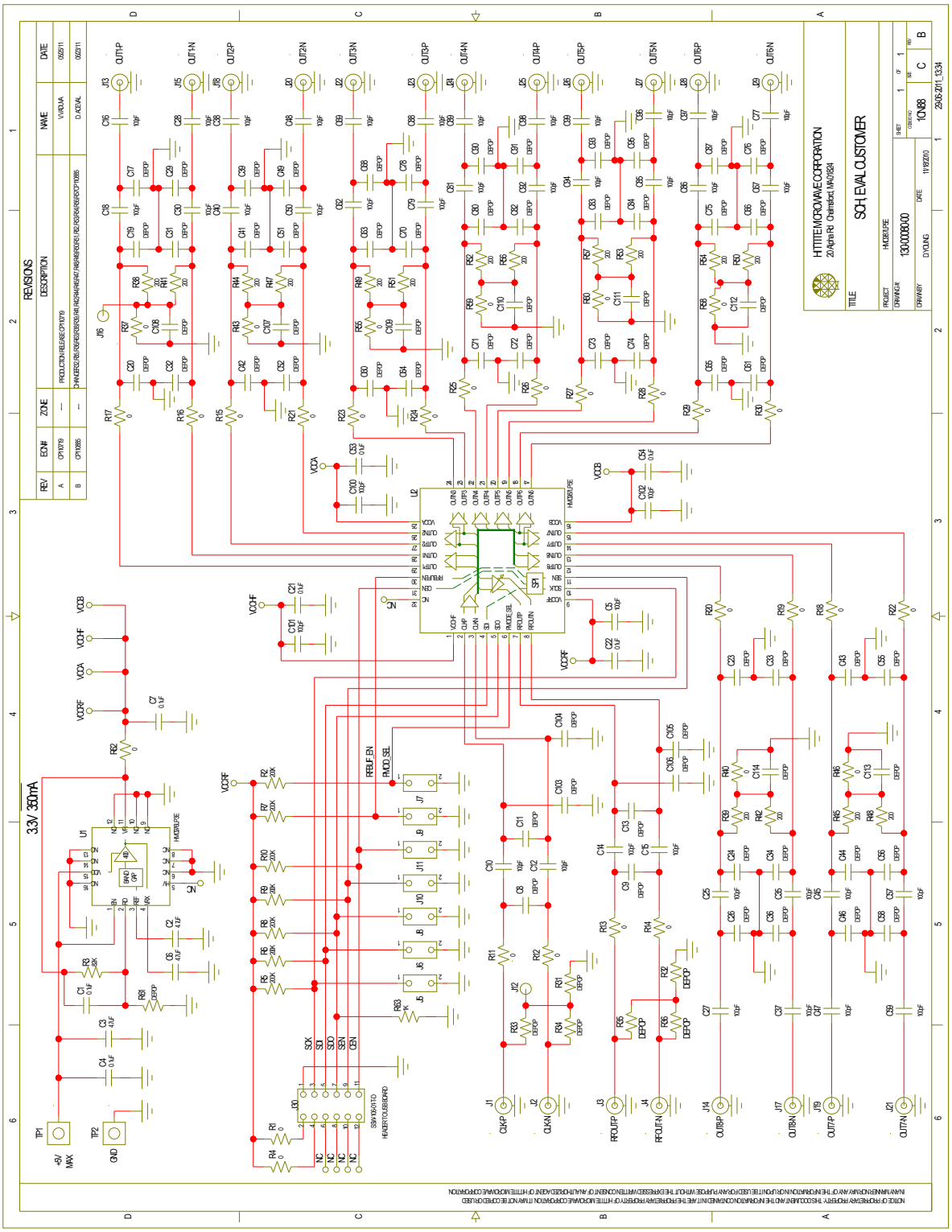


The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohms impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Table 5. Evaluation Order Information

Item	Contents	Part Number
Evaluation PCB	Evaluation PCB	EVAL01-
Evaluation Kit	Evaluation PCB USB Interface Board 6' USB A Male to USB B Female Cable CD ROM (Contains User Manual, Evaluation PCB Schematic, Evaluation Software,	EKIT01-

Evaluation PCB Schematic



Theory of Operation

Parallel Port Control

The various outputs of the can be enabled/disabled by using parallel pin control, or via the SPI. In parallel-mode (PMODE-SEL = 1), the SPI input pins (SCLK, SKI, SEN) are re-interpreted as a 3-bit control bus, and enable the LVPECL drivers according to the following truth table.

SCLK, SDI, SEN

000: OUT2

001: OUT2 + OUT7

010: OUT2 + OUT7 + OUT4

011: OUT2 + OUT7 + OUT4 + OUT6

100: OUT2 + OUT7 + OUT4 + OUT6 + OUT5

101: OUT2 + OUT7 + OUT4 + OUT6 + OUT5 + OUT3

110: OUT2 + OUT7 + OUT4 + OUT6 + OUT5 + OUT3 + OUT8

111: OUT2 + OUT7 + OUT4 + OUT6 + OUT5 + OUT3 + OUT8 + OUT1

Under SPI control (PMODE-SEL = 0, see section "Register Map" for the register map and SPI protocol details), there is slightly more flexibility in that any combination of buffers can be enabled or disabled via the individual buffer enable bits in Reg02h.

The part features switches on both the input and output signals, so that when the part is disabled (via either the CEN pin, or the SPI control bit [0]), the power-down current drops to < 2 µA, regardless of the IO termination scheme.

Input Stage

The input stage, Figure 38, is flexible. It can be driven single-ended or differential, with LVPECL, LVDS, or CML signals. If driven single-ended, a large AC coupling cap to ground should be used on the undriven input. The input impedance is selectable, via Parallel Port Control[3], between 50 Ω or 150 Ω (100 Ω or 300 Ω differential). The DC bias level of 2.0 V can be generated internally by programming Parallel Port Control[1] =1 (default configuration), supplied externally, or generated via an LVPECL termination network inside the part.

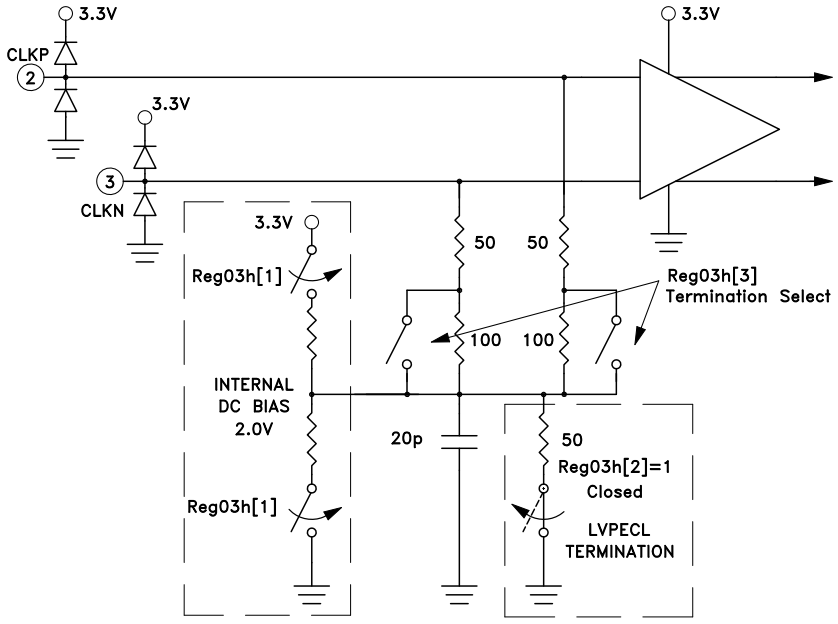


Figure 26. Input Stage

[4] to Figure 28 illustrate common input interface configurations.

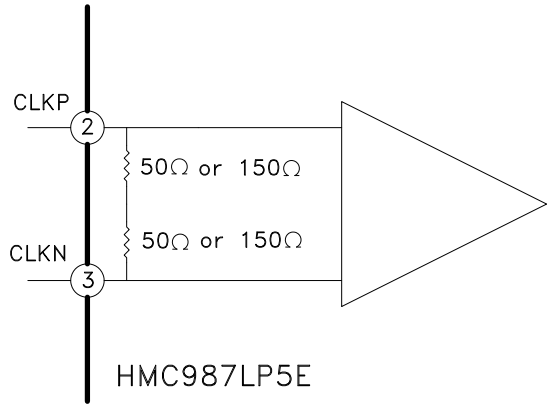


Figure 27. DC Coupled CML Interface

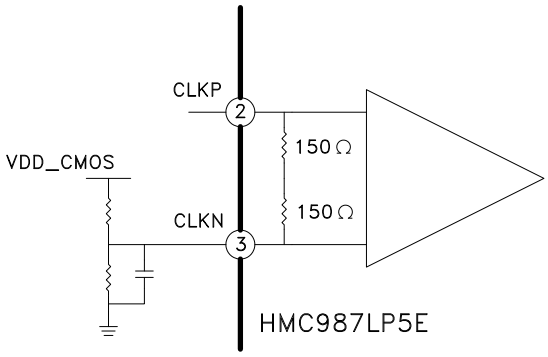


Figure 28. DC Coupled CMOS Interface

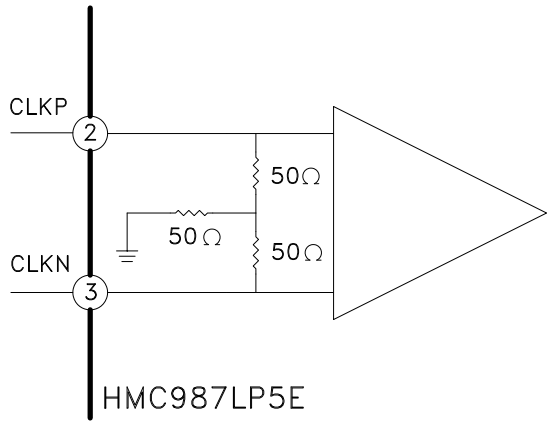


Figure 29. DC Coupled LVPECL Interface

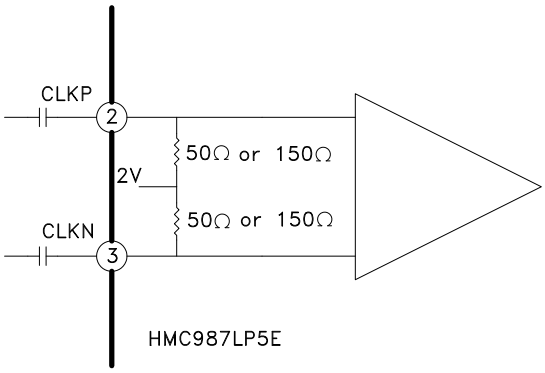


Figure 30. AC Coupled Differential CML / LVPECL / LVDS / CMOS Interface

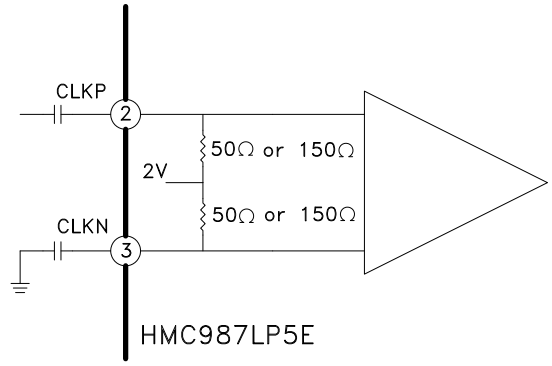


Figure 31. AC Coupled Single-Ended CML / LVPECL / LVDS / CMOS Interface

LVPECL Output Stage

The LVPECL output driver produces up to 1.6 Vppd swing into 50 Ω loads. LVPECL drivers are terminated with off-chip resistors that provide the DC current through the emitter-follower output stage. The output stage has a switch which disconnects the output driver from the load when not used. The switch series resistor significantly improves the output match when driving into 50 Ω transmission lines. The switch series resistor causes a small DC level shift and swing degradation, depending on the termination current.

If unused, disabled LVPECL outputs can be left floating, terminated, or grounded.

For price, delivery and to place orders: Hittite Microwave Corporation, 2 Elizabeth Drive, Chelmsford, MA 01824
Phone: 978-250-3343 Fax: 978-250-3373 Order On-line at www.hittite.com
Application Support: Phone: 978-250-3343 or apps@hittite.com

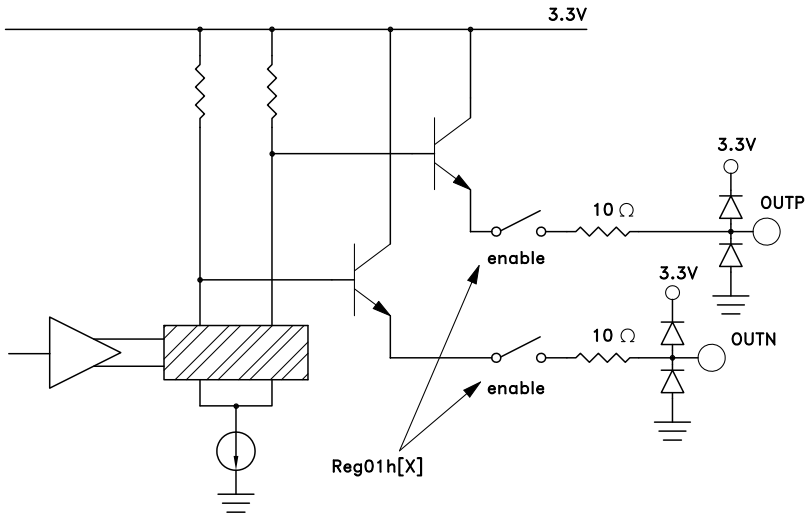


Figure 32. Output Stage

Figure 30 to [8] illustrate common output interface configurations.

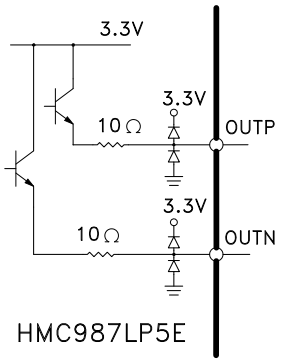


Figure 33. DC Coupled to LVPECL Interface

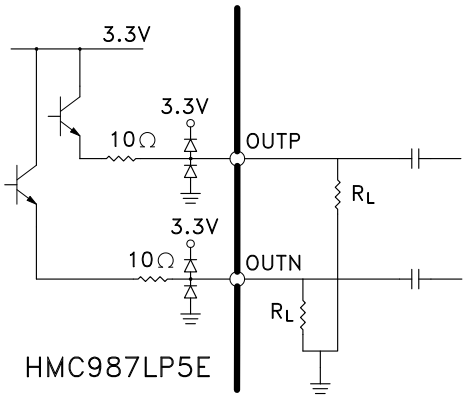


Figure 34. AC coupled to LVDS / CML / LVPECL / CMOS

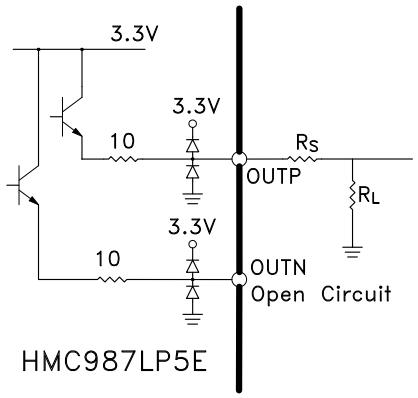


Figure 35. DC Coupled to CMOS Interface

The user has a number of choices in how they connect LVPECL drivers and receivers, and there are great number of resources that deal in detail with this issue. As a quick introduction, there are compromises between matching performance, common mode levels, and signal swing. For clocking applications, the user often has the luxury of using AC coupling, unlike in many data-path situations. Figure 36 shows a simplified interface schematic between an LVPECL output and input stage - where various options and trade-offs for the termination components are provided in Table 6. The Hittite evaluation board has a great deal of flexibility in how the I/Os are configured, and allows the configuration in Figure 33, among many others.

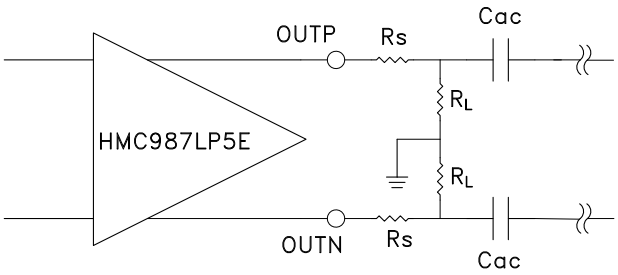


Figure 36. Recommended Interface Diagram

Table 6. Interface Values

Rs - Used to increase Ro to match to 50 Ω environment. already has ~ 10 Ω internally.	
0 Ω	Hittite EVB: Largest signal swing, lowest common mode shift
10 Ω	Better S22
R_L - DC current termination for LVPECL output stage	
120 Ω	Hittite EVB default: Standard LVPECL termination voltages
200 Ω	Reduced current, no performance degradation
300 Ω	Further reduced current, lower output power but flatter frequency response
OPEN	If using internal DC termination network at the Rx
Cac - AC coupling cap	
BIG CAP	Hittite EVB default: If using AC coupling
SHORT	If using internal DC termination network at the Rx

RF Output Stage

The RF output buffer is a CML output stage with 50 Ω impedance (single-ended) and adjustable power. In parallel mode (the PMODE_SEL pin = 1), it is at max gain (~ +3 dBm single-ended), whereas under SPI control, the gain can be lowered in ~3 dB steps down to -9 dBm single-ended. See Interface Values for more information.

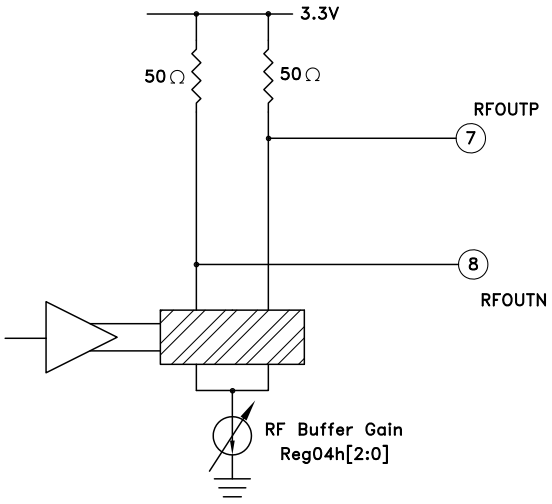


Figure 37. Output Stage

Serial Port Interface (SPI) Control

can be controlled via SPI or parallel port control (for more information on parallel control see "Parallel Port Control"). SPI control offers more flexibility. External pin PMODE-SEL = 1 configures the for parallel port operation, while PMODE-SEL = 0 will enable the SPI control of.

The SPI control is required in order to re-configure the input bias network from its' default state (Parallel Port Control), to adjust the output power control on the RF/CML buffer, and to individually enable arbitrary LVPECL outputs.

Operational Modes

Serial Port Interface features:

a. Compatibility with general serial port protocols that use a shift and strobe approach to communication.

b. Compatible with HMC multi-Chip solutions, useful to address multiple chips of various types from a single serial port bus.

Serial Port Write Operation

Table 7. SPI Open Mode - Write Timing Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
t_1	SDI setup time	3			ns
t2	SDI hold time	3			ns
t3	SEN low duration	10			ns
t4	SEN high duration	10			ns
t5	SCLK 9 Rising Edge to SEN Rising Edge	10			ns
	Serial port Clock Speed	DC	50		MHz
t_6	SEN to SCLK Recovery Time	10			ns

A typical WRITE cycle is shown in Figure 38.

a. The Master (host) places 9 bit data, d8:d0, MSB first, on SDI on the first 9 falling edges of SCLK.
b. The slave () shifts in data on SDI on the first 9 rising edges of SCLK
c. Master places 4 bit register address to be written to, r3:r0, MSB first, on the next 4 falling edges of SCLK (10-13)
d. Slave shifts the register address bits on the next 4 rising edges of SCLK (10-13).
e. Master places 3 bit chip address, a2:a0, MSB first, on the next 3 falling edges of SCLK (14-16).
f. Slave shifts the chip address bits on the 3 rising edges of SCLK (14-16).
g. Master asserts SEN after the 16th rising edge of SCLK.
h. Slave registers the SDI data on the rising edge of SEN.

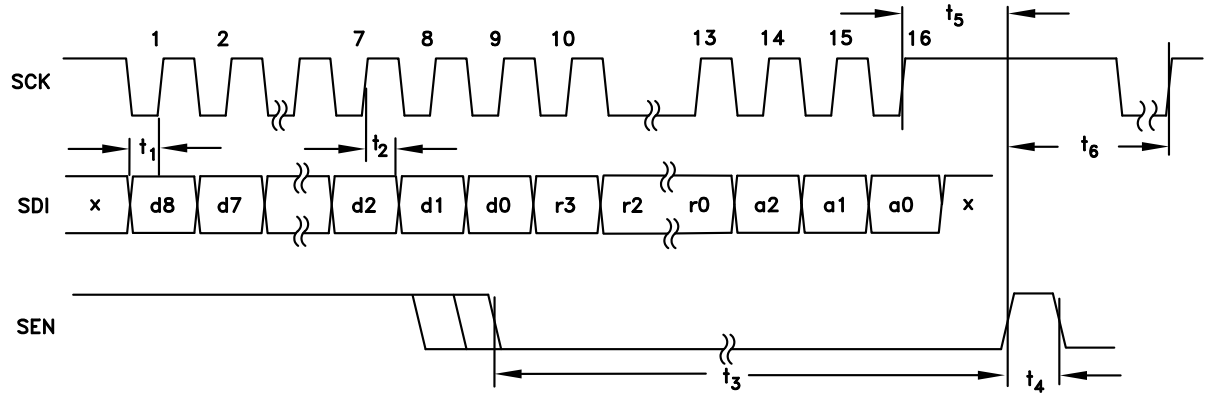


Figure 38. SPI Timing Diagram, Write Operation

Serial Port Read Operation

In order ensure correct read operation a pull-down resistor to ground (~1-2kOhm) is recommended on the Serial Data Out line from the part. A typical READ cycle is shown in Figure 39.

In general, SDO line is always active during the WRITE cycle. SDO will contain the data from the addresses pointed to by Reg00h. If Reg00h is not changed, the same data will always be present on the SDO. If it is desired to READ from a specific address, it is necessary in the first SPI cycle to write the desired address to Reg00h, then in the next SPI cycle the desired data will be available on the SDO.

An example of the two cycle procedure to read from any random address is as follows:

The Master (host), on the first 9 falling edges of SCLK places 9 bit data, d8:d0, MSB first, on SDI as shown in Figure 39. d8:d0 should be set to zero. d3:d0 = address of the register to be READ on the next cycle.

- **a.** The slave () shifts in data on SDI on the first 9 rising edges of SCLK
- **b.** Master places 4 bit register address , r3:r0, (the address the WRITE ADDRESS register), MSB first, on the next 4 falling edges of SCLK (10-13). r3:r0=0000.
- **c.** Slave shifts the register bits on the next 4 rising edges of SCLK (10-13).
- **d.** Master places 3 bit chip address, a2:a0, MSB first, on the next 3 falling edges of SCLK (14-16).
- **e.** Slave shifts the chip address bits on the next 3 rising edges of SCLK (14-16).
- **f.** Master asserts SEN after the 16th rising edge of SCLK.
- **g.** Slave registers the SDI data on the rising edge of SEN.
- **h.** Master clears SEN to complete the address transfer of the two part READ cycle.
- **i.** If we do not wish to write data to the chip at the same time as we do the second cycle , then it is recommended to simply rewrite the same contents on SDI to Register zero on the READ back part of the cycle.
- **j.** Master places the same SDI data as the previous cycle on the next 16 falling edges of SCLK.
- **k.** Slave () shifts the SDI data on the next 16 rising edges of SCLK.
- **l.** Slave places the desired data (i.e. data from address in Reg00h[3:0]) on SDO on the next 16 rising edges of SCLK.
- **m.** Master asserts SEN after the 16th rising edge of SCLK to complete the cycle.

Note that if the chip address bits are unrecognized (a2:a0), the slave will tri-state the SDO output to prevent a possible bus contention issue.

Table 8. SPI Open Mode - Read Timing Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
t_1	SDI setup time	3			ns
t2	SDI hold time	3			ns
t3	SEN low duration	10			ns
t4	SEN high duration	10			ns
t5	SCLK Rising Edge to SDO time		8.2+0.2ns/pF		ns
t6	SEN to SCLK Recovery Time	10			ns
t7	SCLK 16 Rising Edge to SEN Rising Edge	10			ns

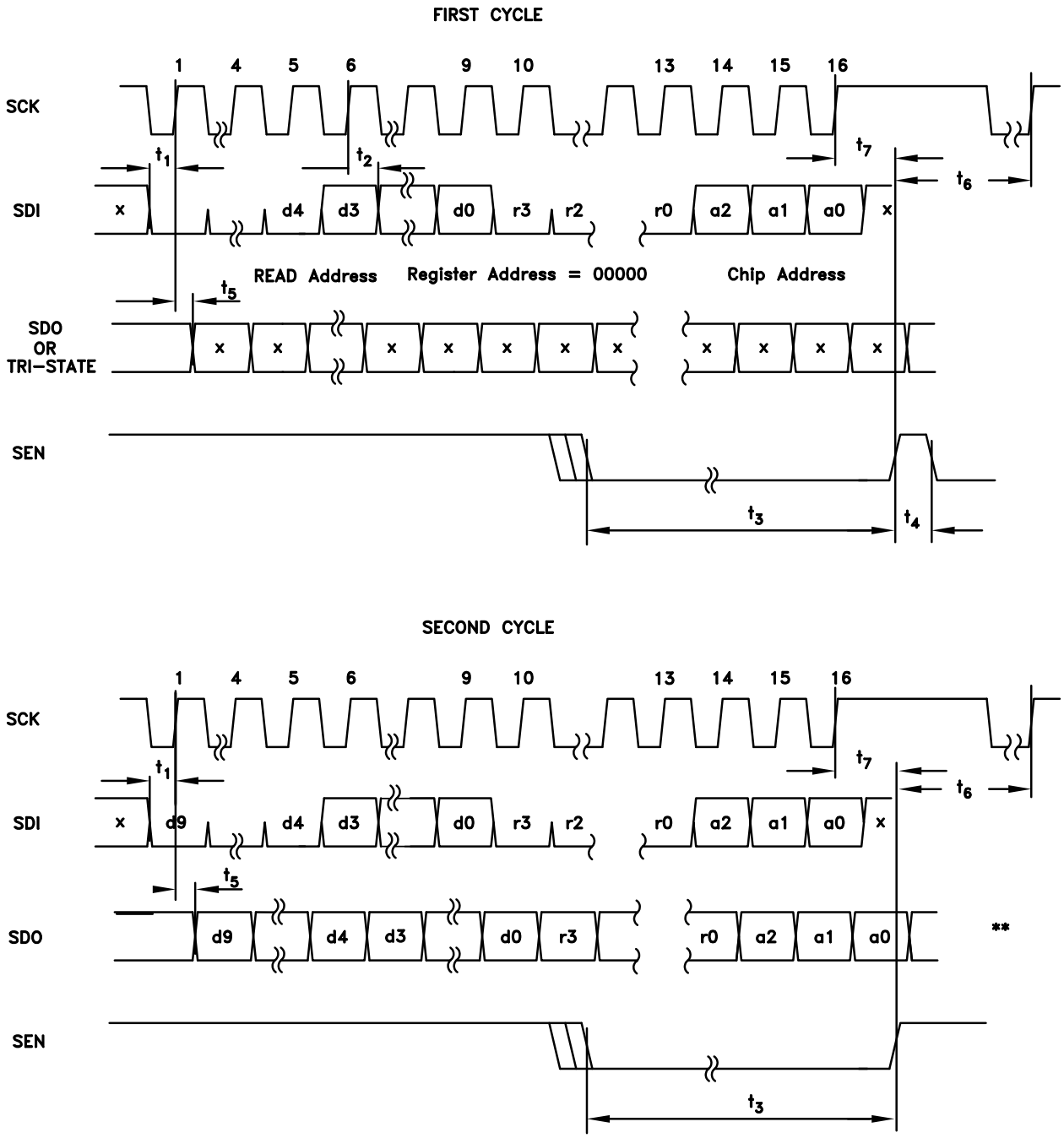


Figure 39. SPI Diagram, Read Operation 2- Cycles

Register Map

Table 9. Reg00h ID Register (Read Only)

Bit	Name	Width	Default	Description
[3:0]	Read Control	4		(Write Only)
[4]	Soft Reset			
[4:0]	Chip ID			(Read Only)

Table 10. Reg01h Master Enable

Bit	Name	Width	Default	Description
[0]	Master Chip Enable	1	1	

Table 11. Reg02h Individual Enables

Bit	Name	Width	Default	Description
[0]	en1	1	1	Enable Buffer 1
[1]	en2	1	1	Enable Buffer 2
[2]	en3	1	1	Enable Buffer 3
[3]	en4	1	1	Enable Buffer 4
[4]	en5	1	1	Enable Buffer 5
[5]	en6	1	1	Enable Buffer 6
[6]	en7	1	1	Enable Buffer 7
[7]	en8	1	1	Enable Buffer 8

Table 12. Reg03h Rx Buffer Configuration

Bit	Name	Width	Default	Description
[0]		1	0	Reserved 0
[1]	DC Internal	1	1	Use internal DC bias string
[2]	DC LVPECL	1	0	Use internal LVPECL Rx termination
[3]	Zin 50	1	1	Input termination select 1 - 50 Ω single-ended, 100 Ω differential 0- 150 Ω single-ended, 300 Ω differential
[4]	RFBUF XOR	1	0	Toggle (XOR with RFBUFEN pin) the internal RF Buffer on/off
[8:5]		4	0	Reserved 0

Table 13. Reg04h Gain Select

Bit	Name	Width	Default	Description
[2:0]	RF Buffer Gain	3	7	0: Disabled 1: -9 dBm single-ended 2: -6 dBm single-ended 3: -3 dBm single-ended 4: 0 dBm single-ended >4: 3 dBm single-ended

Table 14. Reg05h Biases

Bit	Name	Width	Default	Description
[1:0]	Reserved	2	2	Reserved - 2
[3:2]	Reserved	2	2	Reserved - 2
[5:4]	Reserved	2	3	Reserved - 3
[8:6]	Reserved	3	0	Reserved - 0