M5M5408AFP,TP,RT-55L, -70L,-10L -55LL,-70LL,-10LL

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5408A is a 4,194,304-bit CMOS Static RAM organizedas 524,288-word by 8-bit. This device is fabricated usingMitsubishi's high-performance silicon-gate CMOS technology.This state-of-the-art process technology, combined withinnovative circuit design techniques, yields high-density and low-power devices. The M5M5408A is suitable for memoryapplications where high reliability, large storage, simpleinterfacing and battery back-up are important design objectives.

The M5M5408A is available in 32-pin plastic SOP(M5M5408AFP) , 32-pin plastic normal-lead-bend TSOP(M5M5408ATP) and 32-pin plastic reverse-lead-bend TSOP(M5M5408ART) packages. Two types of TSOP's are suitable forSurface Mounting on double-sided printed circuit boards.

FEATURES

Type name	Access time (max.)	Power supply current	
		Active (max.)	Stand-by (max.)
M5M5408AFP, TP, RT -55L	55ns	30mA (1MHz)	100µA (Vcc=5.5V*)
M5M5408AFP, TP, RT -70L	70ns		
M5M5408AFP, TP, RT -10L	100ns		
M5M5408AFP, TP, RT -55LL	55ns	30mA (1MHz)	20µA (Vcc=5.5V*) 0.4µA (Vcc=3V**)
M5M5408AFP, TP, RT -70LL	70ns		
M5M5408AFP, TP, RT -10LL	100ns		

* at 70°C / **at 25°C

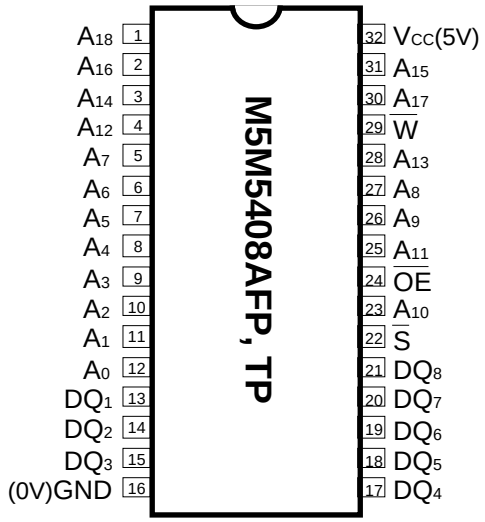
- Single +5V power supply
- No clocks, No refresh
- All inputs and outputs are TTL compatible.
- Easy memory expansion and power down by S
- Data retention supply voltage=2.0V to 5.5V
- Three-state outputs: OR-tie capability
- OE prevents data contention in the I/O bus
- Common Data I/O
- Battery backup capability
- Small stand-by current……0.4µA (typical)
- Package

M5M5408AFP : 32 pin 525 mil SOP
M5M5408ATP : 32 pin 400 mil TSOP(II)
M5M5408ART : 32 pin 400 mil TSOP(II)

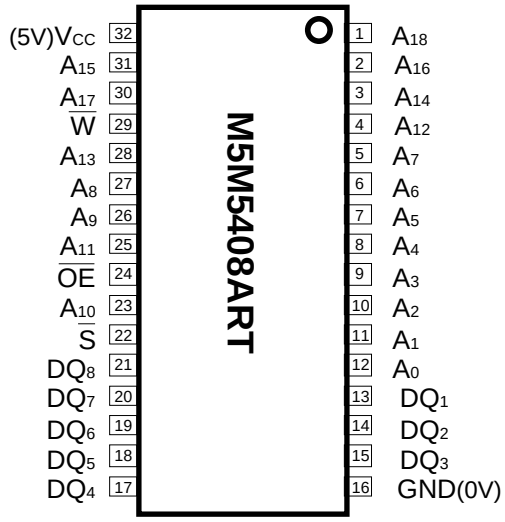
APPLICATION

Small capacity memory units
IC card
Battery operating system

PIN CONFIGURATION (TOP VIEW)



Outline32P2M-A (AFP)
32P3Y-H (ATP)



Outline32P3Y-J (ART)

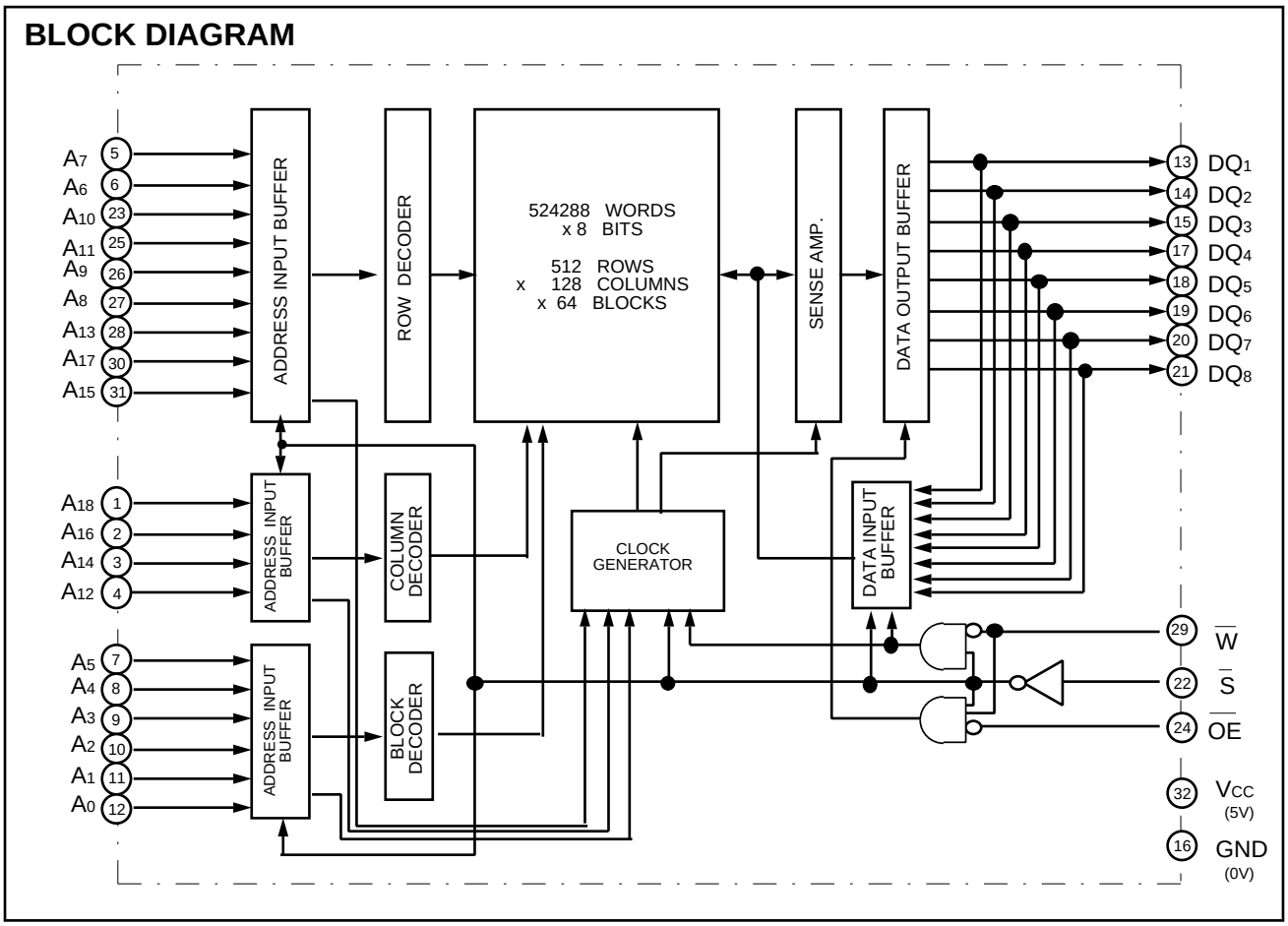
PIN DISCRIPTION

A0 ..... A18: ADDRESS INPUTS
DQ1..... DQ8: DATA INPUTS & OUTPUTS
$\overline{S}$: CHIP SELECT INPUT
$\overline{W}$: WRITE ENABLE INPUT
$\overline{OE}$: OUTPUT ENABLE INPUT
Vcc: Power supply
GND: Ground

M5M5408AFP,TP,RT-55L, -70L,-10L -55LL,-70LL,-10LL

4194304-BIT (524288-WORD BY 8-BIT) CMOS STATIC RAM

BLOCK DIAGRAM



FUNCTION

The operation mode of the M5M5408A is determined by acombination of the device control inputs S, Wand OE.Each mode is summarized in the truth table.

A write cycle is executed whenever the low level Woverlaps with the low level S. The address must be set upbefore the write cycle and must be stable during the entirecycle. The data is latched into a cell on the trailing edge of Wor S, whichever occurs first, requiring the set-up and holdtime relative to these edge to be maintained. The outputenable OE directly controls the output stage. Setting theOE at a high level, the output stage is in a high-impedancestate, and the data bus contention problem in the write cycleis eliminated.

A read cycle is executed by setting W at a high level andOEat a low level while S are in an active state(S=L).

When setting S at a high level, the chips are in a non-selectable mode in which both reading and writing are disabled.In this mode, the output stage is in a high-impedance state,allowing OR-tie with other chips and memory expansion by S.The power supply current is reduced as low as the stand-bycurrent which is specified as Icc3 or Icc4, and the memorydata can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation inthe non-selected mode.

TRUTH TABLE

S	W	OE	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	Data input	Active
L	H	L	Read	Data output	Active
L	H	H	Read	High-impedance	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to GND	- 0.3 ~ 7	V
Vi	Input voltage		- 0.3* ~ Vcc + 0.3	V
Vo	Output voltage		0 ~ Vcc	V
Pd	Power dissipation	Ta=25°C	700	mW
Topr	Operating temperature		0 ~ 70	°C
Tstg	Storage temperature		-65 ~ 150	°C

* -3.0V in case of AC (Pulse width ≤ 50ns)

DC ELECTRICAL CHARACTERISTICS (Ta=0 - 70°C, Vcc=5V±10%, unless otherwise noted)

Symbol	Parameter	Test Conditions		Limits			Unit
				Min.	Typ.	Max.	
VIH	High-level input voltage			2.2		Vcc+0.3	V
VIL	Low-level input voltage			-0.3*		0.8	V
VOH	High-level output voltage	IOH= - 1mA		2.4			V
		IOH= - 0.1mA		Vcc-0.5			V
VOL	Low-level output voltage	IOL = 2 mA				0.4	V
Ii	Input leakage current	Inputs = 0 ~ Vcc				±1	µA
Io	Output leakage current	$\overline{S}$ = VIH $\overline{OE}$= VIH, DQ=0 ~ Vcc				±1	µA
Icc1	Active supply current (AC, MOS-lvel)	$\overline{S}$ ≤ 0.2 Other inputs ≤ 0.2V or ≥Vcc-0.2V DQ = open (duty 100%)	minimum cycle		50	80	mA
			1MHz		25	30	mA
Icc2	Active supply current (AC, TTL-level)	$\overline{S}$ = VIL Other inputs = VIH or VIL DQ = open (duty 100%)	minimum cycle		60	90	mA
			1MHz		30	40	mA
Icc3	Stand-by current	$\overline{S}$ Vcc - 0.2V, Other inputs = 0 ~ Vcc	-L version			100	µA
			-LL version		1	20	µA
Icc4	Stand-by current	$\overline{S}$ = VIH, other inputs=0 ~ Vcc				3	mA

* -3.0V in case of AC (Pulse width ≤ 50ns)

CAPACITANCE (Ta=0 - 70°C, Vcc=5V±10%, unless otherwise noted)

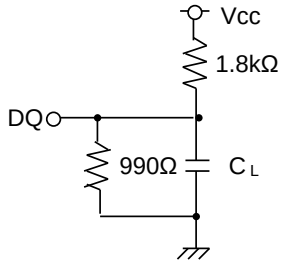
Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Ci	Input capacitance	Vi = GND, Vi = 25mV rms, f = 1MHz			6	pF
Co	Output capacitance	Vo = GND, Vo = 25mV rms, f = 1MHz			8	pF

Note1. Direction for current flowing into IC is indicated as positive value.
2. Typical value is for Ta=25°C and Vcc=5.0V
3. Ci and Co are random samples ,not production tested.

AC ELECTRICAL CHARACTERISTICS (Ta=0 - 70°C, Vcc=5V±10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse ……V_{IH}=2.4V, V_{IL}=0.6V(AFP,TP,RT-70L,-10L,-70LL,-10LL)
V_{IH}=3.0V, V_{IL}=0V(AFP,TP,RT-55L,-55LL)
Input rise and fall time ……5ns
Output reference level ……V_{OH}=V_{OL}=1.5V
For t_{en} and t_{dis}, transition is measured ±500mV from steady state voltage
Output loads Show in Fig. 1;
C_L=100pF(AFP,TP,RT-70L,-10L,-70LL,-10LL)
C_L=30pF(AFP,TP,RT-55L,-55LL)
C_L=5pF (for ten,tdis)



CL Includes jig and scope capacitance

Fig.1 Output load

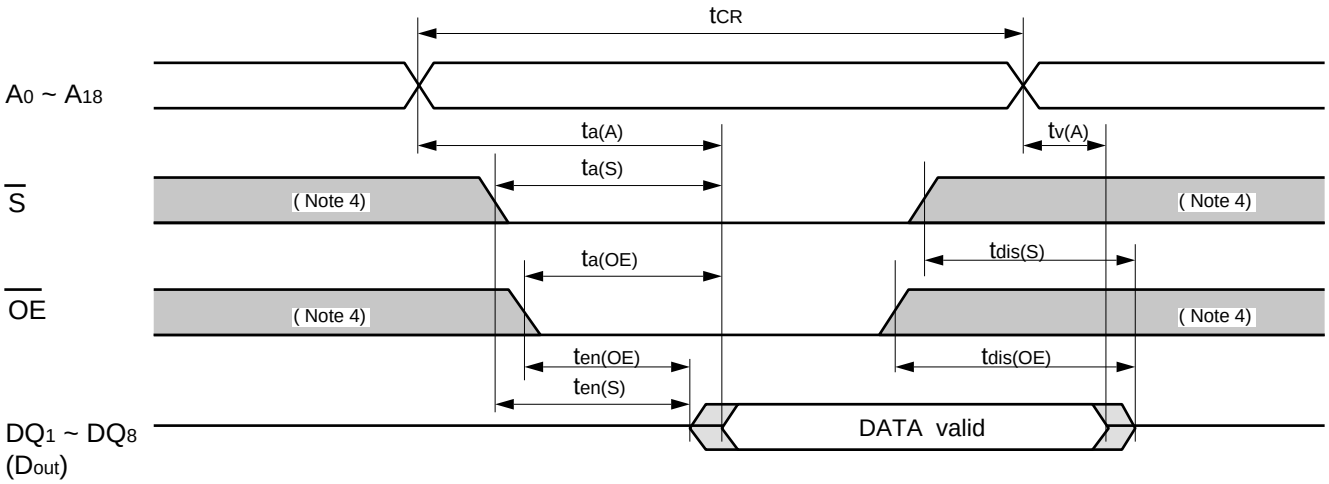
(2) READ CYCLE

Symbol	Parameter	Limits						Unit
		M5M5408AFP,TP,RT -55L, -55LL		M5M5408AFP,TP,RT -70L, -70LL		M5M5408AFP,TP,RT -10L, -10LL		
		Min.	Max.	Min.	Max.	Min.	Max.	
tCR	Read cycle time	55		70		100		ns
ta(A)	Address access time		55		70		100	ns
ta(S)	Chip select access time		55		70		100	ns
ta(OE)	Output enable access time		25		35		50	ns
tdis(S)	Output disable time after S high		20		25		35	ns
tdis(OE)	Output disable time after OE high		20		25		35	ns
ten(S)	Output enable time after S low	10		10		10		ns
ten(OE)	Output enable time after OE low	5		5		5		ns
tv(A)	Data valid time after address change	10		10		10		ns

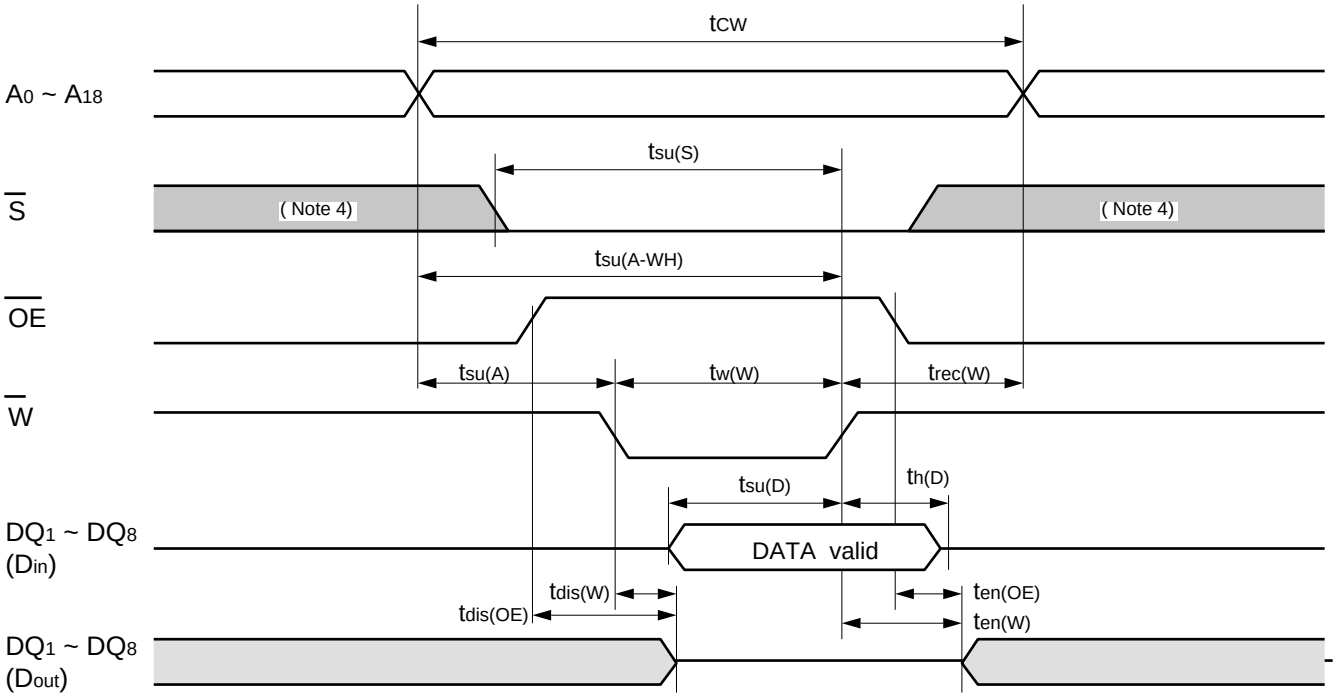
Symbol	Parameter	Limits						Unit
		M5M5408AFP,TP,RT -55L, -55LL		M5M5408AFP,TP,RT -70L, -70LL		M5M5408AFP,TP,RT -10L, -10LL		
		Min.	Max.	Min.	Max.	Min.	Max.	
tCW	Write cycle time	55		70		100		ns
tw(W)	Write pulse width	40		50		60		ns
tsu(A)	Address set up time	0		0		0		ns
tsu(A-WH)	Address set up time with respect to W high	50		60		80		ns
tsu(S)	Chip select set up time	50		60		80		ns
tsu(D)	Data set up time	25		30		35		ns
th(D)	Data hold time	0		0		0		ns
trec(W)	Write recovery time	0		0		0		ns
tdis(W)	Output disable time after W low		20		25		35	ns
tdis(OE)	Output disable time after OE high		20		25		35	ns
ten(W)	Output enable time after W high	5		5		5		ns
ten(OE)	Output enable time after OE low	5		5		5		ns

(4) TIMING DIAGRAMS

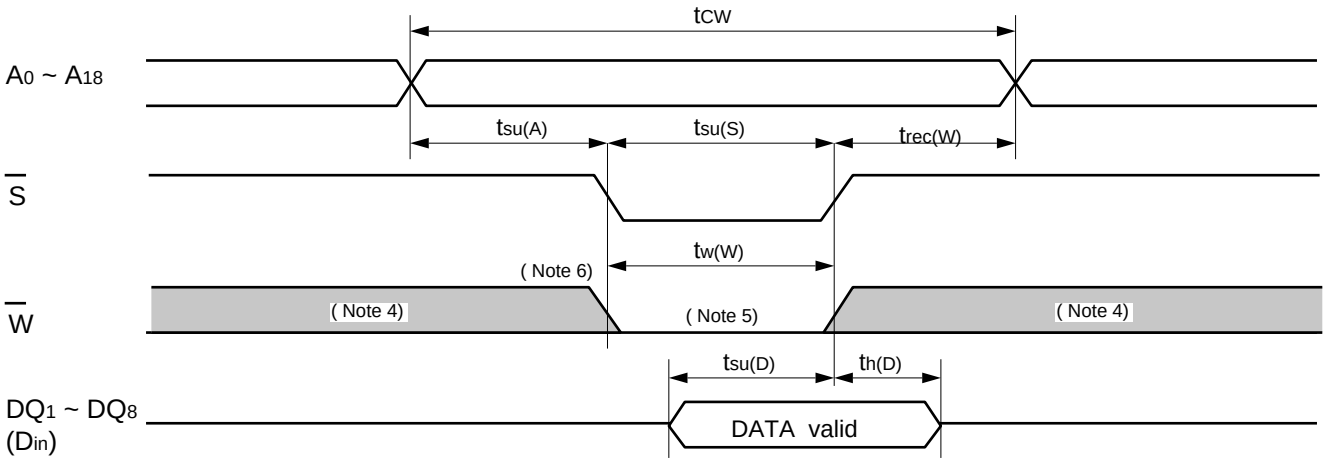
Read cycle



Write cycle ($\overline{WE}$ control mode)



Write cycle ($\overline{S}$ control mode)



Note 4: Hatching indicates the state is "don't care".
5: A Write occurs during the overlap of a low $\overline{S}$ and a low $\overline{W}$.
6: If $\overline{W}$ goes low simultaneously with or prior to $\overline{S}$, the output remains in the high-impedance state.
7: Don't apply inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions		Limits			Unit
				Min.	Typ.	Max.	
Vcc(PD)	Power down supply voltage			2			V
Vi(S)	Chip select input S	Vcc(PD) ≥ 2.2V		2.2			V
		2.2V ≥ Vcc(PD) ≥ 2.0V			Vcc(PD)		V
Icc(PD)	Power down supply current	Vcc=3V, S ≥ Vcc-0.2V, other inputs = 0 ~ 3V	-L version			50	µA
			-LL version		0.4	10*	µA

* Icc (PD) = 1µA at Ta=25°C

(2) TIMING REQUIREMENTS (Ta=0 - 70°C, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
tsu(PD)	Power down set up time		0			ms
trec(PD)	Power down recovery time		5			ms

(3) TIMING DIAGRAM

$\overline{S}$ control mode