TOSHIBA

TOSHIBA Original CMOS 16-Bit Microcontroller

TLCS-900/L1 Series

TMP91C630

TOSHIBA CORPORATION

Semiconductor Company

Preface

Thank you very much for making use of Toshiba microcomputer LSIs.
Before use this LSI, refer the section, “Points of Note and Restrictions”.

Especially, take care below cautions.

CMOS 16-Bit Microcontrollers

TMP91C630F

1. Outline and Features

TMP91C630 is a high-speed 16-bit microcontroller designed for the control of various mid- to large-scale equipment. With 2 Kbytes of boot ROM included, it allows your programs to be erased and rewritten on board.

TMP91C630 comes in a 100-pin flat package. Listed below are the features.

(1) High-speed 16-bit CPU (900/L1 CPU)
- Instruction mnemonics are upward-compatible with TLCS-90/900
- 16 Mbytes of linear address space
- General-purpose registers and register banks
- 16-bit multiplication and division instructions; bit transfer and arithmetic instructions
- Micro DMA: Four-channels (444 ns/2 bytes at 36 MHz)

(2) Minimum instruction execution time: 111 ns (at 36 MHz)

(3) Built-in RAM: 6 Kbytes
Built-in ROM: None
Built-in Boot ROM: 2 Kbytes

(4) External memory expansion

- Expandable up to 16 Mbytes (shared program/data area)
- Can simultaneously support 8-/16-bit width external data bus
  ··· Dynamic data bus sizing

(5) 8-bit timers: 6 channels

- Event counter :2 channels

(6) 16-bit timer/event counter: 1 channel

(7) Serial bus interface: 2 channels

(8) 10-bit AD converter: 8 channels

(9) Watchdog timer

(10) Chip Select/Wait controller: 4 blocks

(11) Interrupts: 35 interrupts

- 9 CPU interrupts: Software interrupt instruction and illegal instruction
- 19 internal interrupts: 7 priority levels are selectable.
- 7 external interrupts: 7 priority levels are selectable.
  (Level mode, rising edge mode and falling edge mode are selectable.)

(12) Input/output ports: 53 pins

(13) Standby function
Three halt modes: Idle2 (programmable), Idle1, Stop

(14) Operating voltage

- VCC = 2.7 V to 3.6 V (fc max = 36 MHz)

(15) Package

- 100-pin QFP: P-LQFP100-1414-0.50F

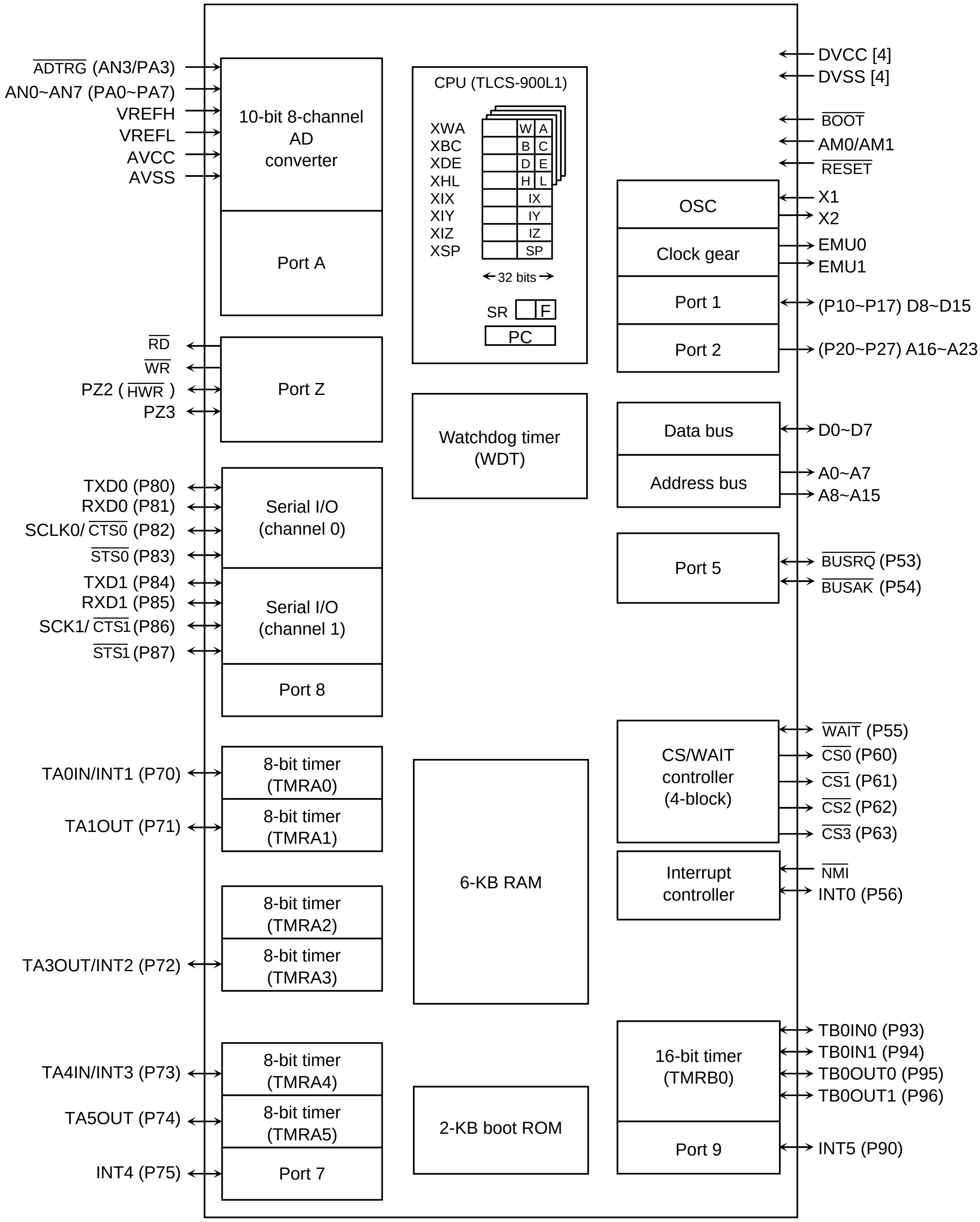


Figure 1.1 TMP91C630 Block Diagram

2. Pin Assignment and Pin Functions

The Pin Assignment and Pin Functions of the TMP91C630F are showed in Figure 2.1.1.

2.1 Pin Assignment Diagram

Figure 2.1.1 shows the pin assignment of the TMP91C630F.

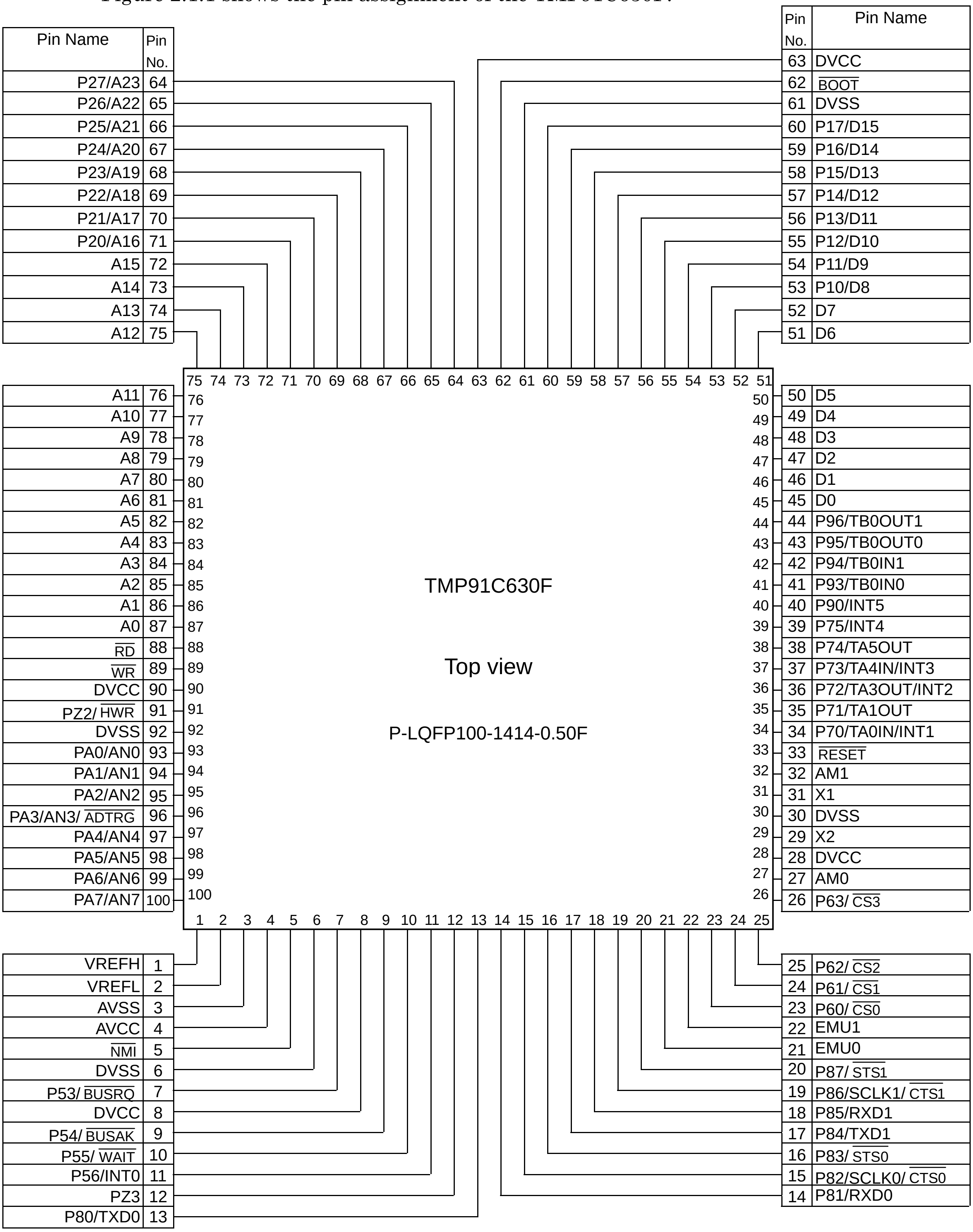


Figure 2.1.1 Pin Assignment Diagram (100-Pin LQFP)

2.2 Pin Names and Functions

The names of the Input/Output pins and their functions are described below.
Table 2.2.1 to Table 2.2.3 show Pin name and functions.

Table 2.2.1 Pin Names and Functions (1/3)

Pin Names	Number of Pins	I/O	Functions
D0 to D7	8	I/O	Data (lower): Bits 0 to 7 of data bus
P10 to P17 D8 to D15	8	I/O I/O	Port 1: I/O port that allows I/O to be selected at the bit level (When used to the external 8-bit bus) Data (upper): Bits 8 to15 of data bus
P20 to P27 A16 to A23	8	Output Output	Port 2: Output port Address: Bits 16 to 23 of address bus
A8 to A15	8	Output	Address: Bits 8 to 15 of address bus
A0 to A7	8	Output	Address: Bits 0 to 7 of address bus
$\overline{RD}$	1	Output	Read: Strobe signal for reading external memory
$\overline{WR}$	1	Output	Write: Strobe signal for writing data to pins D0 to D7
P53 $\overline{BUSRQ}$	1	I/O Input	Port 53: I/O port (with pull-up resistor) Bus request: Signal used to request bus release (high-impedance).
P54 $\overline{BUSAK}$	1	I/O Output	Port 54: I/O port (with pull-up resistor) Bus acknowledge: Signal used to acknowledge bus release (high-impedance).
P55 $\overline{WAIT}$	1	I/O Input	Port 55: I/O port (with pull-up resistor) Wait: Pin used to request CPU bus wait. ((1 + N) waits mode)
P56 INT0	1	I/O Input	Port 56: I/O port (with pull-up resistor) Interrupt request pin0: Interrupt request pin with programmable level/rising edge/falling edge
P60 $\overline{CS0}$	1	Output Output	Port 60: Output port Chip select 0: Outputs 0 when address is within specified address area.
P61 $\overline{CS1}$	1	Output Output	Port 61: Output port Chip select 1: Outputs 0 when address is within specified address area.
P62 $\overline{CS2}$	1	Output Output	Port 62: Output port Chip select 2: Outputs 0 when address is within specified address area.
P63 $\overline{CS3}$	1	Output Output	Port 63: Output port Chip select 3: Outputs 0 when address is within specified address area.
P70 TA0IN INT1	1	I/O Input Input	Port 70: I/O port 8-bit TMRA0 input Interrupt request pin 2: Interrupt request pin with programmable level/rising edge/falling edge
P71 TA1OUT	1	I/O Output	Port 71: I/O port 8-bit TMRA0 or 8-bit TMRA1 output
P72 TA3OUT INT2	1	I/O Output Input	Port 72: I/O port 8-bit TMRA2 or 8-bit TMRA3 output Interrupt request pin 2: Interrupt request pin with programmable level/rising edge/falling edge

Table 2.2.2 Pin Names and Functions (2/3)

Pin Names	Number of Pins	I/O	Functions
P73 TA4IN INT3	1	I/O Input Input	Port 73: I/O port 8-bit TMRA4 input Interrupt request pin 3: Interrupt request pin with programmable level/rising edge/falling edge.
P74 TA5OUT	1	I/O Output	Port 74: I/O port 8-bit TMRA4 or 8-bit TMRA5 output
P75 INT4	1	I/O Input	Port 75: I/O port Interrupt request pin 4: Interrupt request pin with programmable
P80 TXD0	1	I/O Output	Port 80: I/O port (with pull-up resistor) Serial send data 0: Programmable open-drain output pin
P81 RXD0	1	I/O Input	Port 81: I/O port (with pull-up resistor) Serial receive data 0
P82 SCLK0 $\overline{\text{CTS0}}$	1	I/O Input I/O	Port 82: I/O port (with pull-up resistor) Serial clock I/O 0 Serial data send enable 0 (Clear to send)
P83 $\overline{\text{STS0}}$	1	I/O	Port 83: I/O port (with pull-up resistor) Serial data request signal 0
P84 TXD1	1	I/O Output	Port 84: I/O port (with pull-up resistor) Serial send data 0: Programmable open-drain output pin
P85 RXD1	1	I/O Input	Port 85: I/O port (with pull-up resistor) Serial receive data 1
P86 SCLK1 $\overline{\text{CTS1}}$	1	I/O Input I/O	Port 86: I/O port (with pull-up resistor) Serial clock I/O 1 Serial data send enable 1 (Clear to send)
P87 $\overline{\text{STS1}}$	1	I/O	Port 87: I/O port (with pull-up resistor) Serial data request signal 1
P90 INT5	1	I/O Input	Port 90: I/O port Interrupt request pin 5: Interrupt request pin with programmable level/rising edge/falling edge
P93 TB0IN0	1	I/O Input	Port 93: I/O port Timer B0 input 0
P94 TB0IN1	1	I/O Input	Port 94: I/O port Timer B0 input 1
P95 TB0OUT0	1	I/O Output	Port 95: I/O port Timer B0 output 0
P96 TB0OUT1	1	I/O Output	Port 96: I/O port Timer B0 output 1
PA0 to PA7 AN0 to AN7 $\overline{\text{ADTRG}}$	8	Input Input Input	Port A0 to A7: Pins used to input port. Analog input 0 to 7: Pins used to input to AD converter. AD trigger: Signal used to request AD start (PA3).
PZ2 $\overline{\text{HWR}}$	1	I/O Output	Port Z2: I/O port (with pull-up resistor) High write: Strobe signal for writing data to pins D8 to D15
PZ3	1	I/O	Port Z3: I/O port (with pull-up resistor)

Table 2.2.3 Pin Names and Functions (3/3)

Pin Names	Number of Pins	I/O	Functions
$\overline{\text{BOOT}}$	1	Input	This pin sets boot mode (with pull-up resistor)
$\overline{\text{NMI}}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with programmable falling edge level or with both edge levels programmable
AM0 to AM1	2	Input	Operation mode: AM1 = 0 and AM0 = 1: External 16-bit bus is fixed or external 8-/16-bit buses are mixed. AM1 = 0 and AM0 = 0: External 8-bit bus is fixed.
$\overline{\text{RESET}}$	1	Input	Reset: Initializes TMP91C630F (with pull-up resistor)
VREFH	1	Input	Pin for reference voltage input to AD converter (H)
VREFL	1	Input	Pin for reference voltage input to AD converter (L)
AVCC	1	I/O	Power supply pin for AD converter
AVSS	1		GND supply pin for AD converter
X1/X2	2		Oscillator connection pins
DVCC	4		Power supply pins
DVSS	4		GND pins (0 V)
EMU0	1	Output	Open pin
EMU1	1	Output	Open pin

Note 1: An external DMA controller cannot access the device's built-in memory or built-in I/O devices using the $\overline{\text{BUSRQ}}$ and $\overline{\text{BUSAK}}$ signals.

3. Operation

This section describes the basic components, functions and operation of the TMP91C630.

Notes and restrictions which apply to the various items described here are outlined in section 7. Precautions and restrictions at the end of this databook.

3.1 CPU

The TMP91C630 incorporates a high-performance 16-bit CPU (the 900/L1 CPU). For a description of this CPU's operation, please refer to the section of this databook which describes the TLCS-900/L1 CPU.

The following sub-sections describe functions peculiar to the CPU used in the TMP91C630; these functions are not covered in the section devoted to the TLCS-900/L1 CPU.

3.1.1 Reset

When resetting the TMP91C630 microcontroller, ensure that the power supply voltage is within the operating voltage range, and that the internal high-frequency oscillator has stabilized. Then set the $\overline{RESET}$ input to Low level at least for 10 system clocks (8.89 μs at 36 MHz).

Thus, when turn on the switch, be set to the power supply voltage is within the operating voltage range, and that the internal high-frequency oscillator has stabilized. Then hold the $\overline{RESET}$ input to Low level at least for 10 system clocks.

Clock gear is initialized 1/16 mode by Reset operation. It means that the system clock mode f_{SYS} is set to fc/32 (= fc/16 × 1/2).

When the reset has been accepted, the CPU performs the following:

- Sets the program counter (PC) as follows in accordance with the reset vector stored at address FFFF00H to FFFF02H:

  PC<0:7> ← Data in location FFFF00H
  PC<8:15> ← Data in location FFFF01H
  PC<16:23> ← Data in location FFFF02H

- Sets the stack pointer (XSP) to 100H.
- Sets bits <IFF0:IFF2> of the status register (SR) to 111 (thereby setting the interrupt level mask register to level 7).
- Sets the <MAX> bit of the status register to 1 (MAX mode).
  (Note: As this product does not support MIN mode, do not program a 0 to the <MAX> bit.)
- Clears bits <RFP0:RFP2> of the status register to 000 (thereby selecting register bank 0).

When the reset is cleared, the CPU starts executing instructions according to the program counter settings. CPU internal registers not mentioned above do not change when the reset is cleared.

When the reset is accepted, the CPU sets internal I/O, ports and other pins as follows.

- Initializes the internal I/O registers.
- Sets the port pins, including the pins that also act as internal I/O, to general-purpose input or output port mode.

Note: The CPU internal register (except to PC, SR and XSP) and internal RAM data do not change by resetting.

Figure 3.1.1 shows the timing of a reset for the TMP91C630.

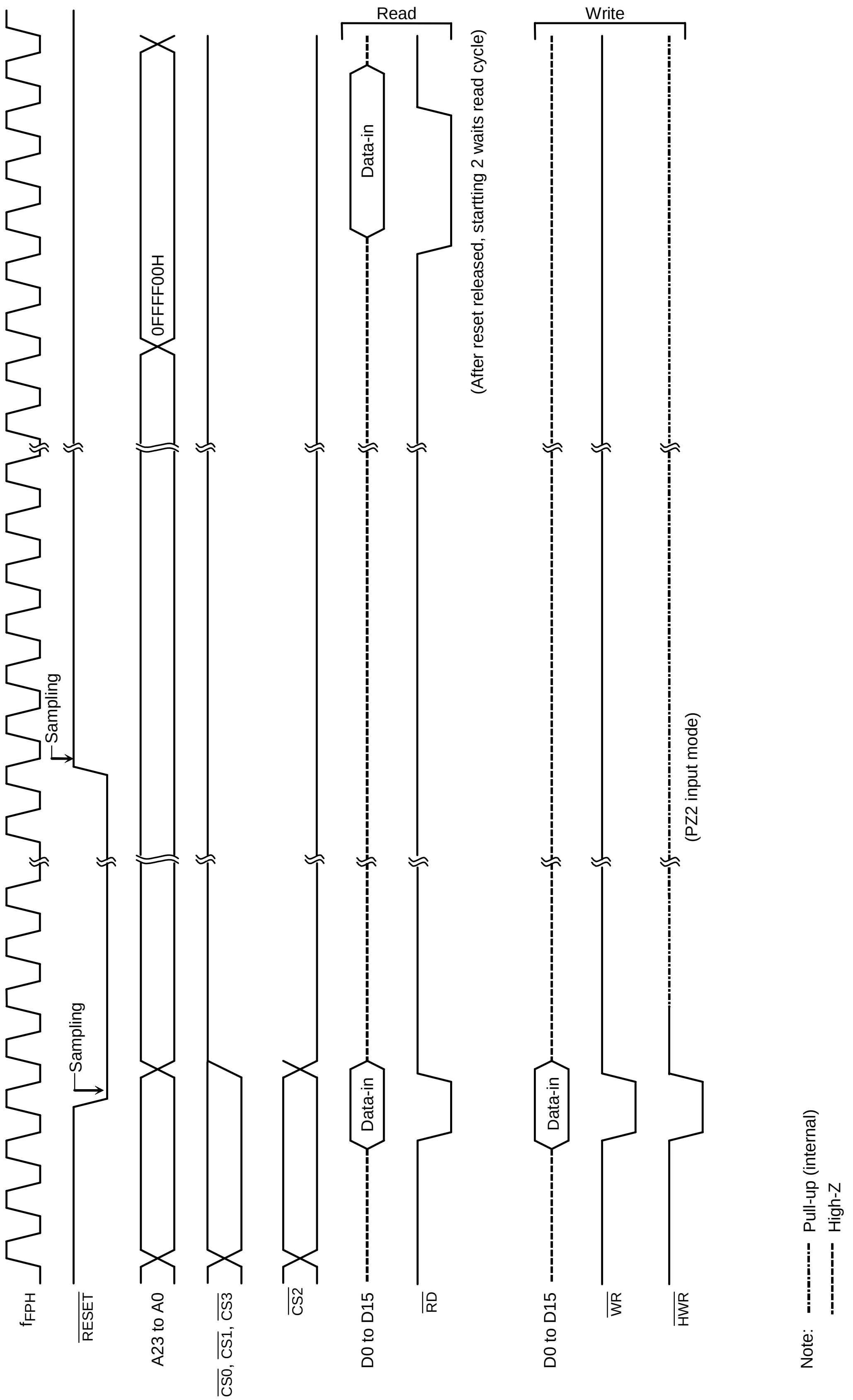


Figure 3.1.1 TMP91C630 Reset Timing Example

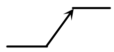
3.2 Outline of Operation Modes

There are multi-chip and multi-boot modes. Which mode is selected depends on the device's pin state after a reset.

- Multi-chip mode: The device normally operations in this mode. After a reset, the device starts executing the external memory program.
- Multi-boot mode: This mode is used to rewrite the external flash memory by serial transfer (UART).

  After a reset, internal boot program starts up, executing an on-board rewrite program.

Table 3.2.1 Operation Mode Setup Table

Operation Mode	Mode Setup Input Pin	
	$\overline{RESET}$	$\overline{BOOT}$
Multi-chip mode		H
Multi-boot mode		L

3.3 Memory Map

Figure 3.3.1 is a memory map of the TMP91C630.

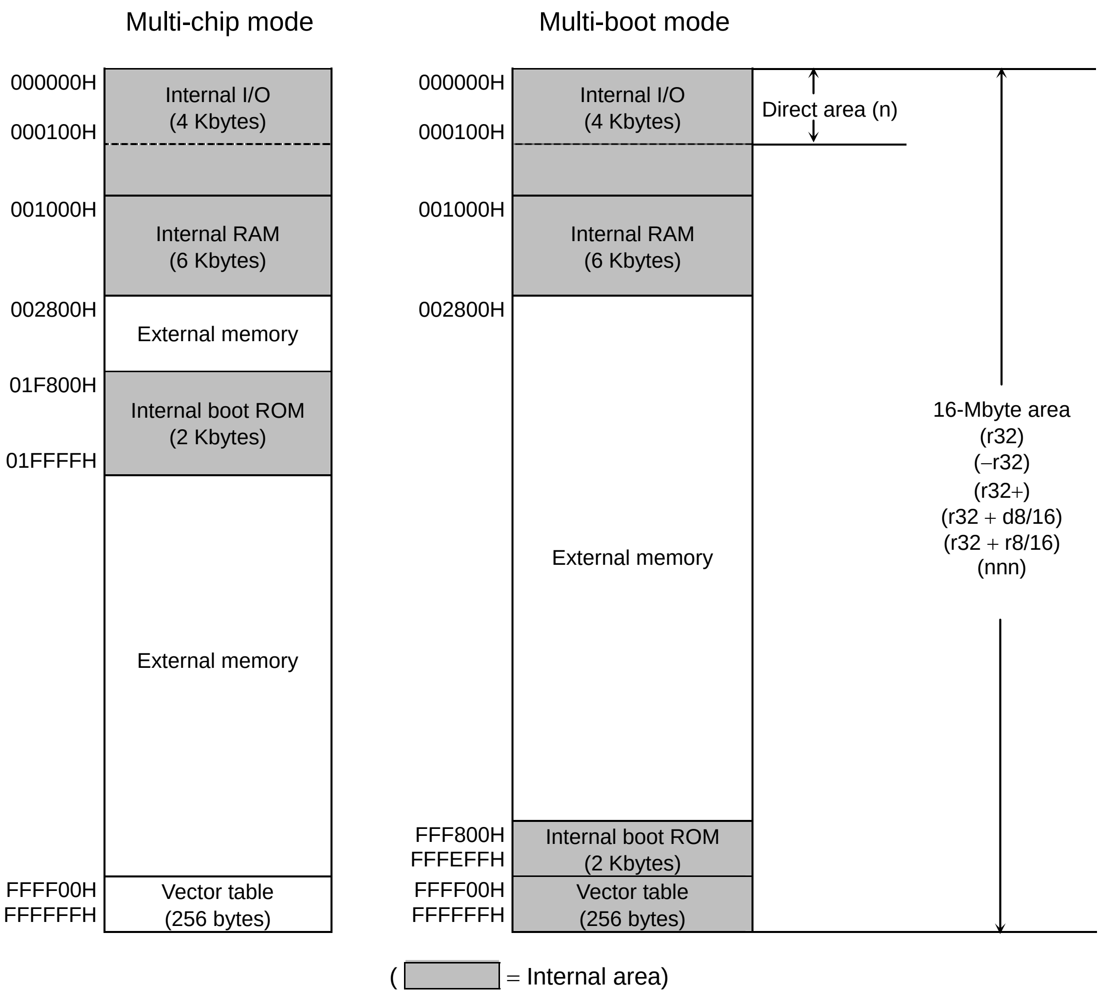


Figure 3.3.1 TMP91C630 Memory Map

4. Electrical Characteristics

4.1 Maximum Ratings

Parameter	Symbol	Rating	Unit
Power supply voltage	Vcc	−0.5 to 4.0	V
Input voltage	VIN	−0.5 to Vcc + 0.5	V
Output current (per pin)	IOL	2	mA
Output current (per pin)	IOH	−2	mA
Output current (total)	ΣIOL	80	mA
Output current (total)	ΣIOH	−80	mA
Power dissipation (Ta = 85°C)	PD	600	mW
Soldering temperature (10 s)	TSOLDER	260	°C
Storage temperature	TSTG	−65 to 150	°C
Operating temperature	TOPR	−40 to 85	°C

Note: The maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no maximum rating value will ever be exceeded.

4.2 DC Characteristics (1/2)

Parameter		Symbol	Condition	Min	Typ. (Note)	Max	Unit
Power supply voltage (AVCC = DVCC) (AVSS = DVSS = 0 V)		Vcc	fc = 10 MHz to 36 MHz	2.7		3.6	V
Input Low Voltage	D0 to D7, P10 to P17 (D8 to D15)	V_{IL}	Vcc = 2.7 V to 3.6 V	−0.3		0.6	V
	The other ports	V_{IL1}	Vcc = 2.7 V to 3.6 V			0.3 Vcc	
	$\overline{\text{RESET}}$, $\overline{\text{NMI}}$, $\overline{\text{BOOT}}$ P56 (INT0), P70 (INT1) P72 (INT2), P73 (INT3) P75 (INT4), P90 (INT5)	V_{IL2}	Vcc = 2.7 V to 3.6 V			0.25 Vcc	
	AM0, 1	V_{IL3}	Vcc = 2.7 V to 3.6 V			0.3	
	X1	V_{IL4}	Vcc = 2.7 V to 3.6 V			0.2 Vcc	
Input High Voltage	D0 to D7, P10 to P17 (D8 to D15)	V_{IH}	Vcc = 2.7 V to 3.6 V	2.0		Vcc + 0.3	
	The other ports	V_{IH1}	Vcc = 2.7 V to 3.6 V	0.7 Vcc			
	$\overline{\text{RESET}}$, $\overline{\text{NMI}}$, $\overline{\text{BOOT}}$ P56 (INT0), P70 (INT1) P72 (INT2), P73 (INT3) P75 (INT4), P90 (INT5)	V_{IH2}	Vcc = 2.7 V to 3.6 V	0.75 Vcc			
	AM0, 1	V_{IH3}	Vcc = 2.7 V to 3.6 V	Vcc − 0.3			
	X1	V_{IH4}	Vcc = 2.7 V to 3.6 V	0.8 Vcc			
Output low voltage		V_{OL}	IOL = 1.6 mA			0.45	V
Output high voltage		V_{OH}	IOH = −400 μA	2.4			

Note: Typical measurement Condition is Ta = 25°C, Vcc = 3.0 V unless otherwise noted.

DC Characteristics (2/2)

Parameter	Symbol	Min	Typ. (Note 1)	Max	Condition	Unit
Input leakage current	ILI		0.02	±5	$0.0 \le V_{IN} \le Vcc$	μA
Output leakage current	ILO		0.05	±10	$0.2 \le V_{IN} \le Vcc - 0.2$	
Power down voltage (at STOP, RAM back-up)	VSTOP	2.0		3.6	$V_{IL2} = 0.2$ Vcc, $V_{IH2} = 0.8$ Vcc	V
$\overline{\text{RESET}}$ pull-up resistor	RRST	80		400	Vcc = 2.7 V to 3.6 V	kΩ
$\overline{\text{BOOT}}$ pull-up resistor	RBT	80		400	Vcc = 2.7 V to 3.6 V	kΩ
Pin capacitance	CIO			10	fc = 1 MHz	pF
Schmitt width $\overline{\text{RESET}}$, $\overline{\text{NMI}}$, $\overline{\text{BOOT}}$, INT0 to 5	VTH	0.4	1.0		Vcc = 2.7 V to 3.6 V	V
Programmable pull-up resistor	RKH	80		400	Vcc = 2.7 V to 3.6 V	kΩ
NORMAL (Note 2): (Note 3)	Icc		17	25	Vcc = 2.7 V to 3.6 V fc = 36 MHz	mA
IDLE2 (Note 3)			4	8		
IDLE1 (Note 3)			1.5	3.5		
STOP			0.1	10	Vcc = 2.7 V to 3.6 V	μA

Note 1: Typical measurement condition is Ta = 25°C, Vcc = 3.0 V unless otherwise noted.

Note 2: Icc measurement conditions (NORMAL):
All functions operate; output pins are open and input pins are fixed.

Note 3: Power supply current from AVCC pin is included in power supply current (Icc) of DVCC pin.

4.3 AC Characteristics

(1) Vcc = 2.7 to 3.6 V

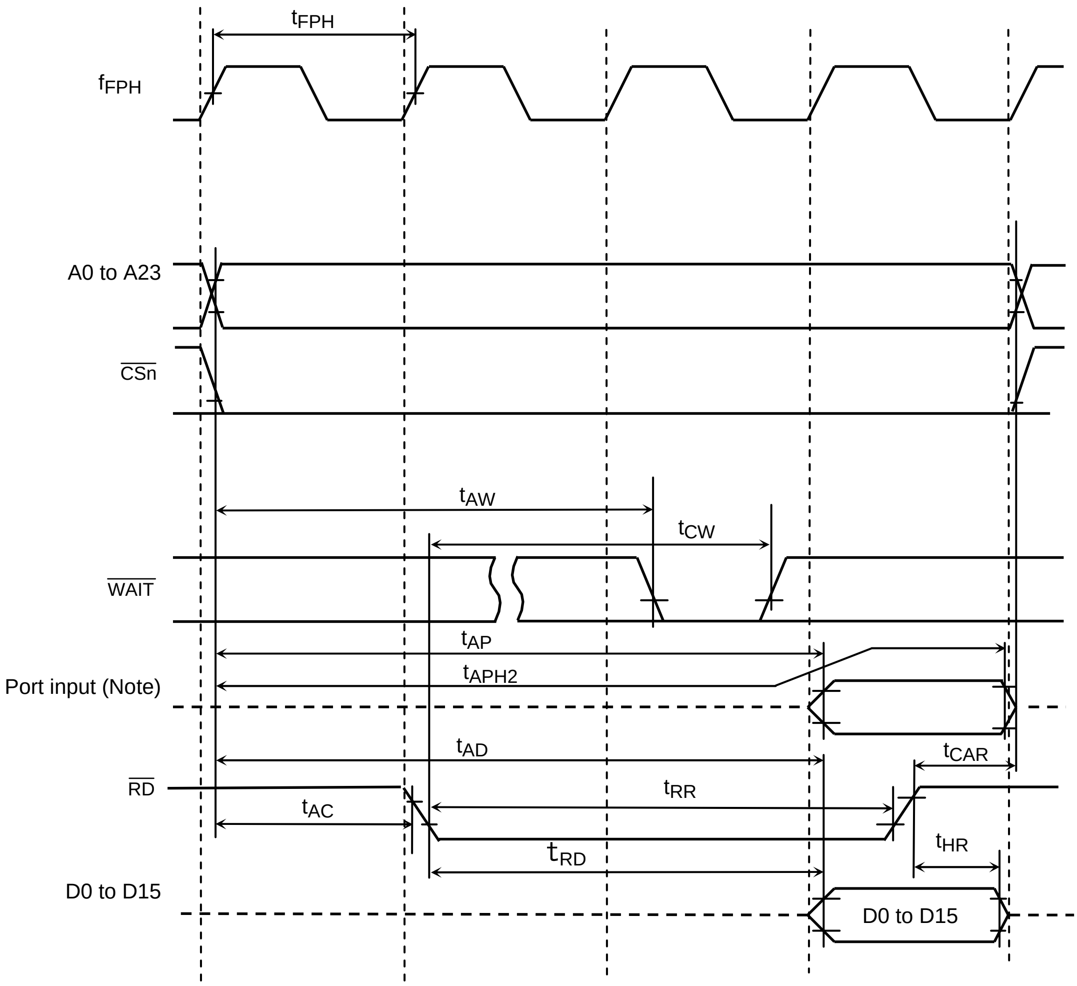
No.	Parameter	Symbol	Variable		f_{FPH} = 36 MHz		Unit
			Min	Max	Min	Max	
1	f_{FPH} period (= x)	t_{FPH}	27.6	100	27.6		ns
2	A0 to 23 valid → $\overline{RD}$ / $\overline{WR}$ fall	t_{AC}	x − 26		1.6		ns
3	$\overline{RD}$ rise → A0 to A23 hold	t_{CAR}	0.5x − 13.8		0.0		ns
4	$\overline{WR}$ rise → A0 to A23 hold	t_{CAW}	x − 13		14.6		ns
5	A0 to A23 valid → D0 to D15 input	t_{AD}		3.5x − 40		56.6	ns
6	$\overline{RD}$ fall → D0 to D15 input	t_{RD}		2.5x − 34		35.0	ns
7	$\overline{RD}$ low width	t_{RR}	2.5x − 25		44.0		ns
8	$\overline{RD}$ rise → D0 to D15 hold	t_{HR}	0		0		ns
9	$\overline{WR}$ low width	t_{WW}	2.0x − 25		30.2		ns
10	D0 to D15 valid → $\overline{WR}$ rise	t_{DW}	1.5x − 35		6.4		ns
11	$\overline{WR}$ rise → D0 to D15 hold (1 + N) waits mode	t_{WD}	x − 25		2.6		ns
12	A0 to A23 valid → $\overline{WAIT}$ input (1 + N) waits mode	t_{AW}		3.5x − 60		36.6	ns
13	$\overline{RD}$ / $\overline{WR}$ fall → $\overline{WAIT}$ hold	t_{CW}	2.5x + 0		69.0		ns
14	A0 to A23 valid → PORT input	t_{APH}		3.5x − 76		20.6	ns
15	A0 to A23 valid → PORT hold	t_{APH2}	3.5x		96.6		ns
16	A0 to A23 valid → PORT valid	t_{APO}		3.5x + 60		156.6	ns

AC Measuring Conditions

- Output Level : High = 0.7 Vcc, Low = 0.3 Vcc, C_L = 50 pF
- Input Level : High = 0.9 Vcc, Low = 0.1Vcc

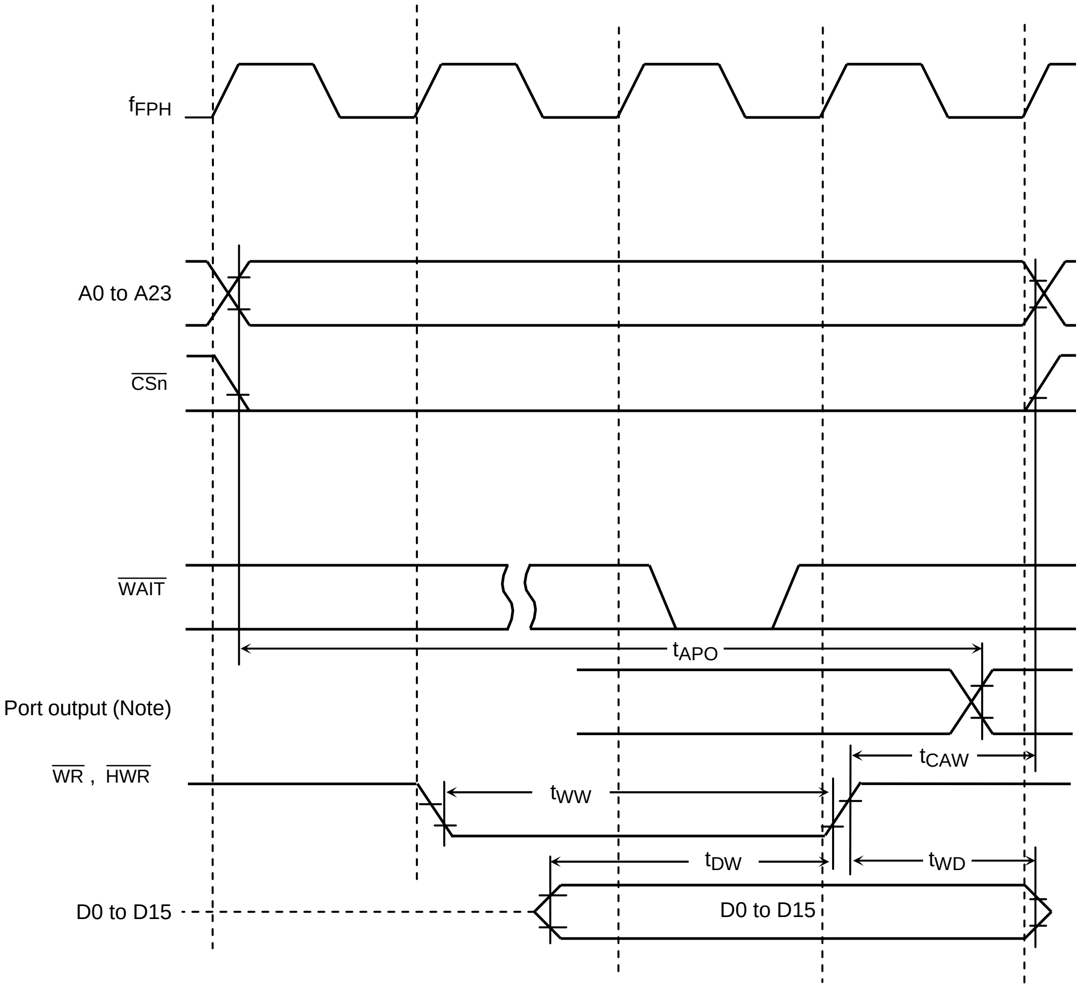
Note: Symbol x in the above table means the period of clock f_{FPH}, it's half period of the system clock f_{SYS} for CPU core. The period of f_{FPH} depends on the clock gear setting.

(2) Read cycle



Note: Since the CPU accesses the internal area to read data from a port, the control signals of external pins such as $\overline{RD}$ and $\overline{CS}$ are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

(3) Write cycle



Note: Since the CPU accesses the internal area to write data to a port, the control signals of external pins such as $\overline{WR}$ and $\overline{CS}$ are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

4.4 AD Conversion Characteristics

AVCC = DVCC, AVSS = DVSS

Parameter	Symbol	Min	Typ.	Max	Unit
Analog reference voltage (+)	VREFH	Vcc – 0.2 V	Vcc	Vcc	V
Analog reference voltage (–)	VREFL	V_{SS}	V_{SS}	Vss + 0.2 V	
Analog input voltage range	VAIN	V_{REFL}		V_{REFH}	
Analog current for analog Reference voltage <VREFON> = 1	IREF (VREFL = 0V)		0.94	1.35	mA
<VREFON> = 0			0.02	5.0	μA
Error (not including quantizing errors)	–		±1.0	±4.0	LSB

Note 1: 1 LSB = (VREFH – VREFL)/1024 [V]

Note 2: The value of Icc includes the current which flows through the AVCC pin.

4.5 Serial Channel Timing (I/O Internal Mode)

Note: Symbol x in the below table means the period of clock f_{FPH}, it's half period of the system clock f_{SYS} for CPU core. The period of f_{FPH} depends on the clock gear setting.

(1) SCLK input mode

Parameter	Symbol	Variable		36 MHz (Note)		Unit
		Min	Max	Min	Max	
SCLK period	t_{SCY}	16X		0.44		μs
Output data → SCLK rising/falling edge*	t_{OSS}	$t_{SCY}/2 - 4X - 85$		25		ns
SCLK rising/falling edge* → Output data hold	t_{OHS}	$t_{SCY}/2 + 2X + 0$		276		ns
SCLK rising/falling edge* → Input data hold	t_{HSR}	3X + 10		92		ns
SCLK rising/falling edge* → Valid data input	t_{SRD}		$t_{SCY} - 0$		440	ns
Valid data input → SCLK rising/falling edge*	t_{RDS}	0		0		ns

*) SCLK rinsing/falling edge: The rising edge is used in SCLK rising mode.
The falling edge is used in SCLK falling mode.

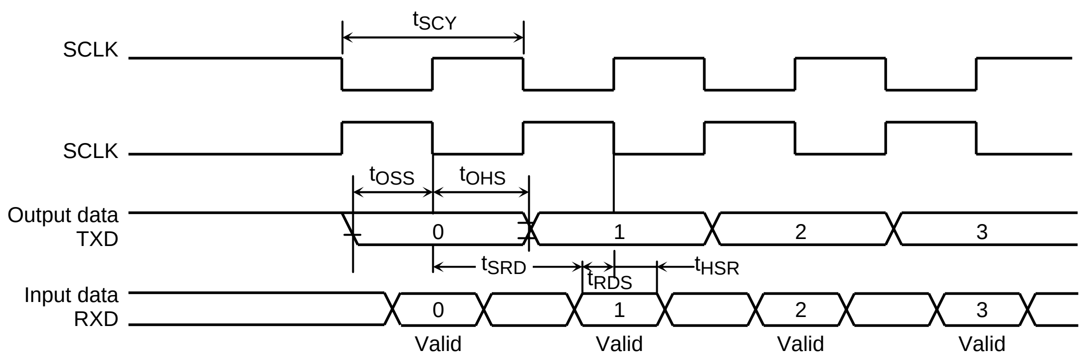
Note: at $t_{SCY} = 16X$

(2) SCLK output mode

Parameter	Symbol	Variable		36 MHz (Note)		Unit
		Min	Max	Min	Max	
SCLK period (programable)	t_{SCY}	16X	8192X	0.44		μs
Output data →SCLK rising/falling edge*	t_{OSS}	$t_{SCY}/2 - 40$		180		ns
SCLK rising/falling edge* → Output data hold	t_{OHS}	$t_{SCY}/2 - 40$		180		ns
SCLK rising/falling edge* → Input data hold	t_{HSR}	0		0		ns
SCLK rising/falling edge* → Valid data input	t_{SRD}		$t_{SCY} - 1X - 90$		324	ns
Valid data input → SCLK rising/falling edge*	t_{RDS}	1X + 90		117		ns

*) SCLK rinsing/falling edge: The rising edge is used in SCLK rising mode.
The falling edge is used in SCLK falling mode.

Note: at $t_{SCY} = 16X$



4.6 Event Counter (TA0IN, TA4IN, TB0IN0, TB0IN1)

Parameter	Symbol	Variable		36 MHz		Unit
		Min	Max	Min	Max	
Clock perild	t_{VCK}	8X + 100		320		ns
Clock low level width	t_{VCKL}	4X + 40		150		ns
Clock high level width	t_{VCKH}	4X + 40		150		ns

Note: Symbol x in the above table means the period of clock f_{FPH}, it's half period of the system clock f_{SYS} for CPU core. The period of f_{FPH} depends on the clock gear setting.

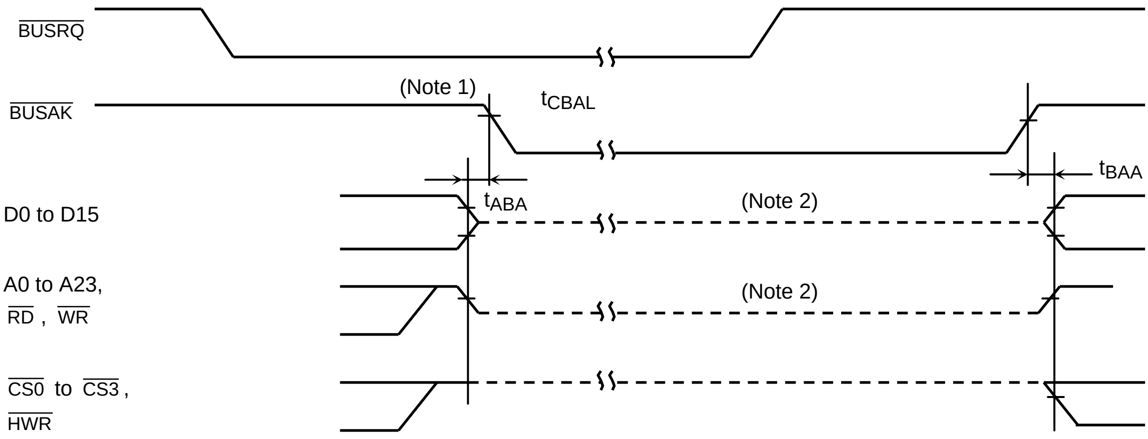
4.7 Interrupts

Note: Symbol x in the above table means the period of clock f_{FPH}, it's half period of the system clock f_{SYS} for CPU core. The period of f_{FPH} depends on the clock gear setting.

(1) $\overline{\text{NMI}}$, INT0 to INT5 interrupts

Parameter	Symbol	Variable		36 MHz		Unit
		Min	Max	Min	Max	
$\overline{\text{NMI}}$, INT0 to INT5 low level width	t_{INTAL}	4X + 40		150		ns
$\overline{\text{NMI}}$, INT0 to INT5 high level width	t_{INTAH}	4X + 40		150		ns

4.8 Bus Request/Bus Acknowledge



Parameter	Symbol	Variable		f_{FPH} = 36 MHz		Unit
		Min	Max	Min	Max	
Output buffer to $\overline{\text{BUSAK}}$ low	t_{ABA}	0	80	0	80	ns
$\overline{\text{BUSAK}}$ high to output buffer on	t_{BAA}	0	80	0	80	ns

Note 1: Even if the $\overline{\text{BUSRQ}}$ signal goes Low, the bus will not be released while the $\overline{\text{WAIT}}$ signal is Low. The bus will only be released when $\overline{\text{BUSRQ}}$ goes Low while $\overline{\text{WAIT}}$ is High.

Note 2: This line shows only that the output buffer is in the Off state.
It does not indicate that the signal level is fixed.
Just after the bus is released, the signal level set before the bus was released is maintained dynamically by the external capacitance. Therefore, to fix the signal level using an external resister during bus release, careful design is necessary, since fixing of the level is delayed.
The internal programmable pull-up/pull-down resistor is switched between the Active and Non-Active states by the internal signal.