54F/74F547

Octal Decoder/Demultiplexer With Address Latches and Acknowledge

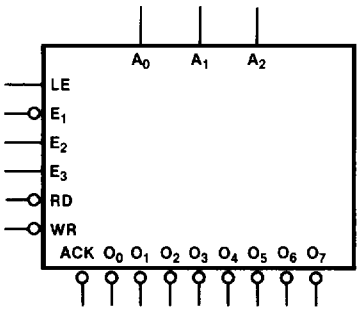
Description

The 'F547 is a 3-to-8 line address decoder with latches for address storage. Designed primarily to simplify multiple chip selection in a microprocessor system, it contains one active LOW and two active HIGH Enables to conserve address space. Also included is an active LOW Acknowledge output that responds to either a Read or Write input signal when the Enables are active.

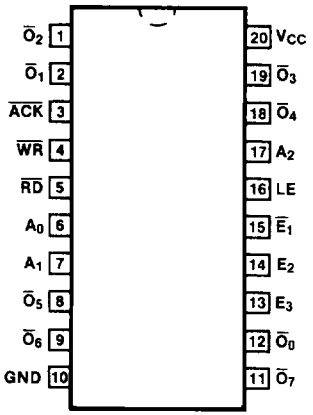
- **3-to-8 Line Address Decoder**
- **Address Storage Latches**
- **Multiple Enables for Address Extension**
- **Open Collector Acknowledge Output**

Ordering Code: See Section 5

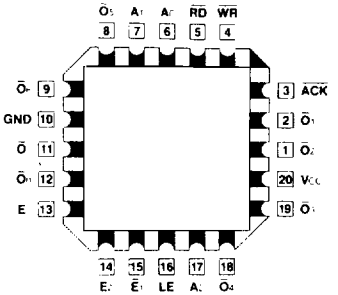
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_0-A_2	Output Select Address Inputs	0.5/0.375
$\overline{E}_1$	Chip Enable Input (Active LOW)	0.5/0.375
E_2, E_3	Chip Enable Inputs	0.5/0.375
$\overline{LE}$	Latch Enable Input	0.5/0.375
$\overline{RD}$	Read Acknowledge Input (Active LOW)	0.5/0.375
$\overline{WR}$	Write Acknowledge Input (Active LOW)	0.5/0.375
$\overline{ACK}$	Open Collector Acknowledge Output (Active LOW)	OC*/12.5
$\overline{O}_0$-$\overline{O}_7$	Decoded Outputs (Active LOW)	25/12.5

*OC = Open Collector

Functional Description

When enabled, the 'F547 accepts the A_0-A_2 Address inputs and decodes them to select one of eight active LOW, mutually exclusive outputs, as shown in the Decoder Truth Table. With LE HIGH, the Address latches are transparent and the output selection changes each time the A_0-A_2 address changes. When LE is LOW, the latches store the last valid address preceding the HIGH-to-LOW transition of the LE input signal. For applications in which the separation of latch enable and chip enable functions is not required, LE and $\overline{E}_1$ can be tied together, such that when HIGH the outputs are OFF and the latches are transparent, and when LOW the latches are storing and the selected output is enabled.

The open collector Acknowledge ($\overline{ACK}$) output is normally HIGH (i.e. OFF) and goes LOW when $\overline{E}_1$, E_2 and E_3 are all active and either the Read ($\overline{RD}$) or Write ($\overline{WR}$) input is LOW, as indicated in the Acknowledge Truth Table.

Acknowledge Truth Table

Inputs					Output
$\overline{E}_1$	E_2	E_3	$\overline{RD}$	$\overline{WR}$	$\overline{ACK}$
H	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
L	H	H	H	H	H
L	H	H	L	X	L
L	H	H	X	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Latch and Output Status Table

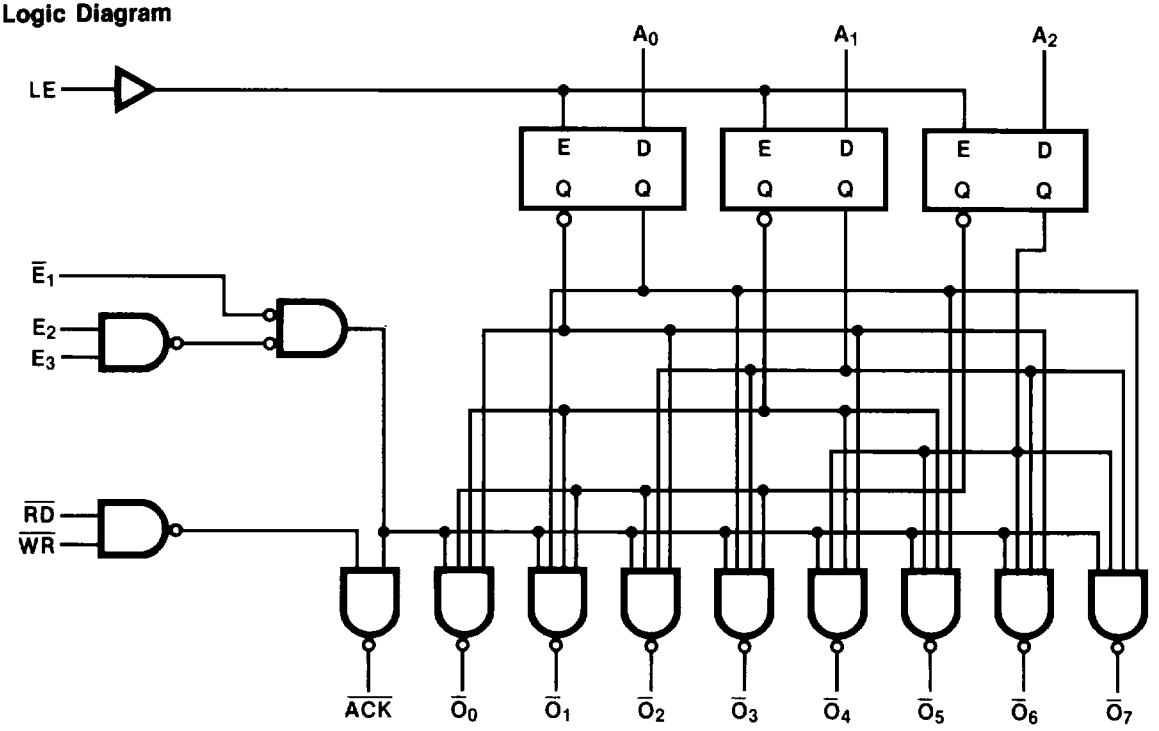
Inputs				Latch	Decoder
$\overline{E}_1$	E_2	E_3	LE	Status	Outputs
L	H	H	H	Transparent	—
L	H	H	L	Storing	Selected Output LOW
H	X	X	X	Storing	All Outputs HIGH
X	L	X	X	Storing	All Outputs HIGH
X	X	L	X	Storing	All Outputs HIGH

Decoder Truth Table*

Inputs			Outputs							
A_2	A_1	A_0	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H
L	H	L	H	H	L	H	H	H	H	H
L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	H	H	H	L	H	H	H
H	L	H	H	H	H	H	H	L	H	H
H	H	L	H	H	H	H	H	H	L	H
H	H	H	H	H	H	H	H	H	H	L

*Assuming $\overline{E}_1$, LOW; E_2 and E_3, HIGH

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		17	25	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			T_A, V_{CC} = Mil $C_L = 50\ pF$		T_A, V_{CC} = Com $C_L = 50\ pF$			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	4.0 5.0	7.0 9.0	9.0 12.0	3.0 5.0	10.5 13.0	4.0 5.0	10.0 13.0	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ to $\overline{O}_n$	4.0 4.0	6.5 6.5	8.5 8.5	3.0 3.5	10.0 10.0	4.0 4.0	9.5 9.5	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay LE to $\overline{O}_n$	4.0 5.0	7.5 14.5	9.5 18.0	4.0 5.0	11.5 20.0	4.0 5.0	10.5 19.0	ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay E_2 or E_3 to $\overline{O}_n$	5.0 5.0	8.5 8.5	11.0 11.0	4.5 4.5	12.5 12.5	5.0 5.0	12.0 12.0	ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$, $\overline{RD}$ or $\overline{WR}$ to $\overline{ACK}$	6.5 4.0	11.0 7.5	14.0 9.5	6.5 3.5	16.0 11.0	6.5 4.0	15.0 10.5	ns	3-1 3-4
t_{PLH} t_{PHL}	Propagation Delay E_2 or E_3 to $\overline{ACK}$	8.0 5.0	13.0 8.5	16.5 11.0	8.0 5.0	18.5 12.5	8.0 5.0	17.5 12.0	ns	3-1 3-3

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A_n to LE	5.0 5.0			5.0 5.0		5.0 5.0		ns	3-15
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A_n to LE	6.0 6.0			6.0 6.0		6.0 6.0			
$t_w(H)$	LE Pulse Width, HIGH	6.0			6.0		6.0		ns	3-7