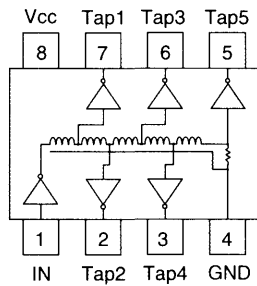


# ACMDM Series Advanced CMOS Logic Buffered 5-Tap Delay Modules

74ACT type input is compatible with TTL • Outputs can Source / Sink 24 mA

- Low Profile 8-Pin Package  
Two Surface Mount Versions
- Available in Low Voltage CMOS  
74LVC Logic version LVMDM Series
- 5 Equal Delay Taps
- Operating Temp.  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

ACMDM 8-Pin Schematic



Electrical Specifications at  $25^{\circ}\text{C}$

74ACT 5 Tap 8-Pin DIP P/N	Tap Delay Tolerances +/- 5% or 2ns (+/- 1ns <13ns)					Tap-to-Tap (ns)
	Tap 1	Tap 2	Tap 3	Tap 4	Total - Tap 5	
ACMDM-30	6.0	12.0	18.0	24.0	$30 \pm 2.0$	$6 \pm 2.0$
ACMDM-35	7.0	14.0	21.0	28.0	$35 \pm 2.0$	$7 \pm 2.0$
ACMDM-40	8.0	16.0	24.0	32.0	$40 \pm 2.0$	$8 \pm 2.0$
ACMDM-50	10.0	20.0	30.0	40.0	$50 \pm 2.5$	$10 \pm 2.0$
ACMDM-60	12.0	24.0	36.0	48.0	$60 \pm 3.0$	$12 \pm 2.0$
ACMDM-75	15.0	30.0	45.0	60.0	$75 \pm 3.75$	$15 \pm 2.5$
ACMDM-80	16.0	32.0	48.0	64.0	$80 \pm 4.0$	$16 \pm 3.0$
ACMDM-100	20.0	40.0	60.0	80.0	$100 \pm 5.0$	$20 \pm 3.0$
ACMDM-125	25.0	50.0	75.0	100.0	$125 \pm 6.25$	$25 \pm 3.0$
ACMDM-150	30.0	60.0	90.0	120.0	$150 \pm 7.5$	$30 \pm 3.0$
ACMDM-200	40.0	80.0	120.0	160.0	$200 \pm 10.0$	$40 \pm 4.0$
ACMDM-250	50.0	100.0	150.0	200.0	$250 \pm 12.5$	$50 \pm 5.0$

## TEST CONDITIONS -- Advanced CMOS, 74ACT

$V_{CC}$  Supply Voltage ..... 5.00VDC  
 Input Pulse Voltage ..... 3.00V  
 Input Pulse Rise Time ..... 3.0 ns max.  
 Input Pulse Width / Period ..... 1000 / 2000 ns

1. Measurements made at  $25^{\circ}\text{C}$
2. Delay Times measured at 1.50V level of input to +2.50V level of Output on leading edge.
3. Rise Times measured from 10% to 90% points.
4. 50pf probe and fixture load on output under test.

## OPERATING SPECIFICATIONS

Supply Voltage,  $V_{CC}$  .....  $5.00 \pm 0.50$  VDC  
 Supply Current,  $I_{CC}$  ..... 14 mA typ., 28 mA max.  
 $I_{CCH}$ ,  $V_{IN} = V_{CC}$ ,  $V_{CC} = 5.5\text{V}$  ..... 40  $\mu\text{A}$  typ.  
 $I_{CCL}$ ,  $V_{IN} = 0\text{V}$ ,  $V_{CC} = 5.5\text{V}$  ..... 25 mA typ.  
 Logic "1" Input:  $V_{IH}$  ..... 2.00 V min., 5.50V max.  
 Logic "0" Input:  $V_{IL}$  ..... 0.80 V max.  
 Logic "1" Voltage Out,  $V_{OH}$  ..... 3.8 V min.  
 Logic "0" Voltage Out,  $V_{OL}$  ..... 0.44 V max.  
 Max. Input Current,  $I_{IN}$  .....  $\pm 1.0$   $\mu\text{A}$   
 Minimum Input Pulse Width ..... 40% of Delay min.  
 Operating Temperature Range .....  $-40^{\circ}$  to  $+85^{\circ}\text{C}$   
 Storage Temperature Range .....  $-65^{\circ}$  to  $+150^{\circ}\text{C}$

## P/N Description ACMDM - XXX X

74ACT Buffered 5 Tap Delay  
 Molded Package Series:  
 8-pin DIP: ACMDM  
 Total Delay in nanoseconds (ns)  
 Lead Style: Blank = Thru-hole  
 G = "Gull Wing" SMD  
 J = "J" Bend SMD

Examples: ACMDM-25G = 25ns (5ns per tap) 74ACT, 8-Pin G-SMD  
 ACMDM-100 = 100ns (20ns per tap) 74ACT, 8-Pin DIP

Dimensions in Inches (mm)

