Comlinear Corporation

12-Bit, Fast Sampling Wideband Track-and-Hold

CLC942

APPLICATIONS:

- flash A/D driver
- high-resolution, subranging A/D driver
- signal deglitching (as in CCD or D/A systems)
- communication systems
- radar and IF processors

FEATURES (typical):

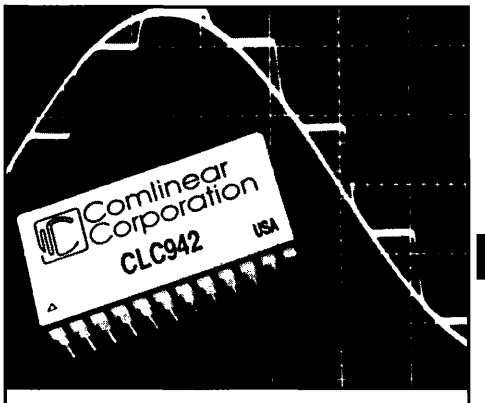
- 25ns hold-to-track acquisition time (0.01%)
- 5ns track-to-hold settling time
- 1.4ps aperture jitter
- 70MHz small-signal bandwidth
- 78dB feedthrough rejection
- ECL control signal

DESCRIPTION:

The CLC942 is a 12-Bit accurate, fast sampling, wideband track-and-hold amplifier which offers ultra-fast switching performance. Closed-loop monolithic buffers ensure that switching accuracy is fully realized, even at the fastest sampling rates. The CLC942 is an improved alternate source for the HTS-0010 and the SHC600.

The CLC942 is an ideal device for driving flash A/D's, especially those configured in high resolution, subranging architectures. The very fast 25ns hold-to-track acquisition time (0.01%) and 5ns track-to-hold settling time permit the high sampling rates needed in applications such as radar and communications. Other specifications, such as the 1.4ps aperture jitter, 15mV pedestal offset, and -74dBc harmonic distortion are similarly supportive of A/D system performance goals. The CLC942 is fully compatible with demanding flash A/D input requirements as demonstrated by its ±2.2V output range and its ability to drive up to 90pF loads.

The CLC942 is constructed using thin film resistor/bipolar transistor technology as well as custom integrated circuits. The CLC942AI is specified over a temperature range of -25°C to +85°C, while the CLC942A8C is specified over a range of -55°C to +125°C. Both devices are packaged in a 24-pin, 600 mil wide, ceramic DIP.



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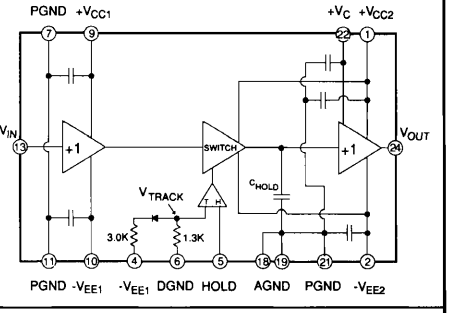
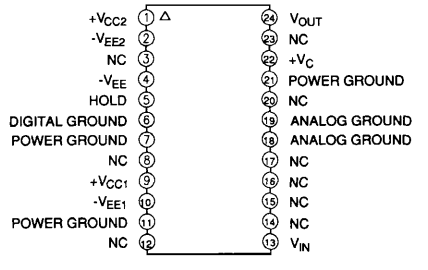
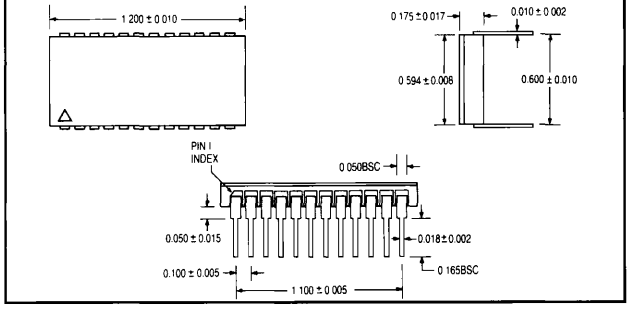
CLC942 Equivalent Circuit



CLC942 Pin Out



Package Dimensions



Electrical Characteristics ($+V_{CC1,2} = +5.0V$; $-V_{EE1,2} = -5.0V$; $+V_C = +15V$; $R_L = 100\Omega$; unless otherwise specified)

PARAMETER[1]	CONDITIONS	TYP	MAX & MIN RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC942A8	+25°C	-55°C	+25°C	+125°C		
Ambient Temperature	CLC942AI	+25°C	-25°C	+25°C	+85°C		
TRACK-MODE DYNAMICS							
*-3dB bandwidth		70	40	50	50	MHz	SSBW
slew rate		300	220	250	220	V/μs	SR
2nd harmonic distortion	$2V_{pp}$; 4MHz;$R_L = 1k\Omega$	-74	-62	-65	-65	dBc	HD2A
	$2V_{pp}$;20MHz;$R_L = 1k\Omega$	-50	-38	-44	-43	dBc	HD2
3rd harmonic distortion	$2V_{pp}$; 4MHz;$R_L = 1k\Omega$	-75	-70	-72	-70	dBc	HD3A
	$2V_{pp}$;20MHz;$R_L = 1k\Omega$	-64	-54	-55	-43	dBc	HD3
HOLD-MODE DYNAMICS							
*droop rate		20	450	230	3000	μV/μs	DR
*feedthrough rejection	20MHz, $V_{IN} = 2V_{pp}$	78	70	72	70	dB	FTR
TRACK-TO-HOLD SWITCHING							
*effective aperture delay		-1.5	-3	-4	-6	ns	TA
*aperture jitter		1.4	2.0	2.0	2.0	ps_{rms}	UHD
*pedestal offset		8	12	12	15	mV	PO
* temperature coefficient	endpoint average	10	40	40	40	μV/°C	DPO
sensitivity to supply	(-5.0V)	3	6	6	6	mV/V	PORR
switching transient peak-to-peak amplitude	$f_S = 2MHz$	8	13	13	16	mV_{pp}	HTA
track-to-hold settling time	to 1mV	5	13	7	8	ns	HTS
HOLD-TO-TRACK SWITCHING							
acquisition time to 0.1%	$V_{IN} = 2V_{pp}$, $R_L = 100\Omega$	20	31	24	32	ns	ATS
to 0.01%		25	36	31	36	ns	ATSP
DC ACCURACY							
*gain	1kHz, $4V_{pp}$, no load	0.997	0.993	0.995	0.995	V/V	G
temperature coefficient		15	40	40	40	ppm/°C	DG
non-linearity		0.005	0.025	0.020	0.020	%	GNL
*offset voltage		15	55	40	50	mV	VIO
* temperature coefficient	endpoint average	50	150	150	150	μV/°C	DVIO
*power supply rejection ratio		52	40	45	45	dB	PSRR
DIGITAL INPUT							
differential input threshold	$\lvert V_{TRACK} - V_{HOLD} \rvert$ (min.)		250	250	250	mV	VDIF
input bias current	logic HIGH	15	60	30	35	μA	IIH
	logic LOW	35	125	65	65	μA	IIL
ANALOG INPUT							
input voltage range[2]			±2.2	±2.2	±2.2	V	VI
input resistance		150	50	85	85	kΩ	RIN
input capacitance		3.5	5.5	5.5	5.5	pF	CIN
*input bias current		10	34	34	34	μA	IB
ANALOG OUTPUT							
*output resistance	at 1kHz	0.2	0.5	0.5	0.5	Ω	RO
POWER REQUIREMENTS							
*supply current ($+V_{CC1}$ and $+V_{CC2}$)	$V_{IN} = 0V$, track mode, no load	50	64	64	64	mA	ICC
*supply current ($-V_{EE1}$ and $-V_{EE2}$)	$V_{IN} = 0V$, track mode, no load	65	81	81	81	mA	IEE
*supply current ($+V_C$)	$V_{IN} = 0V$, track mode, no load	15	17	17	18	mA	I15
power dissipation	$V_{IN} = 0V$, track mode, no load	0.80	0.98	0.98	0.995	W	PD

MTBF is 2.22 million hours (A8C version, GF@70°C case, per MIL-HDBK-217E)

NOTES:

1. Parameters preceded by an * are the final electrical test parameters and are 100% tested. A8C units are tested at -55°C (power stable), +25°C (low-duty cycle pulse testing), and +125°C (low-duty cycle pulse testing). AI units are tested only at +25°C, although their performance is guaranteed at -25°C and +85°C as indicated above.
2. For optimum performance, the differential voltage between the input and the output should not exceed 3V in HOLD mode.
3. Absolute Maximum Ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.
4. Junction-to-Case temperature rise is approximately 16°C; $\theta_{CA} = 35°C/W$

Recommended Operating Conditions

supply voltage	$+V_{CC1}$ and $+V_{CC2}$	+5.0V (+4.5V min)
	$-V_{EE1}$ and $-V_{EE2}$	-5.0V (-4.5V min)
	$+V_C$	+11.0V to +15.75V
	$-V_{EE}$	-5.0V ± 5%
ANALOG to DIGITAL ground differential		10mV
analog input voltage range[2]		±2.2V
input to output differential voltage		3V
HOLD input voltage range		-0.75V to -1.9V
HOLD to V_{TRACK} differential voltage		0.6V
HOLD signal rise/fall time		<16ns

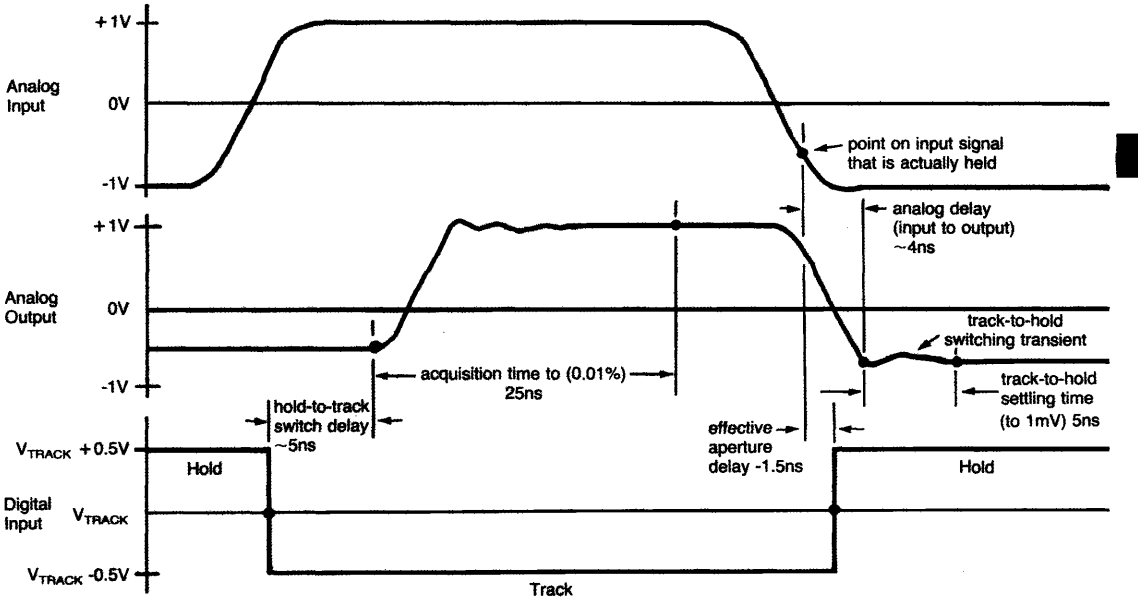
Protected under one or more of the following patents: 4,358,739; 4,502,020; 4,628,279; 4,639,685; 4,713,628; 4,757,275; 4,766,367; 4,780,689

Absolute Maximum Ratings[3]

supply voltage	$+V_{CC1}$ and $+V_{CC2}$	0V to +7.0V
	$-V_{EE1}$ and $-V_{EE2}$	-7.0V to 0V
	$+V_C$	+20V
	$-V_{EE}$	-7.0V to +3.0V
ANALOG to POWER ground differential		200mV
analog input voltage range		$-V_{EE1}$ to $+V_{CC1}$
V_{TRACK} and HOLD voltage range		$(V_{EE1}+2V)$ to $(V_{CC1}-2V)$
Output Current		±50mA continuous
Power Dissipation[4]		see thermal model
Junction Temperature		+175°C
Operating Temperature Range		
CLC942AI		-25°C to +85°C
CLC942A8		-55°C to +125°C
Storage Temperature Range		-65°C to +150°C
Lead Solder Duration (+300°C)		10 sec

Comlinear reserves the right to change specifications without notice.

Typical TRACK-and-HOLD Waveforms



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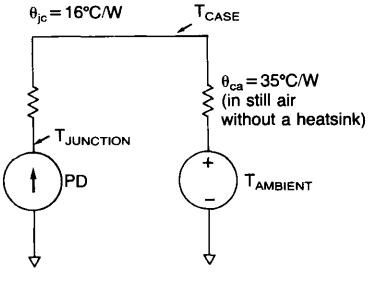
Thermal Model



$PD = |(I_{CC})\ (V_{CC})| + |(I_{EE})\ (V_{EE})|$

$\theta_{ca} = \theta_{cs} + \theta_{sa}$ (with heatsink)

Where θ_{sa} = Heatsink-to-Ambient (°C/W);

θ_{cs} = Case-to-Heatsink (°C/W)

and usually $\theta_{sa} >> \theta_{cs}$,

therefore θ_{ca} (with heatsink) $\approx \theta_{sa}$

$T_{junction} = T_{ambient} + (\theta_{jc}+\theta_{ca})\ PD = T_{ambient} + (\theta_{ja})\ PD$

where $\theta_{ja} = \theta_{jc} + \theta_{ca}$

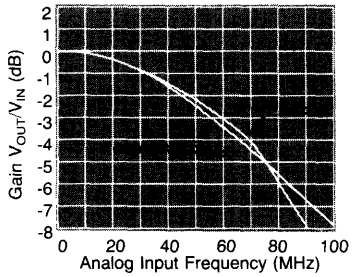
or

$T_{junction} = T_{case} + (\theta_{jc})\ PD$,

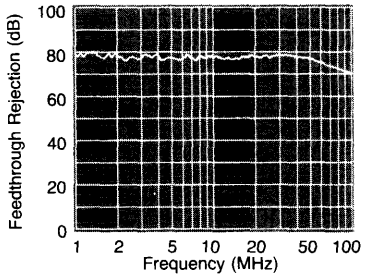
where in either case $T_{junction} < T_{junction}$ (max)

Typical Perfromance Characteristics ($T_A = +25°C$; $R_L = 100\Omega$; $+V_{CC1,2} = +5.0V$; $-V_{EE1,2} = -5.0V$; $+V_C = +15V$)

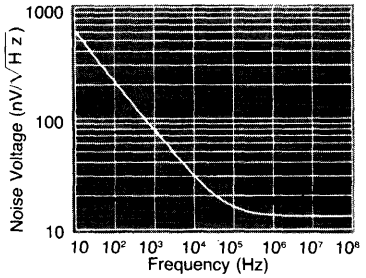
Voltage Gain vs. Frequency



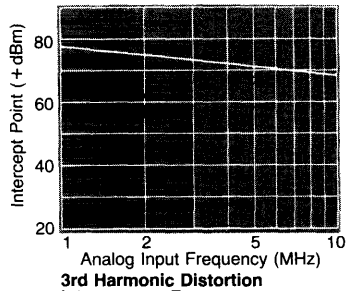
Feedthrough Rejection vs. Frequency



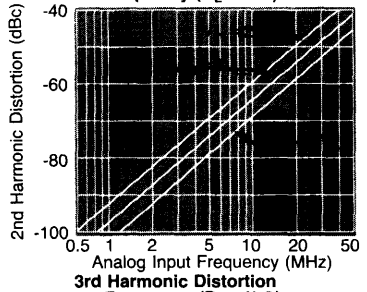
Equivalent Input Noise Voltage



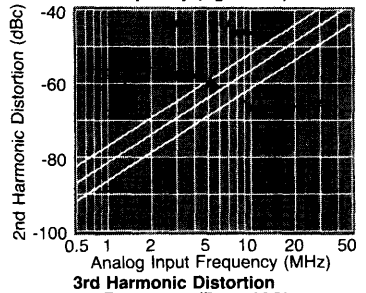
2nd Harmonic Distortion Intercept vs. Frequency



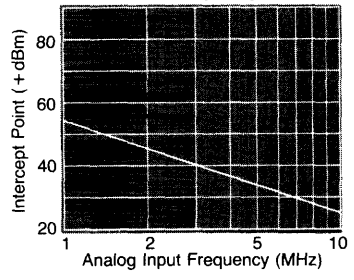
2nd Harmonic Distortion vs. Frequency ($R_L = 1k\Omega$)



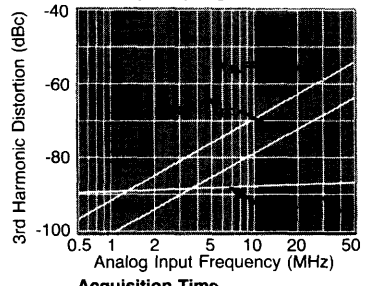
2nd Harmonic Distortion vs. Frequency ($R_L = 100\Omega$)



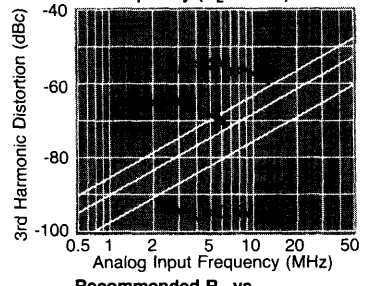
3rd Harmonic Distortion Intercept vs. Frequency



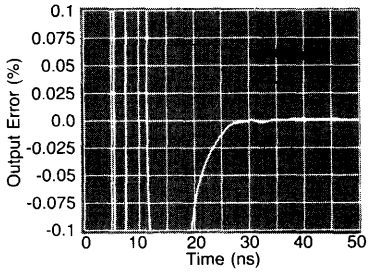
3rd Harmonic Distortion vs. Frequency ($R_L = 1k\Omega$)



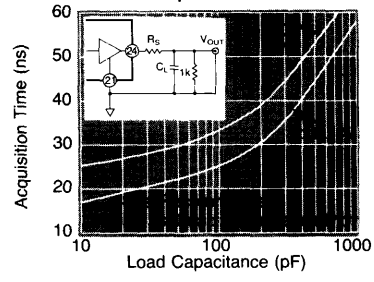
3rd Harmonic Distortion vs. Frequency ($R_L = 100\Omega$)



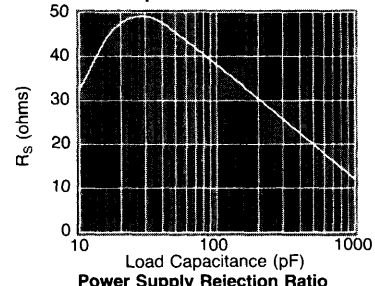
Acquisition Time



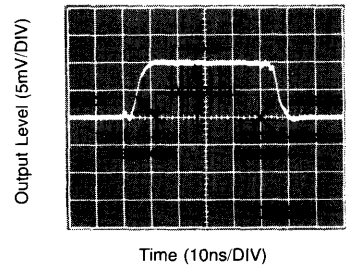
Acquisition Time vs. Load Capacitance



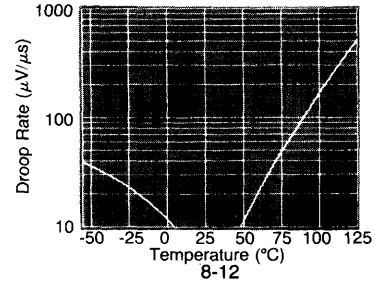
Recommended R_S vs. Load Capacitance



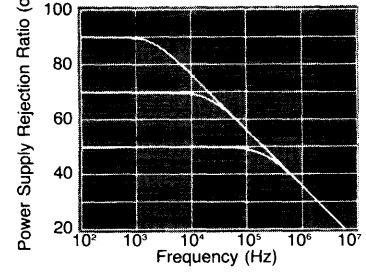
Switching Transients and Pedestal



Droop Rate vs. Temperature



Power Supply Rejection Ratio vs. Frequency



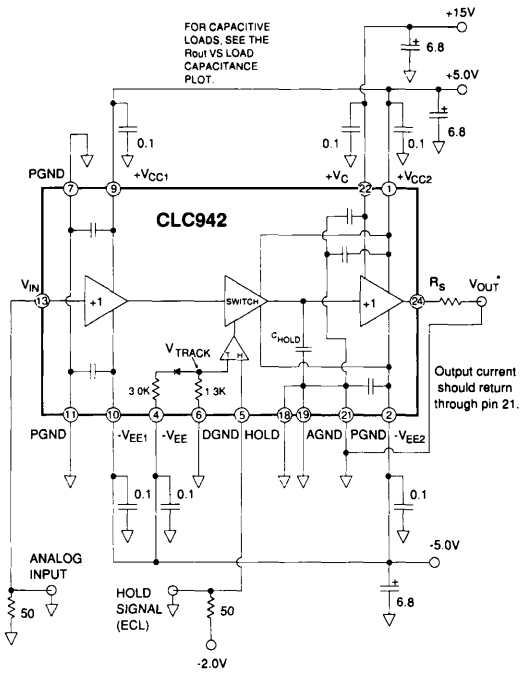


Figure 1: recommended CLC942 application circuit

Layout Considerations

For optimum performance from any precision, high-speed, track-and-hold, such as the CLC942, a high-quality printed circuit board layout is required. The main facet of the printed circuit board is a substantial ground plane around and under the CLC942. The ground plane will serve two main purposes, that of partially shielding the CLC942 from other system signals, as well as providing both power supply and signal return paths.

The input and output signals of the CLC942 should be controlled impedance transmission line such as stripline or micro-stripline for optimum performance (including the use of surface-mount termination components). In any case, as much attention must be paid to the ground return path as to the signal path itself. In general, a ground path at least 250 mils wide should provide an adequate ground return, but the stripline techniques are strongly recommended for high-frequency applications.

All supply lines to the CLC942 should be individually decoupled with 0.1μF capacitors. These decoupling capacitors should be located as close to the supply pins as possible. In addition, the decoupling capacitor lead lengths must also be kept to a minimum to avoid any effects from lead inductance. A better solution is the use of chip capacitors located right at the supply pins.

The use of sockets is not recommended with the CLC942, in that they tend to increase lead-to-lead capacitance as well as lead inductance, both degrading performance. If sockets must be used, low-profile Teflon types or individual "pin" sockets are preferred.

Track/Hold Switching Control

At the heart of the CLC942 is an active bipolar transistor bridge circuit. This bridge circuit allows the input signal to pass through to the HOLD capacitor during the signal acquisition mode, and isolates the HOLD capacitor during the HOLD mode. A differential driver circuit determines the state of the bridge circuit, either "open" or "closed."

In normal mode, only the HOLD side of the bridge driver circuit is used. With the resistor diode network between pins 4 and 6 of the CLC942 bias as in figure 1, the HOLD input (pin 5) responds to standard 10K and 10KH ECL signals. At room temperature, 100K ECL logic family devices may also work with the CLC942, but their use is not guaranteed nor recommended.

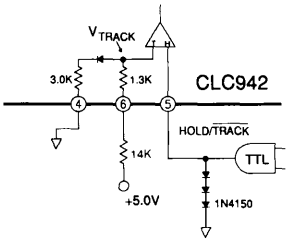


Figure 2: TTL compatible driver circuit

By re-biasing the resistor/diode network between pins 4 and 6, the CLC942 will respond to standard TTL level logic families (Figure 2). The resistors tied to pin 6 and +5.0V, effectively raises the internal threshold level to +1.4V for use with TTL compatible devices. The three series diodes on pin 5 provide over-voltage protection for the inputs of the bridge driver circuit. For optimum dynamic performance from the CLC942, use of the more modern TTL families is recommended, such as the "AS" or "F" series.

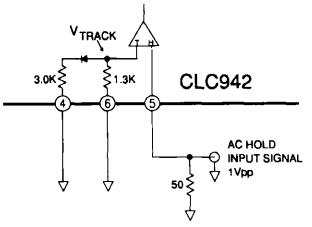


Figure 3: "ground" referenced driver circuit

The resistor/diode network can be further modified for operation with "ground" referenced ac signals. Figure 3 illustrates the required connections, which amount to connecting both pins 4 and 6 to ground. The CLC942 will then operate from a 1.0V_{pp} HOLD input signal. With the 50Ω input termination resistor, the HOLD control signal can be either dc or ac coupled.

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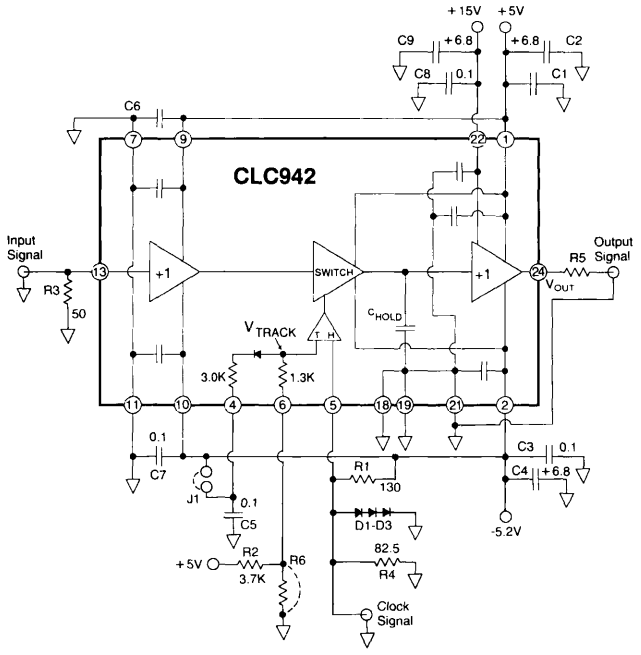
CLC942 Evaluation Board

An evaluation board is available for the CLC942. The board is user-configurable for either TTL, ECL, or "ac-signal" control. Operational details are available below, and the bare board is available from Comlinear Corp. as part number 730017.



CLC942 Evaluation Board Schematic

Configuration Table

Mode	D1-D3	J1	R1	R2	R4	R6
ECL	none	short	130	NC	82.5	short
TTL	used	open	open	3.9k	open	1.5k
GND Ref.	none	open	open	NC	50	short

NC – Not Critical

Parts List

Resistors:

R1	130Ω
R2	3.9kΩ
R3	50Ω *(suggested)*
R4	82.5Ω/50Ω
R5	see "Recomm. R_S" plot
R6	1.5kΩ

Diodes:

D1-D3 1N4150

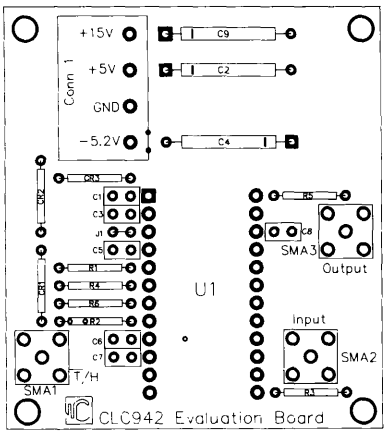
Capacitors: (35V, +80%| -20%)

C1	0.1μF ceramic radial lead
C2	6.8μF(Sprague 150D Series)
C3	0.1μF ceramic radial lead
C4	6.8μF(Sprague 150D Series)
C5	0.1μF ceramic radial lead
C6	0.1μF ceramic radial lead
C7	0.1μF ceramic radial lead
C8	0.1μF ceramic radial lead
C9	6.8μF(Sprague 150D Series)

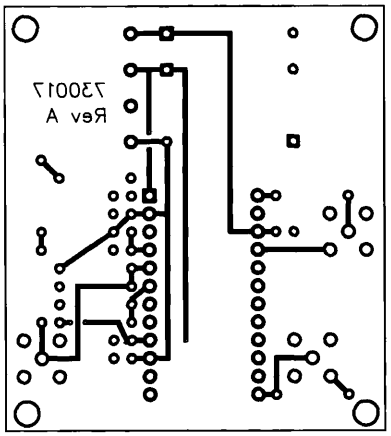
Hardware: (Optional)

SMA Connectors
- Amphenol 901-144 (straight)
- Amphenol 901-143 (angled)

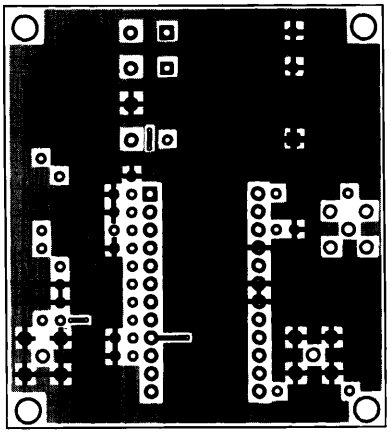
"Sockets"
- Cambion flush mount connector jacks 450-2598-01-06-00



Component Placement Guide



Solder Side (viewed from top)



Component Side (viewed from top)