

8/16-bit Data Bus Static RAM Card

Connector Type

Two-piece 68-pin

MF365A-L2DATXX
MF365A-L9DATXX
MF3129-L2DATXX
MF3129-L9DATXX
MF3527-L2DATXX
MF3527-L9DATXX
MF3513-L2DATXX
MF3513-L9DATXX
MF31M1-L2DATXX
MF31M1-L9DATXX
MF32M1-L2DATXX
MF32M1-L9DATXX

DESCRIPTION

Mitsubishi's static RAM cards provide large memory capacities on a device approximately the size of a credit card (85.6mm×54mm×3.3mm). The cards use an 8/16-bit data bus. The devices use a replaceable lithium battery to maintain data. Available in 64 K byte - 2 M byte capacities, Mitsubishi's Static RAM cards are available with a 68-pin, two-piece connector.

- Electrostatic discharge protection to 15kV
- Buffered interface
- 68-pin connector
- 8-bit and 16-bit data bus width
- Write protect switch
- Battery voltage pin
- JEIDA Ver4.0/4.1 (PCMCIA2.0) compatible

FEATURES

- Uses TSOP (Thin Small Outline Package) to achieve very high memory density coupled with high reliability, without enlarging card size.

APPLICATIONS

- Office automation
- Data Communications
- Computers
- Industrial
- Telecommunications
- Consumer

PRODUCT LIST

Type name	Item	Memory capacity	Low power	Attribute memory	Auxiliary battery	Memory organization	Outline drawing		
MF365A-L2DATXX		64KB	NO	NO	NO	256K bit SRAM×2	68P-003		
MF3129-L2DATXX		128KB				256K bit SRAM×4			
MF3257-L2DATXX		256KB				1M bit SRAM×2			
MF3513-L2DATXX		512KB				1M bit SRAM×4			
MF31M1-L2DATXX		1MB				1M bit SRAM×8			
MF32M1-L2DATXX		2MB				1M bit SRAM×16			
MF365A-L9DATXX		64KB	YES						256K bit SRAM×2
MF3129-L9DATXX		128KB							256K bit SRAM×4
MF3257-L9DATXX		256KB							1M bit SRAM×2
MF3513-L9DATXX		512KB							1M bit SRAM×4
MF31M1-L9DATXX		1MB							1M bit SRAM×8
MF32M1-L9DATXX		2MB							1M bit SRAM×16

PIN ASSIGNMENT

Two-Piece Type (68-pin)

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	GND	Ground	35	GND	Ground
2	D 3	Data I/O	36	CD 1	Card detect 1
3	D 4		37	D11	Data I/O
4	D 5		38	D12	
5	D 6		39	D13	
6	D 7		40	D14	
7	CE 1	Card enable 1	41	D15	
8	A10	Address input	42	CE 2	Card enable 2
9	OE	Output enable	43	NC	No connection
10	A11	Address input	44	NC	
11	A 9		45	NC	
12	A 8		46	A17	Address input
13	A13		47	A18	
14	A14		48	A19	
15	WE	Write enable	49	A20	
16	NC	No connection	50	NC	No connection
17	VCC	Power supply voltage	51	VCC	Power supply voltage
18	NC	No connection	52	NC	No connection
19	A16	A16 (NC for 64KB type)	53	NC	
20	A15	Address input	54	NC	
21	A12		55	NC	
22	A 7		56	NC	
23	A 6		57	NC	
24	A 5	Address input	58	NC	No connection
25	A 4		59	NC	
26	A 3		60	NC	
27	A 2		61	REG	REG function
28	A 1		62	BVD 2	Battery voltage detect 2
29	A 0	Data I/O	63	BVD 1	Battery voltage detect 1
30	D 0		64	D 8	Data I/O
31	D 1		65	D 9	
32	D 2	Write protect	66	D10	
33	WP		67	CD 2	Card detect 2
34	GND	Ground	68	GND	Ground

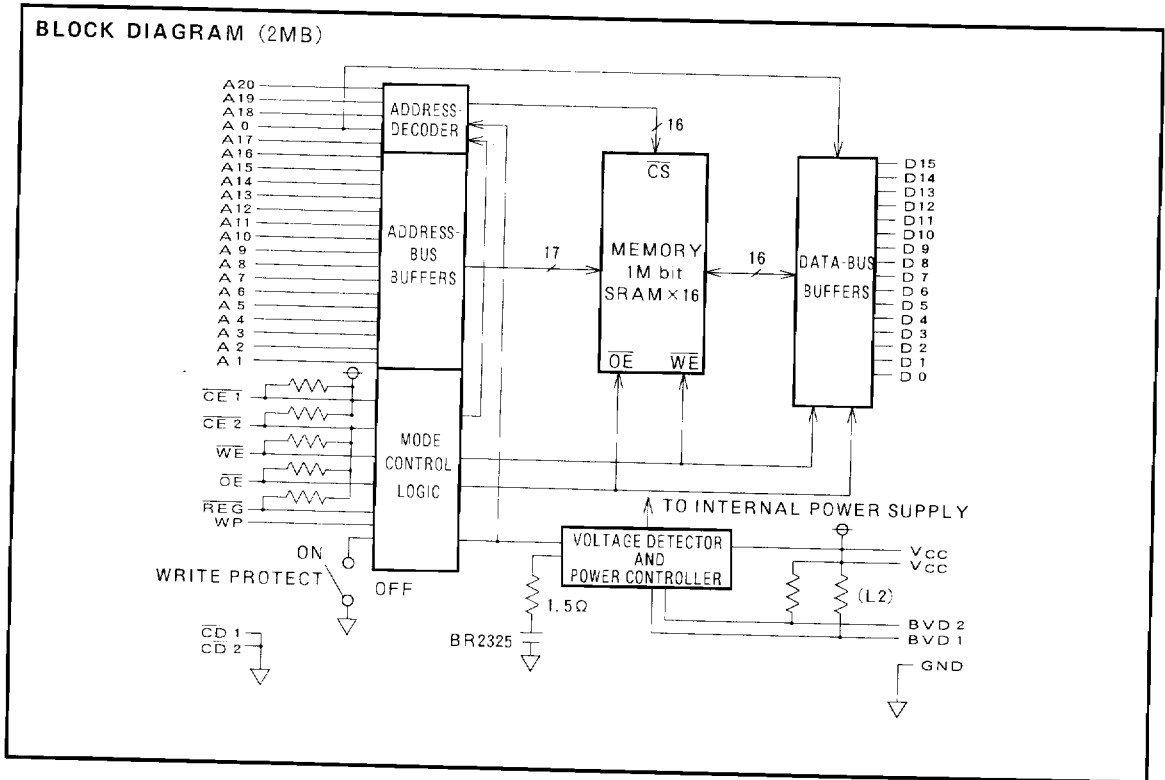
WRITE PROTECT MODE (WP)

When the write protect switch is switched on, this card goes into a write protect mode that allows reading but not writing of data.

In this mode, the WP pin is set to "H" level when V_{CC} is applied.

At shipment the write protect switch is switched off (Normal mode : The card can be written ; WP pin set to "L" level).

STATIC RAM CARDS



FUNCTION TABLE

Mode	REG	CE1	CE2	OE	WE	A0	D15~D8	D7~D0	I _{cc}
Standby	X	H	H	X	X	X	High impedance	High impedance	Standby
Read A (16-bit) common	H	L	L	L	H	X	Odd byte data out	Even byte data out	Active
Write A (16-bit) common	H	L	L	H	L	X	Odd byte data in	Even byte data in	Active
Read B (8-bit) common	H	L	H	L	H	L	High-impedance	Even byte data out	Active
Write B (8-bit) common	H	L	H	H	L	L	High-impedance	Odd byte data out	Active
Read C (8-bit) common	H	H	L	L	H	X	High-impedance	Even byte data in	Active
Write C (8-bit) common	H	H	L	H	L	X	High-impedance	Odd byte data in	Active
Output disable	X	X	X	H	H	X	High-impedance	High-impedance	Active
Read A (16-bit) attribute	L	L	L	L	H	X	Data out (not valid)	Data out (FFh)	Active
Read B (8-bit) attribute	L	L	H	L	H	L	High-impedance	Data out (FFh)	Active
Read C (8-bit) attribute	L	H	L	L	H	X	High-impedance	Data out (not valid)	Active
	L	H	L	L	H	X	Data out (not valid)	High-impedance	Active

Note 1 : H = V_{IH}, L = V_{IL}, X = V_{IH} or V_{IL}

STATIC RAM CARDS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to GND	-0.3~0.6	V
V _I	Input voltage		-0.3~V _{CC} +0.3	V
V _O	Output voltage		0~V _{CC}	V
T _{opr 1}	Operating temperature 1	Read, Write, Operation	0~70	°C
T _{opr 2}	Operating temperature 2	Data retention	0~70	°C
T _{stg}	Storage temperature		-30~80	°C

RECOMMENDED OPERATING CONDITIONS (T_a = 0~55°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V _{CC}	V _{CC} supply voltage	4.75	5.0	5.25	V
GND	System ground		0		V
V _{IH}	High input voltage	2.4		V _{CC}	V
V _{IL}	Low input voltage	0		0.8	V

ELECTRICAL CHARACTERISTICS (T_a = 0~55°C, V_{CC} = 4.75~5.25V unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V _{OH}	High output voltage	I _{OH} = -0.1mA, BVD 1, 2 (L 2)	2.4			V
		I _{OH} = -1.0mA, Other outputs	2.4			
V _{OL}	Low output voltage	I _{OL} = 2mA			0.4	V
I _{IH}	High input current	V _I = V _{CC} V			10	μA
I _{IL}	Low input current	V _I = 0 V	-10		-70	μA
		CE 1, CE 2, WE, OE, REG Other inputs			-10	
I _{OZH}	High output current in state	CE 1 = CE 2 = V _{IH} or OE = V _{IH} or WE = V _{IL} , V _O = V _{CC}			10	μA
I _{OZL}	Low output current in off state	CE 1 = CE 2 = V _{IH} or OE = V _{IH} or WE = V _{IL} , V _O = 0 V			-10	μA
I _{CC 1 • 1}	Active supply current 1 (L 2)	CE 1 = CE 2 = V _{IL} , other inputs V _{IH} or V _{IL} , Outputs=open			220	mA
	Active supply current (L 9)	CE 1 = CE 2 = V _{IL} , other inputs V _{IH} or V _{IL} , Outputs=open			200	
I _{CC 1 • 2}	Active supply current 2 (L 2)	CE 1 = CE 2 ≤ 0.2V, other inputs ≤ 0.2V or ≥ V _{CC} - 0.2V, Outputs=open			200	mA
	Active supply current 2 (L 9)	CE 1 = CE 2 ≤ 0.2V, other inputs ≤ 0.2V or ≥ V _{CC} - 0.2V, Outputs=open			180	
I _{CC 2 • 1}	Standby supply current (L 2)	CE 1 = CE 2 = V _{IH} , other inputs = V _{IH} or V _{IL} , Outputs=open			12	mA
	Standby supply current (L 9)	CE 1 = CE 2 = V _{IL} , other inputs V _{IH} or V _{IL} , Outputs=open			10	
I _{CC 2 • 2}	Standby supply current (L 2)	CE 1 = CE 2 ≥ V _{CC} - 0.2V, other inputs ≤ 0.2V or ≥ V _{CC} - 0.2V			5	mA
	Standby supply current (L 9)	CE 1 = CE 2 ≥ V _{CC} - 0.2V, other inputs ≤ 0.2V or ≥ V _{CC} - 0.2V		0.30	0.65	
V _{BDET 1}	Battery detect reference voltage 1 *	V _{CC} = 5 V, T _a = 25°C	2.27	2.37	2.47	V
V _{BDET 2}	Battery detect reference voltage 2 *	V _{CC} = 5 V, T _a = 25°C	2.55	2.65	2.75	V

Note 2 : Currents flowing into the IC are taken as positive (unsigned).

3 : Typical values are measured at V_{CC} = 5 V, T_a = 25°C.

*Pin asserted when battery voltage drops below specified level.

STATIC RAM CARDS

CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
C _I	Input capacitance	V _I =GND, V _I =25mVrms, f=1 MHz, T _a =25°C			45	pF
C _O	Output capacitance	V _O =GND, V _O =25mVrms, f=1 MHz, T _a =25°C			45	pF

Note 4 : These parameters are not 100% tested.

SWITCHING CHARACTERISTICS

Read Cycle (T_a= 0 ~55°C, V_{CC}=4.75~5.25V, unless otherwise noted)

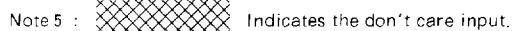
Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _{CR}	Read cycle time	200			ns
t _{a(A)}	Address access time			200	ns
t _{a(CE)}	Card enable access time			200	ns
t _{a(OE)}	Output enable access time			100	ns
t _{dis(CE)}	Output disable time (from CE)			90	ns
t _{dis(OE)}	Output disable time (from OE)			90	ns
t _{en(CE)}	Output enable time (from CE)	5			ns
t _{en(OE)}	Output enable time (from OE)	5			ns
t _{V(A)}	Data valid time after address change	0			ns

TIMING REQUIREMENTS

Write Cycle (T_a= 0 ~55°C, V_{CC}=4.75~5.25V, unless otherwise noted)

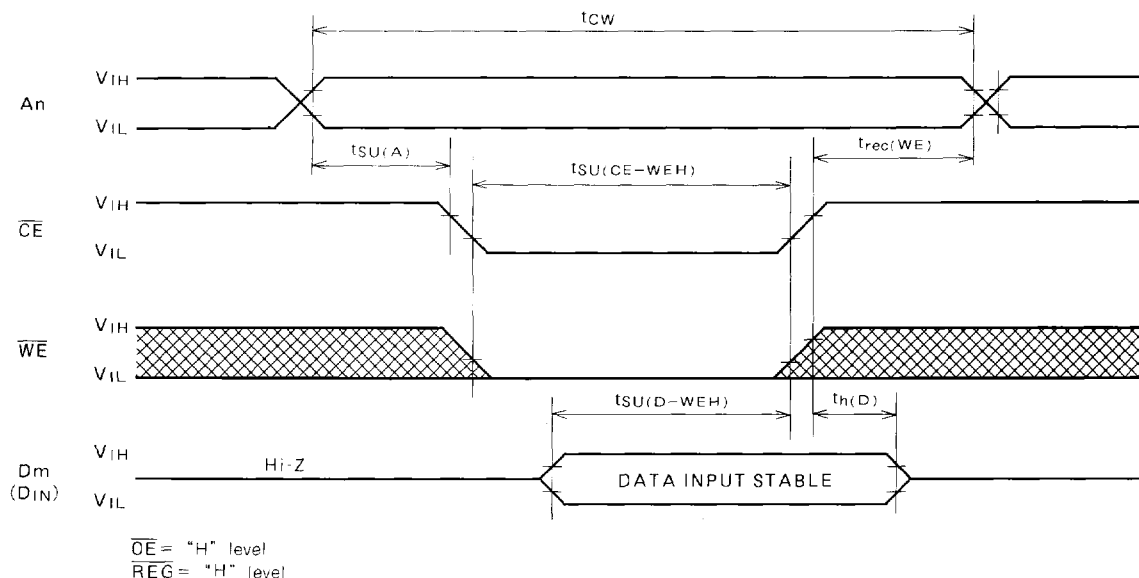
Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _{CW}	Write cycle time	200			ns
t _{w(WE)}	Write pulse width	120			ns
t _{SU(A)}	Address setup time	20			ns
t _{SU(A-WEH)}	Address setup time with respect to WE high	140			ns
t _{SU(CE-WEH)}	Card enable setup time with respect to WE high	140			ns
t _{SU(D-WEH)}	Data setup time with respect to WE high	60			ns
t _{h(D)}	Data hold time	30			ns
t _{rec(WE)}	Write recovery time	30			ns
t _{dis(WE)}	Output disable time (from WE)			90	ns
t _{dis(OE)}	Output disable time (from OE)			90	ns
t _{en(WE)}	Output enable time (from WE)	5			ns
t _{en(OE)}	Output enable time (from OE)	5			ns
t _{SU(OE-WE)}	OE setup time with respect to WE low	10			ns
t _{h(OE-WE)}	OE hold time with respect to WE high	10			ns

Read Cycle



STATIC RAM CARDS

Write Cycle ($\overline{CE}$ control)



SWITCHING CHARACTERISTICS (Attribute)

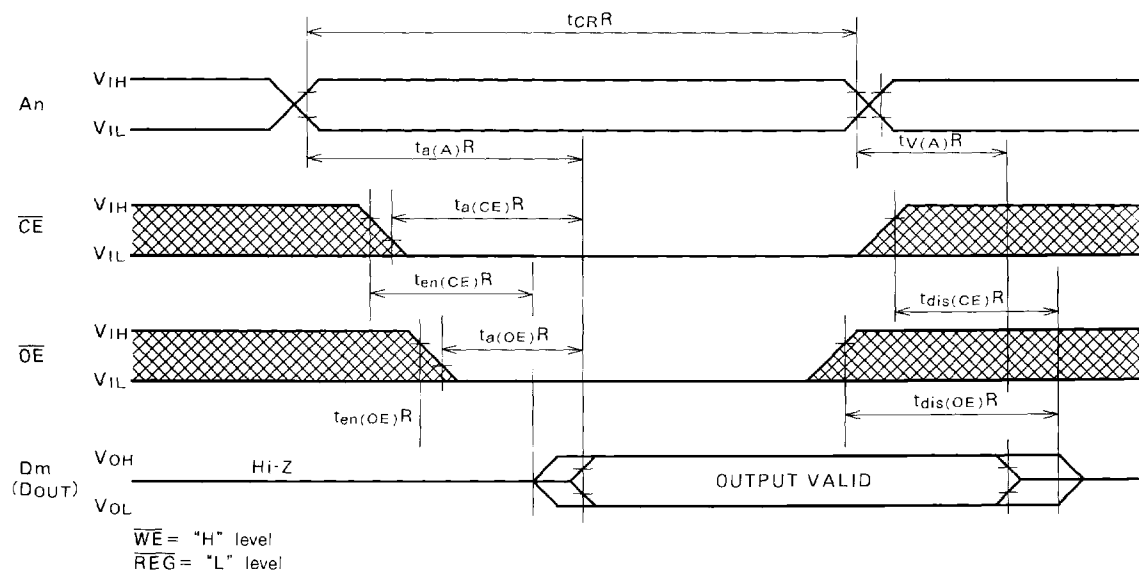
Read Cycle ($T_a = 0 \sim 55^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$, V_i unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{CR}R$	Read cycle time	300			ns
$t_{a(A)}R$	Address access time			300	ns
$t_{a(CE)}R$	Card select access time			300	ns
$t_{a(OE)}R$	Output enable access time			150	ns
$t_{dis(CE)}R$	Output disable time (from $\overline{CE}$)			100	ns
$t_{dis(OE)}R$	Output disable time (from $\overline{OE}$)			100	ns
$t_{en(CE)}R$	Output enable time (from $\overline{CE}$)	5			ns
$t_{en(OE)}R$	Output enable time (from $\overline{OE}$)	5			ns
$t_{V(A)}R$	Data valid time after address change	0			ns

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TIMING DIAGRAM (Attribute)

Read Cycle



Note 6 : Test Conditions

Input pulse levels : $V_{IL}=0.4V$, $V_{IH}=2.8V$

Input pulse rise, fall time : $t_r=t_f=10ns$

Reference voltage

Input : $V_{IL}=0.8V$, $V_{IH}=2.4V$

Output : $V_{OL}=0.8V$, $V_{OH}=2.0V$

(t_{en} and t_{dis} are measured when output voltage is $\pm 500mV$ from steady state.)

Load : 100pF + 1 TTL gate

5 pF + 1 TTL gate (at t_{en} and t_{dis} measuring)

7 : The data write is performed during the interval when both $\overline{CE}$ and $\overline{WE}$ are low.

8 : Don't apply inverted phase signal externally when Dm pin is in output mode.

9 : $\overline{CE}$ is indicated as follows :

Read A/Write A : $\overline{CE} = \overline{CE1} = \overline{CE2}$

Read B/Write B : $\overline{CE} = \overline{CE1}$, $\overline{CE2}$ = "H" level

Read C/Write C : $\overline{CE} = \overline{CE2}$, $\overline{CE1}$ = "H" level

STATIC RAM CARDS

ELECTRICAL CHARACTERISTICS

BATTERY BACKUP ($T_a = 0 \sim 55^\circ\text{C}$, unless otherwise noted)

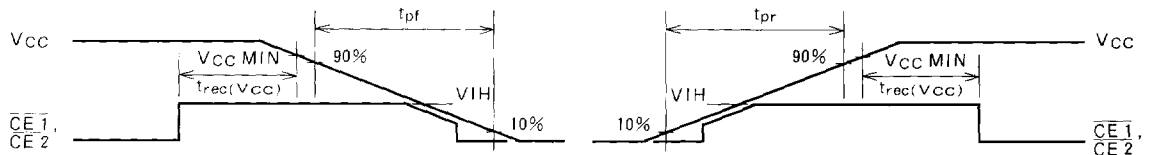
Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{BATT}	Back-up enable battery voltage	All pins open	2.6			V
$V_{I(CE)}$	Card enable voltage	$2.4\text{V} \leq V_{CC} \leq 5.25\text{V}$ $0\text{V} \leq V_{CC} < 2.4\text{V}$	2.4 $V_{CC}-0.1$	V_{CC}	$V_{CC}+0.1$	V
$I_{CC(BUP)}$	Battery back-up supply current	All pins open, $V_{BATT} = 3\text{V}$, $T_a = 25^\circ\text{C}$	64KB		3	μA
			128KB		5	
			256KB		3	
			512KB		5	
			1MB		9	
			2MB		17	
$I_{CC(BUP)}$	Battery back-up supply current	All pins open, $V_{BATT} = 3\text{V}$	64KB		40	μA
			128KB		70	
			256KB		100	
			512KB		200	
			1MB		400	
			2MB		800	

TIMING REQUIREMENTS ($T_a = 0 \sim 55^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{pr}	Power supply rise time	0.1		300	ms
t_{pf}	Power supply fall time	3		300	ms
$t_{su}(V_{CC})$	Set up time at power on	20			ms
$t_{rec}(V_{CC})$	Recovery time at power off	1000			ns

CARD INSERTION/REMOVAL TIMING DIAGRAM

$V_{CC\text{ MIN}}$ means Minimum Operating Voltage = 4.75V.



Note 10 : The battery must not be removed unless V_{CC} is present, otherwise all data will be lost.

BATTERY SPECIFICATIONS

A replaceable battery (type BR2325) with a capacity of 165mAh is used :

Estimated battery life when the card is left continuously without external power.

MF365A-L2DATXX	MF365A-L9DATXX	5.9years
MF3129-L2DATXX	MF3129-L9DATXX	3.6years
MF3257-L2DATXX	MF3257-L9DATXX	5.9years
MF3513-L2DATXX	MF3513-L9DATXX	3.6years
MF31M1-L2DATXX	MF31M1-L9DATXX	2.0years
MF32M1-L2DATXX	MF32M1-L9DATXX	1.1years

Conditions

Temperature : 25°C

Humidity : 60%RH