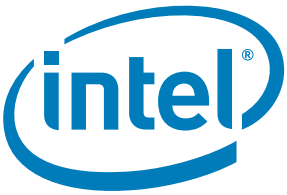

Intel StrataFlash® Cellular Memory (M18)

Datasheet

Product Features

- High-Performance Read, Program and Erase
  - 96 ns initial read access
  - 512-Mbit, 1-Gbit device: 108 MHz with zero wait-state synchronous burst reads: 7 ns clock-to-data output
  - 256-Mbit device: 133 MHz with zero wait-state synchronous burst reads: 5.5 ns clock-to-data output
  - 8-, 16-, and continuous-word synchronous-burst Reads
  - Programmable WAIT configuration
  - Customer-configurable output driver impedance
  - Buffered Enhanced Factory Programming: 3.2 µs/Word (typ), 65 nm; 4.2 µs/Word (typ), 90 nm
  - Block Erase: 0.9 s per block (typ)
  - 20 µs (typ) program suspend
  - 20 µs (typ) erase suspend
- Architecture
  - 16-bit wide data bus
  - Multi-Level Cell Technology
  - Symmetrically-Blocked Array Architecture
  - 256-Kbyte Erase Blocks
  - 1-Gbit device: Eight 128-Mbit partitions
  - 512-Mbit device: Eight 64-Mbit partitions
  - 256-Mbit device: Eight 32-Mbit partitions.
  - Read-While-Program and Read-While-Erase
  - Status Register for partition/device status
  - Blank Check feature
- Quality and Reliability
  - Expanded temperature: –30 °C to +85 °C
  - Minimum 100,000 erase cycles per block
  - ETOX™ X Process Technology (65 nm)
  - ETOX™ IX Process Technology (90 nm)
- Power
  - Core voltage: 1.7 V - 2.0 V
  - I/O voltage: 1.7 V - 2.0 V
  - Standby current: 70 µA (typ), 65 nm
  - Standby current: 50 µA (typ), 90 nm
  - Deep Power-Down mode: 2 µA (typ)
  - Automatic Power Savings mode
  - 16-word synchronous-burst read current: 23 mA (typ) @ 108 MHz
- Software
  - Intel® Flash Data Integrator (Intel® FDI) optimized
  - Basic Command Set and Extended Command Set compatible
  - Common Flash Interface
- Security
  - OTP Registers: 64 unique pre-programmed bits 2112 user-programmable bits
  - Absolute write protection with V_{PP} = GND
  - Power-transition erase/program lockout
  - Individual zero-latency block locking
  - Individual block lock-down
- Density and Packaging
  - Density: 1 Gbit, 512 Mbit, 256 Mbit
  - Address-data multiplexed and non-multiplexed interfaces
  - x16D (105-ball) Flash SCSP
  - x16C (107-ball) Flash SCSP
  - 0.8 mm pitch lead-free solder-ball

Document Number: 309823-005US
November 2006

Contents

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Revision History

Date	Revision	Description
14-April-06	001	Initial Release
28-April-06	002	Updated the template (naming and branding). On the cover page, changed BEFP from 1.6 µs/byte (typ) to 3.2 µs/Word (typ).
20-June-06	003	Correced the BEFP on the cover page to read 3.2 µs/Word and synchronized the BEFP on the cover with that in Table 22, "Program-Erase Characteristics, 256-Mbit, 512-Mbit and 1-Gbit" on page 67. Added Figure 1, "Mechanical Specifications for x16D (105-ball) package (8x10x1.0 mm)" on page 15. Added the following part numbers to Table 7, "Ordering Information" on page 12: —PF48F6000M0Y0BE —PF38F6070M0Y0BE —PF38F6070M0Y0VE —PF48F6000M0Y1BE
October 2006	004	Removed information on the 90 nm Extended Flash Array (EFA) feature that is no longer supported.
November 2006	005	Revised to include 65 nm, 1-Gbit device information. Moved sections for Device ID, Additional Information, and Order Information to Functional Description chapter. Created a separate M18 Developer's Manual to include the following information: —Bus Interface —Flash Operations —Device Command Codes —Flow Charts —Common Flash Interface —Next State Table Removed line item PF5566MMY0C0 (512+512 M18 + 128 + 128 PSRAM) from Table 7, "Ordering Information" on page 12 and removed its package (8x11x1.4, x16C 107 ball). Added the following line items to Table 7, "Ordering Information" on page 12: —PF48F6000M0Y0BE, 65 nm —PF38F6070M0Y0BE, 65 nm —PF38F4060M0Y0B0 —PF58F0031M0Y1BE, 65 nm —PF38F6070M0Y0C0, 65 nm —PF38F4060M0Y0C0 —PF38F4060M0Y1C0 —PF38F6070M0Y0VE, 65 nm Added the following packages to support new line items: —8x10x1.0, x16D 105 ball —11x15x1.2, x16D 105 ball —11x11x1.2, x16C 107 ball —8x10x1.2, x16C 107 ball —10x11x1.2, x16SB 165 ball

1.0 Introduction

Intel StrataFlash® Cellular Memory (M18) is the 6th generation Intel StrataFlash® memory with multi-level cell (MLC) technology. It provides high-performance, low-power synchronous-burst read mode and asynchronous read mode at 1.8 V. It features flexible, multi-partition read-while-program and read-while-erase capability, enabling background programming or erasing in one partition simultaneously with code execution or data reads in another partition. The eight partitions allow flexibility for system designers to choose the size of the code and data segments. The Intel StrataFlash® Cellular Memory (M18) is manufactured using Intel 65 nm ETOX™ X and 90 nm ETOX™ IX process technology and is available in industry-standard chip-scale packaging.

1.1 Document Purpose

This document describes the specifications of the Intel StrataFlash® Cellular Memory (M18) device.

1.2 Nomenclature

Table 1. Definition of Terms

Term	Definition
1.8 V	Refers to VCC and VCCQ voltage range of 1.7 V to 2.0 V
Block	A group of bits that erase with one erase command
Main Array	A group of 256-KB blocks used for storing code or data
Partition	A group of blocks that share common program and erase circuitry and command status register
Programming Region	An aligned 1-KB section within the main array
Segment	A 32-byte section within the programming region
Byte	8 bits
Word	2 bytes = 16 bits
Kb	1024 bits
KB	1024 bytes
KW	1024 words
Mb	1,048,576 bits
MB	1,048,576 bytes

1.3 Acronyms

Table 2. List of Acronyms

Acronym	Meaning
APS	Automatic Power Savings
CFI	Common Flash Interface
DU	Don't Use
ECR	Enhanced Configuration Register (Flash)

Table 2. List of Acronyms

Acronym	Meaning
ETOX	EPROM Tunnel Oxide
FDI	Intel® Flash Data Integrator
RCR	Read Configuration Register (Flash)
RFU	Reserved for Future Use
SCSP	Stacked Chip Scale Package

1.4 Conventions

Table 3. Datasheet Conventions

Convention	Meaning
Group Membership Brackets	Square brackets are used to designate group membership or to define a group of signals with a similar function, such as A[21:1].
VCC vs. V_{CC}	When referring to a signal or package-connection name, the notation used is VCC. When referring to a voltage level, the notation used is subscripted such as V_{CC}.
Device	This term is used interchangeably throughout this document to denote either a particular die, or all die in the package.
F[3:1]-CE#, F[2:1]-OE#	This is the method used to refer to more than one chip-enable or output enable. When each is referred to individually, the reference is F1-CE# and F1-OE# (for die #1), and F2-CE# and F2-OE# (for die #2).
F-VCC	When referencing flash memory signals, the notation used is F-VCC or F-$V_{CC,}$ respectively.
00FFh	Denotes 16-bit hexadecimal numbers
00FF 00FFh	Denotes 32-bit hexadecimal numbers

2.0 Functional Description

The Functional Description includes the following sections:

- Product Overview
- Configuration and Memory Map
- Device ID
- Ordering Information
- Additional Information

2.1 Product Overview

The Intel StrataFlash® Cellular Memory (M18) device provides high read and write performance at low voltage on a 16-bit data bus.

The flash memory device has a multi-partition architecture with read-while-program and read-while-erase capability.

The device supports synchronous burst reads up to 108 MHz using ADV# address-latching on the following densities:

- 512-Mbit devices
- 1-Gbit devices

The device supports synchronous burst reads up to 133 MHz using CLK address-latching on the following densities:

- 256-Mbit devices

In continuous-burst mode, a data Read can traverse partition boundaries.

Upon initial power-up or return from reset, the device defaults to asynchronous array-read mode. Synchronous burst-mode reads are enabled by programming the Read Configuration Register. In synchronous burst mode, output data is synchronized with a user-supplied clock signal. A WAIT signal provides easy CPU-to-flash memory synchronization.

Designed for low-voltage applications, the device supports read operations with V_{CC} at 1.8 V, and erase and program operations with V_{PP} at 1.8 V or 9.0 V. VCC and VPP can be tied together for a simple, ultra-low power design. In addition to voltage flexibility, a dedicated VPP connection provides complete data protection when V_{PP} is less than V_{PPLK}.

A Status Register provides status and error conditions of erase and program operations.

One-Time-Programmable (OTP) registers allow unique flash device identification that can be used to increase flash content security. Also, the individual block-lock feature provides zero-latency block locking and unlocking to protect against unwanted program or erase of the array.

The flash memory device offers three power savings features:

- Automatic Power Savings (APS) mode: The device automatically enters APS following a read-cycle completion.
- Standby mode: Standby is initiated when the system deselects the device by deasserting CE#.
- Deep Power-Down (DPD) mode: DPD provides the lowest power consumption and is enabled by programming in the Enhanced Configuration Register. DPD is initiatied by asserting the DPD pin.

2.2 Configuration and Memory Map

The Intel StrataFlash® Cellular Memory device features a symmetrical block architecture. The flash device main array is divided as follows:

- The main array of the 256-Mbit device is divided into eight 32-Mbit partitions. Each parition is divided into sixteen 256-KByte blocks: 8 x 16 = 128 blocks in the main array of a 256-Mbit device.
- The main array of the 512-Mbit device is divided into eight 64-Mbit partitions. Each parition is divided into thirty-two 256-KByte blocks: 8 x 32 = 256 blocks in the main array of a 256-Mbit device.
- The main array of the 1-Gbit device is divided into eight 128-Mbit partitions. Each parition is divided into sixty-four 256-KByte blocks: 8 x 64 = 512 blocks in the main array of a 1-Gbit device.

Each block is divided into as many as two-hundred-fifty-six 1-KByte programming regions. Each region is divided into as many as thirty-two 32-Byte segments.

Table 4. Main Array Memory Map (Sheet 1 of 2)

		256-Mbit Device			512-Mbit Device			1-Gbit Device	
		Blk#	Address Range		Blk#	Address Range		Blk#	Address Range
Partition 7	32Mbit	127	0FE0000-0FFFFFF	64Mbit	255	1FE0000-1FFFFFF	128Mbit	511	3FE0000-3FFFFFF
		⋮	⋮		⋮	⋮		⋮	⋮
		112	0E00000-0E1FFFF		224	1C00000-1C1FFFF		448	3800000-381FFFF
Partition 6	32Mbit	111	0DE0000-0DFFFFF	64Mbit	223	1BE0000-1BFFFFF	128Mbit	447	37E0000-37FFFFF
		⋮	⋮		⋮	⋮		⋮	⋮
		96	0C00000-0C1FFFF		192	1800000-181FFFF		384	3000000-301FFFF
Partition 5	32Mbit	95	0BE0000-0BFFFFF	64Mbit	191	17E0000-17FFFFF	128Mbit	383	2FE0000-2FFFFFF
		⋮	⋮		⋮	⋮		⋮	⋮
		80	0A00000-0A1FFFF		160	1400000-141FFFF		320	2800000-281FFFF
Partition 4	32Mbit	79	09E0000-09FFFFF	64Mbit	159	13E0000-13FFFFF	128Mbit	319	27E0000-27FFFFF
		⋮	⋮		⋮	⋮		⋮	⋮
		64	0800000-081FFFF		128	1000000-101FFFF		256	2000000-201FFFF
Partition 3	32Mbit	63	07E0000-07FFFFF	64Mbit	127	0FE0000-0FFFFFF	128Mbit	255	1FE0000-1FFFFFF
		⋮	⋮		⋮	⋮		⋮	⋮
		48	0600000-061FFFF		96	0C00000-0C1FFFF		192	1800000-181FFFF
Partition 2	32Mbit	47	05E0000-05FFFFF	64Mbit	95	0BE0000-0BFFFFF	128Mbit	191	17E0000-17FFFFF
		⋮	⋮		⋮	⋮		⋮	⋮
		32	0400000-041FFFF		64	0800000-081FFFF		128	1000000-101FFFF

Table 4. Main Array Memory Map (Sheet 2 of 2)

		256-Mbit Device			512-Mbit Device			1-Gbit Device	
		Blk#	Address Range		Blk#	Address Range		Blk#	Address Range
Partition 1	32Mbit	31	03E0000-03FFFFF	64Mbit	63	07E0000-07FFFFF	128Mbit	127	0FE0000-0FFFFFF
		⋮	⋮		⋮	⋮		⋮	⋮
		16	0200000-021FFFF		32	0400000-041FFFF		64	0800000-081FFFF
Partition 0	32Mbit	15	01E0000-01FFFFF	64Mbit	31	03E0000-03FFFFF	128Mbit	63	07E0000-07FFFFF
		⋮	⋮		⋮	⋮		⋮	⋮
		0	0000000-001FFFF		0	0000000-001FFFF		0	0000000-001FFFF

2.3 Device ID

Table 5. Device ID codes, 90 nm

Density	Product	Device Identifier Code (Hex)
512 Mbit	Non-Mux	887E
	AD-Mux	8881
256 Mbit	Non-Mux	8901
	AD-Mux	8904

Table 6. Device ID codes, 65 nm

Density	Product	Device Identifier Code (Hex)
1 Gbit	Non-Mux	88B0
	AD-Mux	88B1

2.4 Ordering Information

For combinations not listed, please contact your local Intel sales office.

Table 7. Ordering Information

I/O Voltage	Flash (M18)		NAND	RAM	Package		Part Number
(V)	Density (Mbit), Bus	Speed: CLK and tACC	Density (Mbit), Bus	Density (Mbit), Type, Bus	Size (mm)	Ballout	
x16D Shared Bus, Non-Mux							
1.8	1024, Bus A	108 MHz 96 ns	—	—	8 x 10 x 1.0	x16D 105-ball	PF48F6000M0Y0BE 65 nm
1.8	1024, Bus A	108 MHz 96 ns	—	256 LPSDRAM, Bus A	9 x 11 x 1.2	x16D 105-ball	PF38F6070M0Y0BE 65 nm
1.8	512, Bus A	108 MHz 96 ns	—	128 LPSDRAM, Bus A	9 x 11 x 1.2	x16D 105-ball	PF38F5060M0Y0B0
1.8	512, Bus A	108 MHz 96 ns	—	256 LPSDRAM, Bus A	9 x 11 x 1.2	x16D 105-ball	PF38F5070M0Y0B0
1.8	512 + 512, Bus A	108 MHz 96 ns	—	—	8 x 10 x 1.4	x16D 105-ball	PF48F5500M0Y0B0
1.8	256, Bus A	133 MHz 96 ns	—	128 LPSDRAM, Bus A	9 x 11 x 1.2	x16D 105-ball	PF38F5060M0Y0B0
x16D Shared Bus, AD-Mux							
1.8	1024, Bus A	108 MHz 96 ns	2048, Bus A	—	11 x 15 x 1.2	x16D 105-ball	PF58F0031M0Y1BE 65 nm
1.8	512 + 512, Bus A	108 MHz 96 ns	—	—	8 x 10 x 1.4	x16D 105-ball	PF48F5500M0Y1B0
x16C, Shared Bus, Non-Mux							
1.8	1024, Bus A	108 MHz 96 ns	—	256 PSRAM, Bus A	11 x 11 x 1.2	x16C 107-ball	PF38F6070M0Y0C0 65 nm
1.8	512, Bus A	108 MHz 96 ns	—	128 PSRAM, Bus A	8 x 11 x 1.2	x16C 107-ball	PF38F5060M0Y0C0
1.8	512, Bus A	108 MHz 96 ns	—	64 PSRAM, Bus A	8 x 11 x 1.2	x16C 107-ball	PF38F5050M0Y0C0
1.8	256, Bus A	133 MHz 96 ns	—	128 PSRAM, Bus A	8 x 10 x 1.2	x16C 107-ball	PF38F4060M0Y0C0
1.8	256, Bus A	133 MHz 96 ns	—	64 PSRAM, Bus A	8 x 10 x 1.2	x16C 107-ball	PF38F4050M0Y0C0
x16C, Shared Bus, AD-Mux							
1.8	256, Bus A	133 MHz 96 ns	—	128 PSRAM, Bus A	8 x 10 x 1.2	x16C 107-ball	PF38F4060M0Y1C0
x16SB, Split Bus, Non-Mux							
1.8	1024, Bus A	108 MHz 96 ns	—	256 LPSDRAM, Bus B	10 x 11 x 1.2	x16SB 165-ball	PF38F6070M0Y0VE 65 nm

Note: To order parts listed above and to obtain a datasheet for the M18 SCSP parts, please contact your local Intel sales office.

2.5 Additional Information

Order Number	Document/Tool
315567	Intel StrataFlash® Cellular Memory (M18) Developer's Manual
307654	Intel StrataFlash® Cellular Memory (M18 SCSP); 2048-Mbit M18 (Non-Mux and AD-Mux I/O) Family with Synchronous PSRAM Datasheet
310048	Designing with Intel StrataFlash® Wireless Memory and Pre-enabling Intel StrataFlash® Cellular Memory, Application Note 822
309311	Intel StrataFlash® Cellular Memory (M18 SCSP) to ARM® PrimeCell™ Design Guide, Application Note 841
315651	Migration Guide for Intel StrataFlash® Cellular Memory (M18) 90 nm to 65 nm, Application Note 860
310058	Effect of Program Buffer Size on System Interrupt Latency, Application Note 816

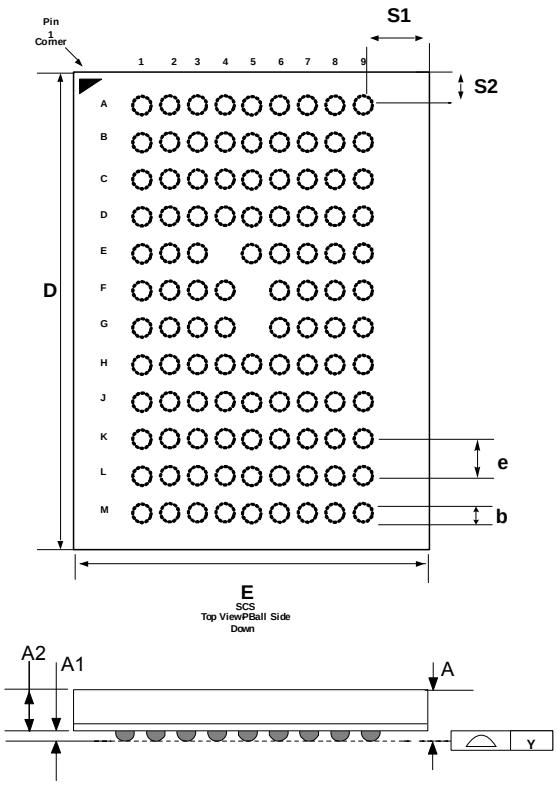
Notes:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.Intel.com for technical documentation and tools.
3. For the most current information on Intel flash products, visit our website at http://developer.intel.com/design/flash/.

3.0 Package Information

The following figures show the ballout package information for the M18 device:

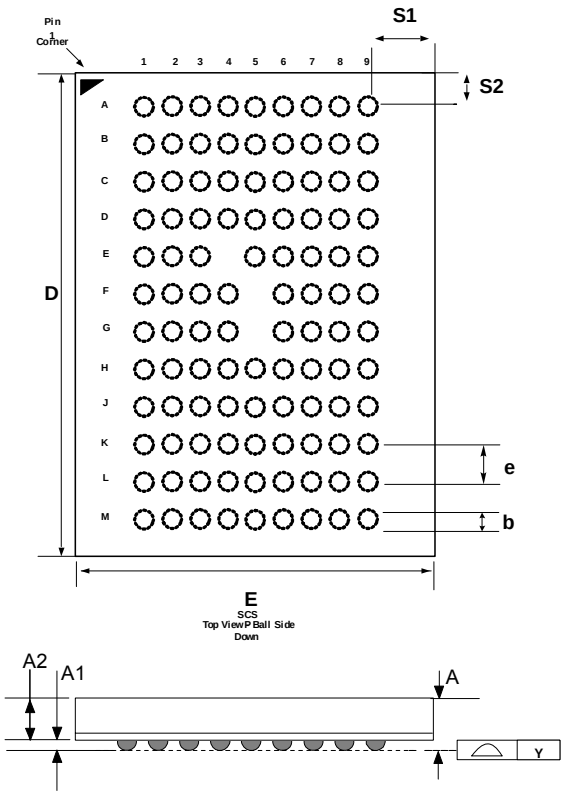
Figure 1. Mechanical Specifications for x16D (105-ball) package (8x10x1.0 mm)



Note: Drawing not to scale.

Dimensions	Symbol	Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A			1.0				0.0394
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		0.660				0.0260	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	9.90	10.00	10.10		0.3898	0.3937	0.3976
Package Body Width	E	7.90	8.00	8.10		0.3110	0.3150	0.3189
Pitch	e		0.800				0.0315	
Ball (Lead) Count	N		105				105	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball Distance Along E	S1	0.700	0.800	0.900		0.0276	0.0315	0.0354
Corner to Ball Distance Along D	S2	0.500	0.600	0.700		0.0197	0.0236	0.0276

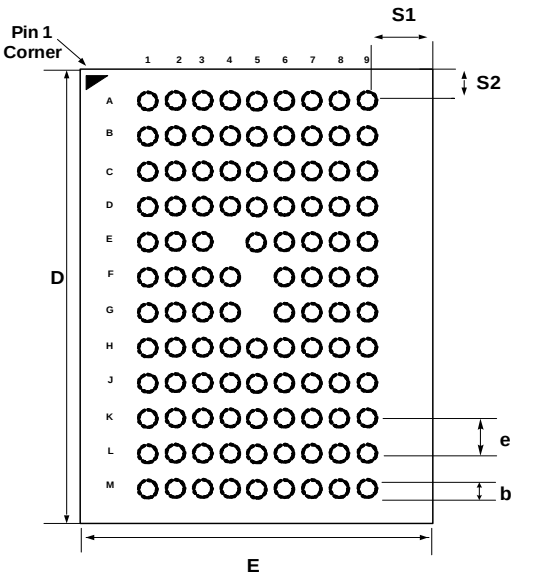
Figure 2. Mechanical Specifications for x16D (105-ball) package (8x10x1.4 mm)



Note: Drawing not to scale.

Dimensions	Symbol	Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A			1.4				0.0551
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		1.070				0.0421	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	9.90	10.00	10.10		0.3898	0.3937	0.3976
Package Body Width	E	7.90	8.00	8.10		0.3110	0.3150	0.3189
Pitch	e		0.800				0.0315	
Ball (Lead) Count	N		105				105	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball Distance Along E	S1	0.700	0.800	0.900		0.0276	0.0315	0.0354
Corner to Ball Distance Along D	S2	0.500	0.600	0.700		0.0197	0.0236	0.0276

Figure 3. Mechanical Specifications for x16D (105-ball) package (9x11x1.2 mm)



Note: Drawing not to scale.

Dimensions	Symbol	Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A			1.2				0.0472
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		0.860				0.0339	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	10.90	11.00	11.10		0.4291	0.4331	0.4370
Package Body Width	E	8.90	9.00	9.10		0.3504	0.3543	0.3583
Pitch	e		0.800				0.0315	
Ball (Lead) Count	N		105				105	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball Distance Along E	S1	1.200	1.300	1.400		0.0472	0.0512	0.0551
Corner to Ball Distance Along D	S2	1.000	1.100	1.200		0.0394	0.0433	0.0472

Figure 4. Mechanical Specifications for x16D (105 balls) Package (11x15x1.2 mm)

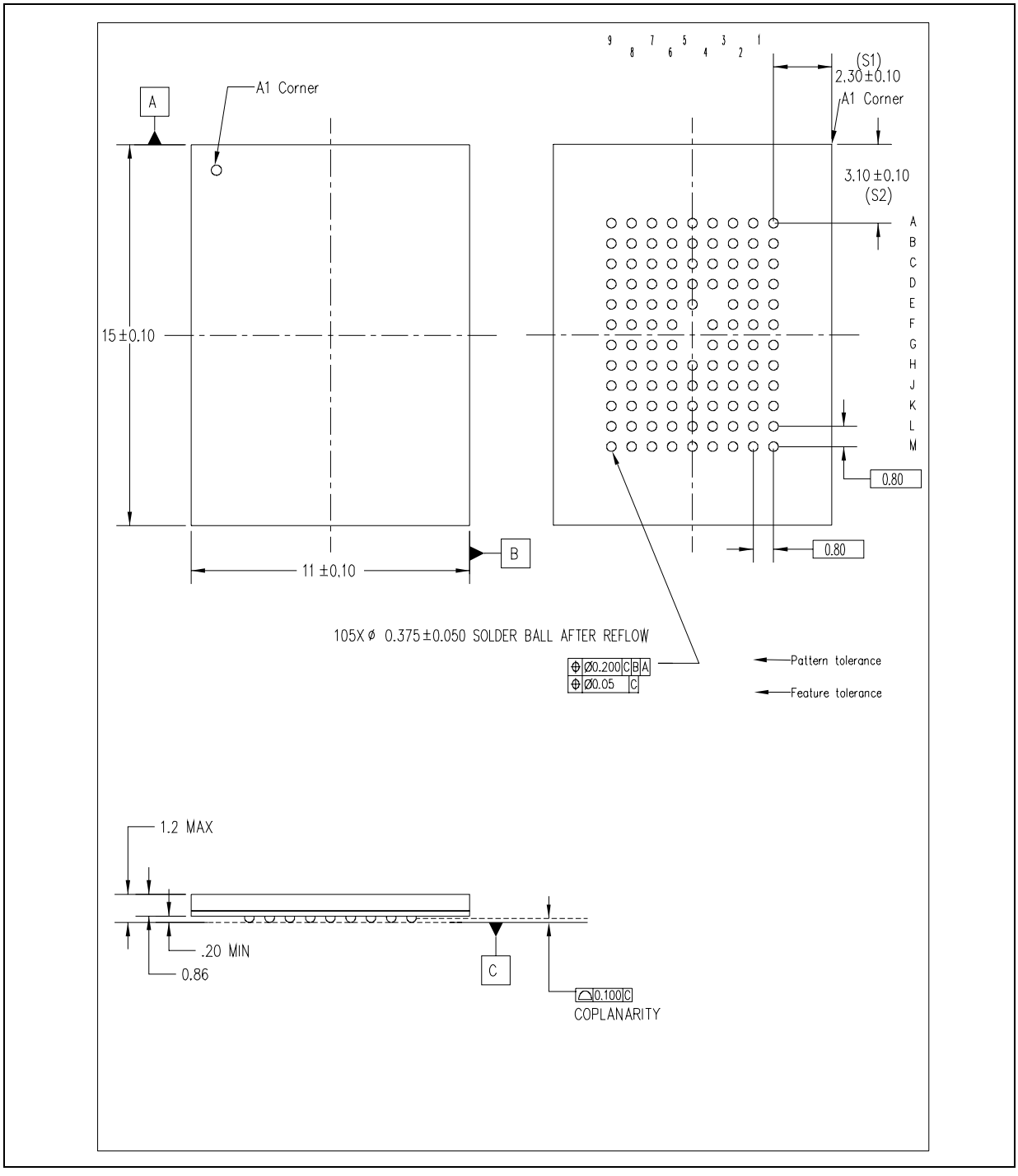
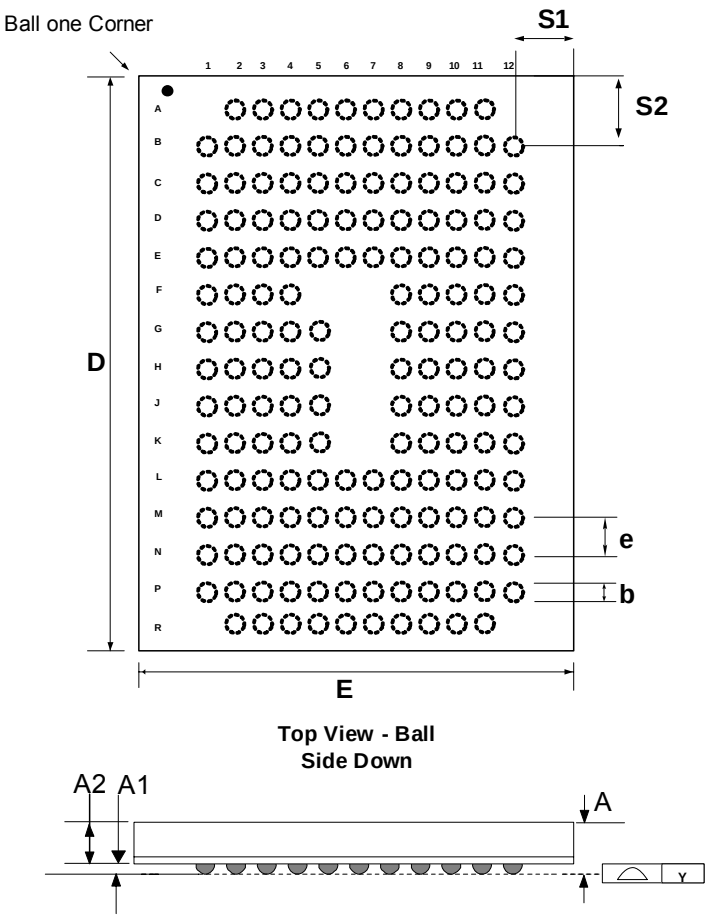


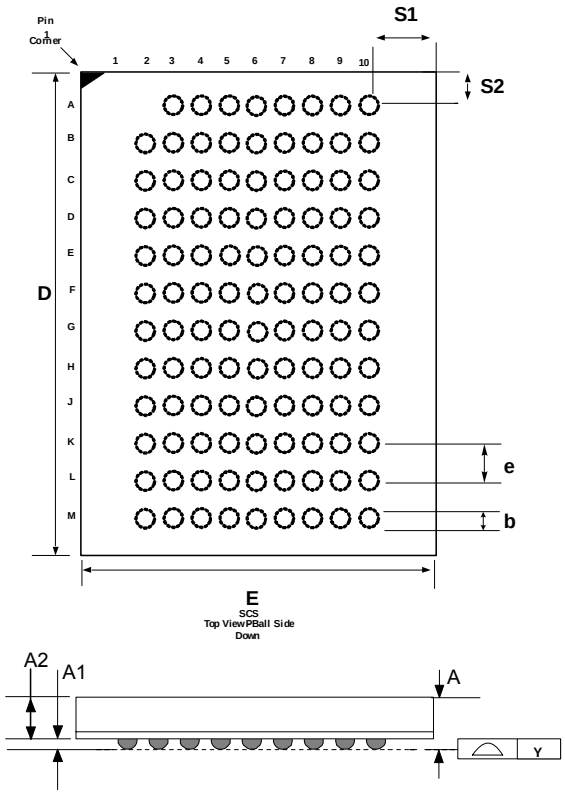
Figure 5. Mechanical Specifications for x16 Split Bus (165-ball) package (10x11x1.2 mm)



Note: Drawing not to scale.

		Millimeters				Inches		
Dimensions	Symbol	Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A			1.2				0.0472
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		0.860				0.0339	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	10.90	11.00	11.10		0.4291	0.4331	0.4370
Package Body Width	E	9.90	10.00	10.10		0.3898	0.3937	0.3976
Pitch	e		0.650				0.0256	
Ball (Lead) Count	N		165				165	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball Distance Along E	S1	1.325	1.425	1.525		0.0522	0.0561	0.0600
Corner to Ball Distance Along D	S2	1.500	1.600	1.700		0.0591	0.0630	0.0669

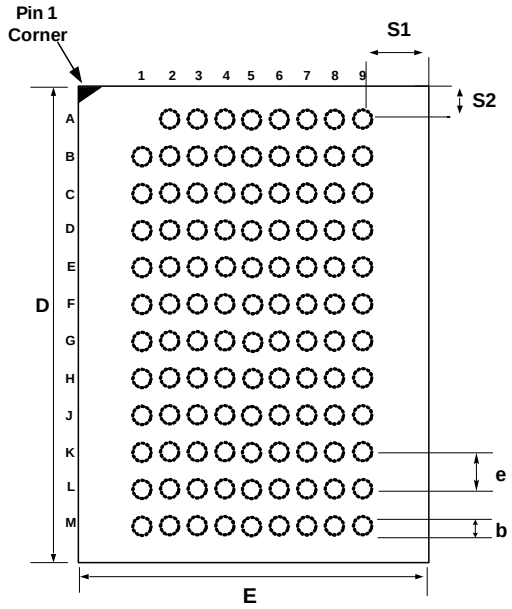
Figure 6. Mechanical Specifications for x16C (107-ball) package (8x10x1.2 mm)



Note: Drawing not to scale.

Dimensions	Symbol	Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A			1.2				0.0472
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		0.860				0.0339	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	9.90	10.00	10.10		0.3898	0.3937	0.3976
Package Body Width	E	7.90	8.00	8.10		0.3110	0.3150	0.3189
Pitch	e		0.800				0.0315	
Ball (Lead) Count	N		107				107	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball Distance Along E	S1	0.700	0.800	0.900		0.0276	0.0315	0.0354
Corner to Ball Distance Along D	S2	0.500	0.600	0.700		0.0197	0.0236	0.0276

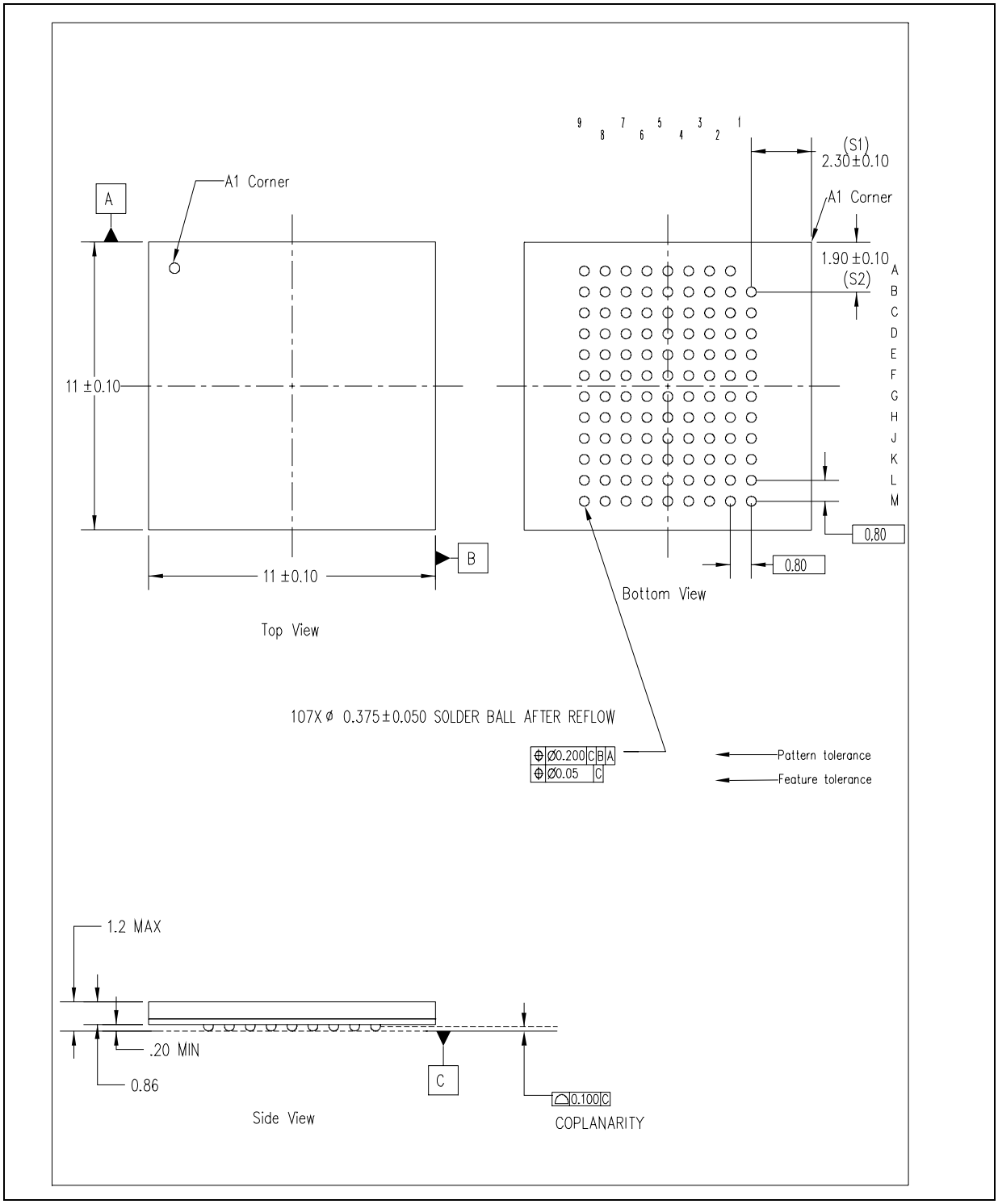
Figure 7. Mechanical Specifications for x16C (107-ball) package (8x11x1.2 mm)



Note: Drawing not to scale

		Millimeters				Inches		
Dimensions	Symbol	Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A			1.2				0.0472
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		0.860				0.0339	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	10.90	11.00	11.10		0.4291	0.4331	0.4370
Package Body Width	E	7.90	8.00	8.10		0.3110	0.3150	0.3189
Pitch	e		0.800				0.0315	
Ball (Lead) Count	N		107				107	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball Distance Along E	S1	0.700	0.800	0.900		0.0276	0.0315	0.0354
Corner to Ball Distance Along D	S2	1.000	1.100	1.200		0.0394	0.0433	0.0472

Figure 8. Mechanical Specifications for x16C (107-ball) package (11x11x1.2 mm)



4.0 Ballout and Signal Descriptions

This section provides ballout and signal description information for x16D (105-ball), x16C (107-ball), and x16 Split Bus (165-ball) packages, Non-Mux, AD-Mux interfaces.

4.1 Signal Ballouts x16D

4.1.1 x16D (105-Ball) Ballout, Non-Mux

Figure 9. x16D (105-Ball) Electrical Ballout, Non-Mux

Pin 1

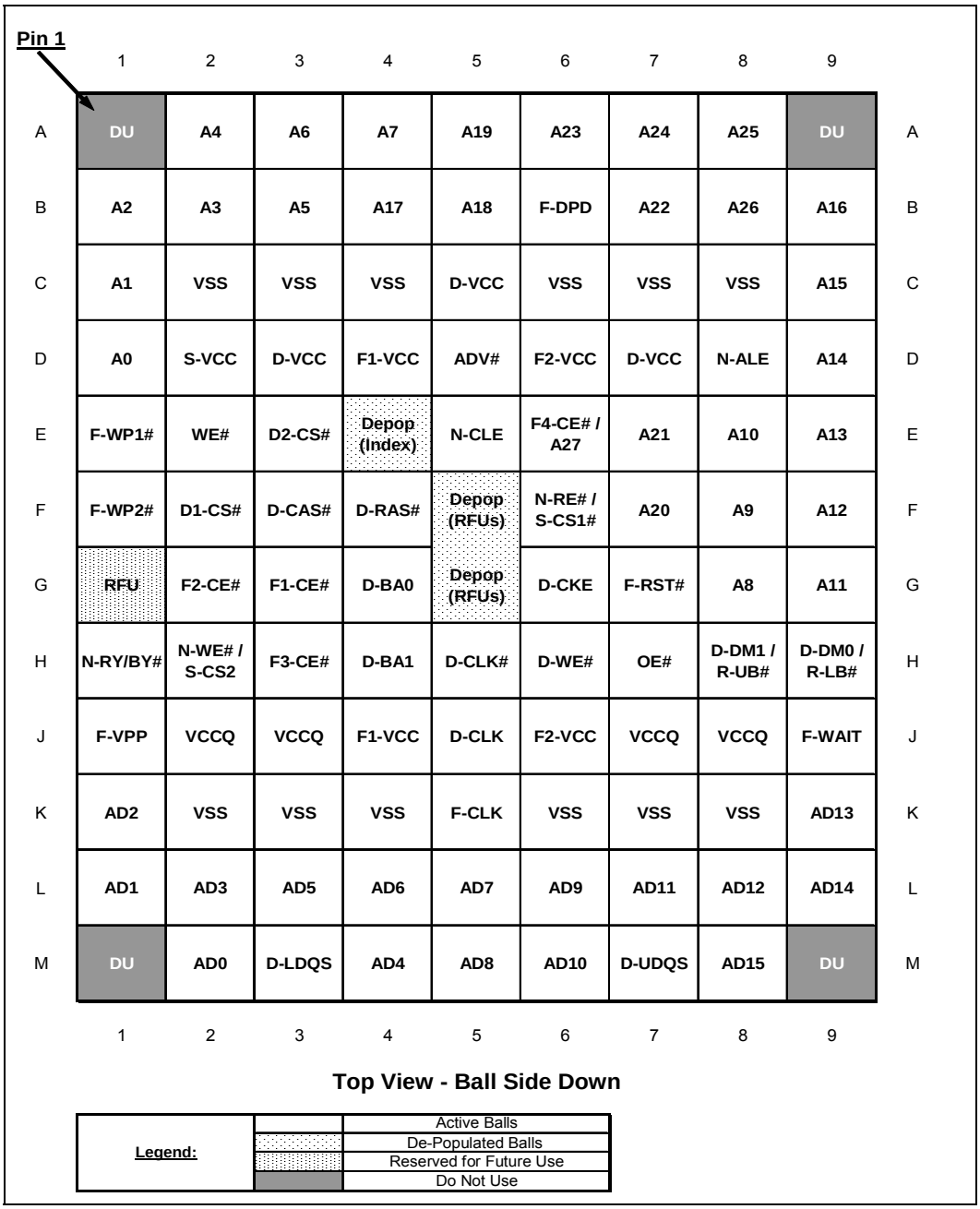
	1	2	3	4	5	6	7	8	9	
A	DU	A4	A6	A7	A19	A23	A24	A25	DU	A
B	A2	A3	A5	A17	A18	F-DPD	A22	A26	A16	B
C	A1	VSS	VSS	VSS	D-VCC	VSS	VSS	VSS	A15	C
D	A0	S-VCC	D-VCC	F1-VCC	ADV#	F2-VCC	D-VCC	N-ALE	A14	D
E	F-WP1#	WE#	D2-CS#	Depop (Index)	N-CLE	F4-CE# / A27	A21	A10	A13	E
F	F-WP2#	D1-CS#	D-CAS#	D-RAS#	Depop (RFUs)	N-RE# / S-CS1#	A20	A9	A12	F
G	RFU	F2-CE#	F1-CE#	D-BA0	Depop (RFUs)	D-CKE	F-RST#	A8	A11	G
H	N-RY/BY#	N-WE# / S-CS2	F3-CE#	D-BA1	D-CLK#	D-WE#	OE#	D-DM1 / S-UB#	D-DM0 / S-LB#	H
J	F-VPP	VCCQ	VCCQ	F1-VCC	D-CLK	F2-VCC	VCCQ	VCCQ	F-WAIT	J
K	DQ2	VSS	VSS	VSS	F-CLK	VSS	VSS	VSS	DQ13	K
L	DQ1	DQ3	DQ5	DQ6	DQ7	DQ9	DQ11	DQ12	DQ14	L
M	DU	DQ0	D-LDQS	DQ4	DQ8	DQ10	D-UDQS	DQ15	DU	M
	1	2	3	4	5	6	7	8	9	

Top View - Ball Side Down

Legend:	
	Active Balls
	De-Populated Balls
	Reserved for Future Use
	Do Not Use

4.1.2 x16D (105-Ball) Ballout, AD-Mux

Figure 10. x16D (105-Ball) Electrical Ballout, AD-Mux



4.2 Signal Descriptions x16D

Table 8. Signal Descriptions, x16D Non-Mux / x16D AD-Mux Ballout (Sheet 1 of 4)

Symbol	Type	Signal Descriptions	Notes
Address and Data Signals, Non-Mux			
A[MAX: 0]	Input	**ADDRESS:** Global device signals. Shared address inputs for all memory die during Read and Write operations. • 4-Gbit: AMAX = A27 • 2-Gbit: AMAX = A26 • 1-Gbit: AMAX = A25 • 512-Mbit: AMAX = A24 • 256-Mbit: AMAX = A23 • 128-Mbit: AMAX = A22 • A[12:0] are the row and A[9:0] are the column addresses for 512-Mbit LPSDRAM. • A[12:0] are the row and A[8:0] are the column addresses for 256-Mbit LPSDRAM. • A[11:0] are the row and A[8:0] are the column addresses for 128-Mbit LPSDRAM. Unused address inputs should be treated as RFU.	1
DQ[15:0]	Input/ Output	**DATA INPUT/OUTPUTS:** Global device signals. DQ[15:0] are used to input commands and write-data during Write cycles, and to output read-data during Read cycles. During NAND accesses, DQ[7:0] are used to input commands, address-data, and write-data, and to output read-data. Data signals are High-Z when the device is deselected or its output is disabled.	
F-ADV#	Input	**FLASH ADDRESS VALID:** Flash-specific signal; low-true input. During synchronous flash Read operations, the address is latched on the rising edge of F-ADV#, or on the first rising edge of F-CLK after F-ADV# goes low for devices that support up to 108 MHz, or on the last rising edge of F-CLK after F-ADV# goes low for devices that support up to 133 MHz. In an asynchronous flash Read operation, the address is latched on the rising edge of F-ADV# or continuously flows through while F-ADV# is low.	
Address and Data Signals, AD-Mux			
A[MAX:16]	Input	**ADDRESS:** Global device signals. Shared address inputs for all Flash and SRAM memory die during Read and Write operations. • 4-Gbit: AMAX = A27 • 2-Gbit: AMAX = A26 • 1-Gbit: AMAX = A25 • 512-Mbit: AMAX = A24 • 256-Mbit: AMAX = A23 • 128-Mbit: AMAX = A22 Unused address inputs should be treated as RFU.	1
AD[15:0]	Input / Output	**ADDRESS-DATA MULTIPLEXED INPUTS/ OUTPUTS:** AD-Mux flash and SRAM lower address and data signals; LPSDRAM data signals. During AD-Mux flash and SRAM Write cycles, AD[15:0] are used to input the lower address followed by commands or write-data. During AD-Mux flash Read cycles, AD[15:0] are used to input the lower address followed by read-data output. During LPSDRAM accesses, AD[15:0] are used to input commands and write-data during Write cycles or to output read-data during Read cycles. During NAND accesses, AD[7:0] are used to input commands, address, or write-data, and to output read-data. AD[15:0] are High-Z when the flash or SRAM is deselected or its output is disabled.	
A[15:0]	Input	RFU, except for DRAM.	

Table 8. Signal Descriptions, x16D Non-Mux / x16D AD-Mux Ballout (Sheet 2 of 4)

Symbol	Type	Signal Descriptions	Notes
F-ADV#	Input	**FLASH ADDRESS VALID:** Flash-specific signal; low-true input. During synchronous flash Read operations, the address is latched on the rising edge of F-ADV#, or on the first rising edge of F-CLK after F-ADV# goes low for devices that support up to 108 MHz, or on the last rising edge of F-CLK after F-ADV# goes low for devices that support up to 133 MHz. In an asynchronous flash Read operation, the address is latched on the rising edge of F-ADV#.	
Control Signals			
F[4:1]-CE#	Input	**FLASH CHIP ENABLE:** Flash-specific signal; low-true input. When low, F-CE# selects the associated flash memory die. When high, F-CE# deselects the associated flash die. Flash die power is reduced to standby levels, and its data and F-WAIT outputs are placed in a High-Z state. • F1-CE# is dedicated to flash die #1. • F[4:2]-CE# are dedicated to flash die #4 through #2, respectively, if present. Otherwise, any unused flash chip enable should be treated as RFU. • For NOR/NAND stacked device, F1-CE# selects NOR die #1, F2-CE# selects NOR die #2 while F4-CE# selects NAND die #1 and NAND die #2 using virtual chip-select scheme, F3-CE# selects NAND die #3 if present.	1
F-CLK	Input	**FLASH CLOCK:** Flash-specific signal; rising active-edge input. F-CLK synchronizes the flash with the system clock during synchronous operations.	
D-CLK	Input	**LPSDRAM CLOCK:** LPSDRAM-specific signal; rising active-edge input. D-CLK synchronizes the LPSDRAM and DDR LPSDRAM with the system clock.	2
D-CLK#	Input	**DDR LPSDRAM CLOCK:** DDR LPSDRAM-specific signal; falling active-edge input. D-CLK# synchronizes the DDR LPSDRAM with the system clock.	2
OE#	Input	**OUTPUT ENABLE:** Flash- and SRAM-specific signal; low-true input. When low, OE# enables the output drivers of the selected flash or SRAM die. When high, OE# disables the output drivers of the selected flash or SRAM die and places the output drivers in High-Z.	
F-RST#	Input	**FLASH RESET:** Flash-specific signal; low-true input. When low, F-RST# resets internal operations and inhibits writes. When high, F-RST# enables normal operation.	
F-WAIT	Output	**FLASH WAIT:** Flash -specific signal; configurable-true output. When asserted, F-WAIT indicates invalid output data. F-WAIT is driven whenever F-CE# and OE# are low. F-WAIT is High-Z whenever F-CE# or OE# is high.	
WE#	Input	**WRITE ENABLE:** Flash- and SRAM-specific signal; low-true input. When low, WE# enables Write operations for the enabled flash or SRAM die.	
D-WE#	Input	**LPSDRAM WRITE ENABLE:** LPSDRAM-specific signal; low-true input. D-WE#, together with A[MAX:0], D-BA[1:0], D-CKE, D-CS#, D-CAS#, and D-RAS#, define the LPSDRAM command or operation. D-WE# is sampled on the rising edge of D-CLK.	2
F-WP[2:1]#	Input	**FLASH WRITE PROTECT:** Flash-specific signals; low-true inputs. When low, F-WP# enables the Lock-Down mechanism. When high, F-WP# overrides the Lock-Down function, enabling locked-down blocks to be unlocked with the Unlock command. • F-WP1# is dedicated to flash die #1. • F-WP2# is common to all other flash dies, if present. Otherwise it is RFU. • For NOR/NAND stacked device, F-WP1# selects all NOR dies, while F-WP2# selects all NAND dies.	
F-DPD	Input	**FLASH DEEP POWER-DOWN:** Flash-specific signal; configurable-true input. When enabled in the ECR, F-DPD is used to enter and exit Deep Power-Down mode.	
N-CLE	Input	**NAND COMMAND LATCH ENABLE:** NAND-specific signal; high-true input. When high, N-CLE enables commands to be latched on the rising edge of N-WE#.	2
N-ALE	Input	**NAND ADDRESS LATCH ENABLE:** NAND-specific signal; high-true input. When high, N-ALE enables addresses to be latched on the rising edge of N-WE#.	2

Table 8. Signal Descriptions, x16D Non-Mux / x16D AD-Mux Ballout (Sheet 3 of 4)

Symbol	Type	Signal Descriptions	Notes
N-RE#	Input	**NAND READ ENABLE:** NAND-specific signal; low-true input. When low, N-RE# enables the output drivers of the selected NAND die. When high, N-RE# disables the output drivers of the selected NAND die and places the output drivers in High-Z.	2, 4
N-RY/BY#	Output	**NAND READY/BUSY:** NAND-specific signal; low-true output. When low, N-RY/BY# indicates the NAND is busy performing a read, program, or erase operation. When high, N-RY/BY# indicates the NAND device is ready.	2
N-WE#	Input	**NAND WRITE ENABLE:** NAND-specific signal; low-true input. When low, N-WE# enables Write operations for the enabled NAND die.	2, 5
D-CKE	Input	**LPSDRAM CLOCK ENABLE:** LPSDRAM-specific signal; high-true input. When high, D-CKE indicates that the next D-CLK edge is valid. When low, D-CKE indicates that the next D-CLK edge is invalid and the selected LPSDRAM die is suspended.	2
D-BA[1:0]	Input	**LPSDRAM BANK SELECT:** LPSDRAM-specific input signals. D-BA[1:0] selects one of four banks in the LPSDRAM die.	2
D-RAS#	Input	**LPSDRAM ROW ADDRESS STROBE:** LPSDRAM-specific signal; low-true input. D-RAS#, together with A[MAX:0], D-BA[1:0], D-CKE, D-CS#, D-CAS#, and D-WE#, define the LPSDRAM command or operation. D-RAS# is sampled on the rising edge of D-CLK.	2
D-CAS#	Input	**LPSDRAM COLUMN ADDRESS STROBE:** LPSDRAM-specific signal; low-true input. D-CAS#, together with A[MAX:0], D-BA[1:0], D-CKE, D-CS#, D-RAS#, and D-WE#, define the LPSDRAM command or operation. D-CAS# is sampled on the rising edge of D-CLK.	2
D[2:1]-CS#	Input	**LPSDRAM CHIP SELECT:** LPSDRAM-specific signal; low-true input. When low, D-CS# selects the associated LPSDRAM memory die and starts the command input cycle. When D-CS# is high, commands are ignored but operations continue. • D-CS#, together with A[MAX:0], D-BA[1:0], D-CKE, D-RAS#, D-CAS#, and D-WE#, define the LPSDRAM command or operation. D-CS# is sampled on the rising edge of D-CLK. • D[2:1]-CS# are dedicated to LPSDRAM die #2 and die #1, respectively, if present. Otherwise, any unused LPSDRAM chip selects should be treated as RFU.	2
D-DM[1:0]	Input	**LPSDRAM DATA MASK:** LPSDRAM-specific signal; high-true input. When high, D-DM[1:0] controls masking of input data during writes and output data during reads. • D-DM1 corresponds to the data on DQ[15:8]. • D-DM0 corresponds to the data on DQ[7:0].	2, 3
D-UDQS D-LDQS	Input / Output	**LPSDRAM UPPER/LOWER DATA STROBE:** DDR LPSDRAM-specific input/output signals. D-UDQS and D-LDQS provide as output the read-data strobes, and as input the write-data strobes. • D-UDQS corresponds to the data on DQ[15:8]. • D-LDQS corresponds to the data on DQ[7:0].	2
S-CS1# S-CS2	Input	**SRAM CHIP SELECTS:** SRAM-specific signals; S-CS1# low-true input, S-CS2 high-true input. When both are asserted, S-CS1# and S-CS2 select the SRAM die. When either is deasserted, the SRAM die is deselected and its power is reduced to standby levels.	2, 4, 5
S-UB# S-LB#	Input	**SRAM UPPER/LOWER BYTE ENABLES:** SRAM-specific signals; low-true inputs. When low, S-UB# enables DQ[15:8] and S-LB# enables DQ[7:0] during SRAM Read and Write cycles. When high, S-UB# masks DQ[15:8] and S-LB# masks DQ[7:0].	2, 3
Power Signals			
F-VPP	Power	**FLASH PROGRAM/ERASE VOLTAGE:** Flash specific. F-VPP supplies program or erase power to the flash die.	

Table 8. Signal Descriptions, x16D Non-Mux / x16D AD-Mux Ballout (Sheet 4 of 4)

Symbol	Type	Signal Descriptions	Notes
F1-VCC	Power	**FLASH CORE POWER SUPPLY:** Flash specific. F1-VCC supplies the core power to the NOR flash die.	
F2-VCC	Power	**FLASH CORE POWER SUPPLY:** Flash specific. F2-VCC supplies the core power to either 1) the NOR flash die in stack packages with multiple NOR flash dies, or 2) NAND flash die in stack packages with NOR-NAND flash dies.	6
VCCQ	Power	**I/O POWER SUPPLY:** Global device I/O power. VCCQ supplies the device input/output driver voltage.	
D-VCC	Power	**LPSDRAM CORE POWER SUPPLY:** LPSDRAM specific. D-VCC supplies the core power to the LPSDRAM die.	2
S-VCC	Power	**SRAM POWER SUPPLY:** SRAM specific. S-VCC supplies the core power to the SRAM die.	2
VSS	Ground	**DEVICE GROUND:** Global ground reference for all signals and power supplies. Connect all VSS balls to system ground. Do not float any VSS connections.	
DU	—	**DO NOT USE:** This ball should not be connected to any power supplies, signals, or other balls. This ball can be left floating.	
RFU	—	**RESERVED FOR FUTURE USE:** Reserved by Intel for future device functionality and enhancement. This ball must be left floating.	

Notes:
1. F4-CE# and A27 share the same package ball at location E6. Only one signal function is available, depending on the stacked device combination.
2. Only available on stacked device combinations with NAND, SRAM, and/or LPSDRAM die; otherwise, treated as RFU.
3. D-DM[1:0] and S-UB#/S-LB# share the same package balls at locations H8 and H9, respectively. Only one signal function for each ball location is available, depending on the stacked device combination.
4. S-CS1# and N-RE# share the same package ball at location F6. Only one signal function is available, depending on the stacked device combination.
5. S-CS2 and N-WE# share the same package ball at location H2. Only one signal function is available, depending on the stacked device combination.
6. In stack packages with only one NOR flash die, this signal can be left floating.

4.3 Signal Ballouts x16C

4.3.1 x16C (107-Ball) Ballout, Non-Mux

Figure 11. x16C (107-Ball) Electrical Ballout, Non-Mux

Pin 1

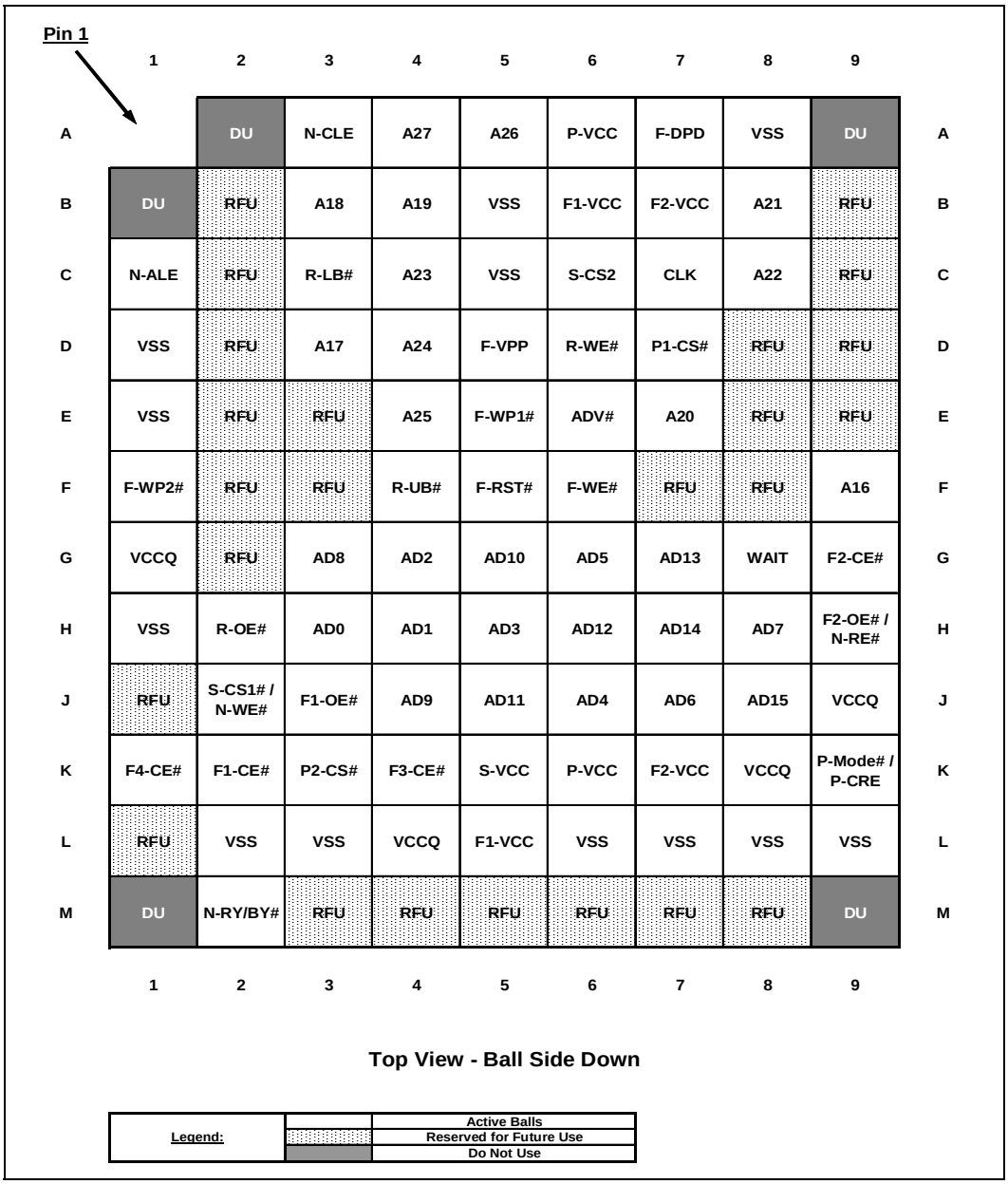
	1	2	3	4	5	6	7	8	9	
A		DU	N-CLE	A27	A26	P-VCC	F-DPD	VSS	DU	A
B	DU	A4	A18	A19	VSS	F1-VCC	F2-VCC	A21	A11	B
C	N-ALE	A5	R-LB#	A23	VSS	S-CS2	CLK	A22	A12	C
D	VSS	A3	A17	A24	F-VPP	R-WE#	P1-CS#	A9	A13	D
E	VSS	A2	A7	A25	F-WP1#	ADV#	A20	A10	A15	E
F	F-WP2#	A1	A6	R-UB#	F-RST#	F-WE#	A8	A14	A16	F
G	VCCQ	A0	DQ8	DQ2	DQ10	DQ5	DQ13	WAIT	F2-CE#	G
H	VSS	R-OE#	DQ0	DQ1	DQ3	DQ12	DQ14	DQ7	F2-OE# / N-RE#	H
J	RFU	S-CS1# / N-WE#	F1-OE#	DQ9	DQ11	DQ4	DQ6	DQ15	VCCQ	J
K	F4-CE#	F1-CE#	P2-CS#	F3-CE#	S-VCC	P-VCC	F2-VCC	VCCQ	P-Mode# / P-CRE	K
L	RFU	VSS	VSS	VCCQ	F1-VCC	VSS	VSS	VSS	VSS	L
M	DU	N-RY/BY#	RFU	RFU	RFU	RFU	RFU	RFU	DU	M
	1	2	3	4	5	6	7	8	9	

Top View - Ball Side Down

Legend:	Active Balls
	Reserved for Future Use
	Do Not Use

4.3.2 x16C (107-Ball) Ballout, AD-Mux

Figure 12. x16C (107-Ball) Electrical Ballout, AD-Mux



4.4 Signal Descriptions x16C

Table 9. Signal Descriptions for x16C / x16C AD-Mux Ballout (Sheet 1 of 3)

Symbol	Type	Signal Descriptions	Notes
Address and Data Signals, Non-Mux			
A[MAX:0]	Input	**ADDRESS:** Global device signals. Shared address inputs for all memory die during Read and Write operations. • 4-Gbit: AMAX = A27• 128-Mbit: AMAX = A22 • 2-Gbit: AMAX = A26• 64-Mbit: AMAX = A21 • 1-Gbit: AMAX = A25• 32-Mbit: AMAX = A20 • 512-Mbit: AMAX = A24• 16-Mbit: AMAX = A19 • 256-Mbit: AMAX = A23• 8-Mbit: AMAX = A18 Unused address inputs should be treated as RFU.	
DQ[15:0]	Input / Output	**DATA INPUT/OUTPUTS:** Global device signals. Inputs data and commands during Write cycles, outputs data during Read cycles. Data signals are High-Z when the device is deselected or its output is disabled.	
ADV#	Input	**ADDRESS VALID:** Flash- and Synchronous PSRAM-specific signal; low-true input. During synchronous flash Read operations, the address is latched on the rising edge of F-ADV#, or on the first rising edge of F-CLK after F-ADV# goes low for devices that support up to 108 MHz, or on the last rising edge of F-CLK after F-ADV# goes low for devices that support up to 133 MHz. In an asynchronous flash Read operation, the address is latched on the rising edge of ADV# or continuously flows through while ADV# is low.	
Address and Data Signals, AD-Mux			
A[MAX:16]	Input	**ADDRESS:** Global device signals. Shared address inputs for all memory die during Read and Write operations. • 4-Gbit: AMAX = A27• 128-Mbit: AMAX = A22 • 2-Gbit: AMAX = A26• 64-Mbit: AMAX = A21 • 1-Gbit: AMAX = A25• 32-Mbit: AMAX = A20 • 512-Mbit: AMAX = A24• 16-Mbit: AMAX = A19 • 256-Mbit: AMAX = A23• 8-Mbit: AMAX = A18 Unused address inputs should be treated as RFU.	
AD[15:0]	Input / Output	**ADDRESS-DATA MULTIPLEXED INPUTS/ OUTPUTS:** Global device signals. During AD-Mux Write cycles, AD[15:0] are used to input the lower address followed by commands or data. During AD-Mux Read cycles, AD[15:0] are used to input the lower address followed by read-data output. During NAND accesses, AD[7:0] is used to input commands, address-data, or write-data, and output read-data. AD[15:0] are High-Z when the device is deselected or its output is disabled.	
ADV#	Input	**ADDRESS VALID:** Flash- and Synchronous PSRAM-specific signal; low-true input. During synchronous flash Read operations, the address is latched on the rising edge of F-ADV#, or on the first rising edge of F-CLK after F-ADV# goes low for devices that support up to 108 MHz, or on the last rising edge of F-CLK after F-ADV# goes low for devices that support up to 133 MHz. In an asynchronous flash Read operation, the address is latched on the rising edge of ADV#.	
Control Signals			
F[4:1]-CE#	Input	**FLASH CHIP ENABLE:** Flash-specific signal; low-true input. When low, F-CE# selects the associated flash memory die. When high, F-CE# deselects the associated flash die. Flash die power is reduced to standby levels, and its data and F-WAIT outputs are placed in a High-Z state. • F1-CE# is dedicated to flash die #1. • F[4:2]-CE# are dedicated to flash die #4 through #2, respectively, if present. Otherwise, any unused flash chip enable should be treated as RFU. • For NOR/NAND stacked device, F1-CE# selects NOR die #1, F2-CE# selects NOR die #2 while F4-CE# selects NAND die #1 and NAND die #2 using virtual chip-select scheme, F3-CE# selects NAND die #3 if present.	

Table 9. Signal Descriptions for x16C / x16C AD-Mux Ballout (Sheet 2 of 3)

Symbol	Type	Signal Descriptions	Notes
CLK	Input	**CLOCK:** Flash- and Synchronous PSRAM-specific input signal. CLK synchronizes the flash and/or synchronous PSRAM with the system clock during synchronous operations.	
F[2:1]-OE#	Input	**FLASH OUTPUT ENABLE:** Flash-specific signal; low-true input. When low, F-OE# enables the output drivers of the selected flash die. When high, F-OE# disables the output drivers of the selected flash die and places the output drivers in High-Z. • For NOR only stacked device, F[2:1]-OE# are common to all NOR dies in the device. • For NOR/NAND stacked device, F1-OE# enables all NOR dies, F2-OE# selects all NAND dies if present.	2
R-OE#	Input	**RAM OUTPUT ENABLE:** PSRAM- and SRAM-specific signal; low-true input. When low, R-OE# enables the output drivers of the selected memory die. When high, R-OE# disables the output drivers of the selected memory die and places the output drivers in High-Z.	1
F-RST#	Input	**FLASH RESET:** Flash-specific signal; low-true input. When low, F-RST# resets internal operations and inhibits writes. When high, F-RST# enables normal operation.	
WAIT	Output	**WAIT:** Flash -and Synchronous PSRAM-specific signal; configurable true-level output. When asserted, WAIT indicates invalid output data. When deasserted, WAIT indicates valid output data. • WAIT is driven whenever the flash or the synchronous PSRAM is selected and its output enable is low. • WAIT is High-Z whenever flash or the synchronous PSRAM is deselected, or its output enable is high.	
F-WE#	Input	**FLASH WRITE ENABLE:** Flash-specific signal; low-true input. When low, F-WE# enables Write operations for the enabled flash die. Address and data are latched on the rising edge of F-WE#.	
R-WE#	Input	**RAM WRITE ENABLE:** PSRAM- and SRAM-specific signal; low-true input. When low, R-WE# enables Write operations for the selected memory die. Data is latched on the rising edge of R-WE#.	1
F-WP[2:1]#	Input	**FLASH WRITE PROTECT:** Flash-specific signals; low-true inputs. When low, F-WP# enables the Lock-Down mechanism. When high, F-WP# overrides the Lock-Down function, enabling locked-down blocks to be unlocked with the Unlock command. • F-WP1# is dedicated to flash die #1. • F-WP2# is common to all other flash dies, if present. Otherwise it is RFU. • For NOR/NAND stacked device, F-WP1# selects all NOR dies, while F-WP2# selects all NAND dies.	
F-DPD	Input	**FLASH DEEP POWER-DOWN:** Flash-specific signal; configurable-true input. When enabled in the ECR, F-DPD is used to enter and exit Deep Power-Down mode.	
N-CLE	Input	**NAND COMMAND LATCH ENABLE:** NAND-specific signal; high-true input. When high, N-CLE enables commands to be latched on the rising edge of N-WE#.	1
N-ALE	Input	**NAND ADDRESS LATCH ENABLE:** NAND-specific signal; high-true input. When high, N-ALE enables addresses to be latched on the rising edge of N-WE#.	1
N-RE#	Input	**NAND READ ENABLE:** NAND-specific signal; low-true input. When low, N-RE# enables the output drivers of the selected NAND die. When high, N-RE# disables the output drivers of the selected NAND die and places the output drivers in High-Z.	1, 2
N-RY/BY#	Output	**NAND READY/BUSY:** NAND-specific signal; low-true output. When low, N-RY/BY# indicates the NAND is busy performing a Read, Program, or Erase operation. When high, N-RY/BY# indicates the NAND device is ready.	1
N-WE#	Input	**NAND WRITE ENABLE:** NAND-specific signal; low-true input. When low, N-WE# enables Write operations for the enabled NAND die.	1, 4
P-CRE	Input	**PSRAM CONTROL REGISTER ENABLE:** Synchronous PSRAM-specific signal; high-true input. When high, P-CRE enables access to the Refresh Control Register (P-RCR) or Bus Control Register (P-BCR). When low, P-CRE enables normal Read or Write operations.	1, 3

Table 9. Signal Descriptions for x16C / x16C AD-Mux Ballout (Sheet 3 of 3)

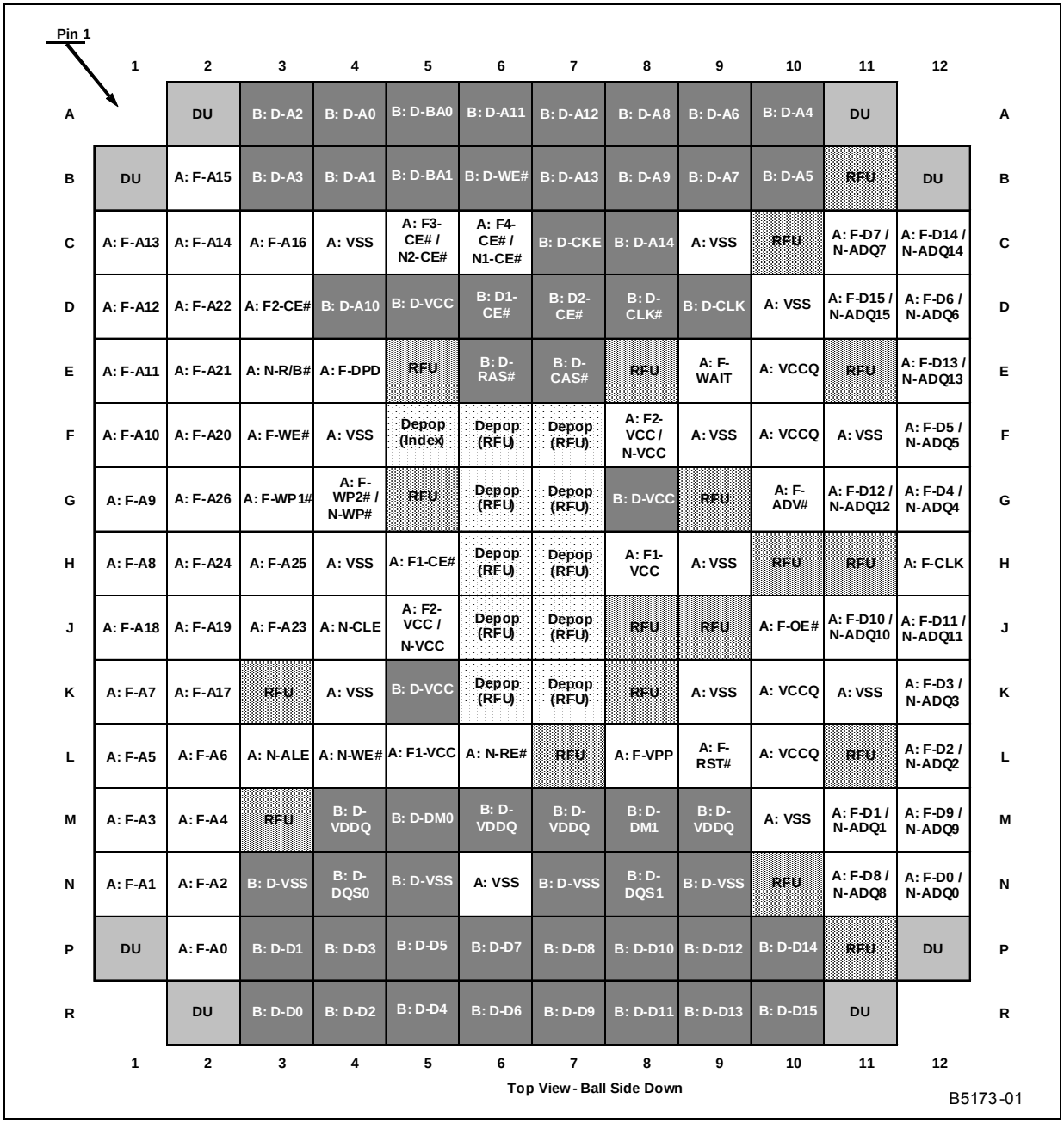
Symbol	Type	Signal Descriptions	Notes
P-MODE#	Input	**PSRAM MODE#:** Asynchronous only PSRAM-specific signal; low-true input. When low, P-MODE# enables access to the configuration register, and to enter or exit Low-Power mode. When high, P-MODE# enables normal Read or Write operations.	1, 3
P[2:1]-CS#	Input	**PSRAM CHIP SELECT:** PSRAM-specific signal; low-true input. When low, P-CS# selects the associated PSRAM memory die. When high, P-CS# deselects the associated PSRAM die. PSRAM die power is reduced to standby levels, and its data and WAIT outputs are placed in a High-Z state. • P1-CS# is dedicated to PSRAM die #1. • P2-CS# IS dedicated to PSRAM die #2. Otherwise, any unused PSRAM chip select should be treated as RFU.	1
S-CS1# S-CS2	Input	**SRAM CHIP SELECTS:** SRAM-specific signals; S-CS1# low-true input, S-CS2 high-true input. When both S-CS1# and S-CS2 are asserted, the SRAM die is selected. When either S-CS1# or S-CS2 is deasserted, the SRAM die is deselected.	1, 4
R-UB# R-LB#	Input	**RAM UPPER/LOWER BYTE ENABLES:** PSRAM- and SRAM-specific signals; low-true inputs. When low, R-UB# enables DQ[15:8] and R-LB# enables DQ[7:0] during PSRAM or SRAM Read and Write cycles. When high, R-UB# masks DQ[15:8] and R-LB# masks DQ[7:0].	1
Power Signals			
F-VPP	Power	**FLASH PROGRAM/ERASE VOLTAGE:** Flash specific. F-VPP supplies program or erase power to the flash die.	
F[2:1]-VCC	Power	**FLASH CORE POWER SUPPLY:** Flash specific. F[2:1]-VCC supplies the core power to the flash die. For NOR/NAND stacked device, F1-VCC is dedicated for all NOR dies, F2-VCC is dedicated for all NAND dies.	5
VCCQ	Power	**I/O POWER SUPPLY:** Global device I/O power. VCCQ supplies the device input/output driver voltage.	
P-VCC	Power	**PSRAM CORE POWER SUPPLY:** PSRAM specific. P-VCC supplies the core power to the PSRAM die.	1
S-VCC	Power	**SRAM POWER SUPPLY:** SRAM specific. S-VCC supplies the core power to the SRAM die.	1
VSS	Ground	**DEVICE GROUND:** Global ground reference for all signals and power supplies. Connect all VSS balls to system ground. Do not float any VSS connections.	
DU	—	**DO NOT USE:** This ball should not be connected to any power supplies, signals, or other balls. This ball can be left floating.	
RFU	—	**RESERVED for FUTURE USE:** Reserved by Intel for future device functionality and enhancement. This ball must be left floating.	

Notes:
1. Only available on stacked device combinations with NAND, SRAM, and/or LPSDRAM die. Otherwise treated as RFU.
2. F2-OE# and N-RE# share the same package ball at location H9. Only one signal function is available, depending on the stacked device combination.
3. P-CRE and P-MODE# share the same package ball at location K9. Only one signal function is available, depending on the stacked device combination.
4. S-CS1# and N-WE# share the same package ball at location J2. Only one signal function is available, depending on the stacked device combination.
5. The F2-VCC signal applies to a NAND flash die if one exists; if not, the F2-VCC signal applies to the NOR flash die.

4.5 Signal Ballouts x16 Split Bus

4.5.1 x16 Split Bus (165-Ball) Ballout, Non-Mux

Figure 13. x16 Split Bus (165 Active Ball) Electrical Ballout, Non-Mux



4.6 Signal Descriptions x16 Split Bus

Table 10. Signal Descriptions, x16 Split Bus, Non-Mux (Sheet 1 of 4)

Symbol	Type	Signal Descriptions	Notes
Address and Data Signals, Non-Mux			
F-A[MAX:0]	Input	FLASH ADDRESS: Flash device signals. Dedicated address inputs for Flash memory die during read and write operations. • 2-Gbit: AMAX = A26 • 1-Gbit: AMAX = A25 • 512-Mbit: AMAX = A24 • 256-Mbit: AMAX = A23 • 128-Mbit: AMAX = A22 Unused address inputs are RFU.	
D-A[MAX:0]	Input	LPSDRAM ADDRESS: LSPDRAM device signals. Dedicated address inputs for LPSDRAM memory die during read and write operations. • A[12:0] are the row and A[9:0] are the column addresses for 512-Mbit LPSDRAM. • A[12:0] are the row and A[8:0] are the column addresses for 256-Mbit LPSDRAM. • A[11:0] are the row and A[8:0] are the column addresses for 128-Mbit LPSDRAM. Unused address inputs are RFU.	
F-DQ[15:0]	Input/ Output	FLASH DATA INPUT/OUTPUTS: Flash device signals. • Inputs Flash data and commands during write cycles. • Outputs data during read cycles. • Data signals are High-Z when the device is deselected or its output is disabled.	
D-DQ[15:0]	Input/ Output	LPSDRAM DATA INPUT/OUTPUTS: LPSDRAM device signals. • Inputs LPSDRAM data and commands during write cycles. • Outputs data during read cycles. • Data signals are High-Z when the device is deselected or its output is disabled.	
Address and Data Signals, A/D Mux			
F-A[MAX:16]	Input	ADDRESS: Flash device signals. Shared address inputs for all Flash memory die during Read and Write operations. • 2-Gbit: AMAX = A26 • 1-Gbit: AMAX = A25 • 512-Mbit: AMAX = A24 • 256-Mbit: AMAX = A23 • 128-Mbit: AMAX = A22 Unused address inputs should be treated as RFU.	
F-ADQ[15:0]	Input / Output	ADDRESS-DATA MULTIPLEXED INPUTS/ OUTPUTS: AD-Mux flash lower address and data signals; LPSDRAM data signals. During AD-Mux flash Write cycles, ADQ[15:0] are used to input the lower address followed by commands or write-data. During AD-Mux flash Read cycles, ADQ[15:0] are used to input the lower address followed by read-data output. During LPSDRAM accesses, ADQ[15:0] are used to input commands and write-data during Write cycles or to output read-data during Read cycles. During NAND accesses, ADQ[7:0] are used to input commands, address, or write-data, and to output read-data. ADQ[15:0] are High-Z when the flash is deselected or its output is disabled.	
Control Signals			

Table 10. Signal Descriptions, x16 Split Bus, Non-Mux (Sheet 2 of 4)

Symbol	Type	Signal Descriptions	Notes
F-ADV#	Input	FLASH ADDRESS VALID: Flash-specific signal; low-true input. During synchronous flash Read operations, the address is latched on the rising edge of F-ADV#, or on the first rising edge of F-CLK after F-ADV# goes low for devices that support up to 108 MHz, or on the last rising edge of F-CLK after F-ADV# goes low for devices that support up to 133 MHz. In an asynchronous flash Read operation, the address is latched on the rising edge of F-ADV#.	
F[4:1]-CE#	Input	FLASH CHIP ENABLE: Flash-specific signal; low-true input. When low, F-CE# selects the associated flash memory die. When high, F-CE# deselects the associated flash die. Flash die power is reduced to standby levels, and its data and F-WAIT outputs are placed in a High-Z state. • F1-CE# is dedicated to flash die #1. • F[4:2]-CE# are dedicated to flash die #4 through #2, respectively, if present. Otherwise, treat any unused flash chip enable as RFU. • When NAND is used, F4-CE# is dedicated for NAND die 1 and NAND die 2. Otherwise, this is RFU.	
F-CLK	Input	FLASH CLOCK: Flash-specific signal; configurable active-edge input. F-CLK synchronizes the flash memory with the system clock during synchronous operations.	
D-CLK	Input	LPSDRAM CLOCK: LPSDRAM-specific signal; rising active-edge input. D-CLK synchronizes the LPSDRAM and DDR LPSDRAM with the system clock.	1
D-CLK#	Input	DDR LPSDRAM CLOCK: DDR LPSDRAM-specific signal; falling active-edge input. D-CLK# synchronizes the DDR LPSDRAM with the system clock.	1
F-OE#	Input	FLASH OUTPUT ENABLE: Flash-specific signal; low-true input. • When low, OE# enables the output drivers of the selected flash die. • When high, OE# disables the output drivers of the selected flash die and places the output drivers in High-Z.	
F-RST#	Input	FLASH RESET: Flash-specific signal; low-true input. • When low, F-RST# resets internal operations and inhibits writes. • When high, F-RST# enables normal operation.	
F-WAIT	Output	FLASH WAIT: Flash-specific signal; configurable-true output. When asserted, F-WAIT indicates invalid output data. • F-WAIT is driven whenever F-CE# and OE# is low. • F-WAIT is High-Z whenever F-CE# or OE# is high.	
F-WE#	Input	FLASH WRITE ENABLE: Flash-specific signal; low-true input. When low, WE# enables write operations for the selected flash die.	
N-WE#	Input	NAND WRITE ENABLE: NAND-specific signal; low-true input. When low, WE# enables write operations for the selected NAND die.	1
D-WE#	Input	LPSDRAM WRITE ENABLE: LPSDRAM-specific signal; low-true input. D-WE#, together with A[MAX:0], D-BA[1:0], D-CKE, D-CS#, D-CAS#, and D-RAS#, define the LPSDRAM command or operation. D-WE# is sampled on the rising edge of D-CLK.	1
F-WP[2:1]#	Input	FLASH WRITE PROTECT: Flash-specific signals; low-true inputs. When low, F-WP# enables the Lock-Down mechanism. When high, F-WP# overrides the Lock-Down function, enabling locked-down blocks to be unlocked with the Unlock command. • F-WP1# is dedicated to flash die #1. • F-WP2# is used for NAND die when available. Otherwise, this signal is for all other NOR die.	
F-DPD	Input	FLASH DEEP POWER-DOWN: Flash-specific signal; configurable-true input. When enabled in the ECR, F-DPD is used to enter or exit Deep Power-Down mode.	
N-CLE	Input	NAND COMMAND LATCH ENABLE: NAND-specific signal; high-true input. When high, N-CLE enables commands to be latched on the rising edge of WE#.	1

Table 10. Signal Descriptions, x16 Split Bus, Non-Mux (Sheet 3 of 4)

Symbol	Type	Signal Descriptions	Notes
N-ALE	Input	NAND ADDRESS LATCH ENABLE: NAND-specific signal; high-true input. When high, N-ALE enables addresses to be latched on the rising edge of WE#.	1
N-R/B#	Output	NAND READY/BUSY: NAND-specific signal; low-true output. • When low, N-RY/BY# indicates the NAND device is busy performing a read, program, or erase operations. • When high, N-RY/BY# indicates the NAND device is ready.	1
N-RE#	Output	NAND READ ENABLE: NAND-specific signal; drives the data onto the flash bus after the falling edge of N-RE#. This signal increments the internal column address and reads out each data.	1
D-CKE	Input	LPSDRAM CLOCK ENABLE: LPSDRAM-specific signal; high-true input. • When high, D-CKE indicates that the next D-CLK edge is valid. • When low, D-CKE indicates that the next D-CLK edge is invalid and the selected LPSDRAM die is suspended.	1
D-BA[1:0]	Input	LPSDRAM BANK SELECT: LPSDRAM-specific input signals. D-BA[1:0] selects one of four banks in the LPSDRAM die.	1
D-RAS#	Input	LPSDRAM ROW ADDRESS STROBE: LPSDRAM-specific signal; low-true input. D-RAS#, together with A[MAX:0], D-BA[1:0], D-CKE, D-CS#, D-CAS#, and D-WE#, define the LPSDRAM command or operation. D-RAS# is sampled on the rising edge of D-CLK.	1
D-CAS#	Input	LPSDRAM COLUMN ADDRESS STROBE: LPSDRAM-specific signal; low-true input. D-CAS#, together with A[MAX:0], D-BA[1:0], D-CKE, D-CS#, D-RAS#, and D-WE#, define the LPSDRAM command or operation. D-CAS# is sampled on the rising edge of D-CLK.	1
D[2:1]-CE#	Input	LPSDRAM CHIP ENABLE: LPSDRAM-specific signal; low-true input. When low, D-CS# selects the associated LPSDRAM memory die and starts the command input cycle. When D-CS# is high, commands are ignored but operations continue. • D-CS#, together with A[MAX:0], D-BA[1:0], D-CKE, D-RAS#, D-CAS#, and D-WE#, define the LPSDRAM command or operation. D-CS# is sampled on the rising edge of D-CLK. • D[2:1]-CS# are dedicated to LPSDRAM die #2 and die #1, respectively, if present. Otherwise, treat any unused LPSDRAM chip selects as RFU.	1
D-DM[1:0]	Input	LPSDRAM DATA MASK: LPSDRAM-specific signal; high-true input. When high, D-DM[1:0] controls masking of input data during writes and output data during reads. • D-DM1 corresponds to the data on DQ[15:8]. • D-DM0 corresponds to the data on DQ[7:0].	1
D-DQS1 D-DQS0	Input / Output	LPSDRAM UPPER/LOWER DATA STROBE: DDR LPSDRAM-specific input/output signals. D-DQS1 and D-DQS0 provide as output the read data strobes, and as input the write data strobes. • D-DQS1 corresponds to the data on DQ[15:8]. • D-DQS0 corresponds to the data on DQ[7:0].	1
Power Signals			
F-VPP	Power	FLASH PROGRAM/ERASE VOLTAGE: Flash specific. F-VPP supplies program or erase power to the flash die.	
F[2:1]-VCC	Power	FLASH CORE POWER SUPPLY: Flash specific. F-VCC supplies the core power to the flash die. • F1-VCC is dedicated for NOR die. • F2-VCC is used for NAND die when available. Otherwise, this signal is for NOR die. (When NAND is available, the F2-VCC signal is named N-VCC.)	
D-VCC	Power	LPSDRAM CORE POWER SUPPLY: LPSDRAM specific. D-VCC supplies the core power to the LPSDRAM die.	1
VCCQ	Power	FLASH I/O POWER SUPPLY: Global device I/O power. VCCQ supplies the device input/output driver voltage to the flash die.	

Table 10. Signal Descriptions, x16 Split Bus, Non-Mux (Sheet 4 of 4)

Symbol	Type	Signal Descriptions	Notes
D-VDDQ	Power	LPSDRAM I/O POWER SUPPLY: Global device I/O power. VDDQ supplies the device input/output driver voltage to the LPSDRAM die.	1
VSS	Ground	FLASH DEVICE GROUND: Global ground reference for all flash signals and power supplies. Connect all A: VSS balls to system ground. Do not float any VSS connections.	
D-VSS	Ground	LPSDRAM DEVICE GROUND: Global ground reference for all LPSDRAM signals and power supplies. Connect all B: D-VSS balls to system ground. Do not float any VSS connections.	1
DU	—	DO NOT USE: Do not connect this ball to any power supplies, signals, or other balls. This ball can be left floating.	
RFU	—	RESERVED for FUTURE USE: Reserved by Intel for future device functionality and enhancement. This ball must be left floating.	

Notes:
6. Available only on stacked device combinations with NAND, and/or LPSDRAM die. Otherwise, treat the signal as RFU.

5.0 Maximum Ratings and Operating Conditions

5.1 Absolute Maximum Ratings

Warning: Stressing the device beyond the Absolute Maximum Ratings may cause permanent damage. These are stress ratings only.

NOTICE: This document contains information available at the time of its release. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

Table 11. Absolute Maximum Ratings

Parameter	Min	Max	Unit	Conditions	Notes
Temperature under Bias Expanded	–30	+85	°C	—	—
Storage Temperature	–65	+125	°C	—	—
F-VCC Voltage	–2.0	V_{CCQ} + 2.0	V	—	1,2
VCCQ	–2.0	V_{CCQ} + 2.0	V	—	1,3
Voltage on any input/output signal (except VCC, VCCQ, and VPP)	–2.0	V_{CCQ} + 2.0	V	—	1,3
F-VPP Voltage	–2.0	+11.5	V	—	1,3
I_{SH} Output Short Circuit Current	—	100	mA	—	4
V_{PPH} Time	—	80	Hours		5
Block Program/Erase Cycles: Main Blocks	100,000	—	Cycles	F-VPP = V_{CC} or F-VPP = V_{PPH}	5

Notes:
1. Voltage is referenced to V_{SS}.
2. During signal transitions, minimum DC voltage may undershoot to –2.0 V for periods < 20 ns; maximum DC voltage may overshoot to V_{CC} (max) + 2.0 V for periods < 20 ns.
3. During signal transitions, minimum DC voltage may undershoot to –1.0 V for periods < 20 ns; maximum DC voltage may overshoot to V_{CCQ} (max) + 1.0 V for periods < 20 ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.
5. Operation beyond this limit may degrade performance.

5.2 Operating Conditions

Warning: Operation beyond the “Operating Conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

Table 12. Operating Conditions

Symbol	Description	Min	Max	Unit	Conditions
T_C	Operating Temperature (Case Temperature)	–30	+85	°C	—
V_{CC}	VCC Supply Voltage	+1.7	+2.0	V	—
V_{CCQ}	I/O Supply Voltage	+1.7	+2.0	V	—
V_{PPL}	Programming Voltage (Logic Level)	+0.9	+2.0	V	—
V_{PPH}	Factory Programming Voltage (High Level)	+8.5	+9.5	V	—

6.0 Electrical Characteristics

6.1 DC Current Specifications

Table 13. DC Current Specifications, 90 nm and 65 nm (Sheet 1 of 3)

Sym	Parameter		Density	1.7 V – 2.0 V		Unit	Test Conditions	Notes
				Typ	Max			
I_{LI}	Input Load Current			—	±1	µA	V_{CC} = V_{CC} Max V_{CCQ} = V_{CCQ} Max V_{IN} = V_{CCQ} or V_{SS}	1
I_{LO}	Output Leakage Current			—	±1	µA	V_{CC} = V_{CC} Max V_{CCQ} = V_{CCQ} Max V_{IN} = V_{CCQ} or V_{SS}	
I_{CCS}	V_{CC} Standby		256-Mbit (90 nm) 512-Mbit (90 nm) 1-Gbit (65 nm)	35 50 70	95 120 185	µA	V_{CC} = V_{CC}Max V_{CCQ} = V_{CCQ}Max CE# = V_{CCQ} RST# = V_{CCQ} or GND (for I_{CCS}) WP# = V_{IH}	1,2
I_{CCAPS}	APS		256-Mb (90 nm) 512-Mb (90 nm) 1-Gbit (65 nm)	35 50 70	95 120 185	µA	V_{CC} = V_{CC} Max V_{CCQ} = V_{CCQ} Max CE# = V_{SSQ} RST# = V_{CCQ} All inputs are at rail to rail (V_{CCQ} or V_{SSQ}).	—
I_{DPD}	DPD		256-Mb (90 nm) 512-Mb (90 nm) 1-Gbit (65 nm)	2	30	µA	V_{CC} = V_{CC} Max V_{CCQ} = V_{CCQ} Max CE# = V_{CCQ} RST# = V_{CCQ} ECR[15] = V_{CCQ} DPD = V_{CCQ} or V_{SSQ} All inputs are at rail to rail (V_{CCQ} or V_{SSQ}).	8
I_{CCR}	Average V_{CC} Read: Asynchronous Single Word Read f = 5 MHz, (1 CLK)		256-Mb (90 nm) 512-Mb (90 nm) 1-Gbit (65 nm)	25	30	mA	V_{CC} = V_{CC}MAX CE# = V_{IL} OE# = V_{IH} Inputs: V_{IL} or V_{IH}	1,3, 4,5
I_{CCR}	Average V_{CC} Read: Page Mode Read f = 13 MHz, (17 CLK)	Burst = 16 Word	256-Mb (90 nm) 512-Mb (90 nm) 1-Gbit (65 nm)	11	15	mA	V_{CC} = V_{CC}MAX CE# = V_{IL} OE# = V_{IH} Inputs: V_{IL} or V_{IH}	1,3, 4,5

Table 13. DC Current Specifications, 90 nm and 65 nm (Sheet 2 of 3)

Sym	Parameter		Density	1.7 V – 2.0 V		Unit	Test Conditions	Notes
				Typ	Max			
I_{CCR}	Average V_{CC} Read: Synchronous Burst Read f = 66 MHz, LC = 7	Burst = 8 Word	256-Mb (90 nm) 512-Mb (90 nm) 1-Gbit (65 nm)	22	32	mA	V_{CC} = V_{CC}MAX CE# = V_{IL} OE# = V_{IH} Inputs: V_{IL} or V_{IH}	1,3, 4,5
		Burst = 16 Word	256-Mb (90 nm) 512-Mb (90 nm) 1-Gbit (65 nm)	19	26	mA		
		Burst = Continuous	256-Mb (90 nm) 512-Mb (90 nm) 1-Gbit (65 nm)	25	34	mA		
I_{CCR}	Average V_{CC} Read: Synchronous Burst Read f = 108 MHz, LC = 10	Burst = 8 Word	256-Mb (90 nm) 512-Mb (90 nm) 1-Gbit (65 nm)	26	36	mA	V_{CC} = V_{CC}MAX CE# = V_{IL} OE# = V_{IH} Inputs: V_{IL} or V_{IH}	1,3, 4,5
		Burst = 16 Word	256-Mb (90 nm) 512-Mb (90 nm) 1-Gbit	23	30	mA		
		Burst = Continuous	256-Mb (90 nm) 512-Mb (90 nm) 1-Gbit (65 nm)	30	42	mA		
I_{CCR}	Average V_{CC} Read: Synchronous Burst Read f = 133 MHz, LC = 13	Burst = 8 Word	256-Mb (90 nm) 512-Mb (90 nm) 1-Gbit (65 nm)	26	35	mA	V_{CC} = V_{CC}MAX CE# = V_{IL} OE# = V_{IH} Inputs: V_{IL} or V_{IH}	1,3, 4,5
		Burst = 16 Word	256-Mb (90 nm) 512-Mb (90 nm) 1-Gbit (65 nm)	24	33	mA		
		Burst = Continuous	256-Mb (90 nm) 512-Mb (90 nm) 1-Gbit (65 nm)	33	46	mA		
I_{CCW}, I_{CCE} I_{CCBC}	V_{CC} Program V_{CC} Erase V_{CC} Blank Check			35	50	mA	V_{PP} = V_{PPL} or V_{PP} = V_{PPH}, program/erase in progress	1,3,4, 5,7

Table 13. DC Current Specifications, 90 nm and 65 nm (Sheet 3 of 3)

Sym	Parameter	Density	1.7 V – 2.0 V		Unit	Test Conditions	Notes
			Typ	Max			
I_{CCWS}, I_{CCES}	V_{CC} Program Suspend V_{CC} Erase Suspend	256-Mb (90 nm)	35	95	µA	CE# = V_{CCQ}; suspend in progress	1,3,6
		512-Mb (90 nm)	50	120			
		1-Gbit (65 nm)	70	185			
I_{PPS}, I_{PPWS}, I_{PPES}	V_{PP} Standby V_{PP} Program Suspend V_{PP} Erase Suspend		0.2	5	µA	V_{PP} = V_{PPL}; suspend in progress	3
I_{PPR}	V_{PP} Read		2	15	µA	$V_{PP} \le V_{CC}$	3
I_{PPW}	V_{PP} Program		0.05	0.1	mA	V_{PP} = V_{PPL} = V_{PPH}, program in progress	3
I_{PPE}	V_{PP} Erase		0.05	0.1	mA	V_{PP} = V_{PPL} = V_{PPH}, erase in progress	3
I_{PPBC}	V_{PP} Blank Check		0.05	0.1	mA	V_{PP} = V_{PPL} = V_{PPH}, blank check in progress	3

Notes:
1. All currents are RMS unless noted. Typical values at typical V_{CC}, T_C = +25 °C.
2. I_{CCS} is the average current measured over any 5 ms time interval 5 µs after CE# is deasserted.
3. Sampled, not 100% tested.
4. V_{CC} read + program current is the sum of V_{CC} read and V_{CC} program currents.
5. V_{CC} read + erase current is the sum of V_{CC} read and V_{CC} erase currents.
6. I_{CCES} is specified with the device deselected. If device is read while in erase suspend, current is I_{CCES} plus I_{CCR}
7. I_{CCW}, I_{CCE} measured over typical or max times specified in Section 7.4, "Program and Erase Characteristics" on page 67
8. I_{DPD} is the current measured 40 µs after entering DPD.

6.2 DC Voltage Specifications

Table 14. DC Voltage Specifications

Symbol	Parameter	V_{CCQ}	1.7 V – 2.0 V		Unit	Test Condition	Notes
			Min	Max			
V_{IL}	Input Low Voltage		0	0.4	V	—	1
V_{IH}	Input High Voltage		V_{CCQ} –0.4	V_{CCQ}		—	—
V_{OL}	Output Low Voltage		—	0.1		V_{CC} = V_{CC}MIN V_{CCQ} = V_{CCQ}MIN I_{OL} = 100 µA	—
V_{OH}	Output High Voltage		V_{CCQ} –0.1	—		V_{CC} = V_{CC}MIN V_{CCQ} = V_{CCQ}MIN I_{OH} = –100 µA	—
V_{PPLK}	V_{PP} Lock-Out Voltage		—	0.4		—	2
V_{LKO}	V_{CC} Lock Voltage		1.0	—		—	—
V_{LKOQ}	V_{CCQ} Lock Voltage		0.9	—		—	—

Notes:
1. During signal transitions, voltage can undershoot to –1.0 V and overshoot to maximum V_{CCQ}+1.0 V for durations of < 2 ns.
2. $V_{PP} \le V_{PPLK}$ inhibits erase and program operations. Do not use V_{PPL} and V_{PPH} outside their valid ranges.

6.3 Capacitance

Table 15. Capacitance

Symbol	Parameter	Min	Typ	Max	Unit	Condition	Notes
C_{IN}	Input Capacitance (Address, CLK, CE#, OE#, ADV#, WE#, WP#, DPD and RST#)	2	4	6	pF	V_{IN} = 0 - 2.0 V	1,2
C_{OUT}	Output Capacitance (Data and WAIT)	2	5	6		V_{OUT} = 0 - 2.0 V	

Notes:
1. T_C = +25°C, f = 1 MHz.
2. Sampled, not 100% tested.

7.0 NOR Flash AC Characteristics

Timing symbols used in the timing diagrams within this document conform to the following conventions:

Figure 14. Timing Symbol Notation Convention

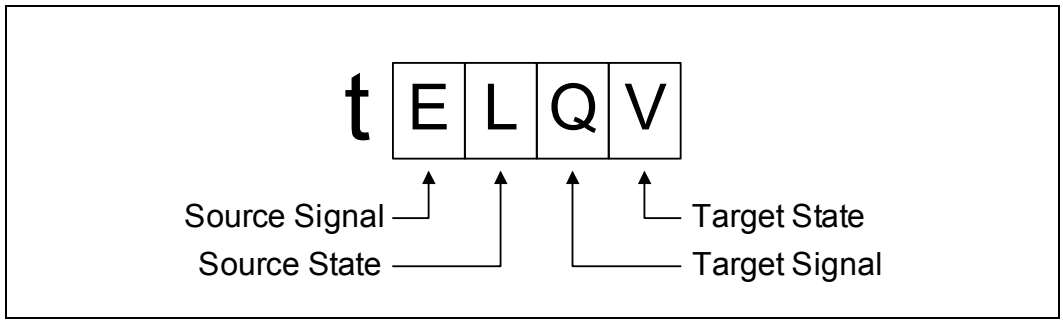


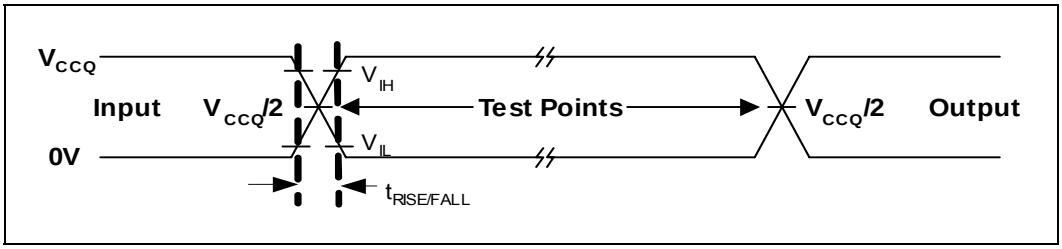
Table 16. Codes for Timing Signals and Timing States

Signal	Code	State	Code
Address	A	High	H
Data - Read	Q	Low	L
Data - Write	D	High-Z	Z
Chip Enable (CE#)	E	Low-Z	X
Output Enable (OE#)	G	Valid	V
Write Enable (WE#)	W	Invalid	I
Address Valid (ADV#)	V	—	—
Reset (RST#)	P	—	—
Clock (CLK)	C	—	—
WAIT	T	—	—

Note: Exceptions to this conventions include tACC and tAPA. tACC is a generic timing symbol that refers to the aggregate initial-access delay as determined by tAVQV, tELQV, and tGLQV (whichever is satisfied last) of the flash device. tAPA is specified in the flash device datasheet, and is the address-to-data delay for subsequent page-mode reads.

7.1 AC Test Conditions

Figure 15. AC Input/Output Reference Waveform

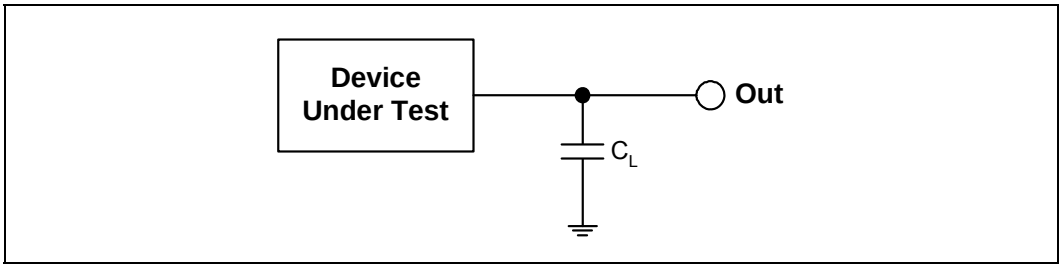


Note: AC test inputs are driven at V_{CCQ} for Logic '1' and 0.0 V for Logic '0'. Input/output timing begins and ends at $V_{CCQ}/2$.

Table 17. AC Input Requirements

Symbol	Parameter	Frequency	Min	Max	Unit	Condition
$t_{RISE/FALL}$	Inputs rise/fall time (Address, CLK, CE#, OE#, ADV#, WE#, WP#)	133MHz, 108MHz	0.3	1.2	ns	V_{IL} to V_{IH} or V_{IH} to V_{IL}
		@66MHz	0	3		
t_{ASKW}	Address-Address skew		0	3		At $V_{CCQ}/2$

Figure 16. Transient Equivalent Testing Load Circuit

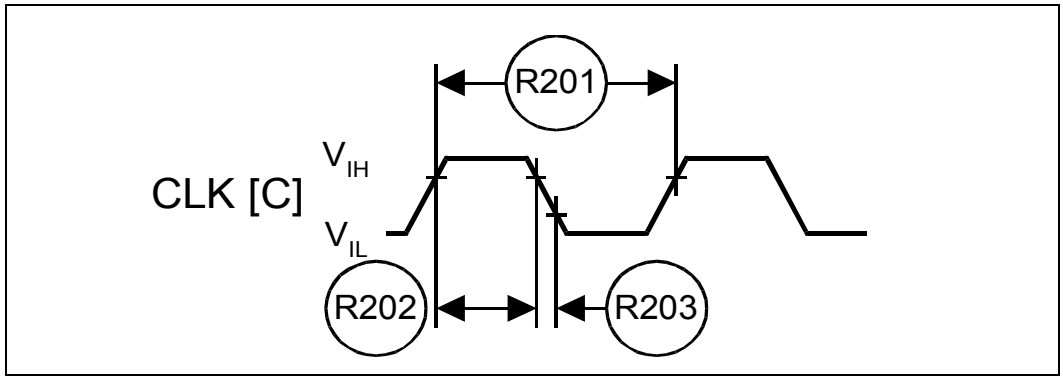


Notes:
1. See the following table for component values.
2. Test configuration component value for worst case speed conditions.
3. C_L includes jig capacitance.

Table 18. Test Configuration Component Value for Worst Case Speed Conditions

Test Configuration	C_L (pF)
1.7 V Standard Test	30
2.0 V Standard Test	30

Figure 17. Clock Input AC Waveform



7.2 Read Specifications

The M18 device includes read specifications for the following speeds and voltage levels:

- 512-Mbit device: 108 MHz, V_{CCQ} = 1.7 V to 2.0 V
- 1-Gbit device: 108 MHz, V_{CCQ} = 1.7 V to 2.0 V
- 256-Mbit device: 133 MHz, V_{CCQ} = 1.7 V to 2.0 V

Devices which support frequencies up to 133 MHz must meet additional timing specifications for synchronous reads (for address latching with CLK) as listed in Table 20.

Table 19. AC Read, 512-Mbit, 1-Gbit, 108 MHz, V_{CCQ} = 1.7 V to 2.0 V (Sheet 1 of 2)

Nbr.	Symbol	Parameter[1]	96 ns		Unit	Notes
			Min	Max		
Asynchronous Specifications						
R1	t_{AVAV}	Read cycle time	96	—	ns	—
R2	t_{AVQV}	Address to output valid	—	96	ns	—
R3	t_{ELQV}	CE# low to output valid	—	96	ns	—
R4	t_{GLQV}	OE# low to output valid	—	20	ns	2
R5	t_{PHQV}	RST# high to output valid	—	150	ns	—
R6	t_{ELQX}	CE# low to output in low-Z	0	—	ns	3
R7	t_{GLQX}	OE# low to output in low-Z	0	—	ns	2,3
R8	t_{EHQZ}	CE# high to output in high-Z	—	9	ns	3
R9	t_{GHQZ}	OE# high to output in high-Z	—	9	ns	
R10	t_{OH}	Output hold from first occurring address, CE#, or OE# change	0	—	ns	
R11	t_{EHEL}	CE# pulse width high	7	—	ns	—
R12	t_{ELTV}	CE# low to WAIT valid	—	11	ns	—
R13	t_{EHTZ}	CE# high to WAIT high Z	—	9	ns	3
R14	t_{GHTV}	OE# high to WAIT valid (AD-Mux only)	—	7	ns	—
R15	t_{GLTV}	OE# low to WAIT valid	—	7	ns	—

Table 19. AC Read, 512-Mbit, 1-Gbit, 108 MHz, V_{CCQ} = 1.7 V to 2.0 V (Sheet 2 of 2)

Nbr.	Symbol	Parameter[1]	96 ns		Unit	Notes
			Min	Max		
R16	t_{GLTX}	OE# low to WAIT in low-Z	0	—	ns	3
R17	t_{GHTZ}	OE# low to WAIT in high-Z (non-mux only)	0	9	ns	3
Latching Specifications						
R101	t_{AVVH}	Address setup to ADV# high	5	—	ns	—
R102	t_{ELVH}	CE# low to ADV# high	9	—	ns	—
R103	t_{VLQV}	ADV# low to output valid	—	96	ns	—
R104	t_{VLVH}	ADV# pulse width low	7	—	ns	—
R105	t_{VHVL}	ADV# pulse width high	7	—	ns	—
R106	t_{VHAX}	Address hold from ADV# high	5	—	ns	4
R107	t_{VHGL}	ADV# high to OE# low (AD-Mux only)	7	—	ns	—
R108	t_{APA}	Page address access (non-mux only)	—	15	ns	—
R111	t_{PHVH}	RST# high to ADV# high	30	—	ns	—
Clock Specifications						
R200	f_{CLK}	CLK frequency	—	108	MHz	—
R201	t_{CLK}	CLK period	9.26	—	ns	—
R202	$t_{CH/CL}$	CLK high/low time	3.5	—	ns	—
R203	$t_{FCLK/RCLK}$	CLK fall/rise time	0.3	1.2	ns	—
Synchronous Specifications						
R301	t_{AVCH}	Address setup to CLK high	5	—	ns	—
R302	t_{VLCH}	ADV# low setup to CLK high	5	—	ns	—
R303	t_{ELCH}	CE# low setup to CLK high	5	—	ns	—
R304	t_{CHQV}	CLK to output valid	—	7	ns	—
R305	t_{CHQX}	Output hold from CLK high	2	—	ns	—
R306	t_{CHAX}	Address hold from CLK high	5	—	ns	4
R307	t_{CHTV}	CLK high to WAIT valid	—	7	ns	—
R311	t_{CHVL}	CLK high to ADV# Setup	2	—	ns	—
R312	t_{CHTX}	WAIT hold from CLK	2	—	ns	—

Notes:

1. See Figure 15, "AC Input/Output Reference Waveform" on page 46 for timing measurements and maximum allowable input slew rate.
2. OE# may be delayed by up to $t_{ELQV} - t_{GLQV}$ after CE#'s falling edge without impact to t_{ELQV}.
3. Sampled, not 100% tested.
4. Address hold in synchronous burst mode is t_{CHAX} or t_{VHAX}, whichever timing specification is satisfied first.

Table 20. AC Read, 256-Mbit, 133 MHz, V_{CCQ} = 1.7 V to 2.0 V (Sheet 1 of 2)

Nbr.	Symbol	Parameter[1]	96 ns		Units	Notes
			Min	Max		
Asynchronous Specifications						
R1	t_{AVAV}	Read cycle time	96	—	ns	—
R2	t_{AVQV}	Address to output valid	—	96	ns	—
R3	t_{ELQV}	CE# low to output valid	—	96	ns	—
R4	t_{GLQV}	OE# low to output valid	—	7	ns	2
R5	t_{PHQV}	RST# high to output valid	—	150	ns	—
R6	t_{ELQX}	CE# low to output in low-Z	0	—	ns	3
R7	t_{GLQX}	OE# low to output in low-Z	0	—	ns	2,3
R8	t_{EHQZ}	CE# high to output in high-Z	—	7	ns	3
R9	t_{GHQZ}	OE# high to output in high-Z	—	7	ns	
R10	t_{OH}	Output hold from first occurring address, CE#, or OE# change	0	—	ns	
R11	t_{EHEL}	CE# pulse width high	7	—	ns	—
R12	t_{ELTV}	CE# low to WAIT valid	—	8	ns	—
R13	t_{EHTZ}	CE# high to WAIT high Z	—	7	ns	3
R14	t_{GHTV}	OE# high to WAIT valid (AD-Mux only)	—	5.5	ns	—
R15	t_{GLTV}	OE# low to WAIT valid	—	5.5	ns	—
R16	t_{GLTX}	OE# low to WAIT in low-Z	0	—	ns	3
R17	t_{GHTZ}	OE# high to WAIT in high-Z (non-mux only)	0	7	ns	3
Latching Specifications						
R101	t_{AVVH}	Address setup to ADV# high	5	—	ns	—
R102	t_{ELVH}	CE# low to ADV# high	7	—	ns	—
R103	t_{VLQV}	ADV# low to output valid		96	ns	—
R104	t_{VLVH}	ADV# pulse width low	7	—	ns	—
R105	t_{VHVL}	ADV# pulse width high	7	—	ns	—
R106	t_{VHAX}	Address hold from ADV# high	5	—	ns	—
R107	t_{VHGL}	ADV# high to OE# low (AD-Mux only)	2	—	ns	—
R108	t_{APA}	Page address access (non-mux only)	—	15	ns	—
R111	t_{PHVH}	RST# high to ADV# high	30	—	ns	—
Clock Specifications						
R200	f_{CLK}	CLK frequency	—	133	MHz	—
R201	t_{CLK}	CLK period	7.5	—	ns	—
R202	$t_{CH/CL}$	CLK high/low time	3.2	—	ns	—
R203	$t_{FCLK/RCLK}$	CLK fall/rise time	0.3	1.2	ns	—
Synchronous Specifications						
R301	t_{AVCH}	Address setup to CLK high	2	—	ns	—
R302	t_{VLCH}	ADV# low setup to CLK high	2	—	ns	—

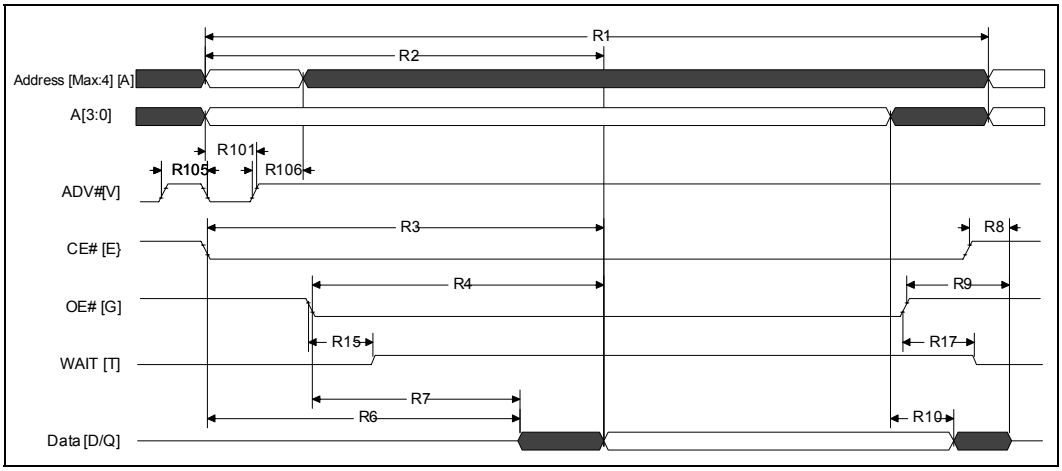
Table 20. AC Read, 256-Mbit, 133 MHz, V_{CCQ} = 1.7 V to 2.0 V (Sheet 2 of 2)

Nbr.	Symbol	Parameter[1]	96 ns		Units	Notes
			Min	Max		
R303	t_{ELCH}	CE# low setup to CLK high	2.5	—	ns	—
R304	t_{CHQV}	CLK to output valid	—	5.5	ns	—
R305	t_{CHQX}	Output hold from CLK high	2	—	ns	—
R306	t_{CHAX}	Address hold from CLK high	2	—	ns	—
R307	t_{CHTV}	CLK high to WAIT valid	—	5.5	ns	—
R311	t_{CHVL}	CLK high to ADV# Setup	2	—	ns	—
R312	t_{CHTX}	WAIT hold from CLK high	2	—	ns	—
R313	t_{CHVH}	ADV# hold from CLK high	2	—	ns	—
R314	t_{CHGL}	CLK to OE# low (AD-Mux only)	2	—	ns	—
R315	t_{ACC}	Read access time from address latching clock	96	—	ns	—
R316	t_{VLVH}	ADV# pulse width low for sync reads	1	2	clks	—
R317	t_{VHCH}	ADV# high to CLK high	2	—	ns	—

Notes:
1. See Figure 15, "AC Input/Output Reference Waveform" on page 46 for timing measurements and maximum allowable input slew rate.
2. OE# may be delayed by up to $t_{ELQV} - t_{GLQV}$ after CE#'s falling edge without impact to t_{ELQV}.
3. Sampled, not 100% tested.

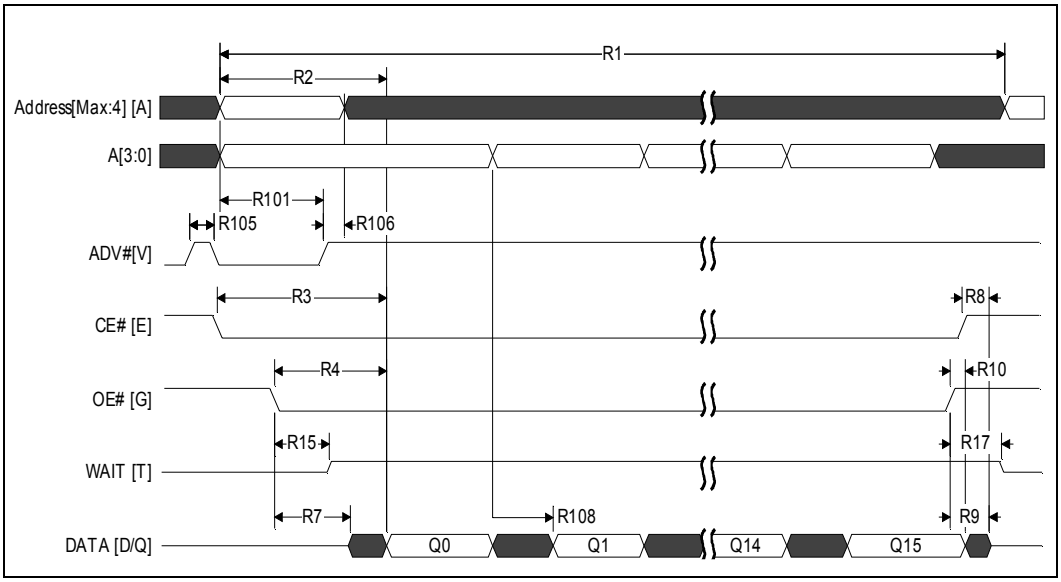
7.2.1 Timings: Non Mux Device, Async Read

Figure 18. Async Single-Word Read: ADV# Latch



Note: WAIT polarity in figure is low-true (RCR10 = 0, default). WAIT deasserted during asynchronous reads.

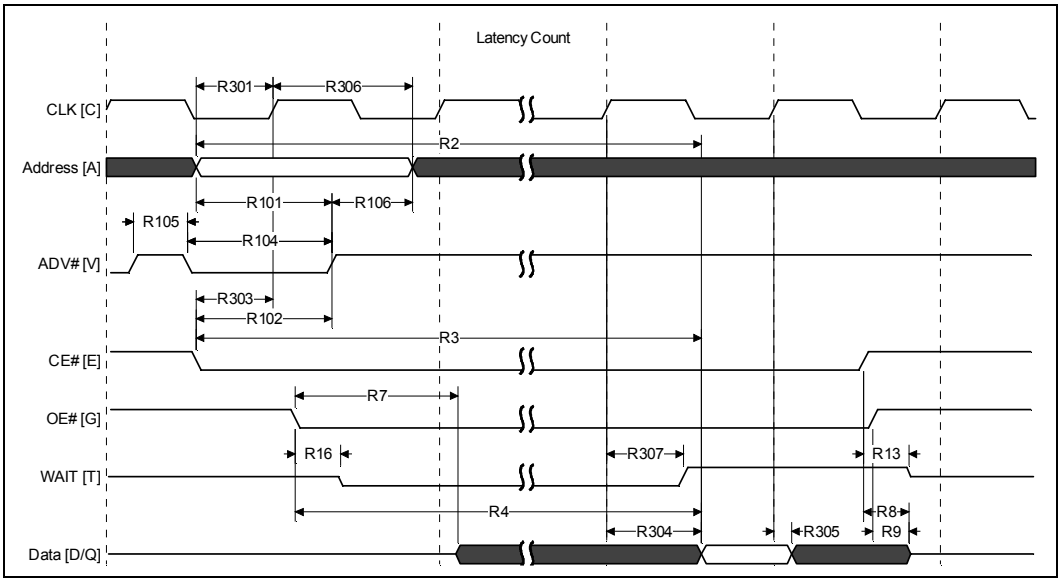
Figure 19. Async Page-Mode Read Timing



Note: WAIT polarity in figure is low-true (RCR10 = 0, default). WAIT deasserted during asynchronous reads.

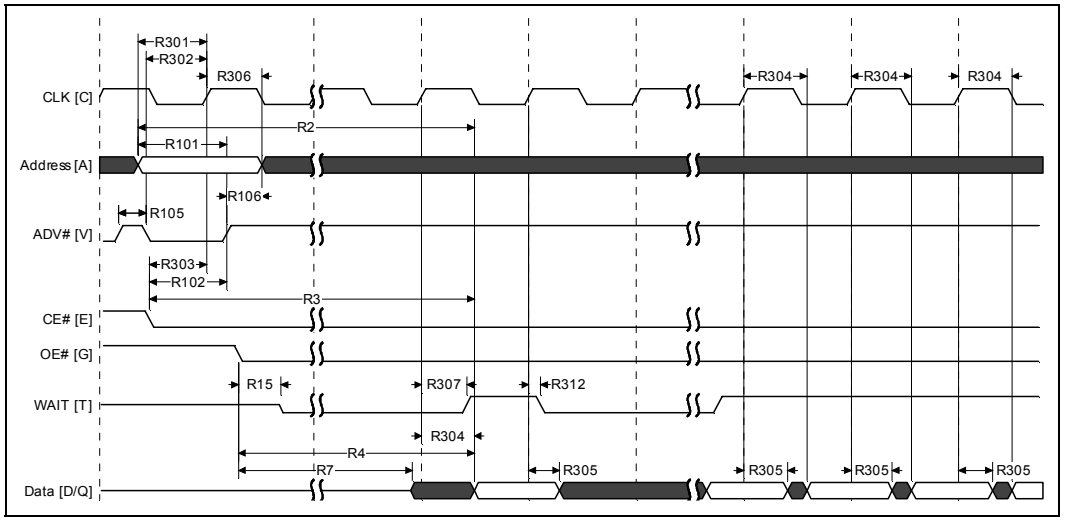
7.2.2 Timings: Non Mux Device, Sync Read, 512-Mbit, 1-Gbit, 108 MHz

Figure 20. Sync Single-Word Array / Non-Array Read, 512-Mbit, 1-Gbit, 108 MHz



Notes:
1. WAIT polarity in figure is low-true (RCR10 = 0, default)
2. This figure illustrates the case in which an n-word burst is initiated to the flash memory array and it is terminated by OE# and CE# deassertion after the first word in the burst.
3. Address latched on rising CLK edge after ADV# low.

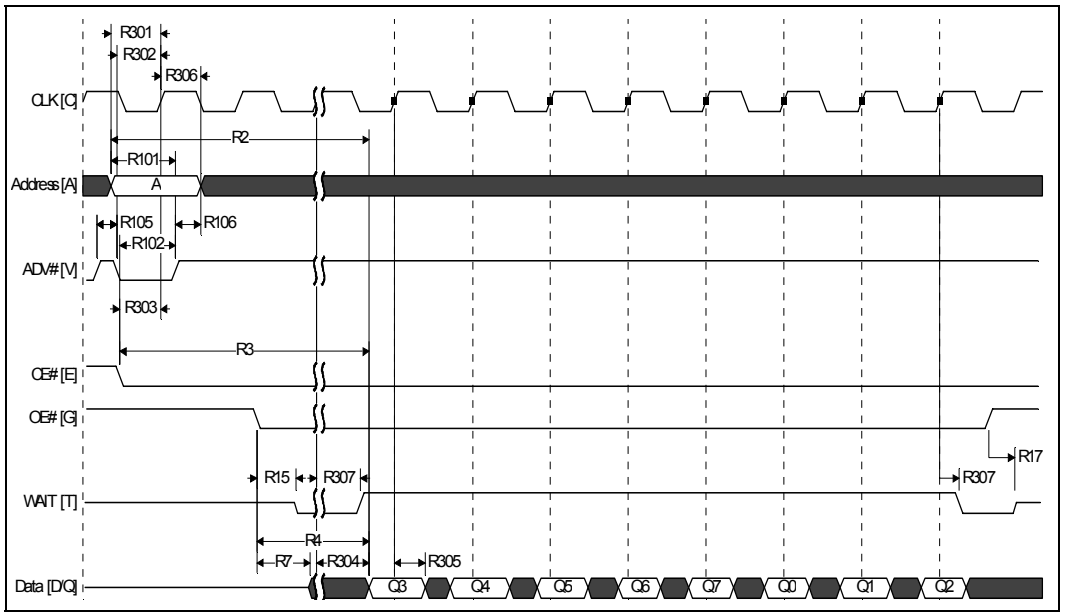
Figure 21. Continuous Burst Read: Output Delay at EOWL, 512-Mbit, 1-Gbit, 108 MHz



Notes:

1. At the End of Word Line (EOWL); the delay incurred when a burst access crosses a 16-word boundary and the starting address is not 16-word boundary aligned.
2. WAIT polarity in figure is low-true (RCR10 = 0, default).
3. Address latched on rising CLK edge after ADV# low.

Figure 22. Sync Burst-Mode Unaligned 8-Word Burst Read, 512-Mbit, 1-Gbit, 108 MHz

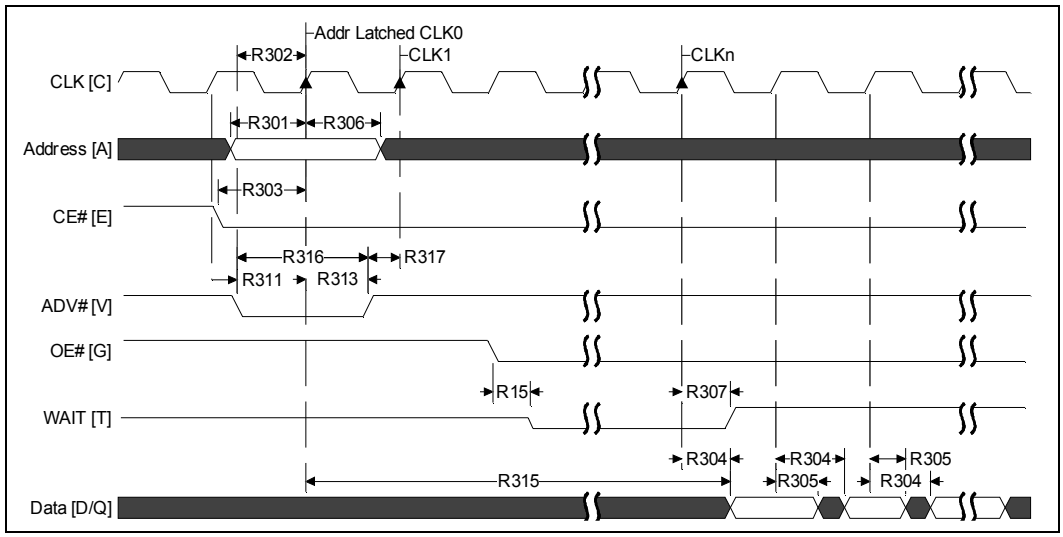


Notes:

1. WAIT polarity in figure is low-true (RCR10 = 0, default).
2. 8-word and 16-word burst are always wrap-only.
3. Address latched on rising CLK edge after ADV# low.

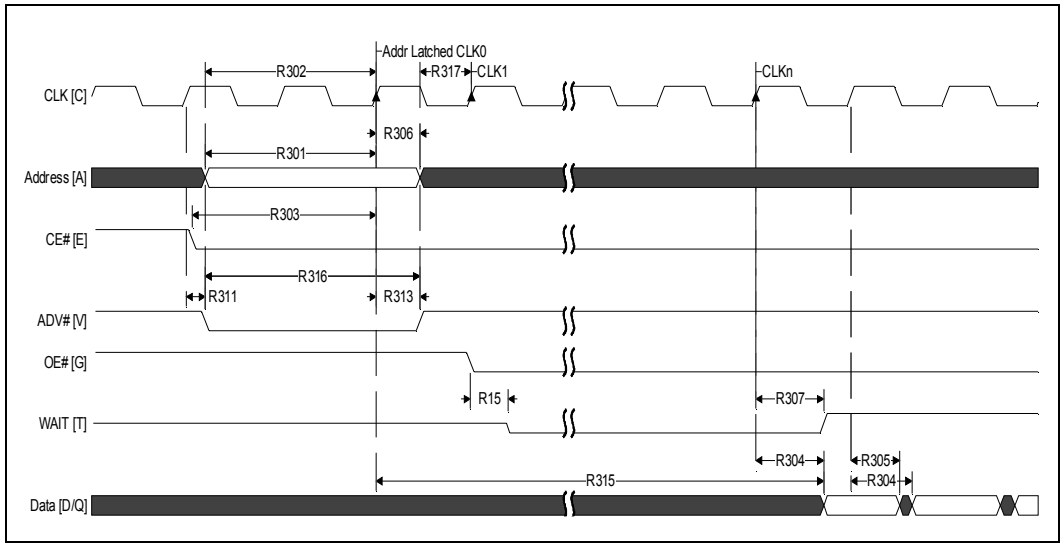
7.2.3 Timings: Non Mux Device, Sync Read, 256-Mbit, 133 MHz

Figure 23. Sync Array/Non-Array Read, 256-Mbit, 133 MHz



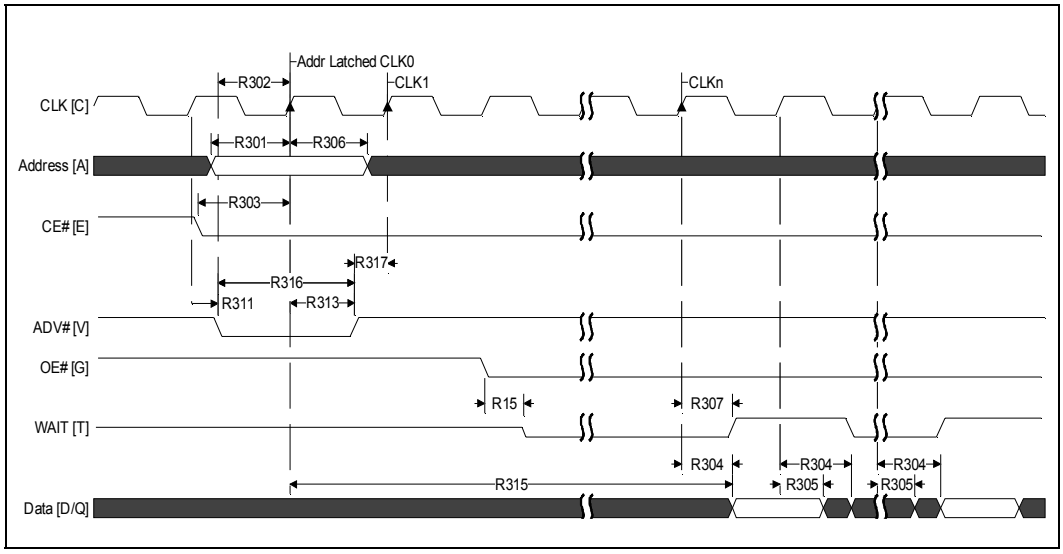
Notes:
1. Address is latched on first CLK edge after ADV# assertion, associated setup and hold timings shown.
2. WAIT polarity in figure is low-true (RCR10 = 0, default).

Figure 24. Sync Array/Non-Array Read: ADV# Max Low Pulse Width, 256-Mbit, 133 MHz



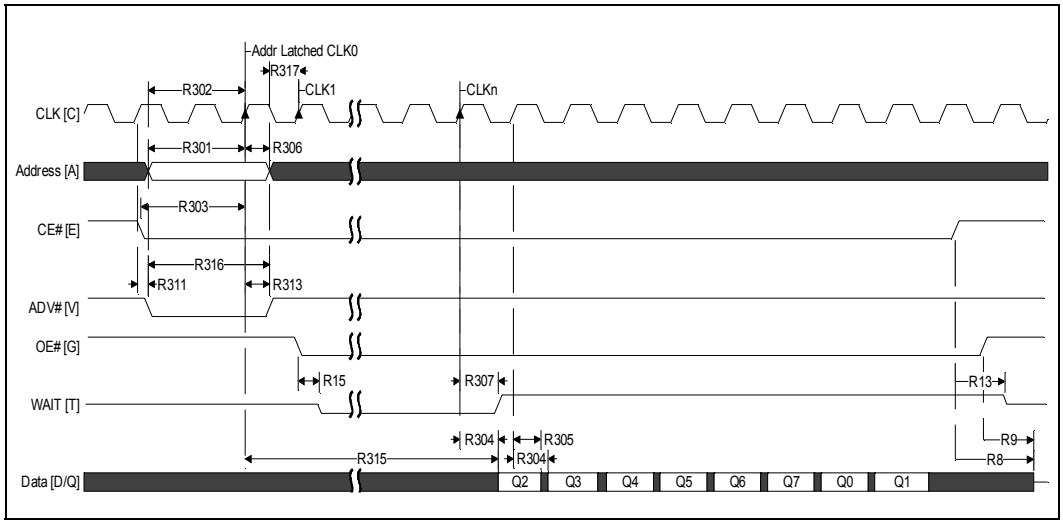
Notes:
1. Address is latched on the second rising CLK edge after ADV# assertion, associated setup and hold timing shown.
2. WAIT polarity in figure is low-true (RCR10 = 0, default).

Figure 25. Continuous Burst Read: Output Delay at EOWL, 256-Mbit, 133 MHz



Notes:
1. At the End of Word Line (EOWL); the delay incurred when a burst access crosses a 16-word boundary and the starting address is not 16-word boundary aligned.
2. WAIT polarity in figure is low-true (RCR10 = 0, default).
3. Address is latched on the first rising CLK edge after ADV# assertion, associated setup and hold timing shown.

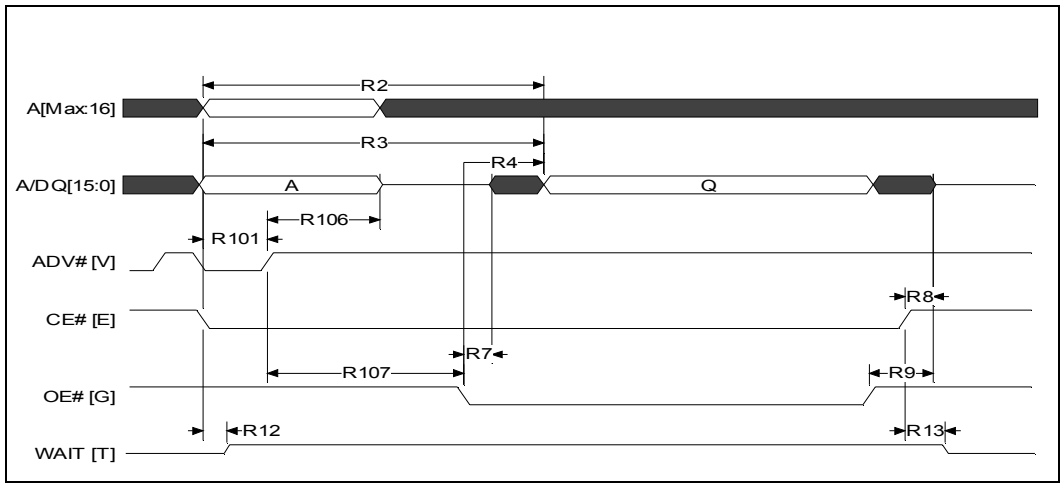
Figure 26. Sync Burst-Mode Unaligned 8-Word Burst Read, 256-Mbit, 133 MHz



Notes:
1. WAIT polarity in figure is low-true (RCR10 = 0, default).
2. 8-word and 16-word burst reads are always wrapped.
3. Address is latched on the second rising CLK edge after ADV# assertion, associated setup and hold timing shown.

7.2.4 Timings: AD-Mux Device, Async Read

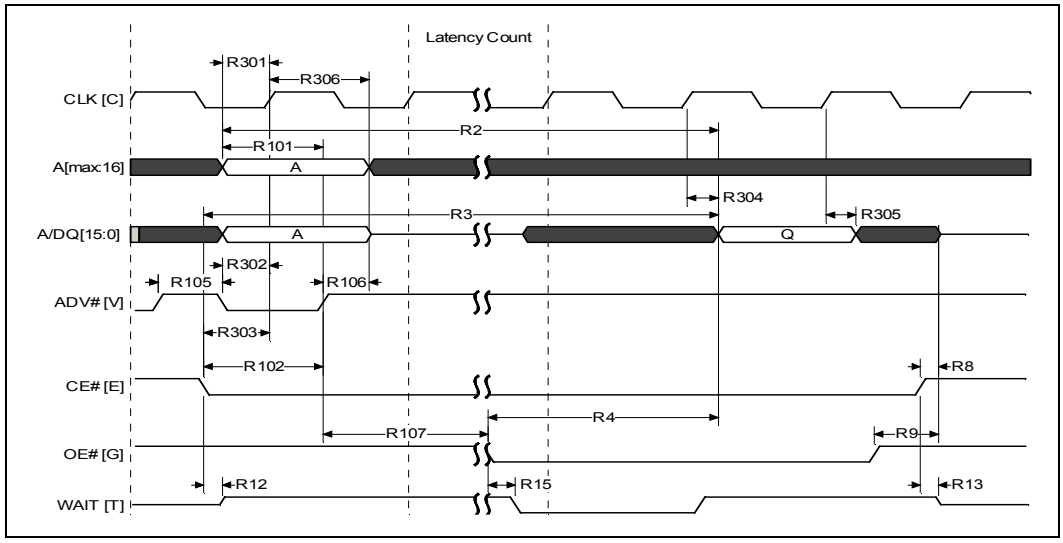
Figure 27. Async Word Read



Note: WAIT polarity in figure is low-true (RCR10 = 0, default). WAIT is deasserted during asynchronous reads.

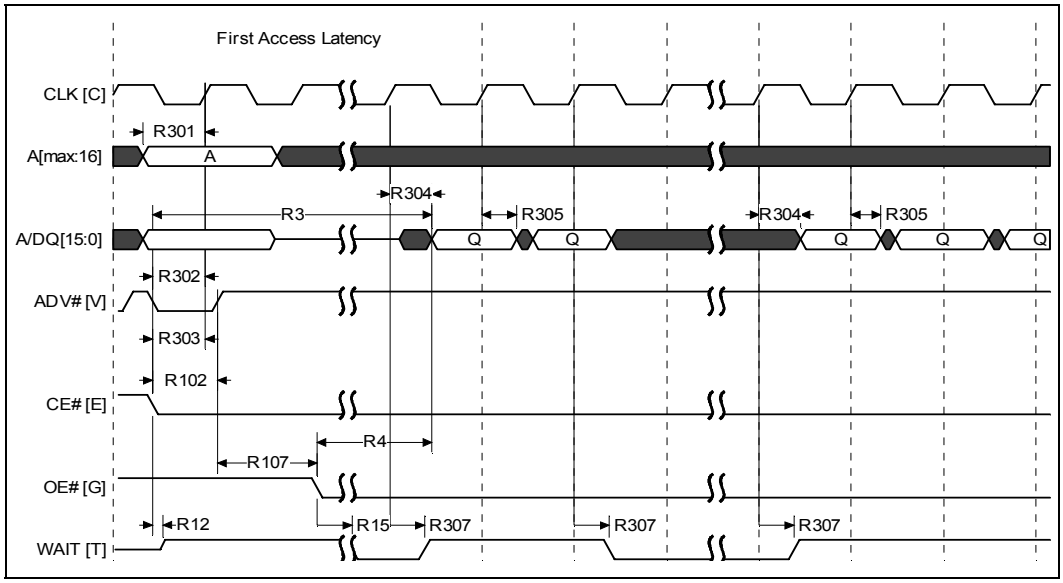
7.2.5 Timings: AD-Mux Device, Sync Read, 512-Mbit, 1-Gbit, 108 MHz

Figure 28. Sync Single-Word Array / Non-Array Read, 512-Mbit, 1-Gbit, 108 MHz



Notes:
1. WAIT polarity in figure is low-true (RCR10 = 0, default)..
2. This figure illustrates the case in which an n-word burst is initiated to the flash memory array and it is terminated by OE# and CE# deassertion after the first word in the burst.
3. Address latched on first CLK edge after ADV# low.

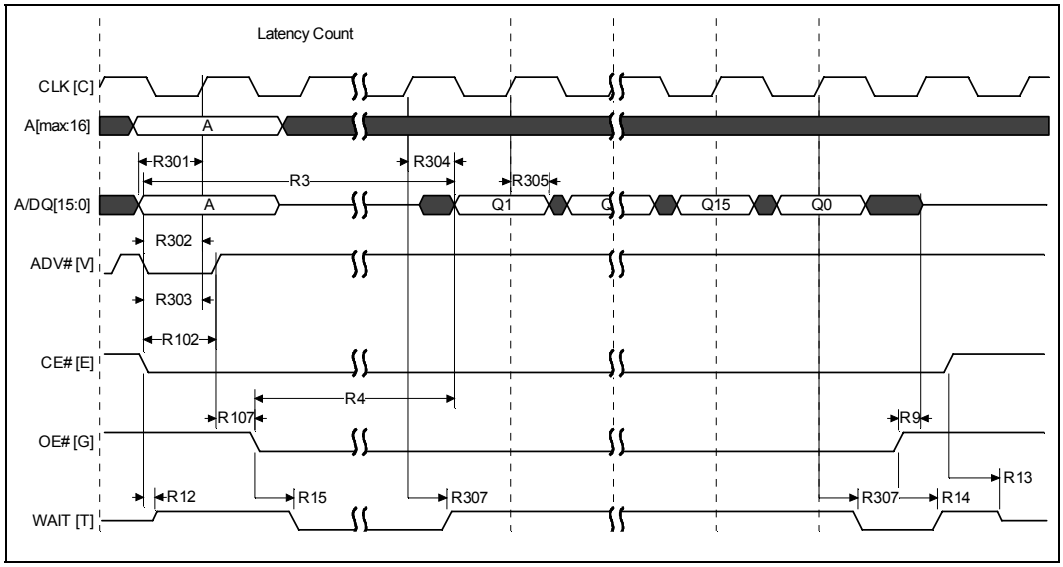
Figure 29. Continuous Burst Read: Output Delay at EOWL, 512-Mbit, 1-Gbit, 108 MHz



Notes:

1. At the End of Word Line (EOWL); the delay incurred when a burst access crosses a 16-word boundary and the starting address is not 16-word boundary aligned.
2. WAIT polarity in figure is low-true (RCR10 = 0, default).
3. Address latched on first CLK edge after ADV# low.

Figure 30. Sync Burst-Mode Unaligned 16-Word Burst Read, 512-Mbit, 1-Gbit, 108 MHz

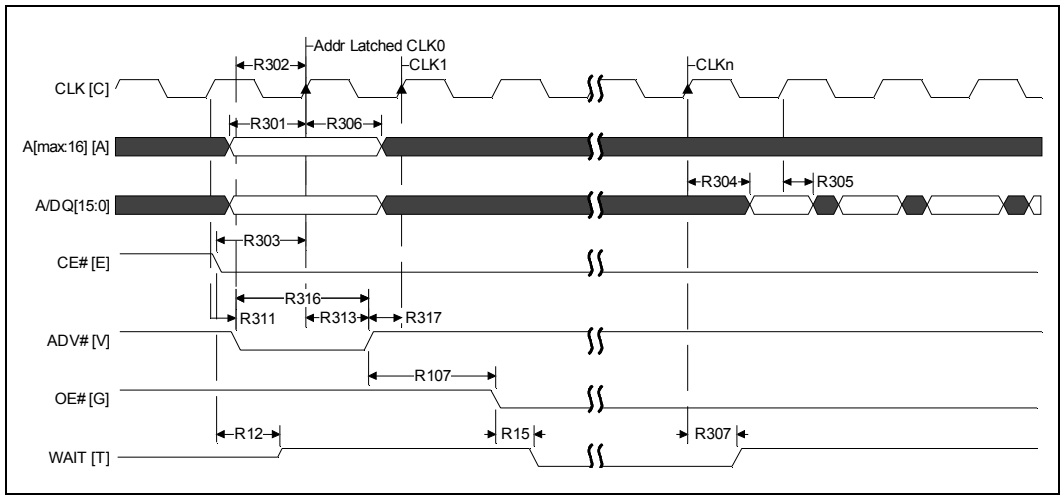


Notes:

1. WAIT polarity in figure is low-true (RCR10 = 0, default).
2. Address latched on first CLK edge after ADV# low.

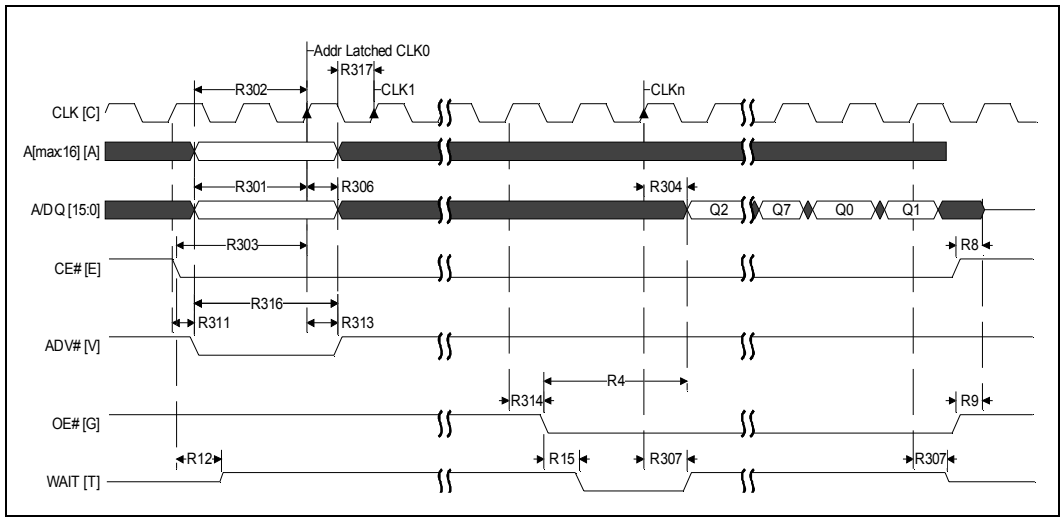
7.2.6 Timings: AD-Mux Device, Sync Read, 256-Mbit, 133 MHz

Figure 31. Sync Array or Non-array Read, 256-Mbit, 133 MHz



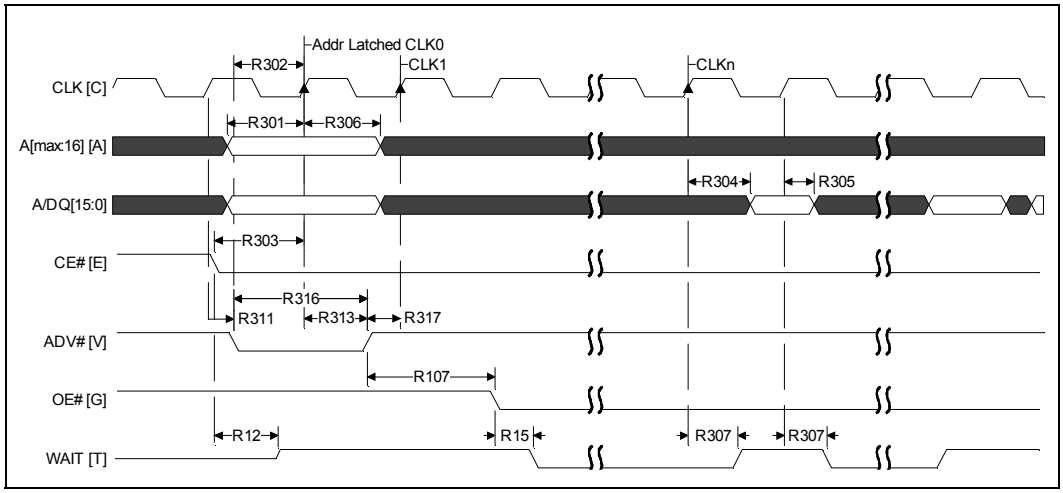
Notes:
1. Address is latched on the first rising CLK edge after ADV# assertion, associated setup and hold timing shown.
2. WAIT polarity in figure is low-true (RCR10 = 0, default).

Figure 32. Sync Unaligned 8-Word Burst Read: ADV# Max Low Pulse Width, 256-Mbit, 133 MHz



Notes:
1. Address is latched on the second rising CLK edge after ADV# assertion, associated setup and hold timing shown.
2. WAIT polarity in figure is low-true (RCR10 = 0, default).
3. 8-word and 16-word burst reads are always wrapped.

Figure 33. Continuous Burst Read: Output Delay at EOWL, 256-Mbit, 133 MHz



Notes:

1. At the End of Word Line (EOWL); the delay incurred when a burst access crosses a 16-word boundary and the starting address is not 16-word boundary aligned
2. WAIT polarity in figure is low-true (RCR10 = 0, default).
3. Address is latched on the first rising CLK edge after ADV# assertion, associated setup and hold timing shown.

7.3 Write Specifications

The M18 device includes write specifications for the following speeds and voltage levels:

- 512-Mbit device: 108 MHz, V_{CCQ} = 1.7 V to 2.0 V
- 1-Gbit device: 108 MHz, V_{CCQ} = 1.7 V to 2.0 V
- 256-Mbit device: 133 MHz, V_{CCQ} = 1.7 V to 2.0 V

Table 21. AC Write Specifications

Number	Symbol	Parameter (1, 2)	Min	Max	Units	Notes
W1	t_{PHWL}	RST# high recovery to WE# low	150	—	ns	1,2,3
W2	t_{ELWL}	CE# setup to WE# low	0	—	ns	1,2
W3	t_{WLWH}	WE# write pulse width low	40	—	ns	1,2,4
W4	t_{DVWH}	Data setup to WE# high	40	—	ns	1,2
W5	t_{AVWH}	Address setup to WE# high	40	—	ns	
W6	t_{WHEH}	CE# hold from WE# high	0	—	ns	
W7	t_{WHDX}	Data hold from WE# high	0	—	ns	
W8	t_{WHAX}	Address hold from WE# high (non-mux only)	0	—	ns	
W9	t_{WHWL}	WE# pulse width high	20	—	ns	1,2,5
W10	t_{VPWH}	VPP setup to WE# high	200	—	ns	1,2,3,7
W11	t_{QVVL}	VPP hold from Status read	0	—	ns	
W12	t_{QVBL}	WP# hold from Status read	0	—	ns	
W13	t_{BHWH}	WP# setup to WE# high	200	—	ns	
W14	t_{WHGL}	WE# high to OE# low	0	—	ns	1,2,8
W15	t_{VLWH}	ADV# low to WE# high (AD-Mux only)	55	—	ns	1,2
W16	t_{WHQV}	WE# high to read valid	t_{AVQV}+30	—	ns	1,2,3,9
Write to Synchronous Read Specifications						
W19	t_{WHCH}	WE# high to Clock high	15	—	ns	1,2,3,6,9
W27	t_{WHEL}	WE# high to CE# low	9	—	ns	1,2,3,6,9
W28	t_{WHVL}	WE# high to ADV# low	7	—	ns	1,2,3,6,9
Bus Write with Active Clock Specifications						
W21	t_{VHWL}	ADV# high to WE# low	—	27	ns	1,2,10,11
W22	t_{CHWL}	Clock high to WE# low	—	27	ns	

Notes:

1. Write timing characteristics during erase suspend are the same as write-only operations.
2. A write operation can be terminated with either CE# or WE#.
3. Sampled, not 100% tested.
4. Write pulse width low (t_{WLWH} or t_{ELEH}) is defined from CE# or WE# low (whichever occurs last) to CE# or WE# high (whichever occurs first). Hence, $t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}$.
5. Write pulse width high (t_{WHWL} or t_{EHEL}) is defined from CE# or WE# high (whichever occurs first) to CE# or WE# low (whichever occurs last). Hence, $t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL}$).
6. t_{WHCH} must be met when transitioning from a write cycle to a synchronous burst read. In addition there must be a CE# toggle after WE# goes high.
7. VPP and WP# should be at a valid level until erase or program success is determined.
8. When doing a Read Status operation following any command that alters the Status Register data, W14 is 20ns.
9. Add 10ns if the write operations results in a RCR or block lock status change, for the subsequent read operation to reflect this change.
10. This specification is applicable only if the part is configured in synchronous mode and an active clock is running. Either t_{VHWL} or t_{CHWL} must be met depending on the whether the address is latched on ADV# or CLK.
11. These specifications are not applicable to 133 MHz devices.

7.3.1 Timings: Non Mux Device, Async Write

Figure 34. Write to Write

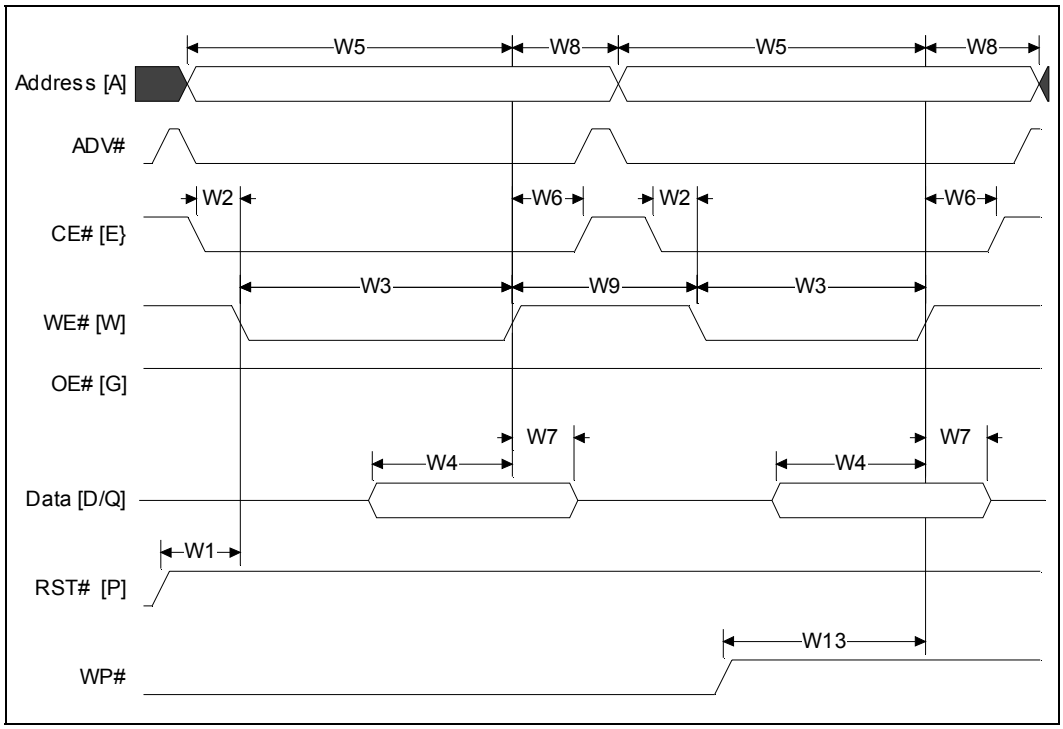
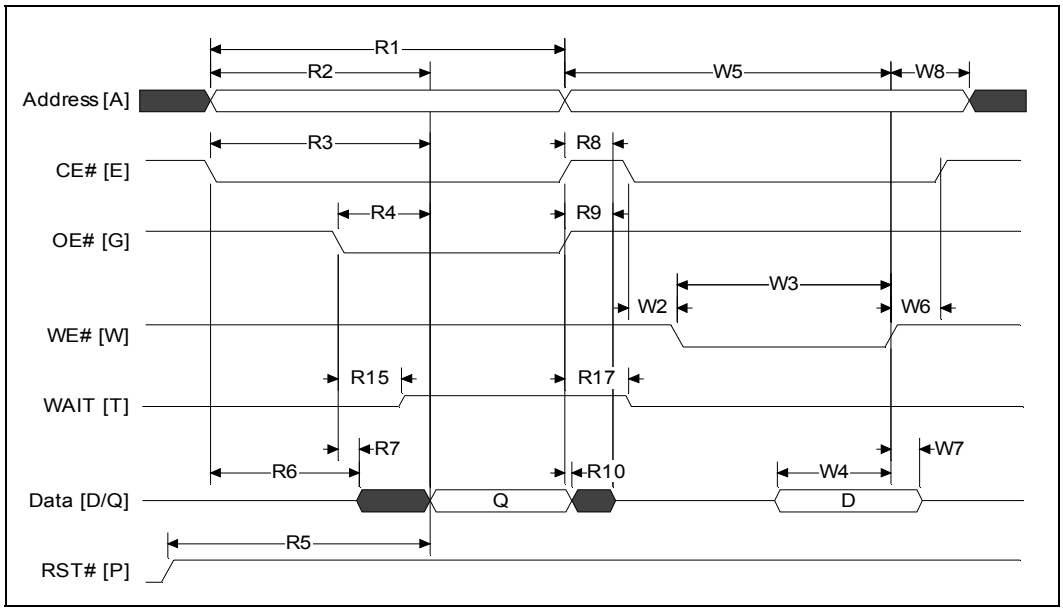
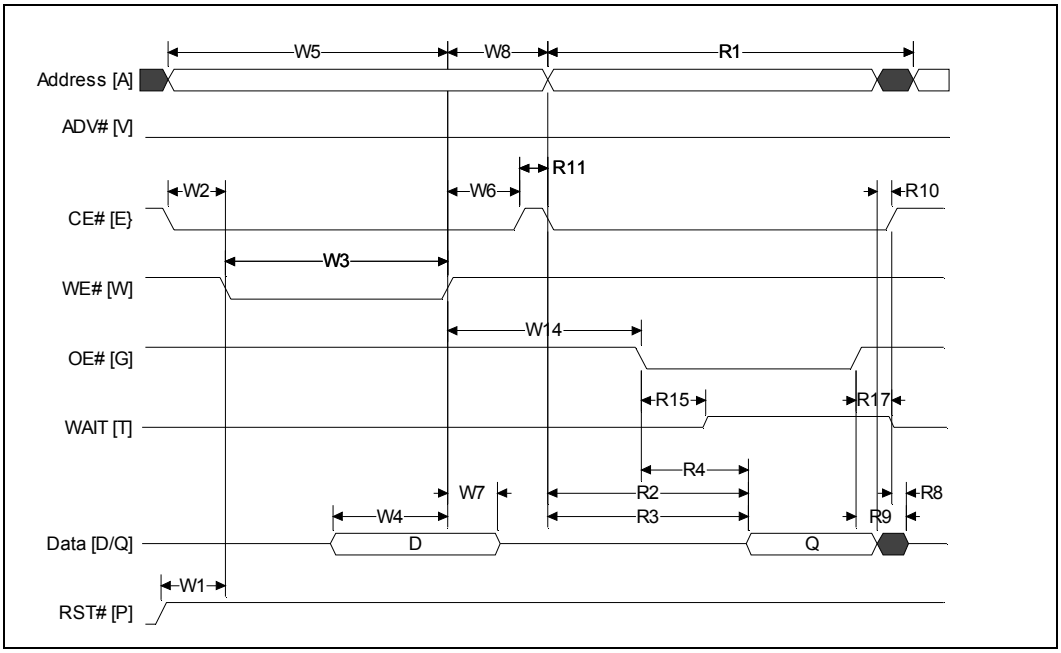


Figure 35. Async Read to Write



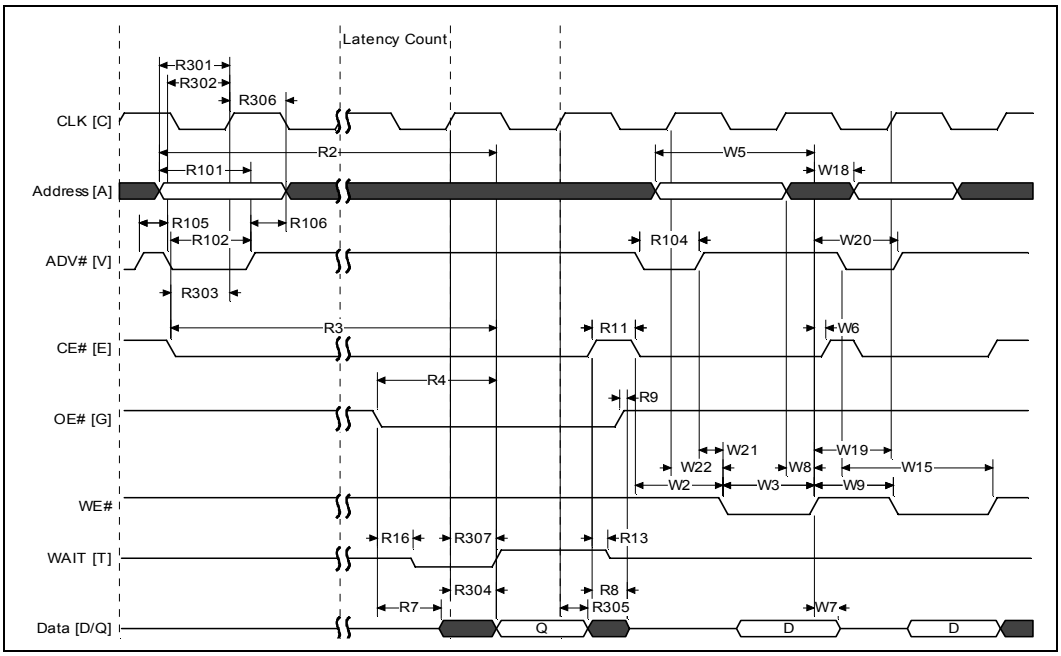
Note: WAIT polarity in figure is low-true (RCR10 = 0, default). WAIT deasserted during asynchronous reads and High-Z during writes.

Figure 36. Write to Async Read



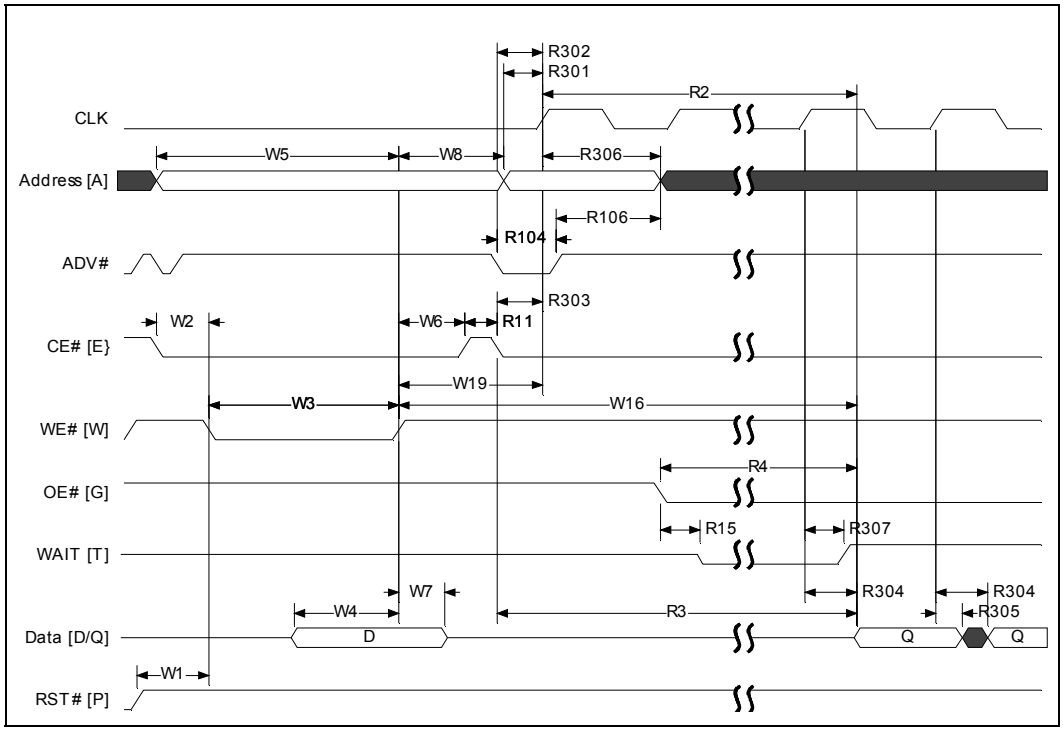
7.3.2 Timings: Non Mux Device, Sync Write, 512-Mbit, 1-Gbit, 108 MHz

Figure 37. Sync Read to Write, 512-Mbit, 1-Gbit, 108 MHz



Notes:
1. WAIT polarity in figure is low-true (RCR10 = 0, default). WAIT is high-Z during write operations.
2. Clock is ignored during write operation.

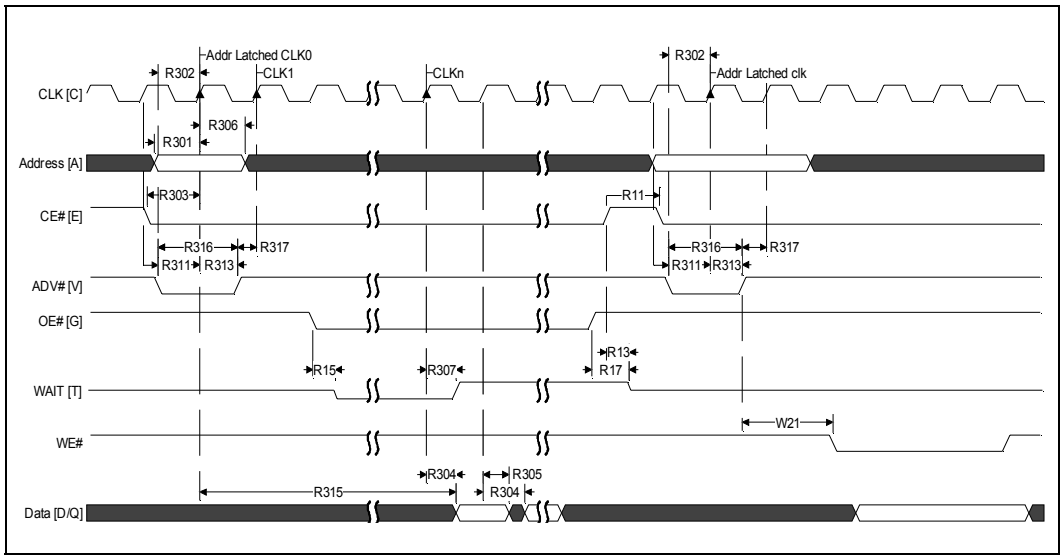
Figure 38. Write to Sync Read, 512-Mbit, 1-Gbit, 108 MHz



Note: WAIT polarity in figure is low-true (RCR10 = 0, default).

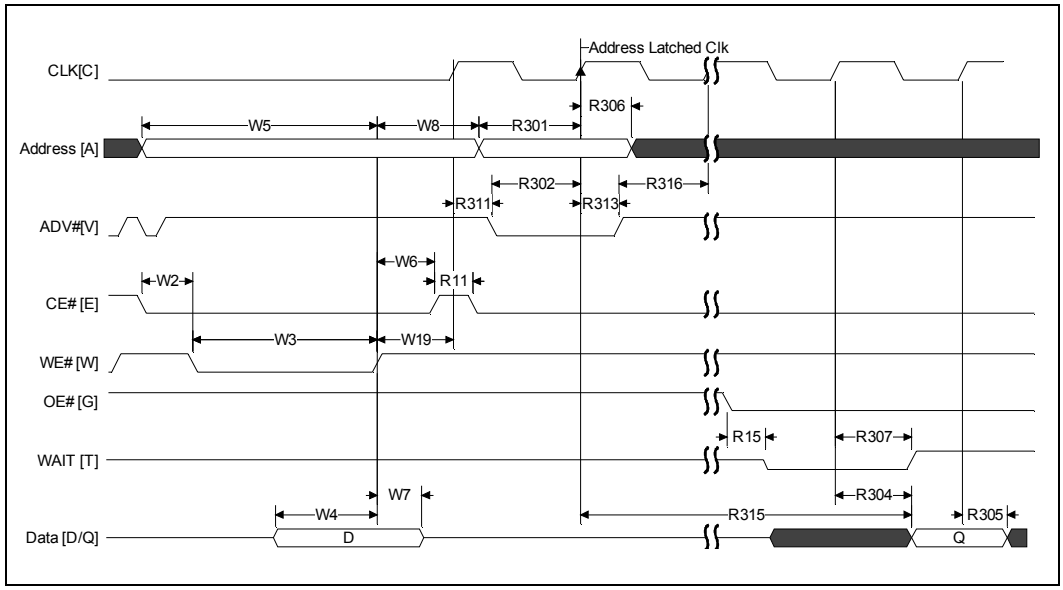
7.3.3 Timings: Non Mux Device, Sync Write, 256-Mbit, 133 MHz

Figure 39. Sync Read to Write, 256-Mbit, 133 MHz



Note: WAIT polarity in figure is low-true (RCR10 = 0, default).

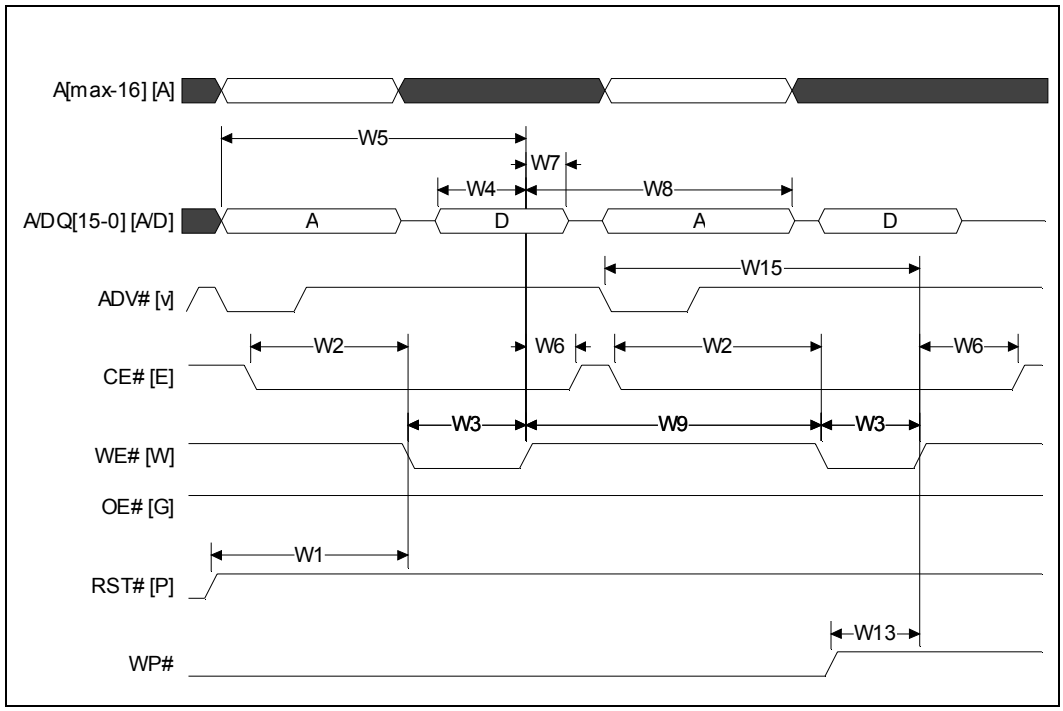
Figure 40. Write to Sync Read, 256-Mbit, 133 MHz



Note: WAIT polarity in figure is low-true (RCR10 = 0, default).

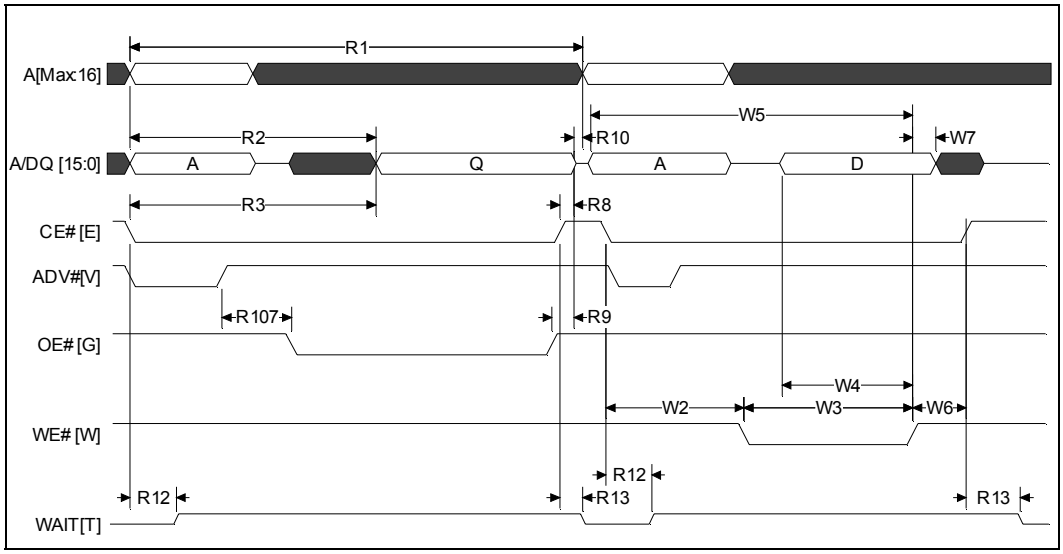
7.3.4 Timings: AD-Mux Device, Async Write

Figure 41. Write to Write



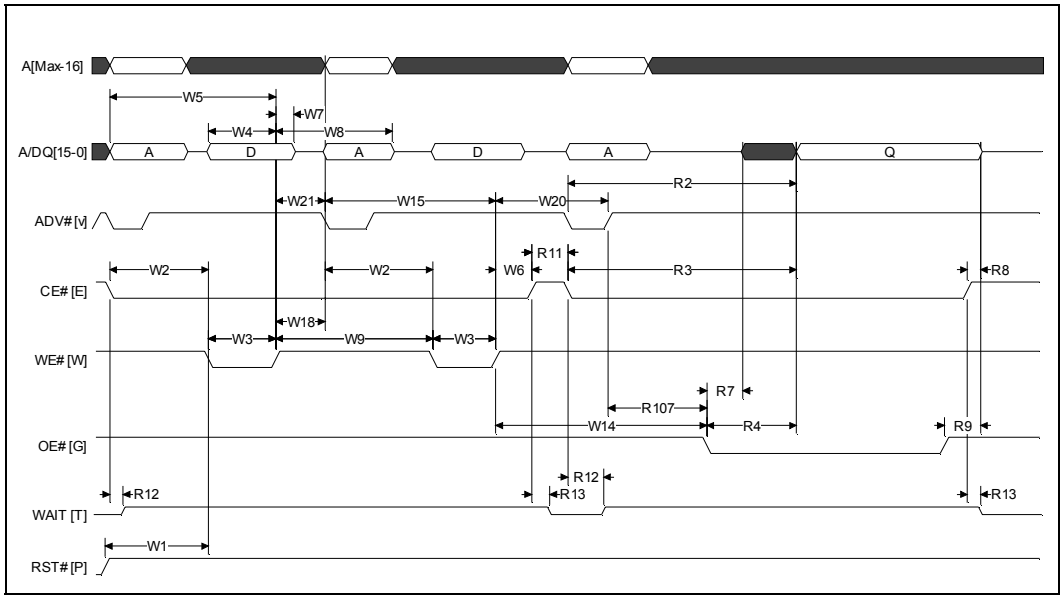
Note: WAIT polarity in figure is low-true (RCR10 = 0, default).

Figure 42. Async Read to Write



Note: WAIT polarity in figure is low-true (RCR10 = 0, default).

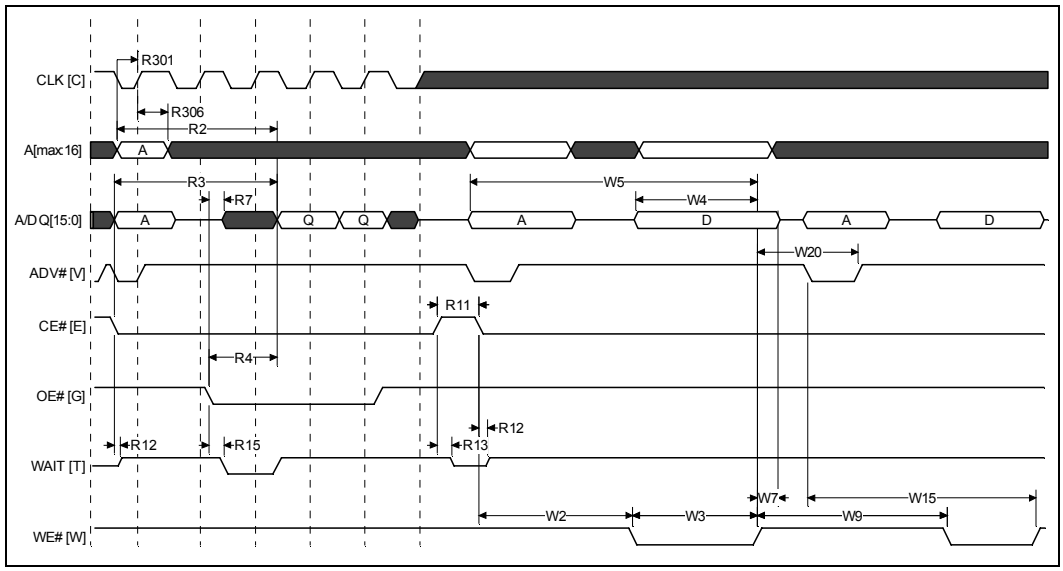
Figure 43. Write to Async Read



Note: WAIT polarity in figure is low-true (RCR10 = 0, default).

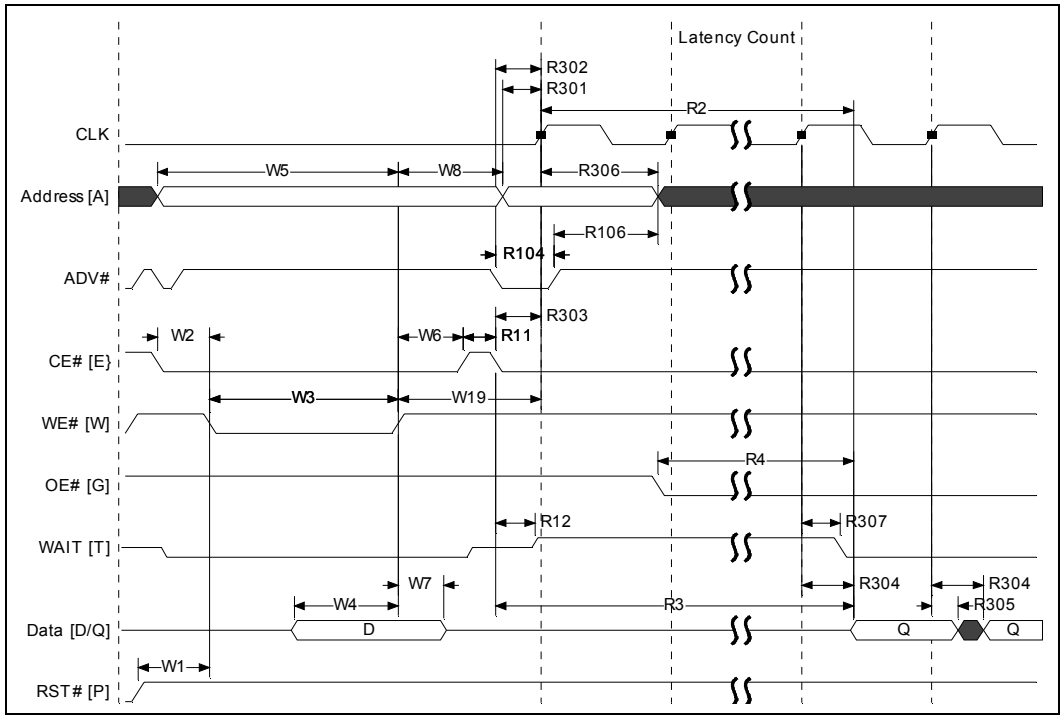
7.3.5 Timings: AD-Mux Device, Sync Write, 512-Mbit, 1-Gbit, 108 MHz

Figure 44. Sync Read to Write, 512-Mbit, 1-Gbit, 108 MHz



Note: WAIT polarity in figure is low-true (RCR10 = 0, default).

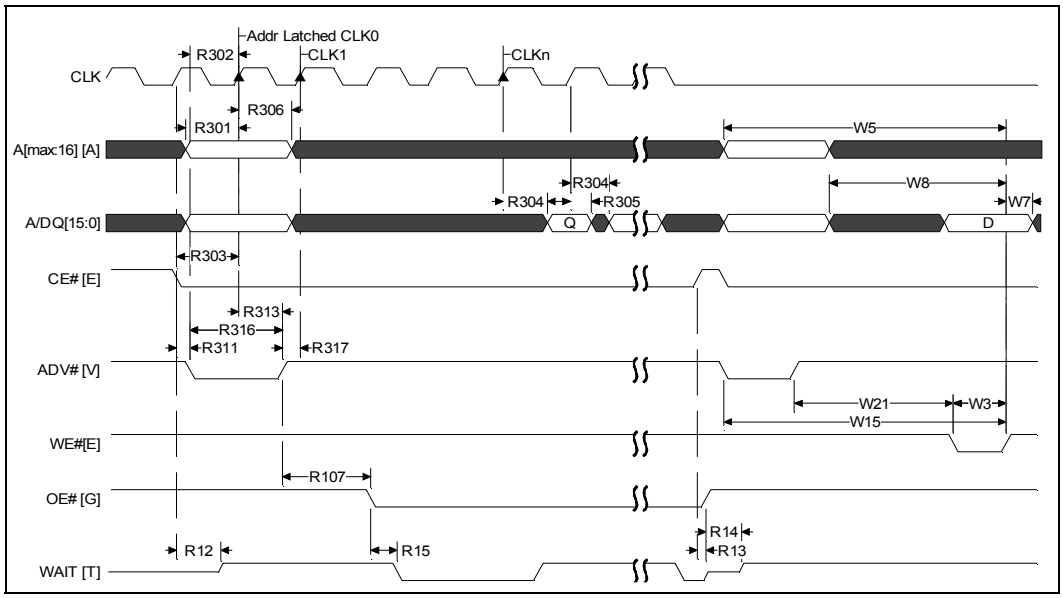
Figure 45. Write to Sync Read, 512-Mbit, 1-Gbit, 108 MHz



Note: WAIT polarity in figure is low-true (RCR10 = 0, default).

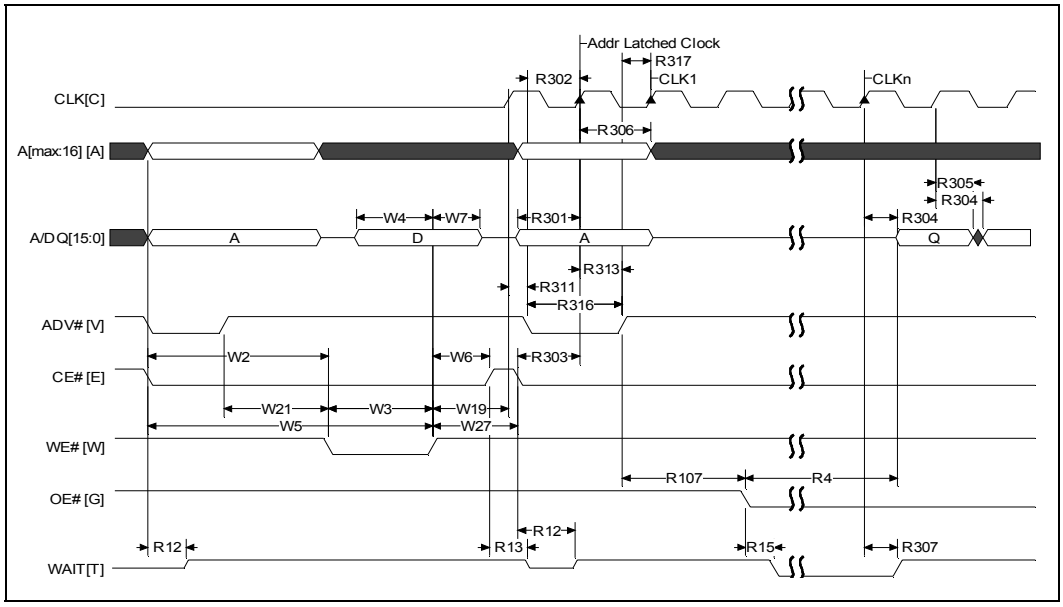
7.3.6 Timings: AD-Mux Device, Sync Write, 256-Mbit, 133 MHz

Figure 46. Sync Read to Write, 256-Mbit, 133 MHz

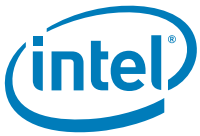


Note: WAIT polarity in figure is low-true (RCR10 = 0, default).

Figure 47. Write to Sync Read, 256-Mbit, 133 MHz



Note: WAIT polarity in figure is low-true (RCR10 = 0, default).



7.4 Program and Erase Characteristics

Table 22. Program-Erase Characteristics, 256-Mbit, 512-Mbit and 1-Gbit (Sheet 1 of 2)

Nbr.	Symbol	Parameter		V_{PPL}/V_{PPH}				Unit	Notes
				Density	Min	Typ	Max		
Conventional Word Programming									
W200	$t_{PROG/W}$	Program Time	Single word (first word)	256-Mbit (90 nm) 512-Mbit (90 nm) 1-Gbit (65 nm)	—	115	230	µs	1,2
			Single word (subsequent word)	256-Mbit (90 nm) 512-Mbit (90 nm) 1-Gbit (65 nm)	—	50	230		
Buffered Programming									
W200	$t_{PROG/W}$	Program Time	Single word	256-Mbit (90 nm) 512-Mbit (90 nm) 1-Gbit (65 nm)	—	250	500	µs	1
W250	$t_{PROG/PB}$		One Buffer (512 words)	256-Mbit (90 nm) 512-Mbit (90 nm) 1-Gbit (65 nm)	—	2.15 2.15 1.64	4.3 4.3 3.3	ms	
Buffered Enhanced Factory Programming									
W451	$t_{BEFP/W}$	Program Time	Single word	256-Mbit (90 nm) 512-Mbit (90 nm) 1-Gbit (65 nm)	—	4.2 4.2 3.2	—	µs	1,3,4
W452	$t_{BEFP/Setup}$		Buffered EFP Setup	256-Mbit (90 nm) 512-Mbit (90 nm) 1-Gbit (65 nm)	5	—	—		1
Erasing and Suspending									
W501	$t_{ERS/MAB}$	Erase Time	128-Kword Main Array Block	256-Mbit (90 nm) 512-Mbit (90 nm) 1-Gbit (65 nm)	—	0.9	4	s	1

Table 22. Program-Erase Characteristics, 256-Mbit, 512-Mbit and 1-Gbit (Sheet 2 of 2)

Nbr.	Symbol	Parameter		V_{PPL} / V_{PPH}				Unit	Notes
				Density	Min	Typ	Max		
W600	$t_{SUSP/P}$	Suspend Latency	Program suspend	256-Mbit (90 nm) 512-Mbit (90 nm) 1-Gbit (65 nm)	—	20	30	µs	1
W601	$t_{SUSP/E}$		Erase suspend	256-Mbit (90 nm) 512-Mbit (90 nm) 1-Gbit (65 nm)	—	20	30		1
Blank Check									
W702	$t_{BC/MB}$	Blank Check	Main array block	256-Mbit (90 nm) 512-Mbit (90 nm) 1-Gbit (65 nm)	—	3.2	—	ms	1

Notes:
1. Typical values measured at T_C = +25 °C and nominal voltages. Performance numbers are valid for all speed versions. Sampled, but not 100% tested.
2. First and subsequent words refer to first word and subsequent words in Control Mode programming region.
3. Averaged over entire device.
4. BEFP not validated at V_{PPL}.

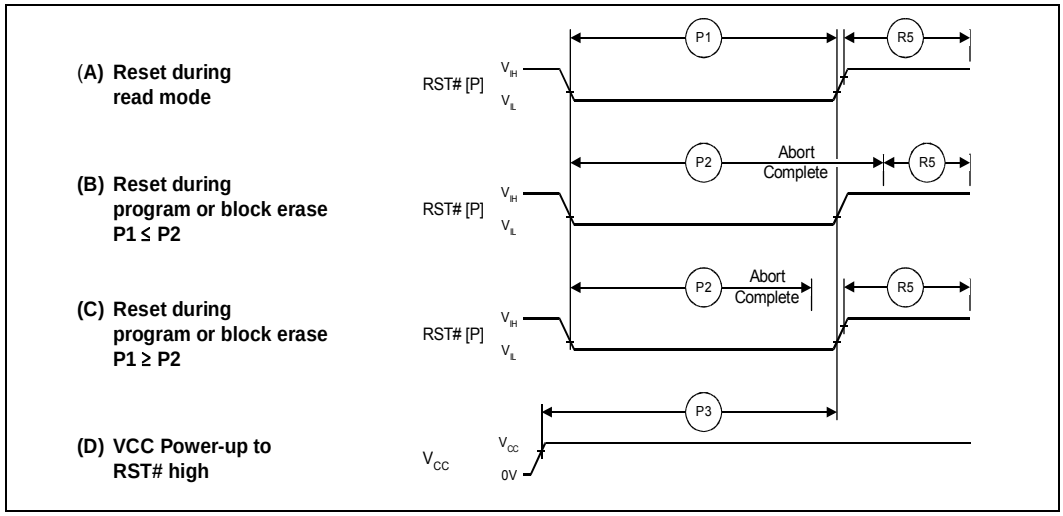
7.5 Reset Specifications

Table 23. Reset Specifications

Nbr.	Symbol	Parameter	Min	Max	Unit	Notes
P1	t_{PLPH}	RST# pulse width low	100		ns	1,2,3,4,7
P2	t_{PLRH}	RST# low to device reset during erase	—	25	µs	1,3,4,7
		RST# low to device reset during program	—	25		1,3,4,7
P3	t_{VCCPH}	V_{CC} Power valid to RST# de-assertion (high)	300	—		1,4,5,6

Notes:
1. These specifications are valid for all device versions (packages and speeds).
2. The device may reset if t_{PLPH} is < $t_{PLPH\ MIN}$, but this is not guaranteed.
3. Not applicable if RST# is tied to Vccq.
4. Sampled, but not 100% tested.
5. If RST# is tied to the V_{CC} supply, device will not be ready until t_{VCCPH} after $V_{CC} \geq V_{CC}$ min.
6. If RST# is tied to any supply/signal with V_{CCQ} voltage levels, the RST# input voltage must not exceed V_{CC} until $V_{CC} \geq V_{CC}$(min).
7. Reset completes within t_{PLPH} if RST# is asserted while no erase or program operation is executing.

Figure 48. Reset Operation Timing



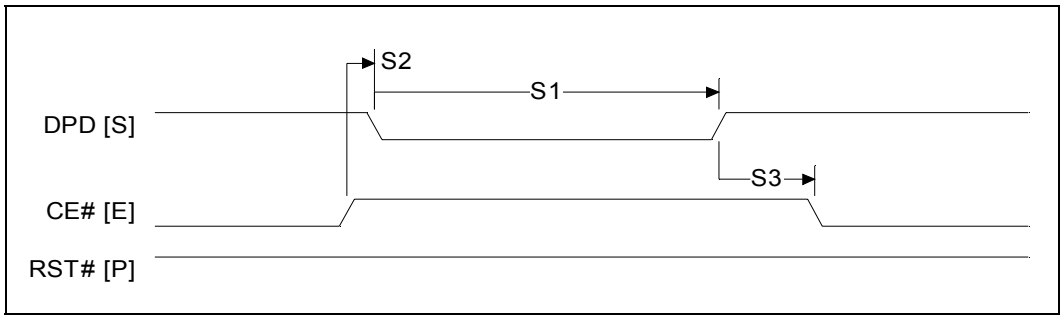
7.6 Deep Power Down Specifications

Table 24. Deep Power Down Specifications

Nbr.	Symbol	Parameter	Min	Max	Unit	Notes
S1	t_{SLSH} (t_{SHSL})	DPD asserted pulse width	100	—	ns	1,2,3
S2	t_{EHSH} (t_{EHSL})	CE# high to DPD asserted	0	—	µs	1,2
S3	t_{SHEL} (t_{SLEL})	DPD deasserted to CE# low	75	—		1,2
S4	t_{PHEL}	RST# high during DPD state to CE# low (DPD deasserted to CE# low)	75	—		1,2

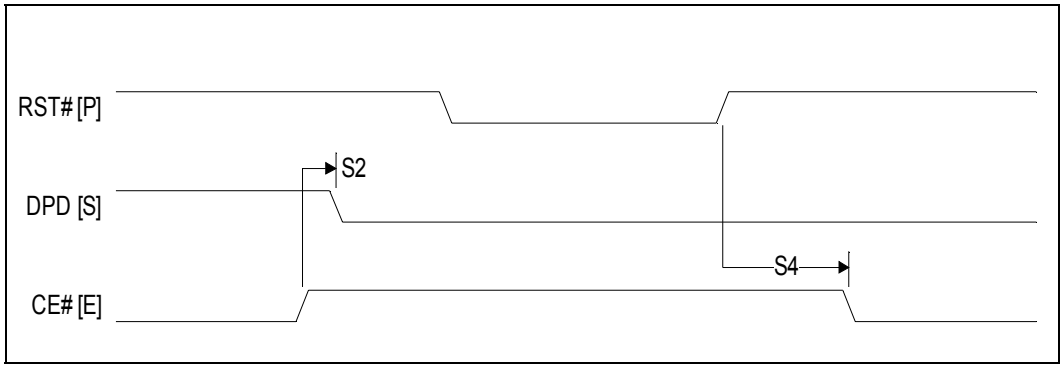
Notes:
1. These specifications are valid for all device versions (packages and speeds).
2. Sampled, but not 100% tested.
3. DPD must remain asserted for the duration of Deep Power Down mode. DPD current levels are achieved 40 µs after entering the DPD mode.

Figure 49. Deep Power Down Operation Timing



Note: DPD pin is low-true (ECR14 = 0)

Figure 50. Reset During Deep Power Down Operation Timing



Note: DPD pin is low-true (ECR14 = 0)